

PCA9537

4-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Rev. 7 — 8 September 2021

Product data sheet
COMPANY PUBLIC

1 General description

The PCA9537 is a 10-pin CMOS device that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I²C-bus/SMBus applications. It was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, LEDs, fans, etc.

The PCA9537 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The PCA9537 open-drain interrupt output ($\overline{\text{INT}}$) is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the device.

The I²C-bus address is fixed and allows only one device on the same I²C-bus/SMBus.

2 Features and benefits

- 4-bit I²C-bus GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins that default to 4 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in TSSOP10 package



3 Ordering information

Table 1. Ordering information

 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Type number	Topside mark	Package		
		Name	Description	Version
PCA9537DP	9537	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1

3.1 Ordering options

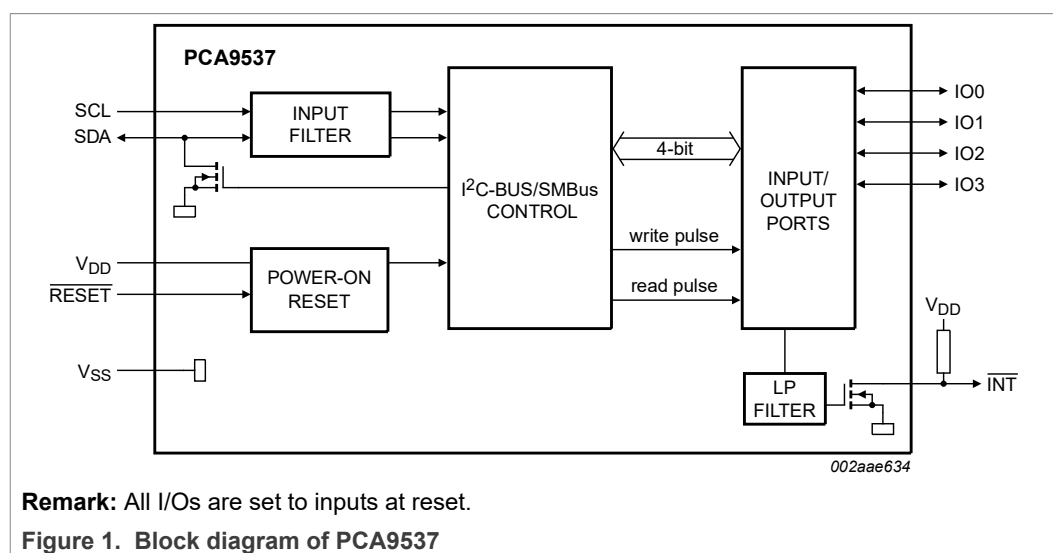
Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9537DP	PCA9537DP,118 ^[1]	TSSOP10	REEL 13" Q1/T1 *STANDARD MARK SMD	2500	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$
	PCA9537DPZ	TSSOP10	REEL 13" Q1/T1 *STANDARD MARK SSB ^[2]	2500	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

[1] Discontinued in 202104010DN - drop in replacement is PCA9537DPZ - this is documented in PCN 2020104008A.

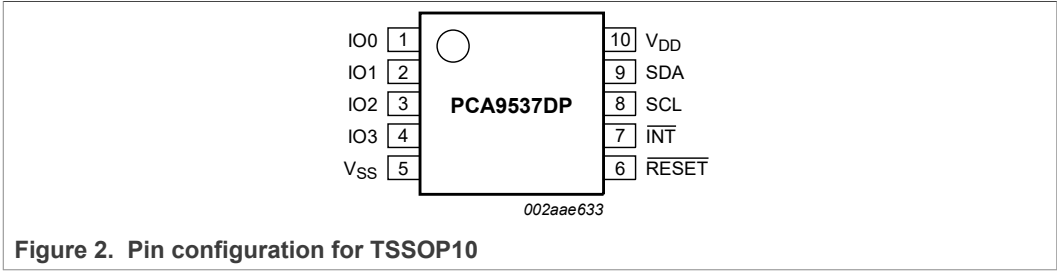
[2] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

4 Block diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

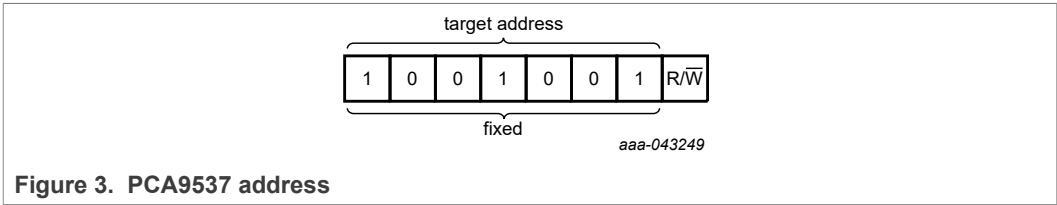
Table 3. Pin description

Symbol	Pin	Description
IO0	1	input/output 0
IO1	2	input/output 1
IO2	3	input/output 2
IO3	4	input/output 3
V _{SS}	5	supply ground
RESET	6	active LOW reset input
INT	7	interrupt output (open-drain)
SCL	8	serial clock line
SDA	9	serial data line
V _{DD}	10	supply voltage

6 Functional description

Refer to [Figure 1](#).

6.1 Device address



6.2 Registers

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the registers will be written or read.

Table 4. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

6.2.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. Register 0 - Input Port register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	I7	read only	1*	not used
6	I6	read only	1*	
5	I5	read only	1*	
4	I4	read only	1*	
3	I3	read only	X*	value 'X' is determined by externally applied logic level
2	I2	read only	X*	
1	I1	read only	X*	
0	I0	read only	X*	

6.2.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output Port register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	O7	R	1*	not used
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	

Table 6. Register 1 - Output Port register bit description...continued

Legend: * default value.

Bit	Symbol	Access	Value	Description
3	O3	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.2.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with 1), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a 0), the Input Port data polarity is retained.

Table 7. Register 2 - Polarity Inversion register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	not used
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	inverts polarity of Input Port register data 0 = Input Port register data retained (default value) 1 = Input Port register data inverted
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

6.2.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

Table 8. Register 3 - Configuration register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	not used
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	configures the directions of the I/O pins 0 = corresponding port pin enabled as an output 1 = corresponding port pin configured as an input (default value)
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

6.3 Power-on reset

When power is applied to V_{DD} , an internal Power-On Reset (POR) holds the PCA9537 in a reset condition until V_{DD} has reached V_{POR} . At that point, the reset condition is released and the PCA9537 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.4 RESET input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(\text{rst})}$. The PCA9537 registers and SMBus/I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input requires a pull-up resistor to V_{DD} if no active connection is used.

6.5 Interrupt output

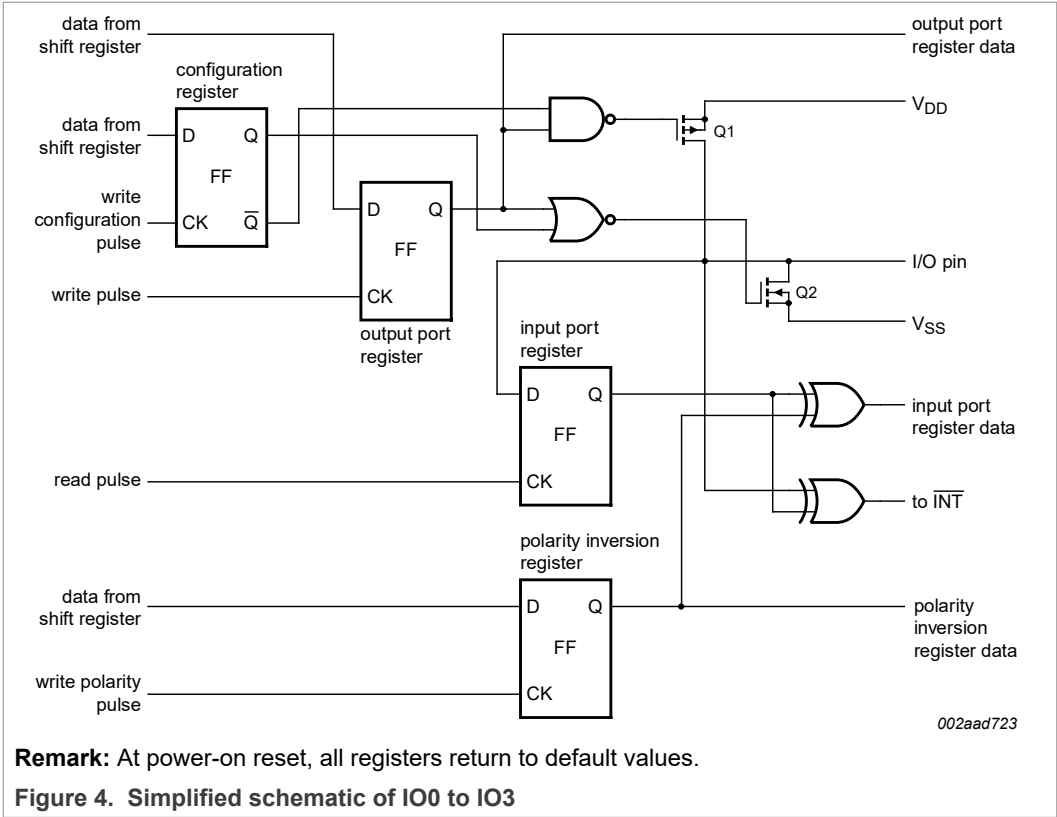
The open-drain interrupt output ($\overline{\text{INT}}$) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is de-activated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

6.6 I/O port

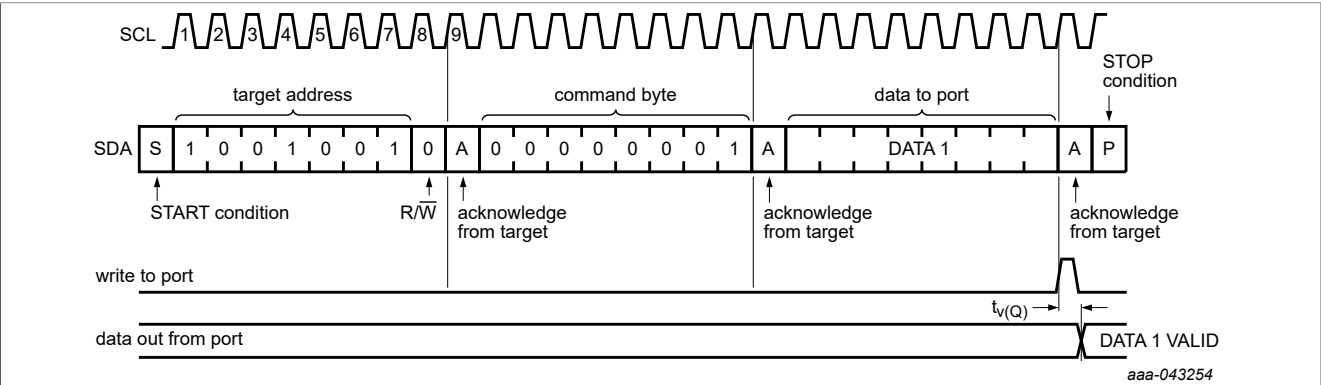
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS} .

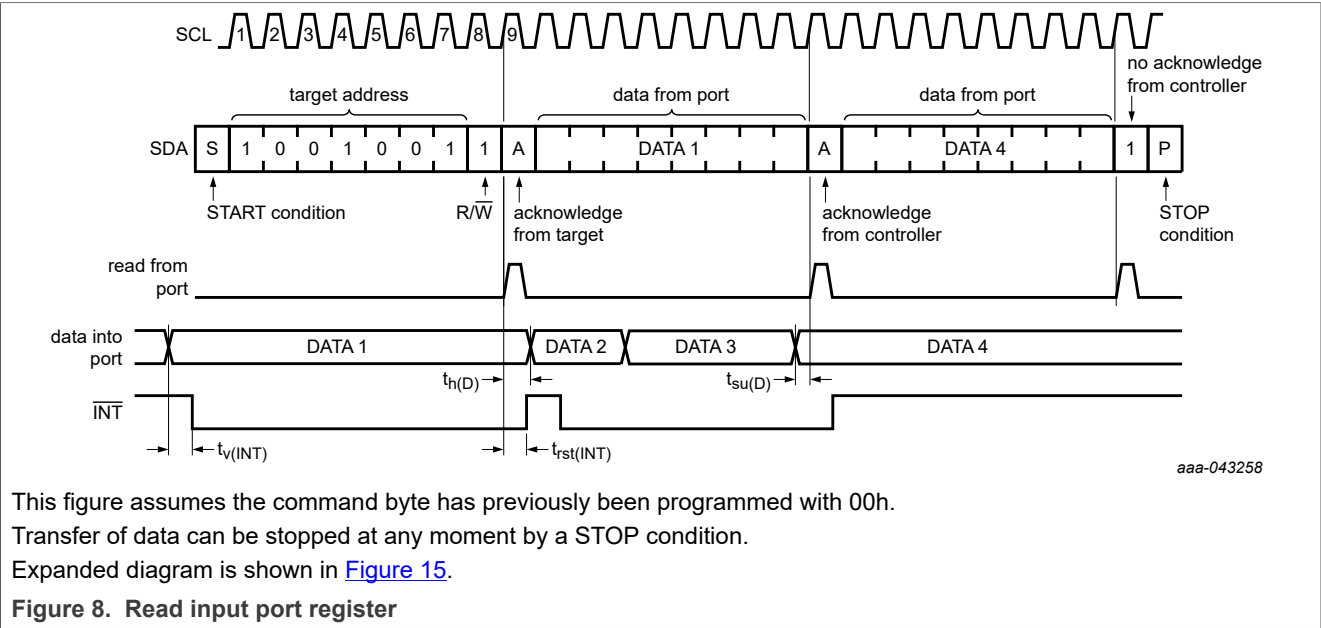
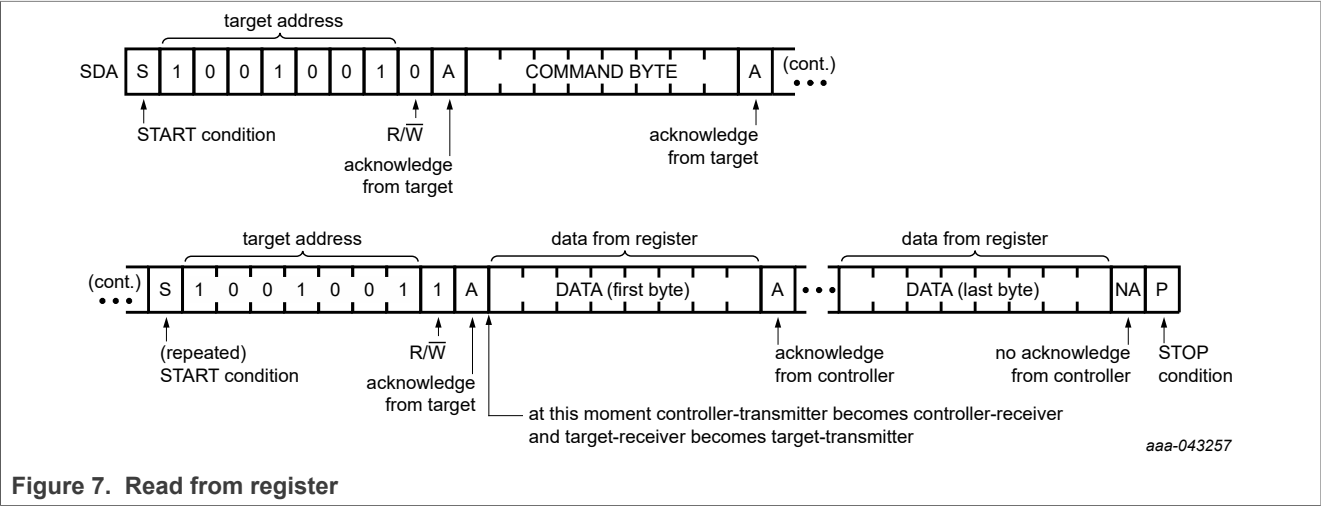
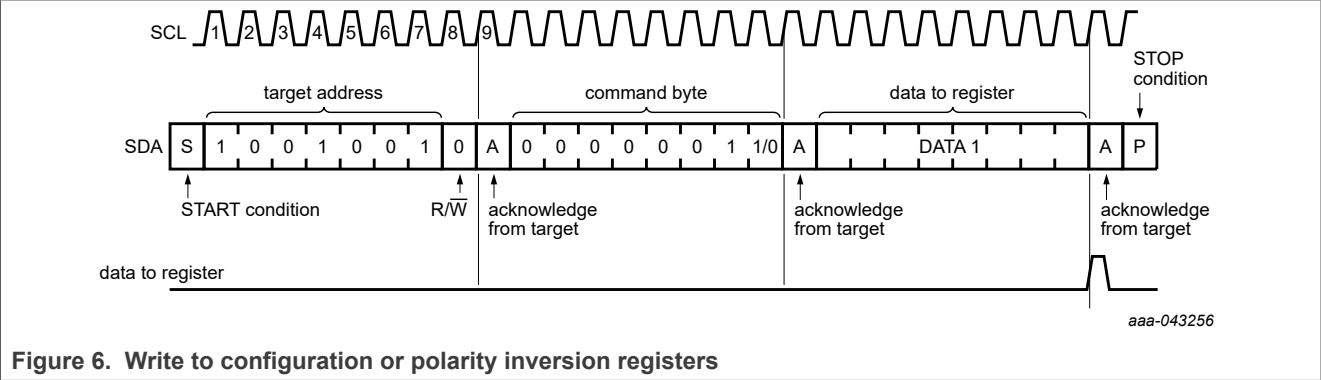


6.7 Bus transactions

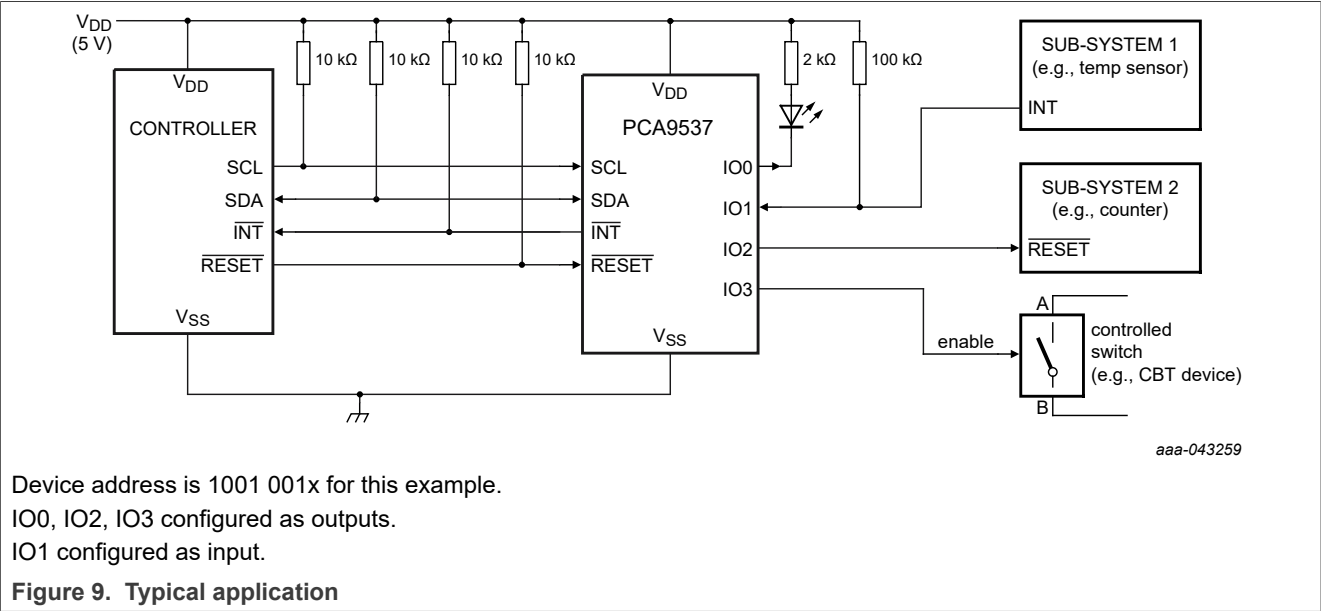
Data is transmitted to the PCA9537 registers using the write mode as shown in [Figure 5](#) and [Figure 6](#). Data is read from the PCA9537 registers using the read mode as shown in [Figure 7](#) and [Figure 8](#). These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.



Expanded diagram is shown in [Figure 16](#).
Figure 5. Write to output port register



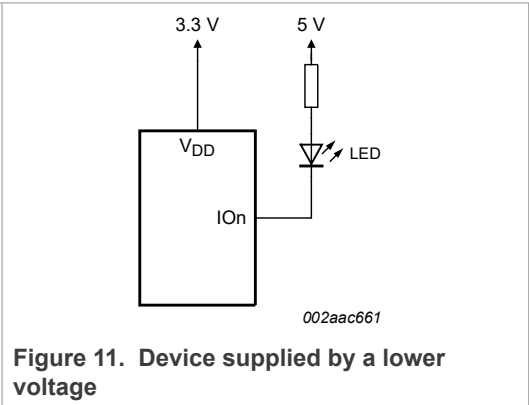
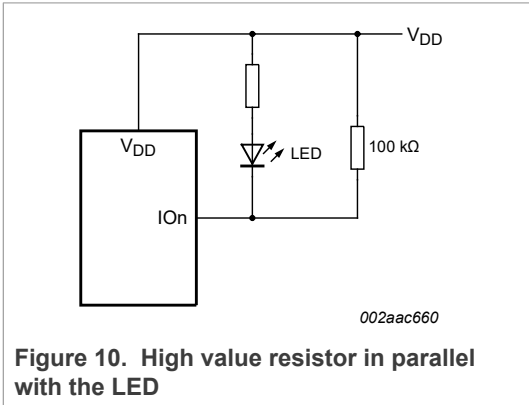
7 Application design-in information



7.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in [Figure 9](#). Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. [Figure 10](#) shows a high value resistor in parallel with the LED. [Figure 11](#) shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.



8 Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+6.0	V
I _I	input current		-	±20	mA
V _{I/O}	voltage on an input/output pin		V _{SS} - 0.5	5.5	V
I _{O(IOn)}	output current on pin IOn		-	±50	mA
I _{DD}	supply current		-	85	mA
I _{SS}	ground supply current		-	100	mA
P _{tot}	total power dissipation		-	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature	operating	-40	+85	°C
T _{j(max)}	maximum junction temperature		-	+125	°C

9 Static characteristics

Table 10. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V _{DD}	supply voltage		2.3	-	5.5	V
I _{DD}	supply current	operating mode; V _{DD} = 5.5 V; no load; f _{SCL} = 100 kHz	-	104	175	µA
I _{stbL}	LOW-level standby current	Standby mode; V _{DD} = 5.5 V; no load; V _I = V _{SS} ; f _{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
I _{stbH}	HIGH-level standby current	Standby mode; V _{DD} = 5.5 V; no load; V _I = V _{DD} ; f _{SCL} = 0 kHz; I/O = inputs	-	0.25	1	µA
V _{POR}	power-on reset voltage	no load; V _I = V _{DD} or V _{SS}	[1] -	1.7	2.2	V
Input SCL; input/output SDA						
V _{IL}	LOW-level input voltage		-0.5	-	+0.3V _{DD}	V
V _{IH}	HIGH-level input voltage		0.7V _{DD}	-	5.5	V
I _{OL}	LOW-level output current	V _{OL} = 0.4 V	3	7	-	mA
I _L	leakage current	V _I = V _{DD} = V _{SS}	-1	-	+1	µA
C _i	input capacitance	V _I = V _{SS}	-	5	10	pF
I/Os						
V _{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V _{IH}	HIGH-level input voltage		2.0	-	5.5	V

4-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Table 10. Static characteristics...continued

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OL}	LOW-level output current	$V_{OL} = 0.5\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	8	10	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	8	14	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	8	17	-	mA
		$V_{OL} = 0.7\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	10	13	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	10	19	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.8	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.6	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.1	-	-	V
		$I_{OH} = -10\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.7	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.5	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.0	-	-	V
I_L	leakage current	$V_I = V_{DD} = V_{SS}$		-1	-	+1	μA
C_i	input capacitance			-	5	10	pF
Interrupt INT							
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$		3	13	-	mA
I_{OH}	HIGH-level output current	$V_{OL} = 0.4\text{ V}$		-1	-	+1	μA
Select input RESET							
V_{IL}	LOW-level input voltage			-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	5.5	V
I_L	leakage current	$V_I = V_{DD} = V_{SS}$		-1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

10 Dynamic characteristics

Table 11. Dynamic characteristics

Symbol	Parameter	Conditions		Standard-mode I ² C-bus		Fast-mode I ² C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	μs

Table 11. Dynamic characteristics...continued

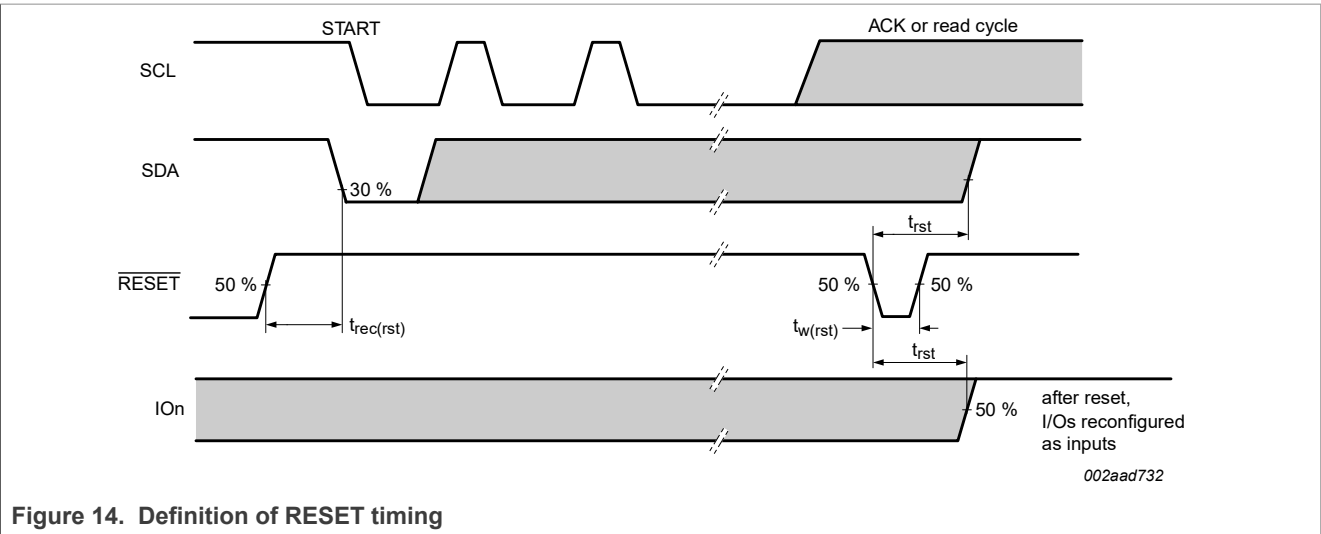
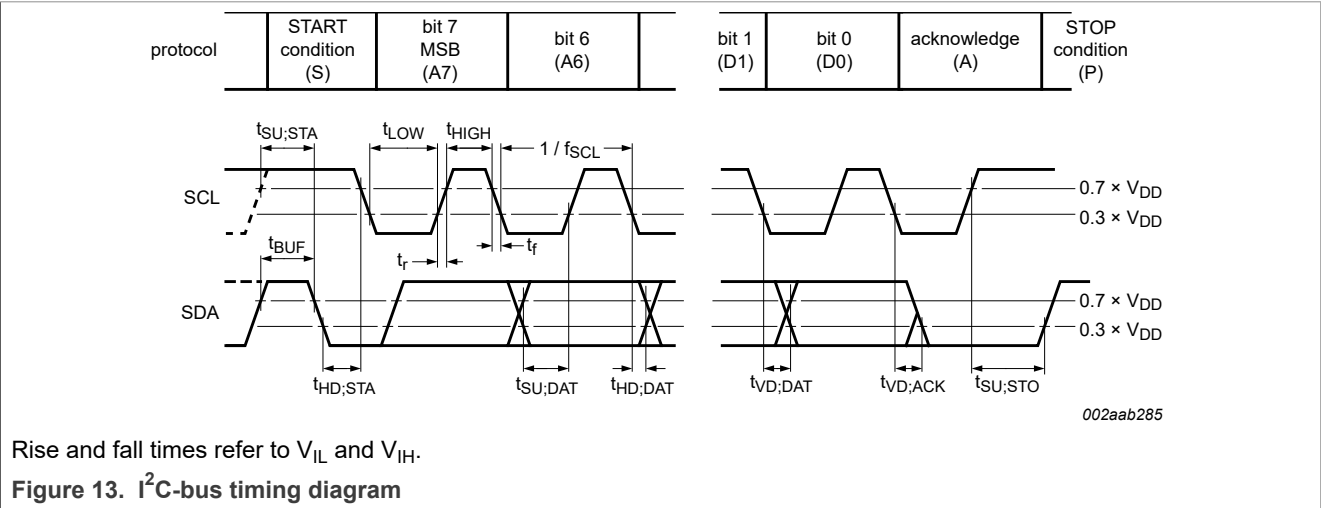
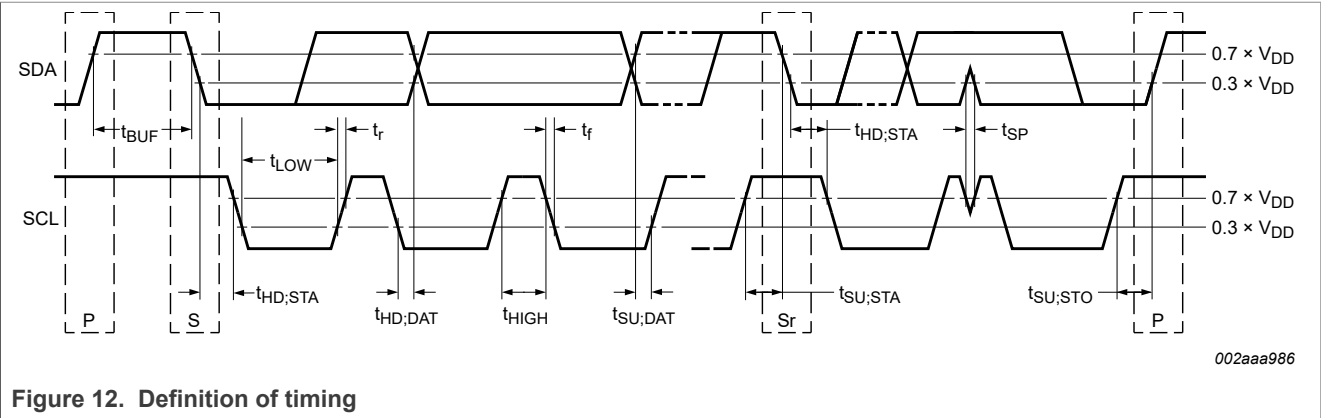
Symbol	Parameter	Conditions		Standard-mode I ² C-bus		Fast-mode I ² C-bus		Unit
				Min	Max	Min	Max	
t _{HD;STA}	hold time (repeated) START condition			4.0	-	0.6	-	μs
t _{SU;STA}	set-up time for a repeated START condition			4.7	-	0.6	-	μs
t _{SU;STO}	set-up time for STOP condition			4.0	-	0.6	-	μs
t _{HD;DAT}	data hold time			0	-	0	-	ns
t _{VD;ACK}	data valid acknowledge time		[1]	0.3	3.45	0.1	0.9	μs
t _{VD;DAT}	data valid time		[2]	300	-	50	-	ns
t _{SU;DAT}	data set-up time			250	-	100	-	ns
t _{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	μs
t _{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	μs
t _r	rise time of both SDA and SCL signals			-	1000	20 + 0.1C _b ^[3]	300	ns
t _f	fall time of both SDA and SCL signals			-	300	20 + 0.1C _b ^[3]	300	ns
t _{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns
Port timing								
t _{V(Q)}	data output valid time			-	200	-	200	ns
t _{SU(D)}	data input set-up time			100	-	100	-	ns
t _{H(D)}	data input hold time			1	-	1	-	μs
Interrupt timing								
t _{V(INT)}	valid time on pin INT			-	4	-	4	μs
t _{rst(INT)}	reset time on pin INT			-	4	-	4	μs
RESET								
t _{w(rst)}	reset pulse width			4	-	4	-	ns
t _{rec(rst)}	reset recovery time			0	-	0	-	ns
t _{rst}	reset time			400	-	400	-	ns

[1] t_{VD;ACK} = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t_{VD;DAT} = minimum time for the SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.

4-bit I²C-bus and SMBus low power I/O port with interrupt and reset



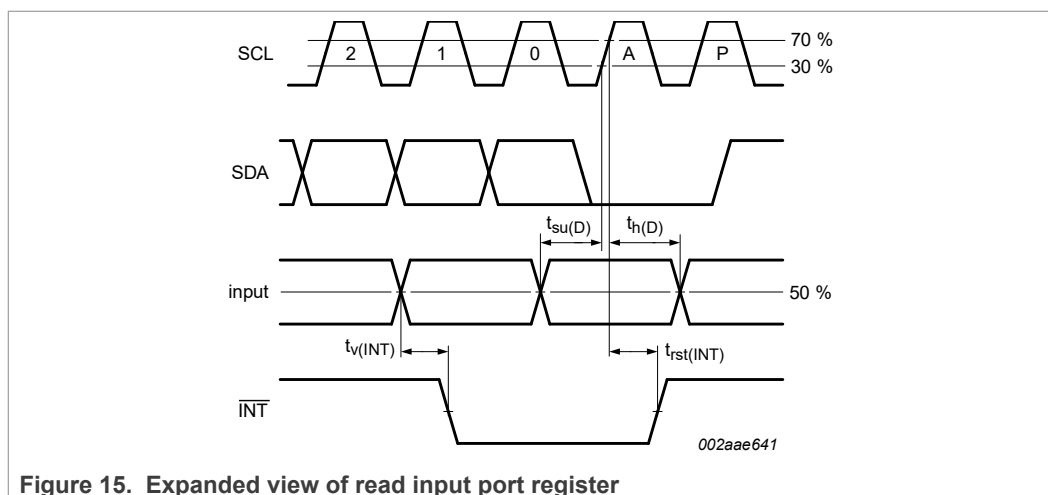
4-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Figure 15. Expanded view of read input port register

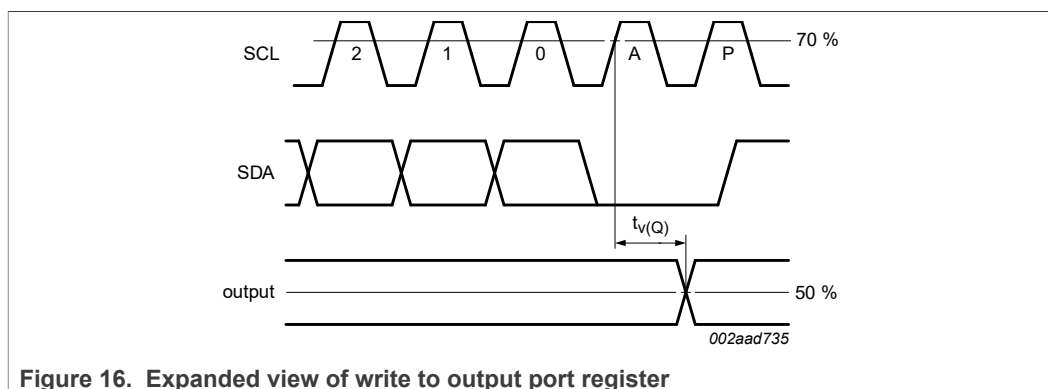


Figure 16. Expanded view of write to output port register

11 Test information

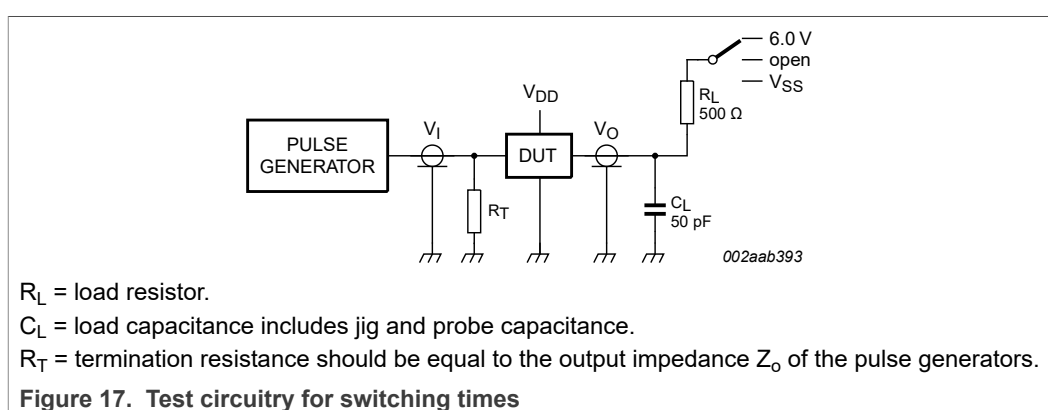


Figure 17. Test circuitry for switching times

4-bit I²C-bus and SMBus low power I/O port with interrupt and reset

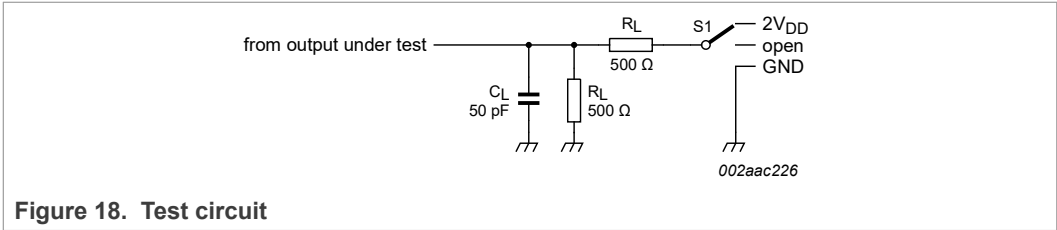


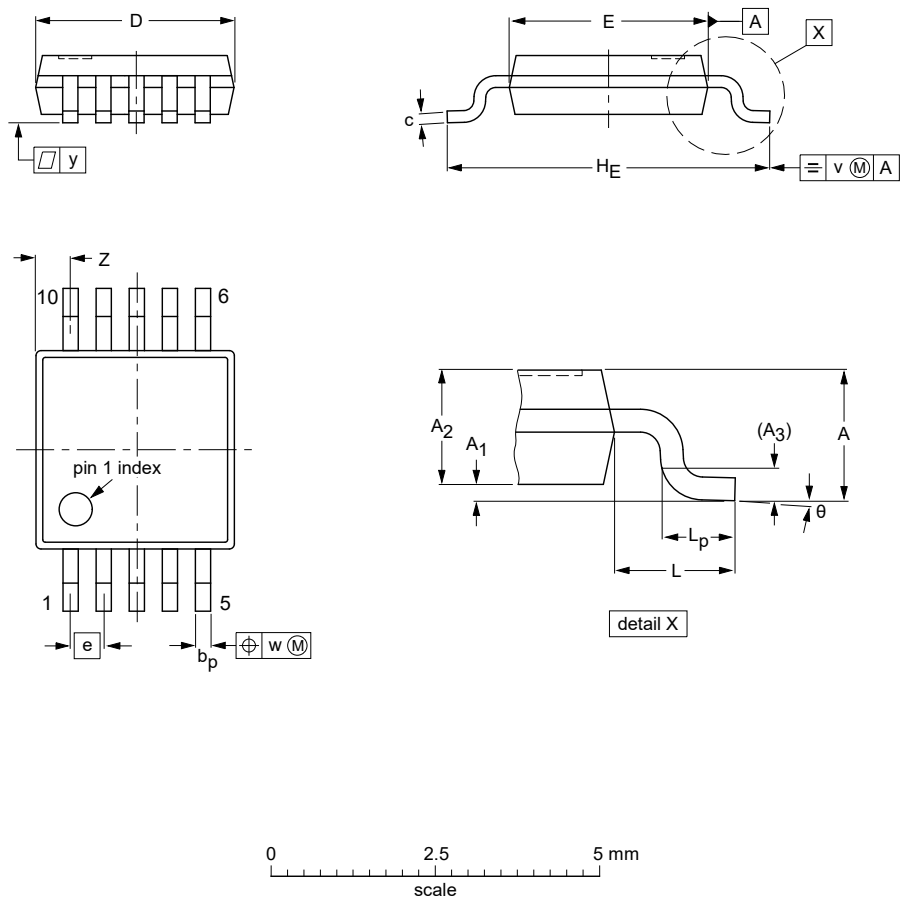
Table 12. Test data

Test	Load		Switch
	R_L	C_L	
$t_{v(Q)}$	500 Ω	50 pF	$2 \times V_{DD}$

12 Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm

SOT552-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						99-07-29 03-02-18

Figure 19. Package outline SOT552-1 (TSSOP10)

13 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 20](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#) and [Table 14](#)

Table 13. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 20](#).

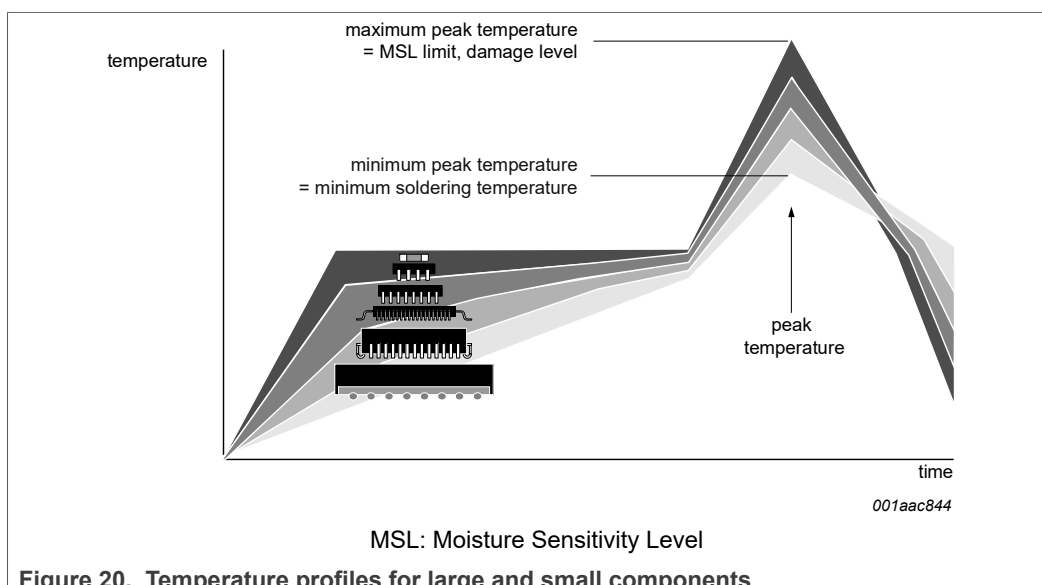


Figure 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365* "Surface mount reflow soldering description".

15 Abbreviations

Table 15. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

16 Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9537 v.7	20210908	Product data sheet	202104008A	PCA9537 v.6
Modifications	- Updated ordering information to reflect discontinuation of ATP-1 device and move to ASEN. See change notice column. - The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy.			
PCA9537 v.6	20171107	Product data sheet	201710002I	PCA9537_5
Modifications:	Table 10: Corrected V_{POR} typ and max limit - Added Section 3.1			
PCA9537_5	20090507	Product data sheet	-	PCA9537_4
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Pin names changed from "I/O0, I/O1, I/O2, I/O3" to "IO0, IO1, IO2, IO3", respectively Section 6.4, 1st sentence: changed symbol from "t_W" to "t_{W(rst)}" Figure 5: changed symbol from "t_{pV}" to "t_{v(Q)}" Figure 8: - changed symbol from "t_{ph}" to "t_{h(D)}" - changed symbol from "t_{ps}" to "t_{su(D)}" - changed symbol from "t_{iv}" to "t_{v(INT)}" - changed symbol from "t_{ir}" to "t_{rst(INT)}" Table 9: - parameter description for symbol V_{I/O} changed from "DC voltage on an I/O" to "voltage on an input/output pin" - parameter description for symbol I_{SS} changed from "supply current" to "ground supply current" - symbol/parameter changed from "I_{I/O}, DC output current on an I/O" to "I_{O(ION)}, output current on pin ION" Table 10, sub-section "Supplies": - symbol/parameter changed from "I_{stbl}, Standby current" to "I_{stbL}, LOW-level standby current" - symbol/parameter changed from "I_{stbh}, Standby current" to "I_{stbH}, HIGH-level standby current" Table 11, sub-section "Port timing": - symbol/parameter changed from "t_{pV}, Output data valid" to "t_{v(Q)}, data output valid time" - symbol/parameter changed from "t_{ps}, Input data setup time" to "t_{su(D)}, data input set-up time" - symbol/parameter changed from "t_{ph}, Input data hold time" to "t_{h(D)}, data input hold time" Table 11, sub-section "Interrupt timing": - symbol/parameter changed from "t_{iv}, Interrupt valid" to "t_{v(INT)}, valid time on pin INT" - symbol/parameter changed from "t_{ir}, Interrupt reset" to "t_{rst(INT)}, reset time on pin INT"			

Table 16. Revision history...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications (continued):	• Table 11, sub-section "RESET": – symbol changed from "t_W" to "t_{w(rst)}" – symbol changed from "t_{REC}" to "t_{rec(rst)}" – symbol/parameter changed from "t_{RESET}, Time to reset" to "t_{rst}, reset time" • Figure 14: – symbol changed from "t_W" to "t_{w(rst)}" – symbol changed from "t_{REC}" to "t_{rec(rst)}" – symbol changed from "t_{RESET}" to "t_{rst}" • Figure 15: – changed symbol from "t_{PH}" to "t_{h(D)}" – changed symbol from "t_{PS}" to "t_{su(D)}" – changed symbol from "t_{IV}" to "t_{v(INT)}" – changed symbol from "t_{IR}" to "t_{rst(INT)}" • Figure 16: changed symbol from "t_{PV}" to "t_{v(Q)}" • (Old) Figure 18, "Test circuit" split into Figure 18 and Table 12 – symbol changed from "t_{pv}" to "t_{v(Q)}" • Added soldering information • Added Table 15			
PCA9537_4	20060921	Product data sheet	-	PCA9537_3
PCA9537_3 (9397 750 14259)	20041129	Product data sheet	-	PCA9537_2
PCA9537_2 (9397 750 14052)	20040930	Objective data sheet	-	PCA9537_1
PCA9537_1 (9397 750 12894)	20040820	Objective data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

4-bit I²C-bus and SMBus low power I/O port with interrupt and reset

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for

such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	2	Tab. 8.	Register 3 - Configuration register bit description	5
Tab. 2.	Ordering options	2	Tab. 9.	Limiting values	10
Tab. 3.	Pin description	3	Tab. 10.	Static characteristics	10
Tab. 4.	Command byte	4	Tab. 11.	Dynamic characteristics	11
Tab. 5.	Register 0 - Input Port register bit description	4	Tab. 12.	Test data	15
Tab. 6.	Register 1 - Output Port register bit description	4	Tab. 13.	SnPb eutectic process (from J-STD-020D)	18
Tab. 7.	Register 2 - Polarity Inversion register bit description	5	Tab. 14.	Lead-free process (from J-STD-020D)	18
			Tab. 15.	Abbreviations	19
			Tab. 16.	Revision history	20

Figures

Fig. 1.	Block diagram of PCA9537	2	Fig. 12.	Definition of timing	13
Fig. 2.	Pin configuration for TSSOP10	3	Fig. 13.	I ² C-bus timing diagram	13
Fig. 3.	PCA9537 address	3	Fig. 14.	Definition of RESET timing	13
Fig. 4.	Simplified schematic of IO0 to IO3	7	Fig. 15.	Expanded view of read input port register	14
Fig. 5.	Write to output port register	7	Fig. 16.	Expanded view of write to output port register	14
Fig. 6.	Write to configuration or polarity inversion registers	8	Fig. 17.	Test circuitry for switching times	14
Fig. 7.	Read from register	8	Fig. 18.	Test circuit	15
Fig. 8.	Read input port register	8	Fig. 19.	Package outline SOT552-1 (TSSOP10)	16
Fig. 9.	Typical application	9	Fig. 20.	Temperature profiles for large and small components	19
Fig. 10.	High value resistor in parallel with the LED	9			
Fig. 11.	Device supplied by a lower voltage	9			

Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
3.1	Ordering options	2
4	Block diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	3
6.1	Device address	3
6.2	Registers	3
6.2.1	Command byte	4
6.2.2	Register 0 - Input Port register	4
6.2.3	Register 1 - Output Port register	4
6.2.4	Register 2 - Polarity Inversion register	5
6.2.5	Register 3 - Configuration register	5
6.3	Power-on reset	6
6.4	RESET input	6
6.5	Interrupt output	6
6.6	I/O port	6
6.7	Bus transactions	7
7	Application design-in information	9
7.1	Minimizing IDD when the I/Os are used to control LEDs	9
8	Limiting values	10
9	Static characteristics	10
10	Dynamic characteristics	11
11	Test information	14
12	Package outline	16
13	Handling information	17
14	Soldering of SMD packages	17
14.1	Introduction to soldering	17
14.2	Wave and reflow soldering	17
14.3	Wave soldering	17
14.4	Reflow soldering	18
15	Abbreviations	19
16	Revision history	20
17	Legal information	22

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[PCA9537DP,118](#) [PCA9537DPZ](#)