

# PCA21125

## SPI-bus Real-Time Clock and calendar

Rev. 2 — 25 November 2014

Product data sheet

### 1. General description

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The PCA21125 is a CMOS<sup>1</sup> Real-Time Clock (RTC) and calendar optimized for low-power consumption and an operating temperature up to 125 °C. Data is transferred via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.0 Mbit/s. Alarm and timer functions are also available with the possibility to generate a wake-up signal on the interrupt pin.

For a selection of NXP Real-Time Clocks, see [Table 46 on page 41](#)

### 2. Features and benefits

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- AEC Q100 compliant for automotive applications.
- Provides year, month, day, weekday, hours, minutes, and seconds based on 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.3 V to 5.5 V
- Low supply current: typical 0.8 µA at T<sub>amb</sub> = 25 °C
- 4-line SPI-bus with separate, but combinable data input and output
- Serial interface at V<sub>DD</sub> = 1.6 V to 5.5 V
- 1 second or 1 minute interrupt output
- Freely programmable timer with interrupt capability
- Freely programmable alarm function with interrupt capability
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- Open-drain interrupt pin

### 3. Applications

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- Automotive time keeping
- Metering

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in [Section 21](#).



## 4. Ordering information

Table 1. Ordering information

| Type number | Package |                                                                        |          |
|-------------|---------|------------------------------------------------------------------------|----------|
|             | Name    | Description                                                            | Version  |
| PCA21125T   | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

### 4.1 Ordering options

Table 2. Ordering options

| Product type number | Orderable part number | Sales item (12NC) | Delivery form          | IC revision |
|---------------------|-----------------------|-------------------|------------------------|-------------|
| PCA21125T/Q900/1    | PCA21125T/Q900/1,1    | 935290408118      | tape and reel, 13 inch | 1           |

## 5. Marking

Table 3. Marking codes

| Type number      | Marking code |
|------------------|--------------|
| PCA21125T/Q900/1 | PC21125      |

6. Block diagram

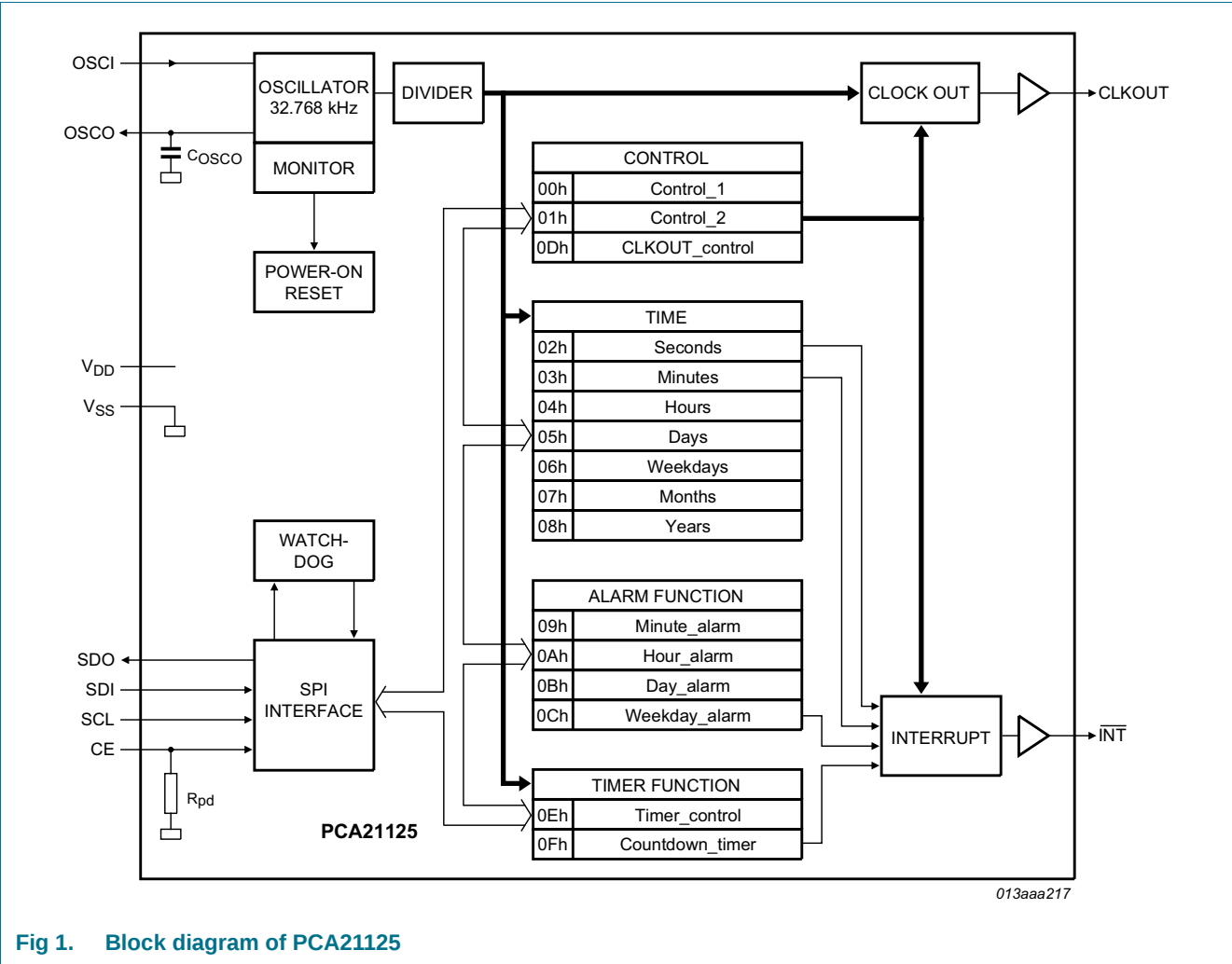
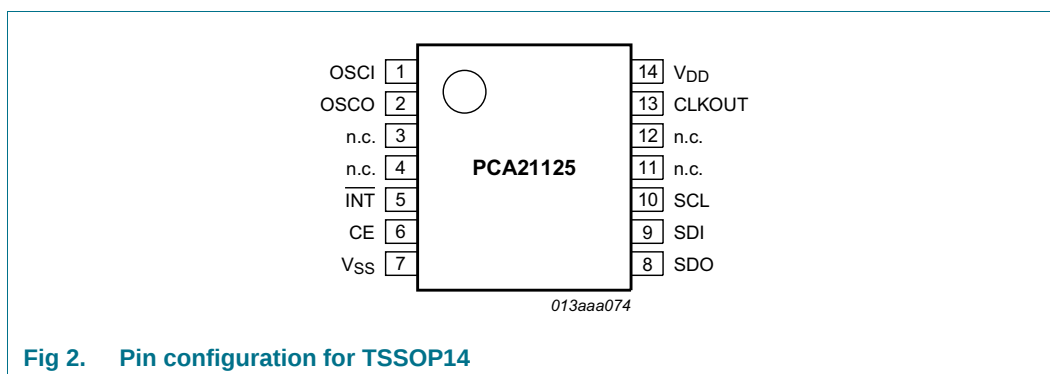


Fig 1. Block diagram of PCA21125

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

**Table 4. Pin description**

*Input or input/output pins must always be at a defined level ( $V_{SS}$  or  $V_{DD}$ ) unless otherwise specified.*

| Symbol                  | Pin    | Description                                                                                                        |
|-------------------------|--------|--------------------------------------------------------------------------------------------------------------------|
| OSCI                    | 1      | oscillator input                                                                                                   |
| OSCO                    | 2      | oscillator output                                                                                                  |
| n.c.                    | 3, 4   | not connected; do not connect and do not use as feed through; connect to $V_{DD}$ if floating pins are not allowed |
| $\overline{\text{INT}}$ | 5      | interrupt output (open-drain; active LOW)                                                                          |
| CE                      | 6      | chip enable input (active HIGH) with 200 k $\Omega$ pull-down resistor                                             |
| $V_{SS}$                | 7      | ground supply voltage                                                                                              |
| SDO                     | 8      | serial data output, push-pull                                                                                      |
| SDI                     | 9      | serial data input; might float when CE inactive                                                                    |
| SCL                     | 10     | serial clock input; might float when CE inactive                                                                   |
| n.c.                    | 11, 12 | not connected; do not connect and do not use as feed through; connect to $V_{DD}$ if floating pins are not allowed |
| CLKOUT                  | 13     | clock output (open-drain)                                                                                          |
| $V_{DD}$                | 14     | supply voltage                                                                                                     |

## 8. Functional description

The PCA21125 contains 16 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the RTC, a programmable clock output, and a 6 MHz SPI-bus.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented:

- The first two registers at addresses 00h and 01h (Control\_1 and Control\_2) are used as control and status registers.
- Registers at addresses 02h to 08h (Seconds, Minutes, Hours, Days, Weekdays, Months, Years) are used as counters for the clock function. Seconds, minutes, hours, days, months, and years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all counters are frozen. Therefore, faulty writing or reading of time and date during a carry condition is prevented.
- Registers at addresses 09h to 0Ch (Minute\_alarm, Hour\_alarm, Day\_alarm, and Weekday\_alarm) define the alarm condition.
- The register at address 0Dh (CLKOUT\_control) defines the clock output mode.
- Registers at addresses 0Eh and 0Fh (Timer\_control and Countdown\_timer) are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see [Table 30](#)). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control\_2 (01h).

## 8.1 Register overview

The time, date, and alarm registers are encoded in BCD to simplify application use. Other registers are either bit-wise or standard binary.

**Table 5. Register overview**

Bits labeled - are not implemented and return logic 0 when read. Bit positions labeled N should always be written with logic 0. After reset, all registers are set according to [Table 38 on page 26](#).

| Address                      | Register name   | Bit             |                        |                                      |                                      |          |                        |          |     |
|------------------------------|-----------------|-----------------|------------------------|--------------------------------------|--------------------------------------|----------|------------------------|----------|-----|
|                              |                 | 7               | 6                      | 5                                    | 4                                    | 3        | 2                      | 1        | 0   |
| Control and status registers |                 |                 |                        |                                      |                                      |          |                        |          |     |
| 00h                          | Control_1       | EXT_TEST        | N                      | STOP                                 | N                                    | POR_OVRD | 12_24                  | N        | N   |
| 01h                          | Control_2       | MI              | SI                     | MSF                                  | TI_TP                                | AF       | TF                     | AIE      | TIE |
| Time and date registers      |                 |                 |                        |                                      |                                      |          |                        |          |     |
| 02h                          | Seconds         | RF              | SECONDS (0 to 59)      |                                      |                                      |          |                        |          |     |
| 03h                          | Minutes         | -               | MINUTES (0 to 59)      |                                      |                                      |          |                        |          |     |
| 04h                          | Hours           | -               | -                      | AMPM                                 | HOURS (1 to 12) in 12-hour mode      |          |                        |          |     |
|                              |                 | -               | -                      | HOURS (0 to 23) in 24-hour mode      |                                      |          |                        |          |     |
| 05h                          | Days            | -               | -                      | DAYS (1 to 31)                       |                                      |          |                        |          |     |
| 06h                          | Weekdays        | -               | -                      | -                                    | -                                    | -        | WEEKDAYS (0 to 6)      |          |     |
| 07h                          | Months          | -               | -                      | -                                    | MONTHS (1 to 12)                     |          |                        |          |     |
| 08h                          | Years           | YEARS (0 to 99) |                        |                                      |                                      |          |                        |          |     |
| Alarm registers              |                 |                 |                        |                                      |                                      |          |                        |          |     |
| 09h                          | Minute_alarm    | AEN_M           | MINUTE_ALARM (0 to 59) |                                      |                                      |          |                        |          |     |
| 0Ah                          | Hour_alarm      | AEN_H           | -                      | AMPM                                 | HOUR_ALARM (1 to 12) in 12-hour mode |          |                        |          |     |
|                              |                 |                 | -                      | HOUR_ALARM (0 to 23) in 24-hour mode |                                      |          |                        |          |     |
| 0Bh                          | Day_alarm       | AEN_D           | -                      | DAY_ALARM (1 to 31)                  |                                      |          |                        |          |     |
| 0Ch                          | Weekday_alarm   | AEN_W           | -                      | -                                    | -                                    | -        | WEEKDAY_ALARM (0 to 6) |          |     |
| CLKOUT control register      |                 |                 |                        |                                      |                                      |          |                        |          |     |
| 0Dh                          | CLKOUT_control  | -               | -                      | -                                    | -                                    | -        | COF[2:0]               |          |     |
| Timer registers              |                 |                 |                        |                                      |                                      |          |                        |          |     |
| 0Eh                          | Timer_control   | TE              | -                      | -                                    | -                                    | -        | -                      | CTD[1:0] |     |
| 0Fh                          | Countdown_timer | T[7:0]          |                        |                                      |                                      |          |                        |          |     |

## 8.2 Control and status registers

### 8.2.1 Register Control\_1

Table 6. Control\_1 - control and status register 1 (address 00h) bit description

| Bit    | Symbol   | Value            | Description                                                                                      | Reference                                             |
|--------|----------|------------------|--------------------------------------------------------------------------------------------------|-------------------------------------------------------|
| 7      | EXT_TEST | 0 <sup>[1]</sup> | normal mode                                                                                      | <a href="#">Section 8.8</a>                           |
|        |          | 1                | external clock test mode                                                                         |                                                       |
| 6      | N        | 0                | unused                                                                                           | -                                                     |
| 5      | STOP     | 0 <sup>[1]</sup> | RTC source clock runs                                                                            | <a href="#">Section 8.9</a>                           |
|        |          | 1                | RTC clock is stopped <sup>[2]</sup>                                                              |                                                       |
| 4      | N        | 0                | unused                                                                                           | -                                                     |
| 3      | POR_OVRD | 0                | Power-On Reset Override facility is disabled;<br><b>Remark:</b> set logic 0 for normal operation | <a href="#">Section 8.10.1</a>                        |
|        |          | 1 <sup>[1]</sup> | Power-On Reset Override sequence reception enabled                                               |                                                       |
| 2      | 12_24    | 0 <sup>[1]</sup> | 24-hour mode selected                                                                            | <a href="#">Table 11</a> and <a href="#">Table 19</a> |
|        |          | 1                | 12-hour mode selected                                                                            |                                                       |
| 1 to 0 | N        | 00               | unused                                                                                           | -                                                     |

[1] Default value.

[2] CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available; divider chain flip-flops are asynchronously set logic 0.

### 8.2.2 Register Control\_2

Table 7. Control\_2 - control and status register 2 (address 01h) bit description

| Bit | Symbol | Value            | Description                                                                              | Reference                                                                   |
|-----|--------|------------------|------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 7   | MI     | 0 <sup>[1]</sup> | minute interrupt disabled                                                                | <a href="#">Section 8.6.1</a>                                               |
|     |        | 1                | minute interrupt enabled                                                                 |                                                                             |
| 6   | SI     | 0 <sup>[1]</sup> | second interrupt disabled                                                                | <a href="#">Section 8.6.1</a>                                               |
|     |        | 1                | second interrupt enabled                                                                 |                                                                             |
| 5   | MSF    | 0 <sup>[1]</sup> | no minute or second interrupt generated                                                  | <a href="#">Section 8.6.1</a>                                               |
|     |        | 1                | flag set when minute or second interrupt generated                                       |                                                                             |
| 4   | TI_TP  | 0 <sup>[1]</sup> | interrupt pin follows TF and MSF (see <a href="#">Figure 9</a> )                         | <a href="#">Section 8.6</a> et seq. and <a href="#">Section 8.7</a> et seq. |
|     |        | 1                | interrupt pin generates a pulse                                                          |                                                                             |
| 3   | AF     | 0 <sup>[1]</sup> | no alarm interrupt generated                                                             | <a href="#">Section 8.4.5</a>                                               |
|     |        | 1                | flag set when alarm triggered;<br><b>Remark:</b> flag must be cleared to clear interrupt |                                                                             |
| 2   | TF     | 0 <sup>[1]</sup> | no countdown timer interrupt generated                                                   | <a href="#">Section 8.6</a> et seq. and <a href="#">Section 8.7</a> et seq. |
|     |        | 1                | flag set when countdown timer interrupt generated                                        |                                                                             |
| 1   | AIE    | 0 <sup>[1]</sup> | no interrupt generated from alarm flag                                                   | <a href="#">Section 8.7.3</a>                                               |
|     |        | 1                | interrupt generated when alarm flag set                                                  |                                                                             |
| 0   | TIE    | 0 <sup>[1]</sup> | no interrupt generated from countdown timer flag                                         | <a href="#">Section 8.7</a>                                                 |
|     |        | 1                | interrupt generated when countdown timer flag set                                        |                                                                             |

[1] Default value.

### 8.3 Time and date registers

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for register Seconds in [Table 9](#).

Loading these registers with values outside of the given range results in unpredictable time and date generation (see [Figure 3 "Data flow of the time function"](#)).

#### 8.3.1 Register Seconds

**Table 8. Seconds - seconds and clock integrity status register (address 02h) bit description**

| Bit    | Symbol  | Value            | Description                                                                               |
|--------|---------|------------------|-------------------------------------------------------------------------------------------|
| 7      | RF      | 0                | clock integrity is guaranteed                                                             |
|        |         | 1 <sup>[1]</sup> | clock integrity is not guaranteed;<br>chip reset has occurred since flag was last cleared |
| 6 to 4 | SECONDS | 0 to 5           | ten's place                                                                               |
| 3 to 0 |         | 0 to 9           | unit place                                                                                |

[1] Start-up value.

**Table 9. Seconds coded in BCD format**

| Seconds value in decimal | Upper-digit (ten's place) |       |       | Digit (unit place) |       |       |       |
|--------------------------|---------------------------|-------|-------|--------------------|-------|-------|-------|
|                          | Bit 6                     | Bit 5 | Bit 4 | Bit 3              | Bit 2 | Bit 1 | Bit 0 |
| 00                       | 0                         | 0     | 0     | 0                  | 0     | 0     | 0     |
| 01                       | 0                         | 0     | 0     | 0                  | 0     | 0     | 1     |
| 02                       | 0                         | 0     | 0     | 0                  | 0     | 1     | 0     |
| :                        | :                         | :     | :     | :                  | :     | :     | :     |
| 09                       | 0                         | 0     | 0     | 1                  | 0     | 0     | 1     |
| 10                       | 0                         | 0     | 1     | 0                  | 0     | 0     | 0     |
| :                        | :                         | :     | :     | :                  | :     | :     | :     |
| 58                       | 1                         | 0     | 1     | 1                  | 0     | 0     | 0     |
| 59                       | 1                         | 0     | 1     | 1                  | 0     | 0     | 1     |

#### 8.3.2 Register Minutes

**Table 10. Minutes - minutes register (address 03h) bit description**

| Bit    | Symbol  | Value  | Description |
|--------|---------|--------|-------------|
| 7      | -       | 0      | unused      |
| 6 to 4 | MINUTES | 0 to 5 | ten's place |
| 3 to 0 |         | 0 to 9 | unit place  |

### 8.3.3 Register Hours

**Table 11. Hours - hours register (address 04h) bit description**

| Bit                         | Symbol | Value  | Description  |
|-----------------------------|--------|--------|--------------|
| 7 to 6                      | -      | 00     | unused       |
| 12-hour mode <sup>[1]</sup> |        |        |              |
| 5                           | AMPM   | 0      | indicates AM |
|                             |        | 1      | indicates PM |
| 4                           | HOURS  | 0 to 1 | ten's place  |
| 3 to 0                      |        | 0 to 9 | unit place   |
| 24-hour mode <sup>[1]</sup> |        |        |              |
| 5 to 4                      | HOURS  | 0 to 2 | ten's place  |
| 3 to 0                      |        | 0 to 9 | unit place   |

[1] Hour mode is set by bit 12\_24 in register Control\_1 (see [Table 6](#)).

### 8.3.4 Register Days

**Table 12. Days - days register (address 05h) bit description**

| Bit    | Symbol              | Value  | Place value | Description                    |
|--------|---------------------|--------|-------------|--------------------------------|
| 7 to 6 | -                   | 00     | -           | unused                         |
| 5 to 4 | DAYS <sup>[1]</sup> | 0 to 3 | ten's place | actual day coded in BCD format |
| 3 to 0 |                     | 0 to 9 | unit place  |                                |

[1] The PCA21125 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

### 8.3.5 Register Weekdays

**Table 13. Weekdays - weekdays register (address 06h) bit description**

| Bit    | Symbol   | Value  | Description                                         |
|--------|----------|--------|-----------------------------------------------------|
| 7 to 3 | -        | 00000  | unused                                              |
| 2 to 0 | WEEKDAYS | 0 to 6 | actual weekday, values see <a href="#">Table 14</a> |

**Table 14. Weekday assignments**

| Day <sup>[1]</sup> | Bit |   |   |
|--------------------|-----|---|---|
|                    | 2   | 1 | 0 |
| Sunday             | 0   | 0 | 0 |
| Monday             | 0   | 0 | 1 |
| Tuesday            | 0   | 1 | 0 |
| Wednesday          | 0   | 1 | 1 |
| Thursday           | 1   | 0 | 0 |
| Friday             | 1   | 0 | 1 |
| Saturday           | 1   | 1 | 0 |

[1] Definition may be reassigned by the user.

### 8.3.6 Register Months

**Table 15. Months - months register (address 07h) bit description**

| Bit    | Symbol | Value  | Description |
|--------|--------|--------|-------------|
| 7 to 5 | -      | 000    | unused      |
| 4      | MONTHS | 0 to 1 | ten's place |
| 3 to 0 |        | 0 to 9 | unit place  |

**Table 16. Month assignments in BCD format**

| Month     | Upper-digit<br>(ten's place) | Digit (unit place) |       |       |       |
|-----------|------------------------------|--------------------|-------|-------|-------|
|           | Bit 4                        | Bit 3              | Bit 2 | Bit 1 | Bit 0 |
| January   | 0                            | 0                  | 0     | 0     | 1     |
| February  | 0                            | 0                  | 0     | 1     | 0     |
| March     | 0                            | 0                  | 0     | 1     | 1     |
| April     | 0                            | 0                  | 1     | 0     | 0     |
| May       | 0                            | 0                  | 1     | 0     | 1     |
| June      | 0                            | 0                  | 1     | 1     | 0     |
| July      | 0                            | 0                  | 1     | 1     | 1     |
| August    | 0                            | 1                  | 0     | 0     | 0     |
| September | 0                            | 1                  | 0     | 0     | 1     |
| October   | 1                            | 0                  | 0     | 0     | 0     |
| November  | 1                            | 0                  | 0     | 0     | 1     |
| December  | 1                            | 0                  | 0     | 1     | 0     |

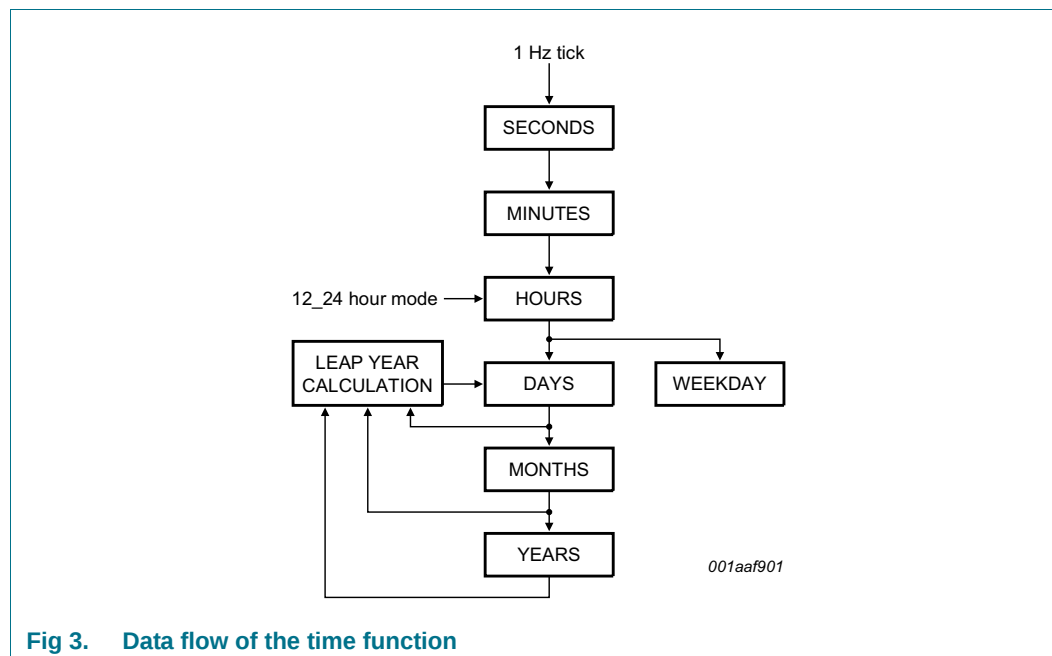
### 8.3.7 Register Years

**Table 17. Years - years register (08h) bit description**

| Bit    | Symbol | Value  | Place value | Description                     |
|--------|--------|--------|-------------|---------------------------------|
| 7 to 4 | YEARS  | 0 to 9 | ten's place | actual year coded in BCD format |
| 3 to 0 |        | 0 to 9 | unit place  |                                 |

### 8.3.8 Setting and reading the time

[Figure 3](#) shows the data flow and data dependencies starting from the 1 Hz clock tick.



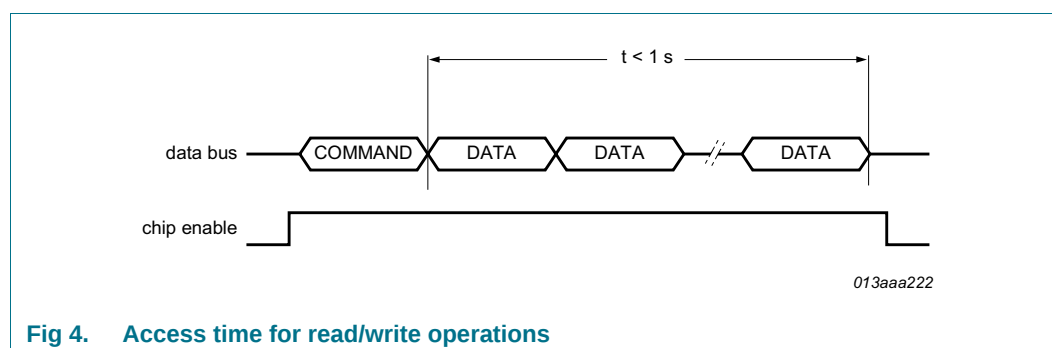
**Fig 3. Data flow of the time function**

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see [Figure 4](#)).



**Fig 4. Access time for read/write operations**

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

## 8.4 Alarm registers

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AEN\_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday value.

### 8.4.1 Register Minute\_alarm

**Table 18. Minute\_alarm - minute alarm register (address 09h) bit description**

| Bit    | Symbol       | Value            | Place value | Description                                  |
|--------|--------------|------------------|-------------|----------------------------------------------|
| 7      | AEN_M        | 0                | -           | minute alarm is enabled                      |
|        |              | 1 <sup>[1]</sup> | -           | minute alarm is disabled                     |
| 6 to 4 | MINUTE_ALARM | 0 to 5           | ten's place | minute alarm information coded in BCD format |
| 3 to 0 |              | 0 to 9           | unit place  |                                              |

[1] Default value.

### 8.4.2 Register Hour\_alarm

**Table 19. Hour\_alarm - hour alarm register (address 0Ah) bit description**

| Bit                         | Symbol     | Value            | Description            |
|-----------------------------|------------|------------------|------------------------|
| 7                           | AEN_H      | 0                | hour alarm is enabled  |
|                             |            | 1 <sup>[1]</sup> | hour alarm is disabled |
| 6                           | -          | 0                | unused                 |
| 12-hour mode <sup>[2]</sup> |            |                  |                        |
| 5                           | AMPM       | 0                | indicates AM           |
|                             |            | 1                | indicates PM           |
| 4                           | HOUR_ALARM | 0 to 1           | ten's place            |
| 3 to 0                      |            | 0 to 9           | unit place             |
| 24-hour mode <sup>[2]</sup> |            |                  |                        |
| 5 to 4                      | HOURS      | 0 to 2           | ten's place            |
| 3 to 0                      |            | 0 to 9           | unit place             |

[1] Default value.

[2] Hour mode is set by bit 12\_24 in register Control\_1 (see [Table 6](#)).

### 8.4.3 Register Day\_alarm

Table 20. Day\_alarm - day alarm register (address 0Bh) bit description

| Bit    | Symbol    | Value            | Place value | Description                               |
|--------|-----------|------------------|-------------|-------------------------------------------|
| 7      | AEN_D     | 0                | -           | day alarm is enabled                      |
|        |           | 1 <sup>[1]</sup> | -           | day alarm is disabled                     |
| 6      | -         | 0                | -           | unused                                    |
| 5 to 4 | DAY_ALARM | 0 to 3           | ten's place | day alarm information coded in BCD format |
| 3 to 0 |           | 0 to 9           | unit place  |                                           |

[1] Default value.

### 8.4.4 Register Weekday\_alarm

Table 21. Weekday\_alarm - weekday alarm register (address 0Ch) bit description

| Bit    | Symbol        | Value            | Description                                   |
|--------|---------------|------------------|-----------------------------------------------|
| 7      | AEN_W         | 0                | weekday alarm is enabled                      |
|        |               | 1 <sup>[1]</sup> | weekday alarm is disabled                     |
| 6 to 3 | -             | 0000             | unused                                        |
| 2 to 0 | WEEKDAY_ALARM | 0 to 6           | weekday alarm information coded in BCD format |

[1] Default value.

### 8.4.5 Alarm flag

By clearing the MSB, AEN\_X (Alarm Enable), of one or more of the alarm registers the corresponding alarm condition(s) are active. When an alarm occurs, AF (register Control\_2, see Table 7) is set logic 1. The asserted AF can be used to generate an interrupt (INT). The AF is cleared by command.

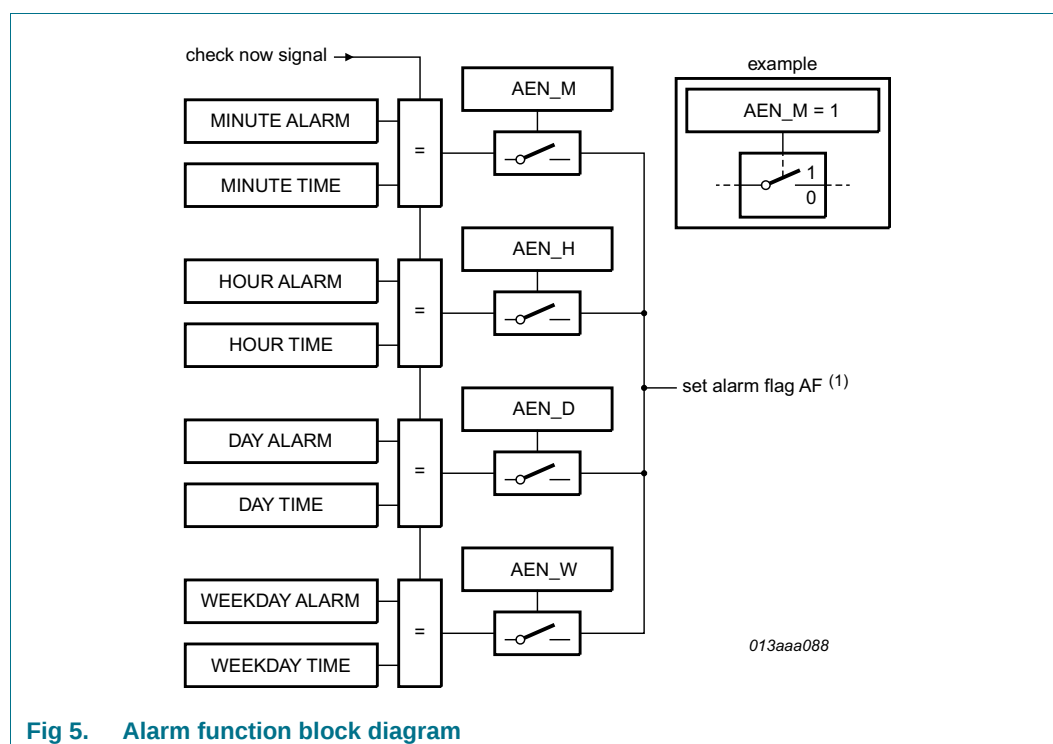


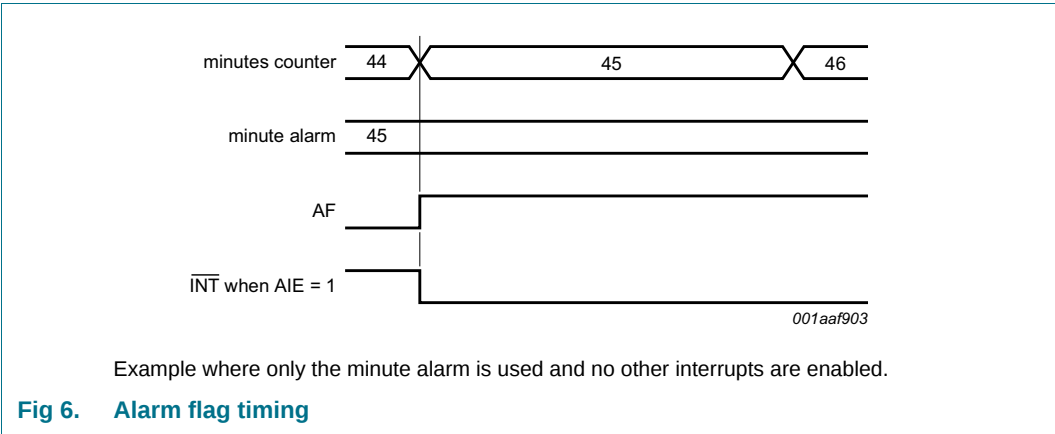
Fig 5. Alarm function block diagram

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day, or weekday, and its corresponding Alarm Enable bit (AEN\_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control\_2, see [Table 7](#)). If bit AIE is enabled, the INT pin follows the condition of bit AF. AF remains set until cleared by the interface. Once AF has been cleared, it is only set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN\_X bit logic 1 are ignored.

Generation of interrupts from the alarm function is described in [Section 8.7.3](#).

[Figure 6](#), [Table 22](#) and [Table 23](#) show an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.



**Fig 6. Alarm flag timing**

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

**Table 22. Flag location in register Control\_2**

| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | MSF   | -     | AF    | TF    | -     | -     |

[Table 23](#) shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

**Table 23. Example to clear only AF (bit 3) in register Control\_2**

| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | 1     | -     | 0     | 1     | -     | -     |

## 8.5 Register CLKOUT\_control and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by control bits COF[2:0] in register CLKOUT\_control (0Dh); see [Table 24](#). Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

**Table 24. CLKOUT\_control - CLKOUT control register (address 0Dh) bit description**

| Bit    | Symbol   | Value                        | Description                    |
|--------|----------|------------------------------|--------------------------------|
| 7 to 3 | -        | 00000                        | unused                         |
| 2 to 0 | COF[2:0] | see <a href="#">Table 25</a> | frequency output at pin CLKOUT |

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is LOW.

The duty cycle of the selected clock is not controlled, but due to the nature of the clock generation, all clock frequencies, except 32.768 kHz, have a duty cycle of 50 : 50.

The stop function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details, see [Section 8.9](#).

**Table 25. CLKOUT frequency selection**

| Bits COF[2:0]      | CLKOUT frequency (Hz) | Typical duty cycle <sup>[1]</sup> (%) | Effect of STOP |
|--------------------|-----------------------|---------------------------------------|----------------|
| 000 <sup>[2]</sup> | 32768                 | 60 : 40 to 40 : 60                    | no effect      |
| 001                | 16384                 | 50 : 50                               | no effect      |
| 010                | 8192                  | 50 : 50                               | no effect      |
| 011                | 4096                  | 50 : 50                               | CLKOUT = LOW   |
| 100                | 2048                  | 50 : 50                               | CLKOUT = LOW   |
| 101                | 1024                  | 50 : 50                               | CLKOUT = LOW   |
| 110                | 1                     | 50 : 50                               | CLKOUT = LOW   |
| 111                | CLKOUT = LOW          |                                       |                |

[1] Duty cycle definition: HIGH-level time (%) : LOW-level time (%).

[2] Default value.

## 8.6 Timer registers

The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see [Table 30](#)). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute.

Registers Control\_2 (01h), Timer\_control (0Eh), and Countdown\_timer (0Fh) are used to control the timer function and output.

Table 26. Timer\_control - timer control register (address 0Eh) bit description

| Bit    | Symbol   | Value             | Description                            | Reference     |
|--------|----------|-------------------|----------------------------------------|---------------|
| 7      | TE       | 0 <sup>[1]</sup>  | countdown timer is disabled            | Section 8.6.2 |
|        |          | 1                 | countdown timer is enabled             |               |
| 6 to 2 | -        | 00000             | unused                                 |               |
| 1 to 0 | CTD[1:0] | 00                | 4.096 kHz countdown timer source clock |               |
|        |          | 01                | 64 Hz countdown timer source clock     |               |
|        |          | 10                | 1 Hz countdown timer source clock      |               |
|        |          | 11 <sup>[1]</sup> | 1/60 Hz countdown timer source clock   |               |

[1] Default value.

Table 27. Countdown\_timer - countdown timer register (address 0Fh) bit description

| Bit    | Symbol | Value     | Description                          | Reference     |
|--------|--------|-----------|--------------------------------------|---------------|
| 7 to 0 | T[7:0] | 0h to FFh | countdown timer value <sup>[1]</sup> | Section 8.6.2 |

[1] Countdown period in seconds:  $CountdownPeriod = \frac{T}{SourceClockFrequency}$  where T is the countdown value.

### 8.6.1 Second and minute interrupt

The second and minute interrupts (bits SI and MI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently of one another, however a minute interrupt enabled on top of a second interrupt is not distinguishable since it occurs at the same time; see Figure 7.

The minute and second flag (MSF) is set logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the INT pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an INT pulse will still be generated.

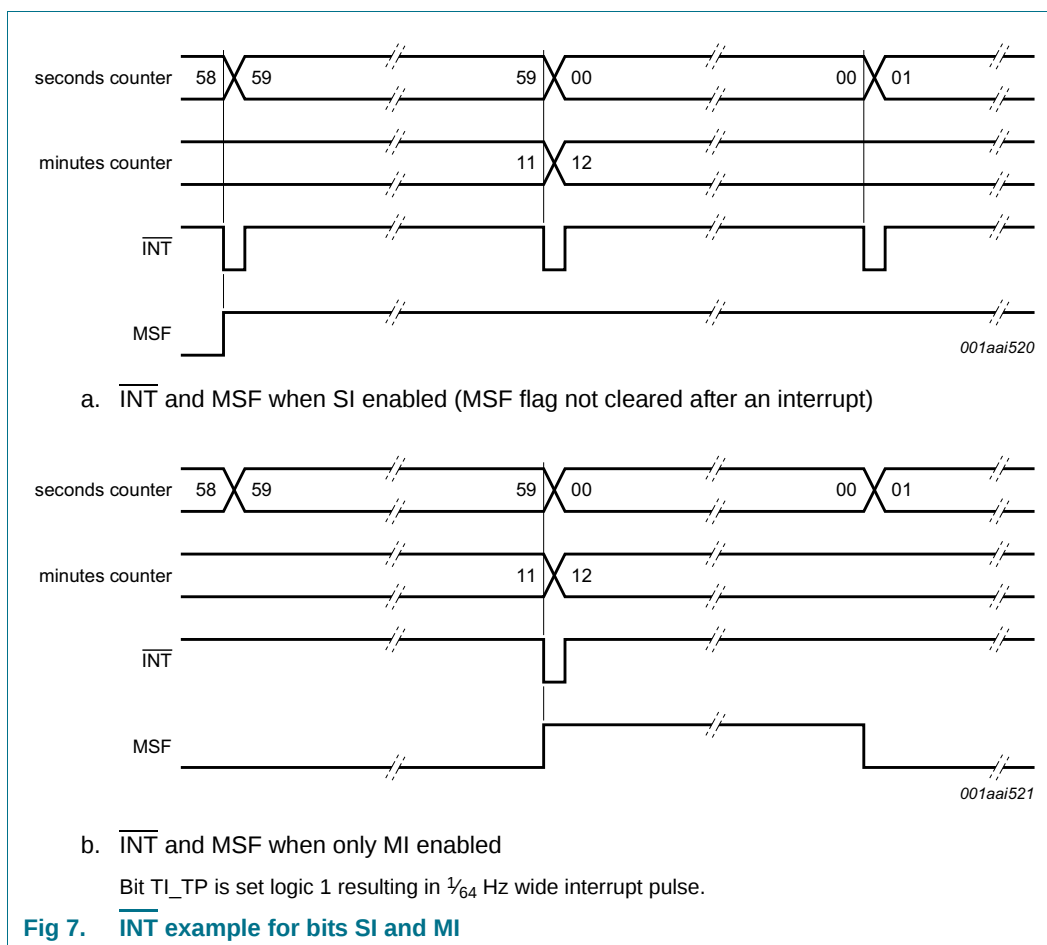
Table 28. Effect of bits MI and SI on INT generation

| Minute interrupt (bit MI) | Second interrupt (bit SI) | Result                       |
|---------------------------|---------------------------|------------------------------|
| 0                         | 0                         | no interrupt generated       |
| 1                         | 0                         | an interrupt once per minute |
| 0                         | 1                         | an interrupt once per second |
| 1                         | 1                         | an interrupt once per second |

Table 29. Effect of bits MI and SI on bit MSF

| Minute interrupt (bit MI) | Second interrupt (bit SI) | Result                                                        |
|---------------------------|---------------------------|---------------------------------------------------------------|
| 0                         | 0                         | MSF never set                                                 |
| 1                         | 0                         | MSF set when <b>minutes</b> counter increments <sup>[1]</sup> |
| 0                         | 1                         | MSF set when <b>seconds</b> counter increments                |
| 1                         | 1                         | MSF set when <b>seconds</b> counter increments                |

[1] If bit MI = 1 and bit SI = 0, bit MSF is cleared automatically after 1 second.



The purpose of the flag is to allow the controlling system to interrogate the PCA21125 and identify the source of the interrupt such as the minute/second or countdown timer.

### 8.6.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or  $\frac{1}{60}$  Hz) and enables or disables the timer.

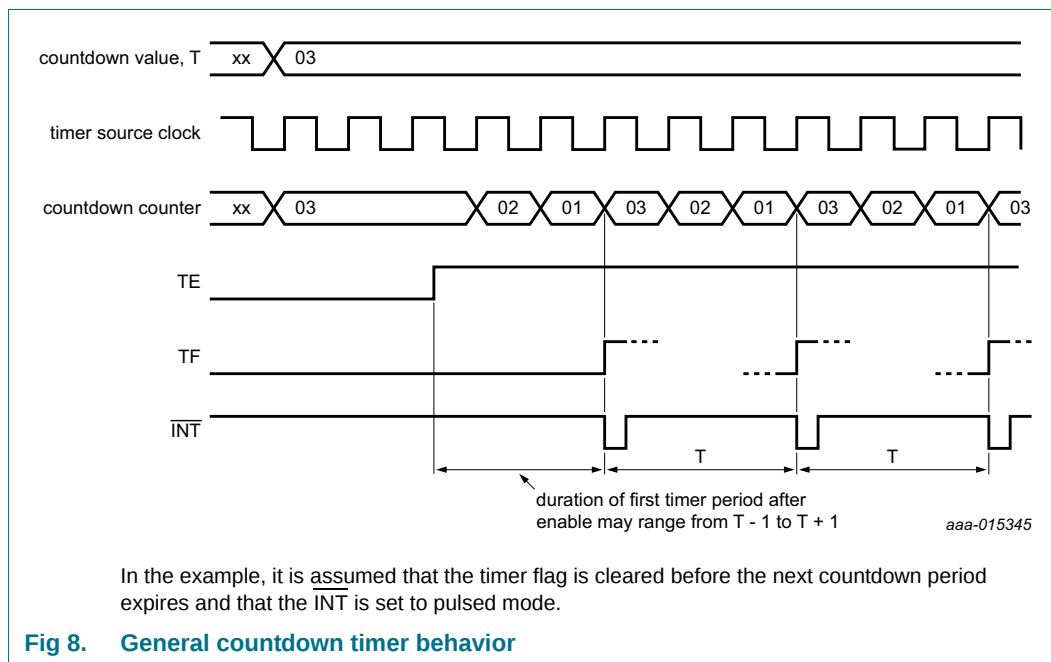
**Table 30. CTD[1:0] for timer frequency selection and countdown timer durations**

| CTD[1:0] | Timer source clock frequency | Delay                           |                                   |
|----------|------------------------------|---------------------------------|-----------------------------------|
|          |                              | Minimum timer duration<br>T = 1 | Maximum timer duration<br>T = 255 |
| 00       | 4.096 kHz                    | 244 $\mu$ s                     | 62.256 ms                         |
| 01       | 64 Hz                        | 15.625 ms                       | 3.984 s                           |
| 10       | 1 Hz                         | 1 s                             | 255 s                             |
| 11       | $\frac{1}{60}$ Hz            | 60 s <sup>[1]</sup>             | 4 h 15 min                        |

[1] When not in use, CTD[1:0] must be set to  $\frac{1}{60}$  Hz for power saving.

**Remark:** Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in a corresponding deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value  $T$ . Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF in register Control\_2, see [Table 7](#)) will be set and the counter automatically reloads and starts the next timer period. Reading the timer returns the current value of the countdown counter; see [Figure 8](#).



**Fig 8. General countdown timer behavior**

If a new value of  $T$  is written before the end of the current timer period, then this new value takes immediate effect. It is not recommended to change  $T$  without first disabling the counter (by setting bit  $TE = 0$ ). The update of  $T$  is asynchronous with the timer clock, therefore changing it without setting bit  $TE = 0$  results in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value  $T$  will however be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on  $\overline{INT}$  is generated, if this mode is enabled. See [Section 8.7.2](#) for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous with the timer source clock. Subsequent timer periods have no such delay. The amount of delay for the first timer period depends on the chosen source clock; see [Table 31](#).

**Table 31. First period delay for timer counter value  $T$**

| Timer source clock        | Minimum timer period                | Maximum timer period          |
|---------------------------|-------------------------------------|-------------------------------|
| 4.096 kHz                 | $T$                                 | $T + 1$                       |
| 64 Hz                     | $T$                                 | $T + 1$                       |
| 1 Hz                      | $(T - 1) + \frac{1}{64} \text{ Hz}$ | $T + \frac{1}{64} \text{ Hz}$ |
| $\frac{1}{60} \text{ Hz}$ | $(T - 1) + \frac{1}{64} \text{ Hz}$ | $T + \frac{1}{64} \text{ Hz}$ |

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt (INT). The interrupt can be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI\_TP is used to control this mode selection and the interrupt output can be disabled with bit TIE.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

### 8.6.3 Timer flags

When a minute or second interrupt occurs, bit MSF (register Control\_2, see [Table 7](#)) is set logic 1. Similarly, at the end of a timer countdown bit TF is set logic 1. These bits maintain their value until overwritten by command. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Three examples are given for clearing the flags. Flags MSF and TF are cleared by a write command, therefore bits 7, 6, 4, 1, and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.

**Table 32. Flag location in register Control\_2**

| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | MSF   | -     | AF    | TF    | -     | -     |

[Table 33](#), [Table 34](#), and [Table 35](#) show what instruction must be sent to clear the appropriate flag.

**Table 33. Example to clear only TF (bit 2) in register Control\_2**

| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | 1     | -     | 1     | 0     | -     | -     |

**Table 34. Example to clear only MSF (bit 5) in register Control\_2**

| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | 0     | -     | 1     | 1     | -     | -     |

**Table 35. Example to clear both TF and MSF (bits 2 and 5) in register Control\_2**

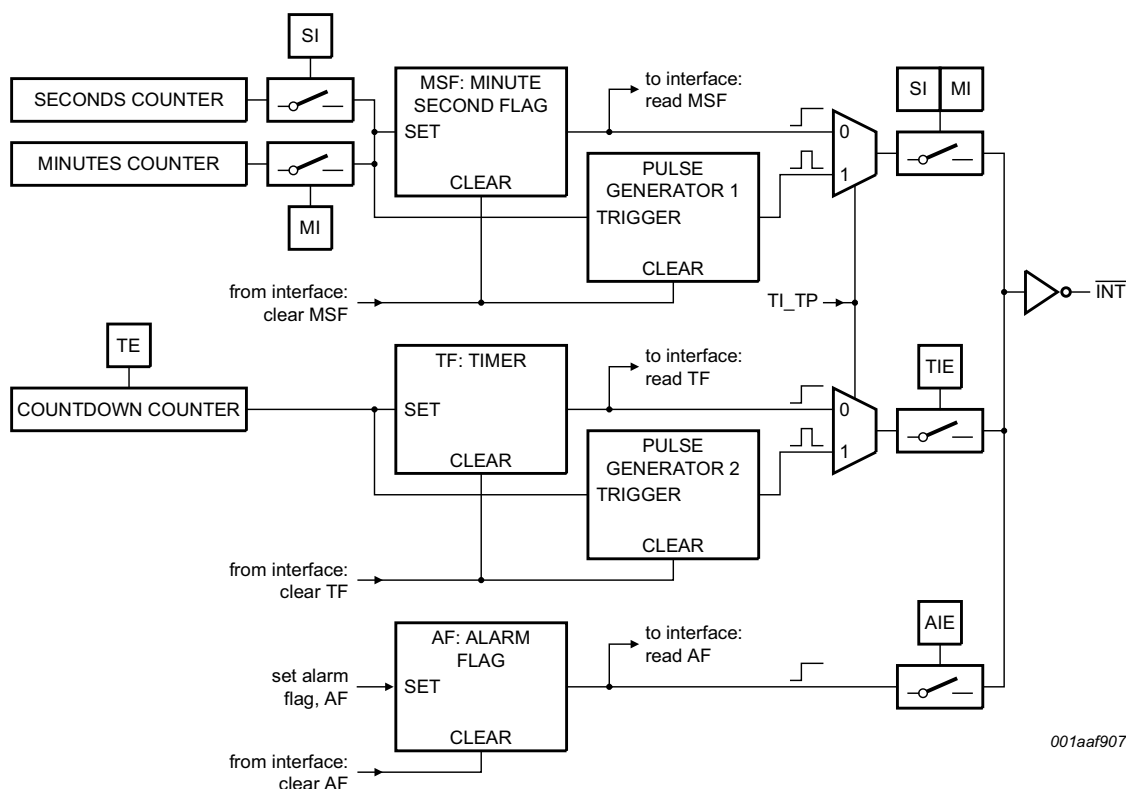
| Register  | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Control_2 | -     | -     | 0     | -     | 1     | 0     | -     | -     |

Clearing the alarm flag (bit AF) operates in the same way; see [Section 8.4.5](#).

## 8.7 Interrupt output

An active LOW interrupt signal is available at pin  $\overline{\text{INT}}$ . Operation is controlled via the bits of register Control\_2. Interrupts can be sourced from three places: second/minute timer, countdown timer, and alarm function.

Bit TI\_TP configures the timer generated interrupts to be either a pulse or to follow the status of the interrupt flags (bits TF and MSF).



When bits SI, MI, TIE and AIE are all disabled, pin  $\overline{\text{INT}}$  remains high-impedance.

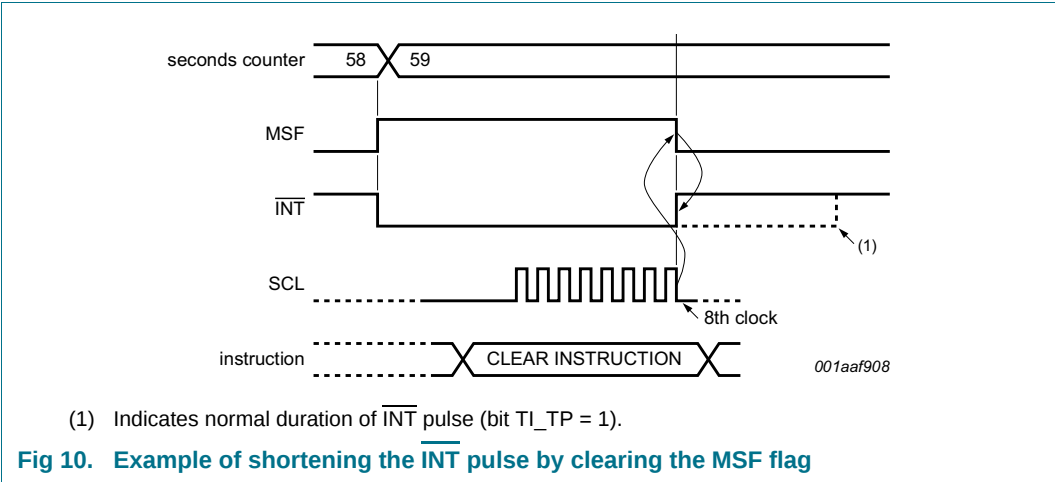
**Fig 9.** Interrupt scheme

**Remark:** Note that the interrupts from the three groups are wired-OR, meaning they will mask one another; see [Figure 9](#).

### 8.7.1 Minute and second interrupts

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of  $\frac{1}{64}$  second duration.

If the MSF flag is clear before the end of the  $\overline{\text{INT}}$  pulse, then the  $\overline{\text{INT}}$  pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see [Figure 10](#). Instructions for clearing MSF are given in [Section 8.6.3](#).



The timing shown for clearing bit MSF in [Figure 10](#) is also valid for the non-pulsed interrupt mode, i.e., when bit  $\text{TI\_TP} = 0$ , where the pulse can be shortened by setting both bits MI and SI logic 0.

8.7.2 Countdown timer interrupts

Generation of interrupts from the countdown timer is controlled via bit TIE (register Control\_2, see [Table 7](#)).

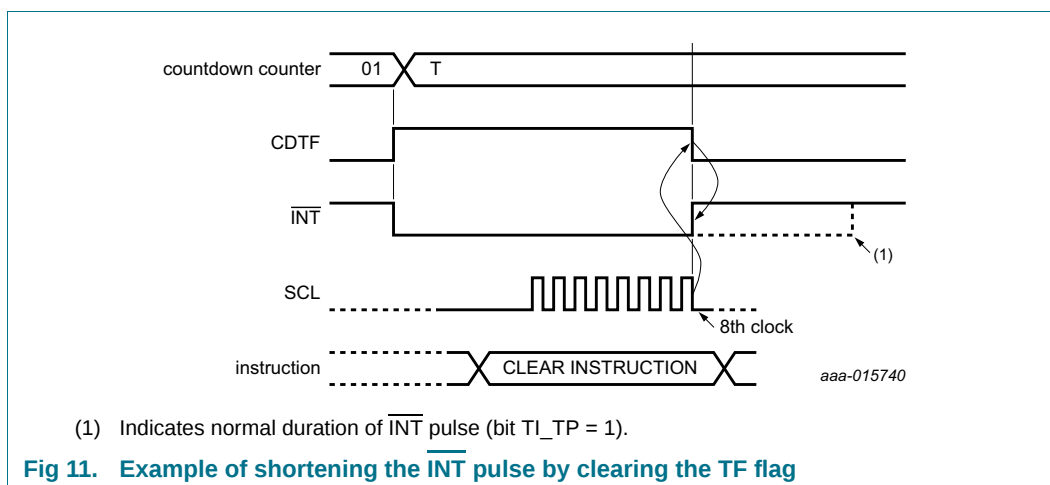
The pulse generator for the countdown timer interrupt also uses an internal clock which is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies; see [Table 36](#).

Table 36.  $\overline{\text{INT}}$  operation (bit  $\text{TI\_TP} = 1$ )

| Source clock (Hz) | $\overline{\text{INT}}$ period (s) |                  |
|-------------------|------------------------------------|------------------|
|                   | $T = 1$ <sup>[1]</sup>             | $T > 1$          |
| 4096              | $\frac{1}{8192}$                   | $\frac{1}{4096}$ |
| 64                | $\frac{1}{128}$                    | $\frac{1}{64}$   |
| 1                 | $\frac{1}{64}$                     | $\frac{1}{64}$   |
| $\frac{1}{60}$    | $\frac{1}{64}$                     | $\frac{1}{64}$   |

[1] T = loaded countdown value. Timer stopped when  $T = 0$ .

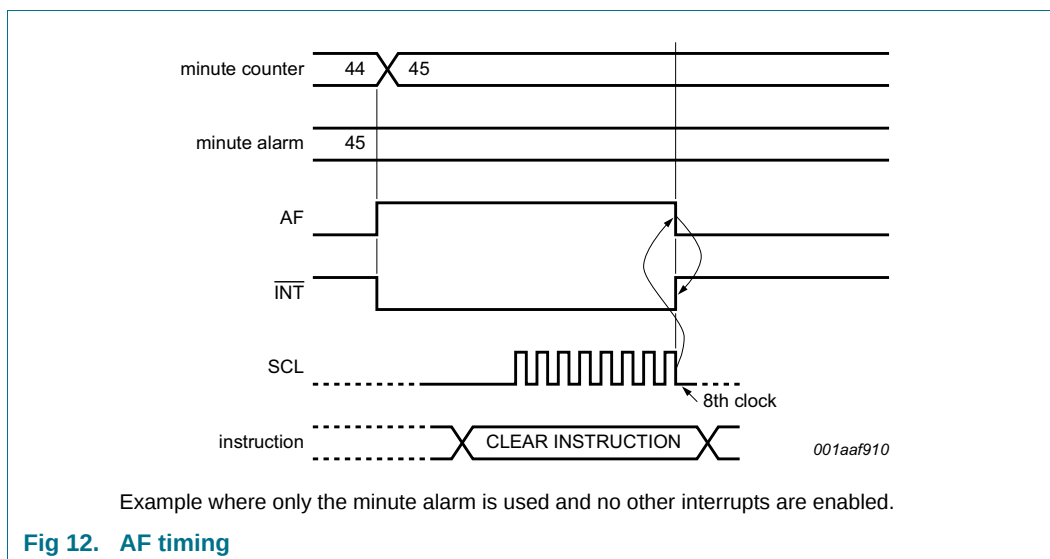
If the TF flag is cleared before the end of the  $\overline{\text{INT}}$  pulse, then the  $\overline{\text{INT}}$  pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see [Figure 11](#). Instructions for clearing TF are given in [Section 8.6.3](#).



The timing shown for clearing bit TF in [Figure 11](#) is also valid for the non-pulsed interrupt mode, i.e., when bit  $\text{TI\_TP} = 0$ , where the pulse can be shortened by setting bit  $\text{TIE} = 0$ .

### 8.7.3 Alarm interrupts

Generation of interrupts from the alarm function is controlled via bit AIE (register Control\_2, see [Table 7](#)). If bit AIE is enabled, the  $\overline{\text{INT}}$  pin follows the status of bit AF. Clearing bit AF immediately clears  $\overline{\text{INT}}$ . No pulse generation is possible for alarm interrupts; see [Figure 12](#).



## 8.8 External clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the  $\text{EXT\_TEST}$  bit in register Control\_1 (see [Table 6](#)). The CLKOUT pin then becomes an input. The test mode replaces the internal signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from pin CLKOUT, is divided down to 1 Hz by a  $2^6$  divide chain called a prescaler; see [Section 8.9](#). The prescaler can be set into a known state by using the STOP bit. When the STOP bit is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

**Remark:** Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT\_TEST test mode (register Control\_1, bit EXT\_TEST = 1).
2. Set STOP (register Control\_1, bit STOP = 1).
3. Clear STOP (register Control\_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

## 8.9 STOP bit function

The STOP bit function (register Control\_1, see [Table 6](#)) allows the accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler ( $F_2$  to  $F_{14}$ ) to be held at reset, thus no 1 Hz ticks are generated. The time circuits can then be set and do not increment until STOP is released; see [Figure 13](#). STOP does not affect the output of 32.768 kHz, 16.384 kHz, or 8.192 kHz; see [Section 8.5](#).

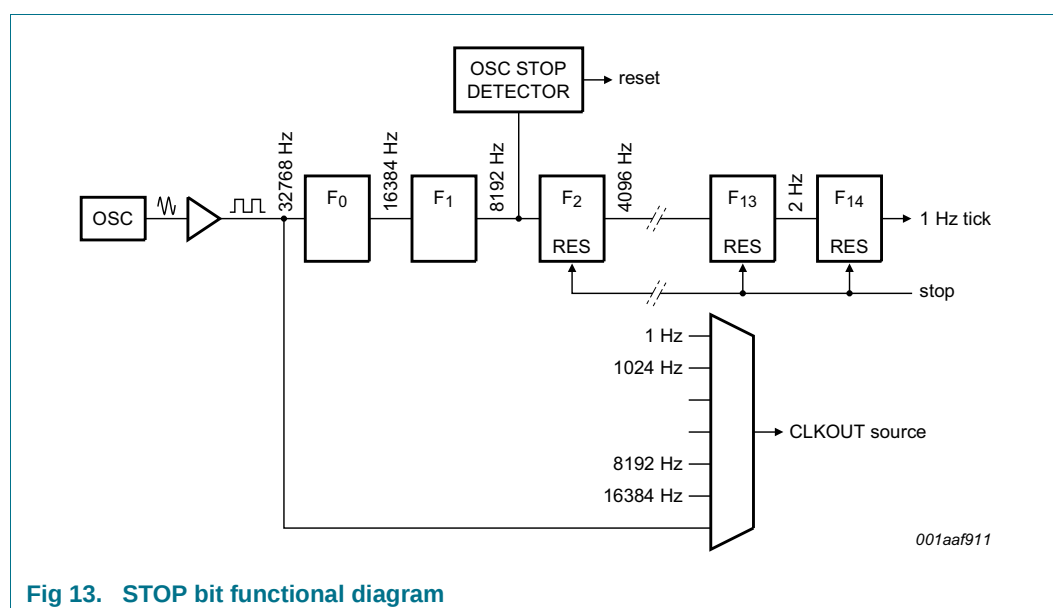


Fig 13. STOP bit functional diagram

The lower two stages of the prescaler ( $F_0$  and  $F_1$ ) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between 0 and one 8.192 kHz cycle; see [Figure 14](#). The first increment of the time circuits is between 0.499878 s and 0.500000 s after STOP is released. The uncertainty is caused by prescaler bits  $F_0$  and  $F_1$  not being reset; see [Table 37](#).

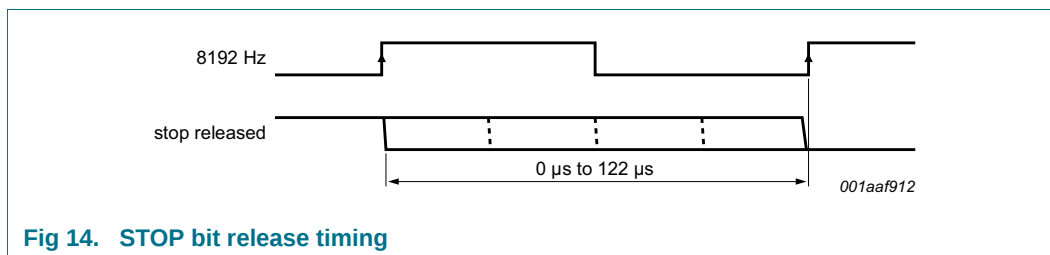


Fig 14. STOP bit release timing

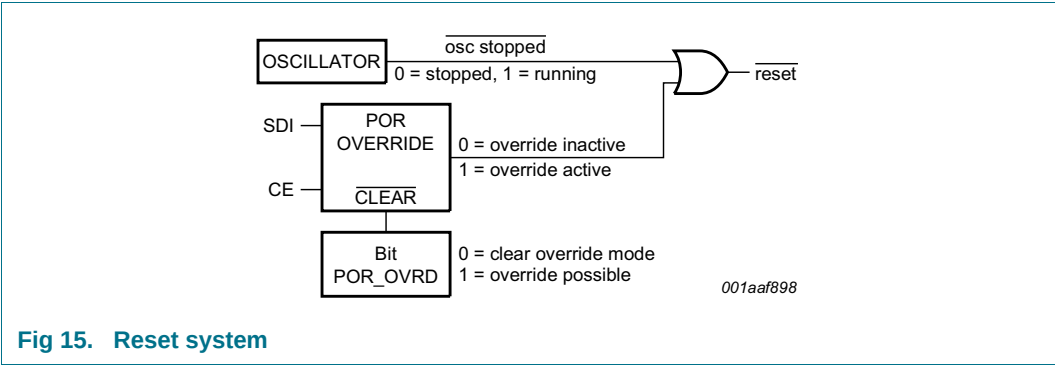
Table 37. Example: first increment of time circuits after STOP release

| Bit STOP                                                                                    | Prescaler bits<br>$F_0F_1F_2$ to $F_{14}$ <sup>[1]</sup> | 1 Hz tick | Time<br>hh:mm:ss | Comment                                                    |
|---------------------------------------------------------------------------------------------|----------------------------------------------------------|-----------|------------------|------------------------------------------------------------|
| Clock is running normally                                                                   |                                                          |           |                  |                                                            |
| 0                                                                                           | 01-0 0001 1101 0100                                      |           | 12:45:12         | prescaler counting normally                                |
| STOP is activated by user. $F_0F_1$ are not reset and values cannot be predicted externally |                                                          |           |                  |                                                            |
| 1                                                                                           | XX-0 0000 0000 0000                                      |           | 12:45:12         | prescaler is reset; time circuits are frozen               |
| New time is set by user                                                                     |                                                          |           |                  |                                                            |
| 1                                                                                           | XX-0 0000 0000 0000                                      |           | 08:00:00         | prescaler is reset; time circuits are frozen               |
| STOP is released by user                                                                    |                                                          |           |                  |                                                            |
| 0                                                                                           | XX-0 0000 0000 0000                                      |           | 08:00:00         | prescaler is now running                                   |
|                                                                                             | XX-1 0000 0000 0000                                      |           | 08:00:00         | -                                                          |
|                                                                                             | XX-0 1000 0000 0000                                      |           | 08:00:00         | -                                                          |
|                                                                                             | XX-1 1000 0000 0000                                      |           | 08:00:00         | -                                                          |
|                                                                                             | :                                                        |           | :                | :                                                          |
|                                                                                             | 11-1 1111 1111 1110                                      |           | 08:00:00         | -                                                          |
|                                                                                             | 00-0 0000 0000 0001                                      |           | 08:00:01         | 0 to 1 transition of $F_{14}$ increments the time circuits |
|                                                                                             | 10-0 0000 0000 0001                                      |           | 08:00:01         | -                                                          |
|                                                                                             | :                                                        |           | :                | :                                                          |
|                                                                                             | 11-1 1111 1111 1111                                      |           | 08:00:01         | -                                                          |
|                                                                                             | 00-0 0000 0000 0000                                      |           | 08:00:01         | -                                                          |
|                                                                                             | 10-0 0000 0000 0000                                      |           | 08:00:01         | -                                                          |
|                                                                                             | :                                                        |           | :                | :                                                          |
|                                                                                             | 11-1 1111 1111 1110                                      |           | 08:00:01         | -                                                          |
|                                                                                             | 00-0 0000 0000 0001                                      |           | 08:00:02         | 0 to 1 transition of $F_{14}$ increments the time circuits |
|                                                                                             |                                                          |           |                  |                                                            |
|                                                                                             |                                                          |           |                  |                                                            |

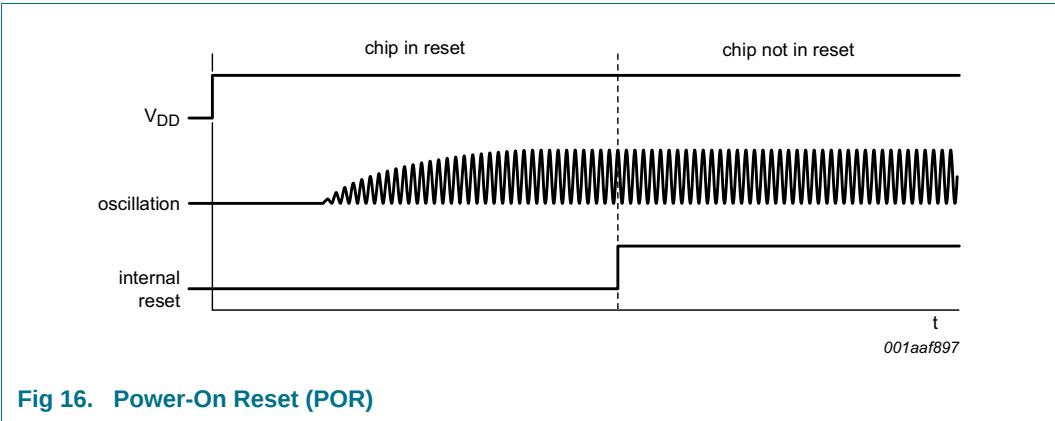
[1]  $F_0$  is clocked at 32.768 kHz.

8.10 Reset

The PCA21125 includes an internal reset circuit which is active whenever the oscillator is stopped; see [Figure 15](#). The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground.



The oscillator is considered to be stopped during the time between power-on and stable crystal resonance; see [Figure 16](#). This time can be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. Whenever an internal reset occurs, the reset flag RF (register Seconds, see [Table 8](#)) is set.



**Table 38. Register reset values**

Bits labeled - are not implemented and return logic 0 when read. Bits labeled X are undefined at power-on and unchanged by subsequent resets.

| Address | Register name   | Bit |   |   |   |   |   |   |   |
|---------|-----------------|-----|---|---|---|---|---|---|---|
|         |                 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00h     | Control_1       | 0   | 0 | 0 | - | 1 | 0 | - | - |
| 01h     | Control_2       | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02h     | Seconds         | 1   | X | X | X | X | X | X | X |
| 03h     | Minutes         | -   | X | X | X | X | X | X | X |
| 04h     | Hours           | -   | - | X | X | X | X | X | X |
| 05h     | Days            | -   | - | X | X | X | X | X | X |
| 06h     | Weekdays        | -   | - | - | - | - | X | X | X |
| 07h     | Months          | -   | - | - | X | X | X | X | X |
| 08h     | Years           | X   | X | X | X | X | X | X | X |
| 09h     | Minute_alarm    | 1   | X | X | X | X | X | X | X |
| 0Ah     | Hour_alarm      | 1   | - | X | X | X | X | X | X |
| 0Bh     | Day_alarm       | 1   | - | X | X | X | X | X | X |
| 0Ch     | Weekday_alarm   | 1   | - | - | - | - | X | X | X |
| 0Dh     | CLKOUT_control  | -   | - | - | - | - | 0 | 0 | 0 |
| 0Eh     | Timer_control   | 0   | - | - | - | - | - | 1 | 1 |
| 0Fh     | Countdown_timer | X   | X | X | X | X | X | X | X |

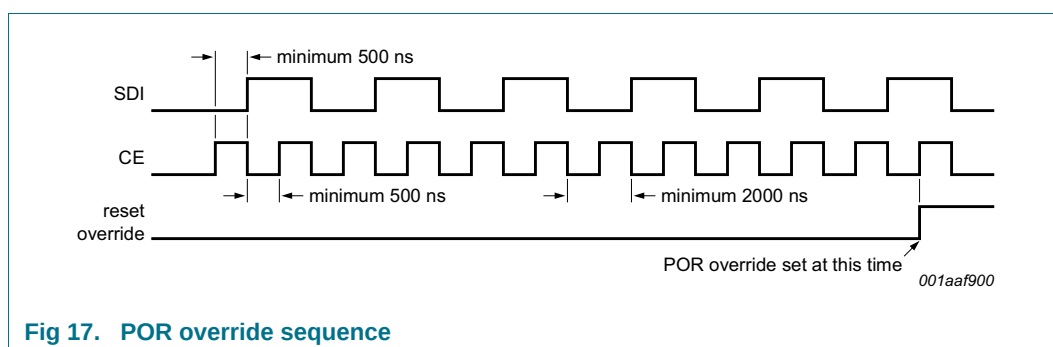
After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- POR override available to be set
- 24-hour mode is selected

The SPI-bus is initialized whenever the chip enable pin CE is inactive (LOW).

### 8.10.1 POR override

The Power-On Reset (POR) duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up the on-board test of the device.

**Fig 17. POR override sequence**

The setting of this mode requires that bit POR\_OVRD (register Control\_1, see [Table 6](#)) be set logic 1 and that the signals at the SPI-bus pins SDI and CE are toggled as illustrated in [Figure 17](#). All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and set-up operation can commence, i.e., entry into the external clock test mode via the SPI-bus access. The override mode can be cleared by writing logic 0 to bit POR\_OVRD. Bit POR\_OVRD must be set logic 1 before a re-entry into the override mode is possible. Setting bit POR\_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the POR override mode. This is the recommended setting.

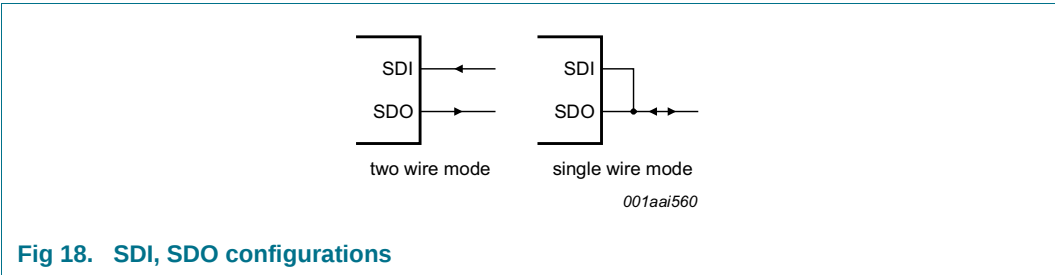
### 8.11 4-line SPI-bus

Data transfer to and from the device is made via a 4-line SPI-bus; see [Table 39](#).

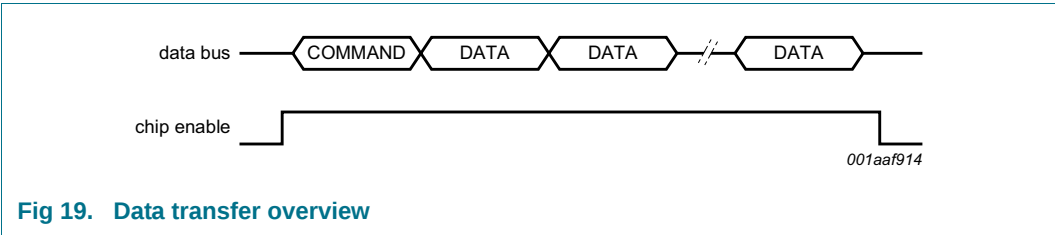
Table 39. Serial interface

| Pin | Function           | Description                                                                                                                                                                                                              |
|-----|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CE  | chip enable input  | when HIGH, data transfer is active<br>when LOW, data transfer is inactive; the interface is reset; pull-down resistor included; active input can be higher than V <sub>DD</sub> , but must not be wired HIGH permanently |
| SCL | serial clock input | when pin CE = LOW, this input might float; input can be higher than V <sub>DD</sub>                                                                                                                                      |
| SDI | serial data input  | when pin CE = LOW, this input might float; input can be higher than V <sub>DD</sub> ; input data is sampled on the rising edge of SCL                                                                                    |
| SDO | serial data output | push-pull output; drives from V <sub>SS</sub> to V <sub>DD</sub> ; output data is changed on the falling edge of SCL                                                                                                     |

The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus (see [Figure 18](#)).



The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first; see [Figure 19](#).

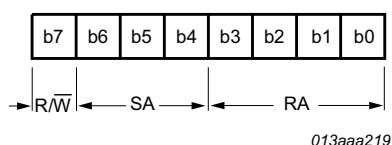


The transmission is initiated by an active HIGH chip enable signal CE and terminated by an inactive LOW signal. The first byte transmitted is the command byte (see [Table 40](#) and [Figure 20](#)). Subsequent bytes are either data to be written or data to be read. Data is captured on the rising edge of the clock and transferred internally on the falling edge.

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The read/write bit (R/W) defines if the following bytes are read or write information.

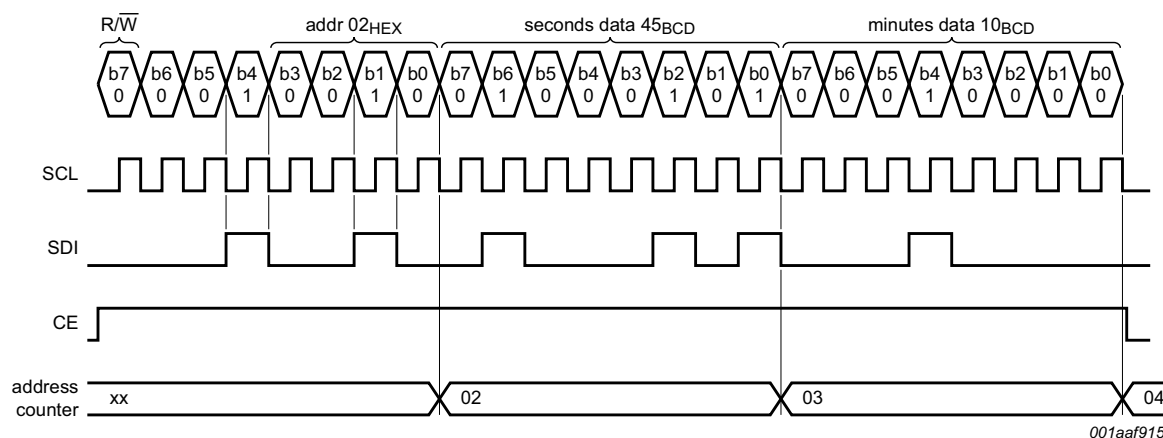
**Table 40. Command byte definition**

| Bit    | Symbol | Value      | Description                                                      |
|--------|--------|------------|------------------------------------------------------------------|
| 7      | R/W    |            | data read or data write selection                                |
|        |        | 0          | write data                                                       |
|        |        | 1          | read data                                                        |
| 6 to 4 | SA     | 001        | subaddress; other codes cause the device to ignore data transfer |
| 3 to 0 | RA     | 00h to 0Fh | register address                                                 |



**Fig 20. Command byte**

In [Figure 21](#), the register Seconds is set to 45 seconds and the register Minutes to 10 minutes.



**Fig 21. Serial bus write example**

In [Figure 22](#), the Months and Years registers are read. In this example, pins SDI and SDO are not connected together.

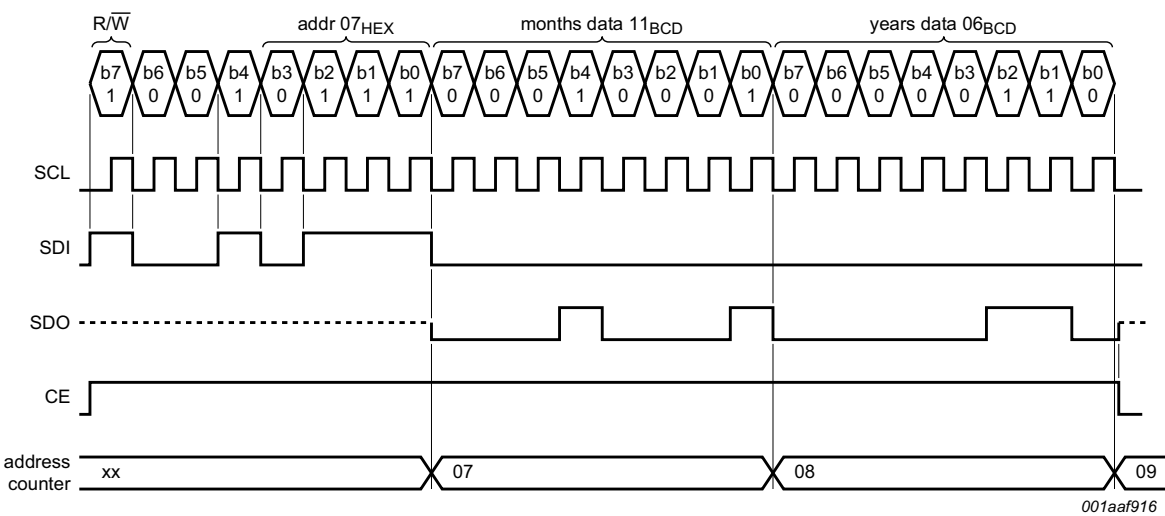


Fig 22. Serial bus read example

8.11.1 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the PCA21125 has a built-in watchdog timer. Should the interface be active for more than 1 s from the time a valid subaddress is transmitted, then the PCA21125 will automatically clear the interface and allow the time counting circuits to continue counting. CE must return LOW once more before a new data transfer can be executed.

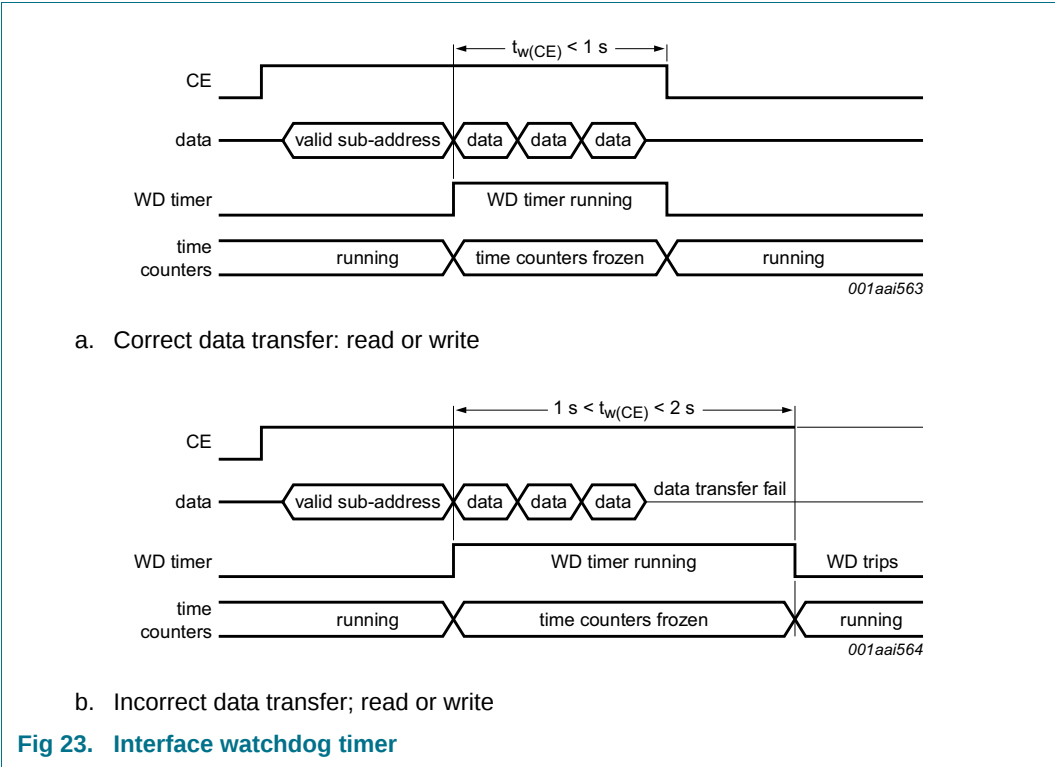


Fig 23. Interface watchdog timer

The watchdog is implemented to prevent the excessive loss of time due to interface access failure, e.g., if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s is lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid subaddress.

## 9. Internal circuitry

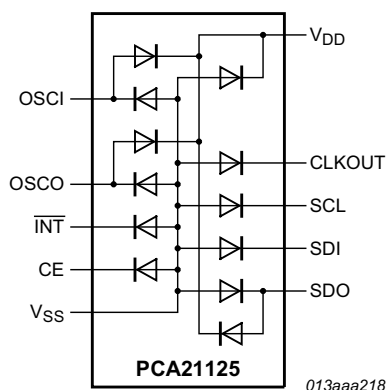


Fig 24. Device diode protection diagram

## 10. Safety notes

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 11. Limiting values

**Table 41. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol           | Parameter                       | Conditions       | Min  | Max   | Unit |
|------------------|---------------------------------|------------------|------|-------|------|
| V <sub>DD</sub>  | supply voltage                  |                  | −0.5 | +6.5  | V    |
| I <sub>DD</sub>  | supply current                  |                  | −50  | +50   | mA   |
| V <sub>I</sub>   | input voltage                   |                  | −0.5 | +6.5  | V    |
| V <sub>O</sub>   | output voltage                  |                  | −0.5 | +6.5  | V    |
| I <sub>I</sub>   | input current                   |                  | −10  | +10   | mA   |
| I <sub>O</sub>   | output current                  |                  | −10  | +10   | mA   |
| P <sub>tot</sub> | total power dissipation         |                  | -    | 300   | mW   |
| T <sub>amb</sub> | ambient temperature             | operating device | −40  | +125  | °C   |
| V <sub>ESD</sub> | electrostatic discharge voltage | HBM [1]          | -    | ±3500 | V    |
|                  |                                 | MM [2]           | -    | ±200  | V    |
|                  |                                 | CDM [3]          | -    | ±1500 | V    |
| I <sub>Iu</sub>  | latch-up current                | [4]              | -    | 100   | mA   |
| T <sub>stg</sub> | storage temperature             | [5]              | −65  | +150  | °C   |

[1] Pass level; Human Body Model (HBM) according to [Ref. 5 "JESD22-A114"](#).

[2] Pass level; Machine Model (MM), according to [Ref. 6 "JESD22-A115"](#).

[3] Pass level; Charged-Device Model (CDM), according to [Ref. 7 "JESD22-C101"](#).

[4] Pass level; latch-up testing, according to [Ref. 8 "JESD78"](#) at maximum ambient temperature (T<sub>amb(max)</sub> = +125 °C).

[5] According to the store and transport requirements (see [Ref. 11 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

## 12. Static characteristics

**Table 42. Static characteristics**

$V_{DD} = 1.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$ ;  $f_{osc} = 32.768 \text{ kHz}$ ; quartz  $R_s = 60 \text{ k}\Omega$ ;  $C_L = 12.5 \text{ pF}$ ; unless otherwise specified.

| Symbol                      | Parameter                 | Conditions                                                                                    | Min                | Typ  | Max                   | Unit |
|-----------------------------|---------------------------|-----------------------------------------------------------------------------------------------|--------------------|------|-----------------------|------|
| Supply: pin V <sub>DD</sub> |                           |                                                                                               |                    |      |                       |      |
| V <sub>DD</sub>             | supply voltage            | SPI-bus inactive;<br>for clock data integrity <a href="#">[1]</a>                             | 1.3                | -    | 5.5                   | V    |
|                             |                           | SPI-bus active                                                                                | 1.6                | -    | 5.5                   | V    |
| I <sub>DD</sub>             | supply current            | SPI-bus active                                                                                |                    |      |                       |      |
|                             |                           | f <sub>SCL</sub> = 6.0 MHz                                                                    | -                  | -    | 500                   | μA   |
|                             |                           | f <sub>SCL</sub> = 1.0 MHz                                                                    | -                  | -    | 100                   | μA   |
|                             |                           | SPI-bus inactive;<br>CLKOUT disabled;<br>V <sub>DD</sub> = 2.0 V to 5.0 V <a href="#">[2]</a> |                    |      |                       |      |
|                             |                           | T <sub>amb</sub> = 25 °C                                                                      | -                  | 820  | -                     | nA   |
|                             |                           | T <sub>amb</sub> = −40 °C to +125 °C                                                          | -                  | 1140 | 3300                  | nA   |
|                             |                           | SPI-bus inactive<br>(f <sub>SCL</sub> = 0 Hz); CLKOUT<br>enabled at 32 kHz                    |                    |      |                       |      |
|                             |                           | T <sub>amb</sub> = 25 °C                                                                      |                    |      |                       |      |
|                             |                           | V <sub>DD</sub> = 5.0 V                                                                       | -                  | 1220 | -                     | nA   |
|                             |                           | V <sub>DD</sub> = 3.0 V                                                                       | -                  | 940  | -                     | nA   |
|                             |                           | V <sub>DD</sub> = 2.0 V                                                                       | -                  | 810  | -                     | nA   |
|                             |                           | T <sub>amb</sub> = −40 °C to +125 °C                                                          |                    |      |                       |      |
|                             |                           | V <sub>DD</sub> = 5.0 V                                                                       | -                  | -    | 4000                  | nA   |
|                             |                           | V <sub>DD</sub> = 3.0 V                                                                       | -                  | -    | 2400                  | nA   |
|                             |                           | V <sub>DD</sub> = 2.0 V                                                                       | -                  | -    | 1900                  | nA   |
| Inputs                      |                           |                                                                                               |                    |      |                       |      |
| V <sub>I</sub>              | input voltage             | pin OSCI                                                                                      | −0.5               | -    | V <sub>DD</sub> + 0.5 | V    |
|                             |                           | pins CE, SDI, SCL                                                                             | −0.5               | -    | +5.5                  | V    |
| V <sub>IL</sub>             | LOW-level input voltage   |                                                                                               | V <sub>SS</sub>    | -    | 0.3V <sub>DD</sub>    | V    |
| V <sub>IH</sub>             | HIGH-level input voltage  |                                                                                               | 0.7V <sub>DD</sub> | -    | V <sub>DD</sub>       | V    |
| I <sub>L</sub>              | leakage current           | V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ;<br>on pins SDI, SCL and<br>CLKOUT       | −1                 | 0    | +1                    | μA   |
| C <sub>I</sub>              | input capacitance         | <a href="#">[3]</a>                                                                           | -                  | -    | 7                     | pF   |
| R <sub>pd</sub>             | pull-down resistance      | pin CE                                                                                        | -                  | 240  | 550                   | kΩ   |
| Outputs                     |                           |                                                                                               |                    |      |                       |      |
| V <sub>O</sub>              | output voltage            | pins OSCO and SDO                                                                             | -                  | -    | V <sub>DD</sub> + 0.5 | V    |
|                             |                           | pins CLKOUT and $\overline{\text{INT}}$ ;<br>refers to external pull-up<br>voltage            | -                  | -    | 5.5                   | V    |
| V <sub>OH</sub>             | HIGH-level output voltage | pin SDO                                                                                       | 0.8V <sub>DD</sub> | -    | V <sub>DD</sub>       | V    |

**Table 42. Static characteristics ...continued**

$V_{DD} = 1.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}$ ;  $f_{osc} = 32.768 \text{ kHz}$ ; quartz  $R_s = 60 \text{ k}\Omega$ ;  $C_L = 12.5 \text{ pF}$ ; unless otherwise specified.

| Symbol     | Parameter                 | Conditions                                                                                                                     | Min      | Typ | Max         | Unit          |
|------------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------|----------|-----|-------------|---------------|
| $V_{OL}$   | LOW-level output voltage  | pin SDO                                                                                                                        | $V_{SS}$ | -   | $0.2V_{DD}$ | V             |
|            |                           | pins CLKOUT and $\overline{\text{INT}}$ ;<br>$V_{DD} = 5 \text{ V}$ ; $I_{OL} = -1.5 \text{ mA}$                               | $V_{SS}$ | -   | 0.4         | V             |
| $I_{OH}$   | HIGH-level output current | output source current;<br>pin SDO;<br>$V_{OH} = 4.6 \text{ V}$ ;<br>$V_{DD} = 5 \text{ V}$                                     | 1.5      | -   | -           | mA            |
| $I_{OL}$   | LOW-level output current  | output sink current;<br>pins $\overline{\text{INT}}$ , SDO and<br>CLKOUT; $V_{OL} = 0.4 \text{ V}$ ;<br>$V_{DD} = 5 \text{ V}$ | 1.5      | -   | -           | mA            |
| $I_{LO}$   | output leakage current    | $V_O = V_{DD} \text{ or } V_{SS}$                                                                                              | -1       | 0   | +1          | $\mu\text{A}$ |
| $C_{ext}$  | external capacitance      | [4]                                                                                                                            | -        | 25  | -           | pF            |
| $C_{OSCO}$ | capacitance on pin OSCO   | [4]                                                                                                                            | -        | 25  | -           | pF            |

[1] For reliable oscillator start at power-up:  $V_{DD} = V_{DD(min)} + 0.3 \text{ V}$ .

[2] Timer source clock =  $\frac{1}{60} \text{ Hz}$ ; voltage on pins CE, SDI and SCL at  $V_{DD}$  or  $V_{SS}$ .

[3] Implicit by design.

[4]  $C_L$  is a calculation of  $C_{ext}$  and  $C_{OSCO}$  in series:  $C_L = \frac{(C_{ext} \cdot C_{OSCO})}{(C_{ext} + C_{OSCO})}$ .

## 13. Dynamic characteristics

**Table 43. Dynamic characteristics**

$V_{DD} = 1.6\text{ V}$  to  $5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ ; all timing values are valid within the operating supply voltage at ambient temperature and referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

| Symbol                  | Parameter                       | Conditions                        | V <sub>DD</sub> = 1.6 V |      | V <sub>DD</sub> = 2.7 V |      | V <sub>DD</sub> = 4.5 V |      | V <sub>DD</sub> = 5.5 V |      | Unit |
|-------------------------|---------------------------------|-----------------------------------|-------------------------|------|-------------------------|------|-------------------------|------|-------------------------|------|------|
|                         |                                 |                                   | Min                     | Max  | Min                     | Max  | Min                     | Max  | Min                     | Max  |      |
| Pin SCL                 |                                 |                                   |                         |      |                         |      |                         |      |                         |      |      |
| f <sub>clk(SCL)</sub>   | SCL clock frequency             |                                   | -                       | 1.5  | -                       | 4.0  | -                       | 5.00 | -                       | 6.25 | MHz  |
| t <sub>SCL</sub>        | SCL time                        |                                   | 660                     | -    | 250                     | -    | 200                     | -    | 160                     | -    | ns   |
| t <sub>clk(H)</sub>     | clock HIGH time                 |                                   | 320                     | -    | 120                     | -    | 100                     | -    | 70                      | -    | ns   |
| t <sub>clk(L)</sub>     | clock LOW time                  |                                   | 320                     | -    | 130                     | -    | 100                     | -    | 90                      | -    | ns   |
| t <sub>r</sub>          | rise time                       | for SCL signal                    | -                       | 100  | -                       | 100  | -                       | 100  | -                       | 100  | ns   |
| t <sub>f</sub>          | fall time                       | for SCL signal                    | -                       | 100  | -                       | 100  | -                       | 100  | -                       | 100  | ns   |
| Pin CE                  |                                 |                                   |                         |      |                         |      |                         |      |                         |      |      |
| t <sub>su(CE)</sub>     | CE set-up time                  |                                   | 30                      | -    | 30                      | -    | 30                      | -    | 30                      | -    | ns   |
| t <sub>h(CE)</sub>      | CE hold time                    |                                   | 100                     | -    | 60                      | -    | 40                      | -    | 30                      | -    | ns   |
| t <sub>rec(CE)</sub>    | CE recovery time                |                                   | 100                     | -    | 100                     | -    | 100                     | -    | 100                     | -    | ns   |
| t <sub>w(CE)</sub>      | CE pulse width                  |                                   | -                       | 0.99 | -                       | 0.99 | -                       | 0.99 | -                       | 0.99 | s    |
| Pin SDI                 |                                 |                                   |                         |      |                         |      |                         |      |                         |      |      |
| t <sub>su</sub>         | set-up time                     |                                   | 25                      | -    | 15                      | -    | 15                      | -    | 10                      | -    | ns   |
| t <sub>h</sub>          | hold time                       |                                   | 100                     | -    | 60                      | -    | 40                      | -    | 30                      | -    | ns   |
| Pin SDO                 |                                 |                                   |                         |      |                         |      |                         |      |                         |      |      |
| t <sub>d(R)SDO</sub>    | SDO read delay time             | bus load = 85 pF                  | -                       | 320  | -                       | 130  | -                       | 100  | -                       | 90   | ns   |
| t <sub>dis(SDO)</sub>   | SDO disable time                | no load value <a href="#">[1]</a> | -                       | 50   | -                       | 30   | -                       | 30   | -                       | 25   | ns   |
| t <sub>t(SDI-SDO)</sub> | transition time from SDI to SDO | to avoid bus conflict             | 0                       | -    | 0                       | -    | 0                       | -    | 0                       | -    | ns   |

[1] Bus is held up by bus capacitance; use RC time constant with application values.

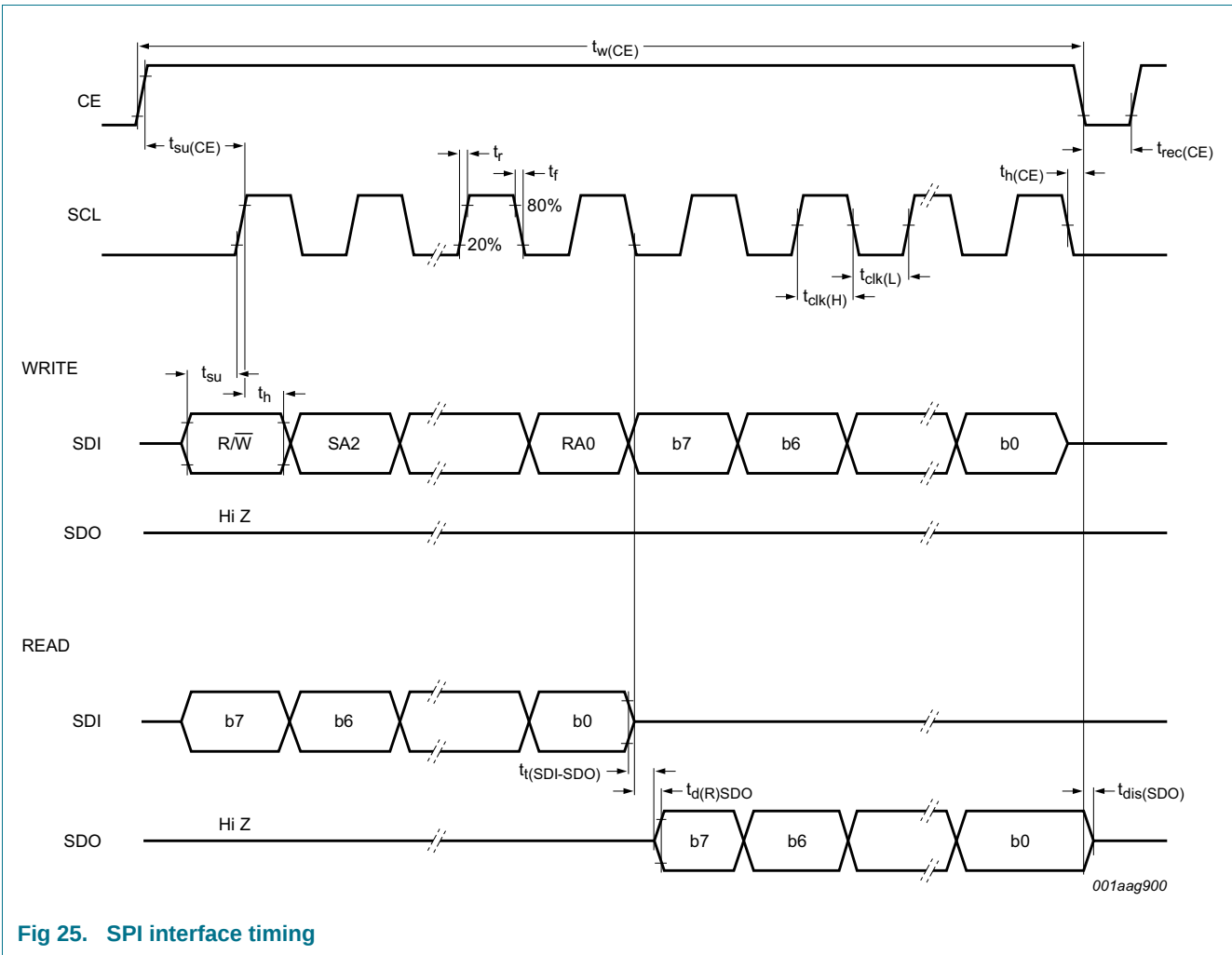
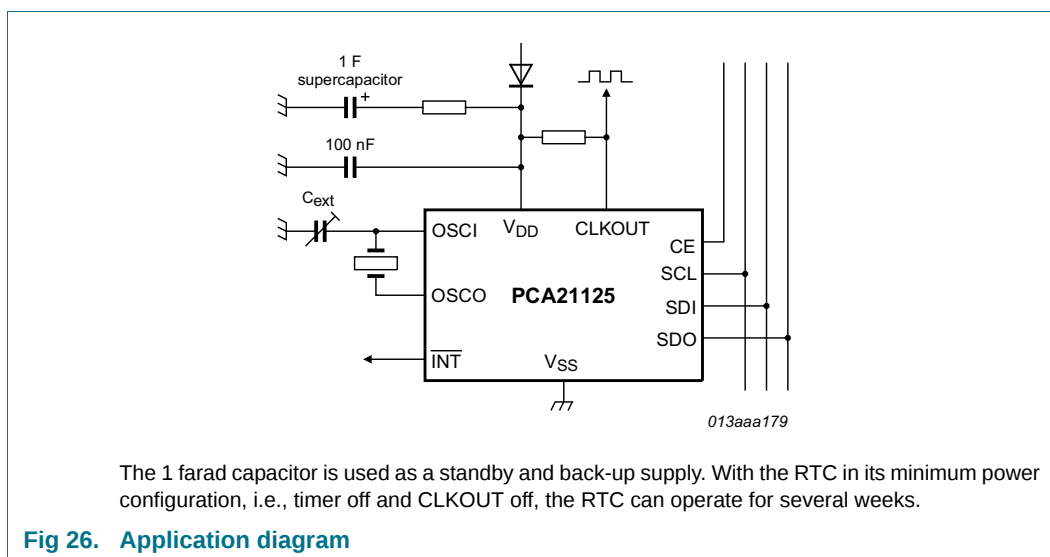


Fig 25. SPI interface timing

## 14. Application information

### 14.1 Application diagram



### 14.2 Quartz frequency adjustment

#### 1. Method 1: fixed OSCI capacitor

A fixed capacitor can be used whose value can be determined by evaluating the average capacitance necessary for the application layout; see [Figure 26](#). The frequency is best measured via the 32.768 kHz signal at pin CLKOUT available after power-on. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average  $\pm 5 \times 10^{-6}$ ). An average deviation of  $\pm 5$  minutes per year can easily be achieved.

#### 2. Method 2: OSCI trimmer

Fast setting of a trimmer is possible using the 32.768 kHz signal at pin CLKOUT available after power-on.

#### 3. Method 3: OSCO output

Direct measurement of OSCO output (accounting for test probe capacitance).

## 15. Test information

### 15.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

16. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm SOT402-1

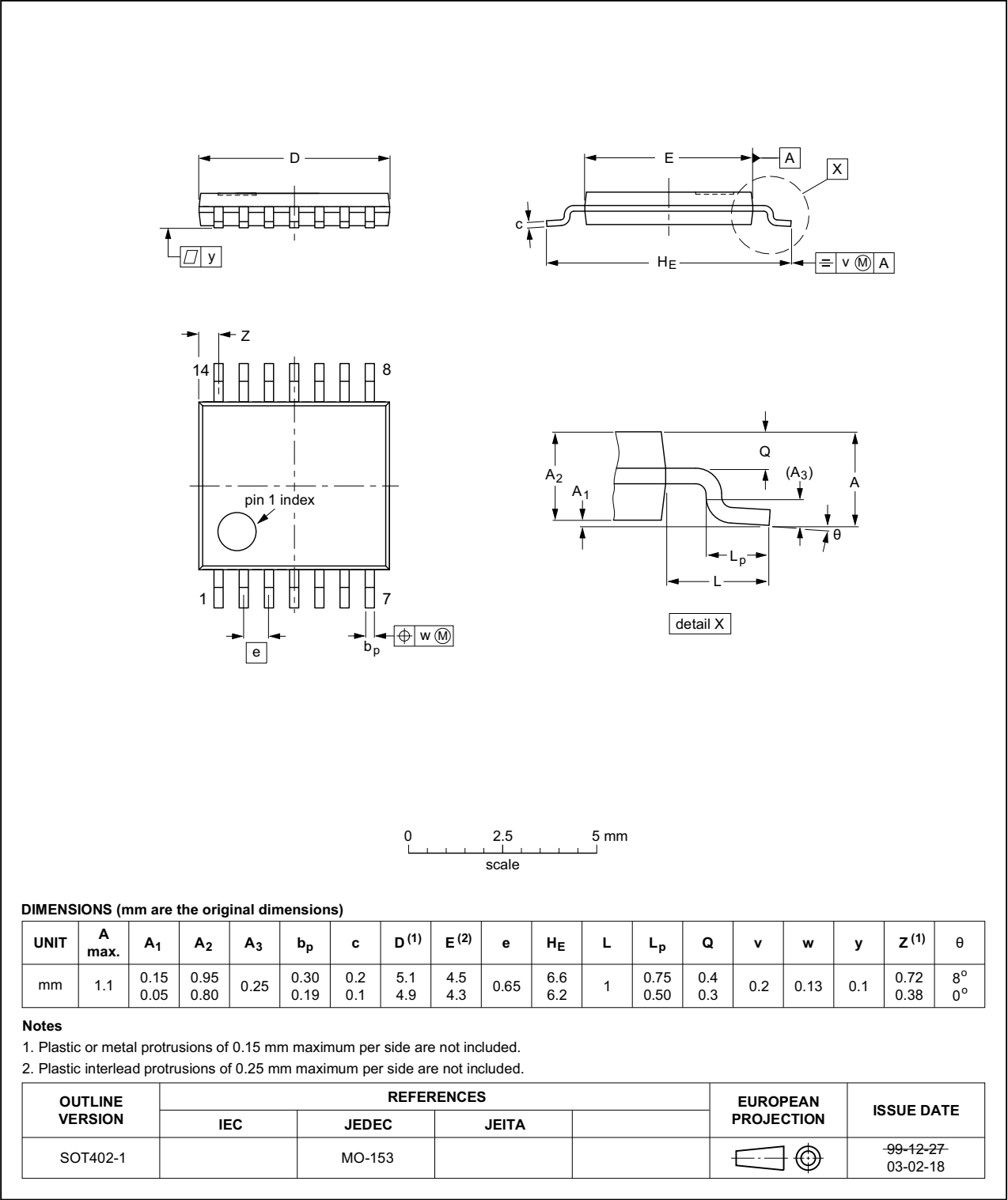


Fig 27. Package outline SOT402-1 (TSSOP14)

## 17. Handling information

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All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 18. Packing information

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### 18.1 Tape and reel information

For tape and reel packing information, see [Ref. 10 "SOT402-1 118" on page 43](#).

## 19. Soldering of SMD packages

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This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "*Surface mount reflow soldering description*".

### 19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages

- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 28](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 44](#) and [45](#)

**Table 44. SnPb eutectic process (from J-STD-020D)**

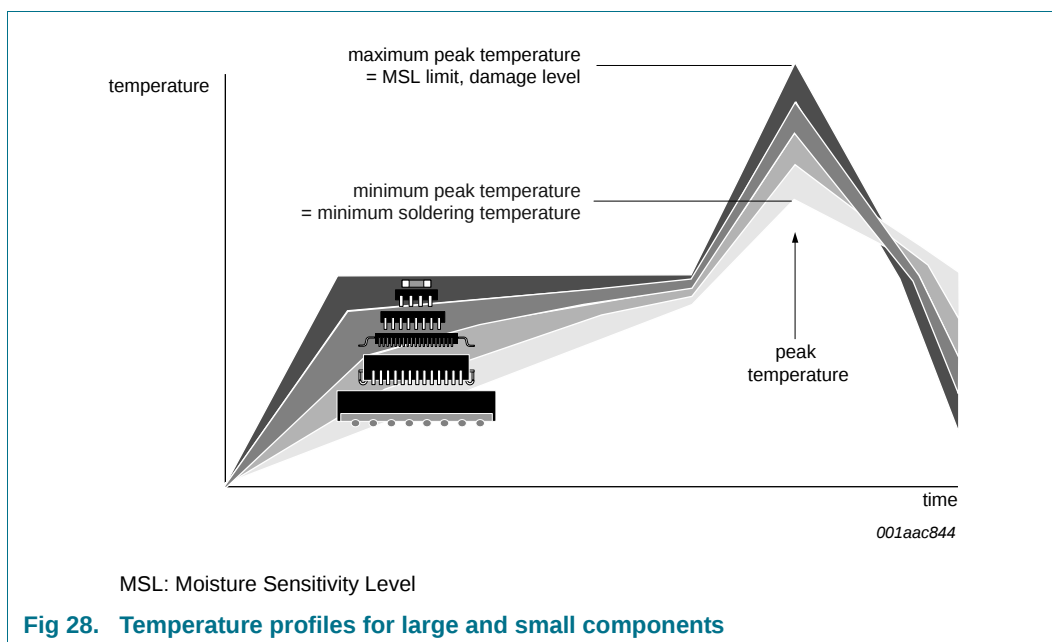
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 45. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 28](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 20. Appendix

### 20.1 Real-Time Clock selection

Table 46. Selection of Real-Time Clocks

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface                | I <sub>DD</sub> , typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features                                                   | Packages                         |
|-----------|------------------------|------------------|--------------------------|--------------------------------|----------------|-------------------------|--------------------|--------------------------------------------------------------------|----------------------------------|
| PCF8563   | X                      | 1                | I <sup>2</sup> C         | 250                            | -              | -                       | -                  | -                                                                  | SO8, TSSOP8, HVSON10             |
| PCF8564A  | X                      | 1                | I <sup>2</sup> C         | 250                            | -              | -                       | -                  | integrated oscillator caps                                         | WLCSP                            |
| PCA8565   | X                      | 1                | I <sup>2</sup> C         | 600                            | -              | -                       | grade 1            | high robustness, T <sub>amb</sub> = -40 °C to 125 °C               | TSSOP8, HVSON10                  |
| PCA8565A  | X                      | 1                | I <sup>2</sup> C         | 600                            | -              | -                       | -                  | integrated oscillator caps, T <sub>amb</sub> = -40 °C to 125 °C    | WLCSP                            |
| PCF85063  | -                      | 1                | I <sup>2</sup> C         | 220                            | -              | -                       | -                  | basic functions only, no alarm                                     | HXSON8                           |
| PCF85063A | X                      | 1                | I <sup>2</sup> C         | 220                            | -              | -                       | -                  | tiny package                                                       | SO8, DFN2626-10                  |
| PCF85063B | X                      | 1                | SPI                      | 220                            | -              | -                       | -                  | tiny package                                                       | DFN2626-10                       |
| PCF85263A | X                      | 2                | I <sup>2</sup> C         | 230                            | X              | X                       | -                  | time stamp, battery backup, stopwatch 1/100 s                      | SO8, TSSOP10, TSSOP8, DFN2626-10 |
| PCF85263B | X                      | 2                | SPI                      | 230                            | X              | X                       | -                  | time stamp, battery backup, stopwatch 1/100s                       | TSSOP10, DFN2626-10              |
| PCF85363A | X                      | 2                | I <sup>2</sup> C         | 230                            | X              | X                       | -                  | time stamp, battery backup, stopwatch 1/100s, 64 Byte RAM          | TSSOP10, DFN2626-10              |
| PCF85363B | X                      | 2                | SPI                      | 230                            | X              | X                       | -                  | time stamp, battery backup, stopwatch 1/100s, 64 Byte RAM          | TSSOP10, DFN2626-10              |
| PCF8523   | X                      | 2                | I <sup>2</sup> C         | 150                            | X              | -                       | -                  | lowest power 150 nA in operation, FM+ 1 MHz                        | SO8, HVSON8, TSSOP14, WLCSP      |
| PCF2123   | X                      | 1                | SPI                      | 100                            | -              | -                       | -                  | lowest power 100 nA in operation                                   | TSSOP14, HVQFN16                 |
| PCF2127   | X                      | 1                | I <sup>2</sup> C and SPI | 500                            | X              | X                       | -                  | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO16                             |

Table 46. Selection of Real-Time Clocks ...continued

| Type name | Alarm, Timer, Watchdog | Interrupt output | Interface                | I <sub>DD</sub> , typical (nA) | Battery backup | Timestamp, tamper input | AEC-Q100 compliant | Special features                                                   | Packages |
|-----------|------------------------|------------------|--------------------------|--------------------------------|----------------|-------------------------|--------------------|--------------------------------------------------------------------|----------|
| PCF2127A  | X                      | 1                | I <sup>2</sup> C and SPI | 500                            | X              | X                       | -                  | temperature compensated, quartz built in, calibrated, 512 Byte RAM | SO20     |
| PCF2129   | X                      | 1                | I <sup>2</sup> C and SPI | 500                            | X              | X                       | -                  | temperature compensated, quartz built in, calibrated               | SO16     |
| PCF2129A  | X                      | 1                | I <sup>2</sup> C and SPI | 500                            | X              | X                       | -                  | temperature compensated, quartz built in, calibrated               | SO20     |
| PCA2129   | X                      | 1                | I <sup>2</sup> C and SPI | 500                            | X              | X                       | grade 3            | temperature compensated, quartz built in, calibrated               | SO16     |
| PCA21125  | X                      | 1                | SPI                      | 820                            | -              | -                       | grade 1            | high robustness, T <sub>amb</sub> = -40 °C to 125 °C               | TSSOP14  |

## 21. Abbreviations

Table 47. Abbreviations

| Acronym | Description                             |
|---------|-----------------------------------------|
| AEC     | Automotive Electronics Council          |
| AM      | Ante Meridiem                           |
| BCD     | Binary Coded Decimal                    |
| CDM     | Charged-Device Model                    |
| CMOS    | Complementary Metal Oxide Semiconductor |
| HBM     | Human Body Model                        |
| IC      | Integrated Circuit                      |
| MM      | Machine Model                           |
| MOS     | Metal Oxide Semiconductor               |
| MSB     | Most Significant Bit                    |
| MSL     | Moisture Sensitivity Level              |
| PCB     | Printed-Circuit Board                   |
| PM      | Post Meridiem                           |
| POR     | Power-On Reset                          |
| RC      | Resistance-Capacitance                  |
| RTC     | Real-Time Clock                         |
| SMD     | Surface Mount Device                    |
| SPI     | Serial Peripheral Interface             |

## 22. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [3] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [4] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [5] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [6] **JESD22-A115** — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [7] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [8] **JESD78** — IC Latch-Up Test
- [9] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [10] **SOT402-1\_118** — TSSOP14; Reel pack; SMD, 13", packing information
- [11] **UM10569** — Store and transport requirements

## 23. Revision history

Table 48. Revision history

| Document ID    | Release date                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Data sheet status  | Change notice | Supersedes   |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|---------------|--------------|
| PCA21125 v.2   | 20141125                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Product data sheet | -             | PCA21125 v.1 |
| Modifications: | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Corrected delay time of first increment of the time circuits</li><li>• Added C<sub>OSCO</sub> value in <a href="#">Table 42</a></li><li>• Added <a href="#">Section 18.1</a> and <a href="#">Section 20.1</a></li><li>• Fixed typos</li></ul> |                    |               |              |
| PCA21125 v.1   | 20091116                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Product data sheet | -             | -            |

## 24. Legal information

### 24.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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