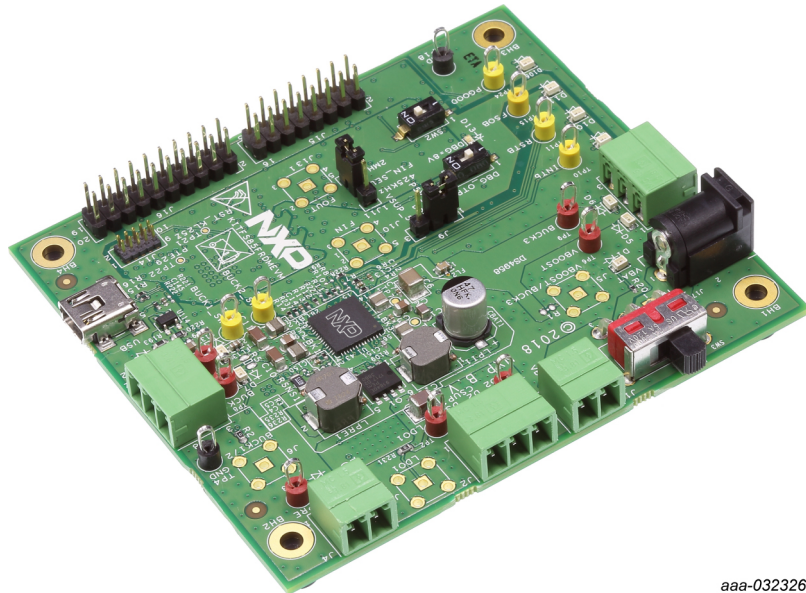


UM11157

KITFS85FRDMEVM evaluation board

Rev. 3 — 6 December 2019

User manual



aaa-032326

Figure 1. KITFS85FRDMEVM

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1 Introduction

This document is the user guide for the KITFS85FRDMEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of FS8500 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS8500 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITFS85FRDMEVM enables development on FS84/FS85 family of devices. The kit can be connected to the FlexGUI software which allows you to play with registers, try OTP configurations, and burn the part.

It is delivered with empty OTP content in order to leave the opportunity to the user to burn the OTP configuration. The board contains a superset device (MC33FS8530AE0S), allowing tests on all the FS84/FS85 derivatives.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <http://www.nxp.com>.

The information page for KITFS85FRDMEVM evaluation board is at <http://www.nxp.com/KITFS85FRDMEVM>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITFS85FRDMEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at <http://community.nxp.com>.

3 Getting ready

Working with the KITFS85FRDMEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board in an anti-static bag
- 3.0 ft USB-STD A to USB-B-mini cable
- Two connectors, terminal block plug, 2 pos., str. 3.81 mm
- Three connectors, terminal block plug, 3 pos., str. 3.81 mm
- Jumpers mounted on board

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 6.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <http://www.nxp.com/KITFS85FRDMEVM> or from the provided link.

- FlexGUI latest version
- FS85_FS84_OTP_Config.xlsm
- Java installation <https://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html>

4 Getting to know the hardware

The KITFS85FRDMEVM provides flexibility to play with all the features of the device and make measurements on the main part of the application. The KL25Z MCU installed on the board, combined with the FlexGUI software allows access to the registers in read and write mode. All regulators are accessible through connectors. Nonuser signal, like DC/DC switcher node is mapped on test points. Digital signals (SPI, I2C, RSTB, etc.) are accessible through connectors. Pin WAKE1 pin has a switch to control (Ignition) them. A VBAT switch is available to power On or Off the device.

This board can be operated in Emulation mode or in OTP mode. In emulation mode, as long as the power is supplied, the board configuration stays valid. The OTP mode uses the fused configuration. The device can be fused three times. In OTP mode, the device always starts with the fused configuration, except if the user wants to overwrite OTP configuration using Emulation mode. This board is able to fuse the OTP without any extra tools or board.

4.1 Kit overview

The KITFS85FRDMEVM is a hardware evaluation tool that allows performance test. The FS85xx part soldered on the board can be fused three times (see [Section 7.3 "Programming the device with an OTP configuration"](#)).

An Emulation mode is possible to test as many configurations as needed. The voltage monitoring hardware configuration is done through resistors. Note that this configuration can be changed by selecting the appropriate bridge resistors:

- VMON1: assigned to VPRE, 4.1 V
- VMON2: assigned to EXT_MON2 (VMON bridge for 3.3 V input)

- VMON3: assigned to BUCK3, 2.3 V
- VMON4: assigned to EXT_MON4 (VMON bridge for 5.0 V input)

This configuration can be changed by installing appropriate bridge resistors. This board was designed to sustain up to 6.0 A total on V_{PRE}.

Layout is done using six layer PCB stack up and by following the rules for DC-DC converter layout design. The FS84/FS85 family can be evaluated with this board as it is populated with a superset part. The FS84xx supports ASIL B design, while FS85xx supports ASIL D design.

An external LDO provides VDDI2C voltage with a choice of 1.8 V or 3.3 V (default). VDDIO is assigned by default to VDDI2C. From USB voltage, an external DC-DC generates the OTP programming voltage (8.0 V) without any need for an external power supply.

4.1.1 KITFS85FRDMEVM features

- VBAT power supply connectors (Jack and Phoenix)
- VPRE output capability up to 6.0 A (external MOSFET)
- VBUCK1/2 in Standalone (default) or Multiphase mode, up to 3.6 A peak
- VBUCK3 up to 3.6 A peak
- VBOOST 5.0 V or 5.74 V, up to 400 mA
- LDO1 and LDO2, from 1.1 V to 5.0 V, up to 400 mA
- Ignition key switch
- FS0B external safety pin
- Embedded USB connection for easy connection to software GUI (access to SPI/I2C bus, IOs, RSTB, FS0B, INTB, Debug, MUX_OUT, regulators)
- LEDs that indicate signal or regulator status
- Support OTP fuse capabilities
- USB connection for register access, OTP emulation, and programming

4.1.2 VMON configuration

The VMONx configuration is highly dependent on the use case. This kit is delivered with a default configuration shown in bold in [Table 1](#). However, the user can assign VMONx differently to address the use case. As an example, VMON1 could be reassigned from VPRE to LDO1 with a wire connected between LDO1 and EXT_MON1. In this case, the user has to define the right value for R240 which depends on the nominal voltage. As a consequence, the *Resistor to set column* in [Table 1](#), indicates that R11 and R227 resistors have to be removed.

[Table 1](#) defines how to connect VMONx.

Table 1. VMONx voltage assignment

The default configuration on the board is indicated in bold.

VMONx inputs	Assignment	Alternate	Nominal voltage	Resistor to set	Resistor value
VMON1	VPRE	—	4.1 V	R11	90.9 kΩ
		VMON_08V	0.8 V	R227	0 Ω
		EXT_MON1	User	R240	User
VMON2	VMON_08V	—	0.8 V	R228	0 Ω
		EXT_MON2	3.3 V	R7	68.1 kΩ

VMONx inputs	Assignment	Alternate	Nominal voltage	Resistor to set	Resistor value
VMON3	BUCK3	—	2.3 V	R38	41.2 k Ω
		VMON_08V	0.8 V	R229	0 Ω
		EXT_MON3	User	R241	User
VMON4	VMON_08V		0.8 V	R230	0 Ω
		EXT_MON4	5.0 V	R40	115 k Ω

VMON_08V is a fixed voltage at 0.8 V which allows to force the right voltage on VMONx. EXT_MONx are available from J16 to feed the desired voltage on VMONx (external). In this case, the resistor value from the upper side of the bridge must be defined.

The resistor location is given in *Resistor to set* column in [Table 1](#). *Nominal voltage* column gives the voltage for which VMONx bridge is defined on the board. The bridge low-side resistor is 22.1 k Ω for each VMON.

4.1.3 VPRE compensation network

This board is delivered with a VPRE compensation network defined for VPRE 4.1 V at 450 kHz. All other VPRE configurations require a new calculation for these components.

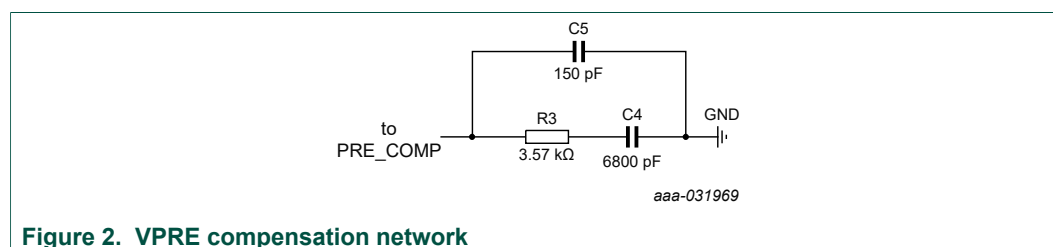


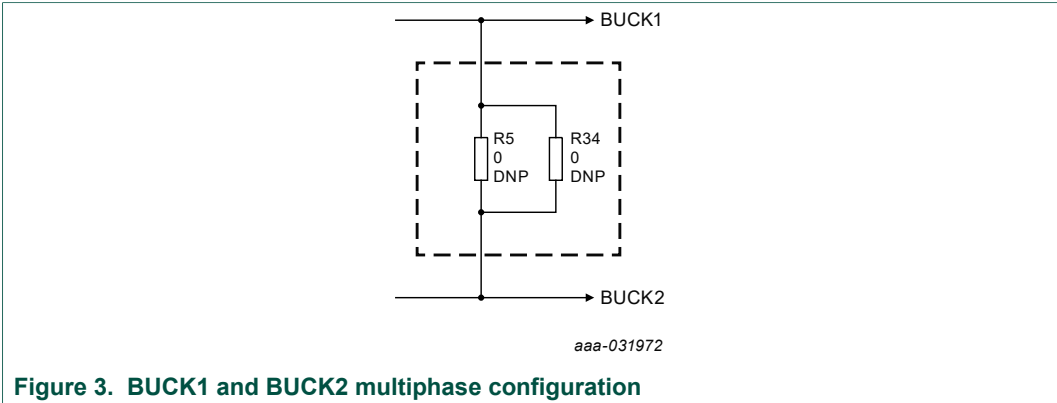
Figure 2. VPRE compensation network

Table 2. Compensation network

Components	VPRE 450 kHz	VPRE 2.2 MHz
C4	6.8 nF	1.5 nF
C5	150 pF	22 pF
R3	3.57 k Ω	16.9 k Ω
LPRE	4.7 μ H or 6.8 μH	1.5 μH , 2.2 μ H, or 4.7 μ H

4.1.4 BUCK1 and BUCK2 multiphase configuration

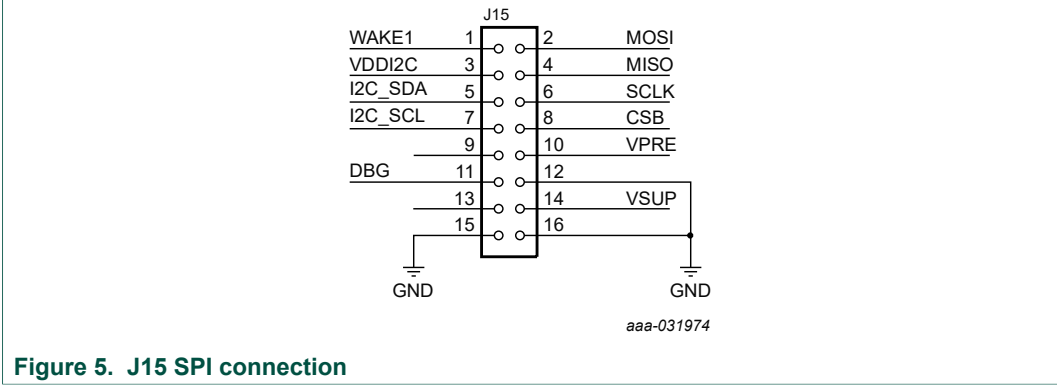
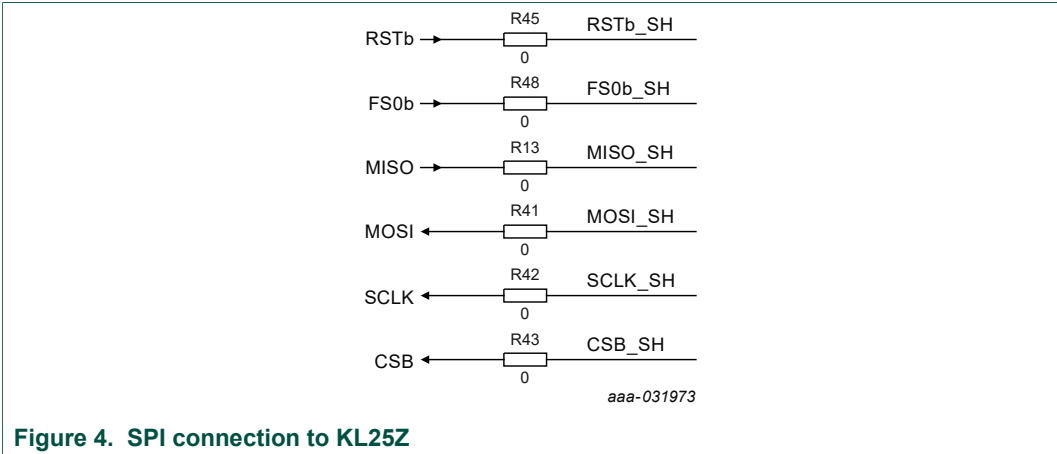
The board is designed to work independently with BUCK1 and BUCK2. Due to R5 and R34, it is possible to connect both connectors together and work in multiphase.



4.1.5 SPI/I2C

The SPI and I2C buses are connected to KL25Z MCU. The user can use either one or the other. The choice can be done at start of the FlexGUI or at any time after launch (see [Section 8 "Using FlexGUI"](#)).

This kit uses a KL25Z MCU to communicate with FlexGUI. It is also possible to connect the SPI to another MCU. In this case, remove R13, R41, R42, and R43 to disconnect the KL25Z MCU (see [Figure 4](#)) and connect the external MCU on J15 connector as shown in [Figure 5](#). The external MCU can be connected on J15 connector as shown in [Figure 5](#). In addition to this change, be sure that VDDIO voltage domain is the same on MCU side and SBC side.



4.1.6 VDDI2C

An external LDO is provided to feed VDDI2C. This LDO can also be used to feed VDDIO, which is the default implementation.

The I2C is compatible with 1.8 V or 3.3 V, while VDDIO is compatible with 3.3 V and 5.0 V. For this reason, the LDO default configuration is 3.3 V. The LDO is supplied by 5.0 V coming from the USB.

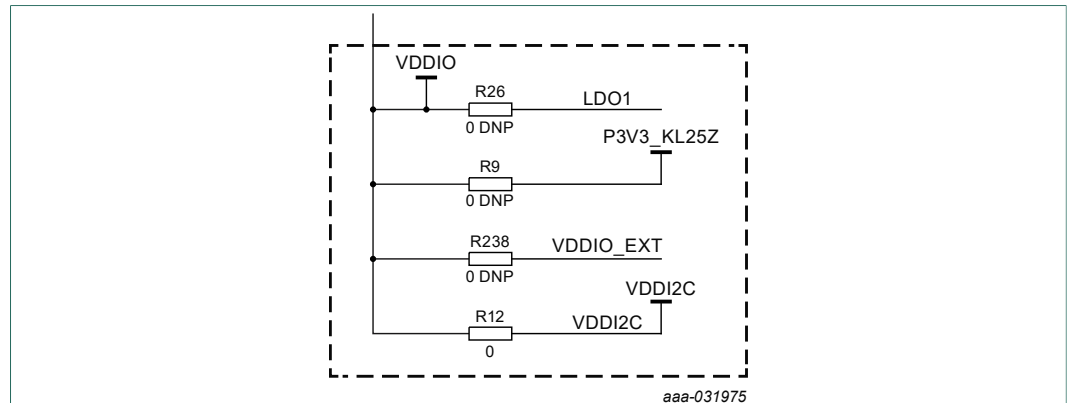


Figure 6. VDDIO selection

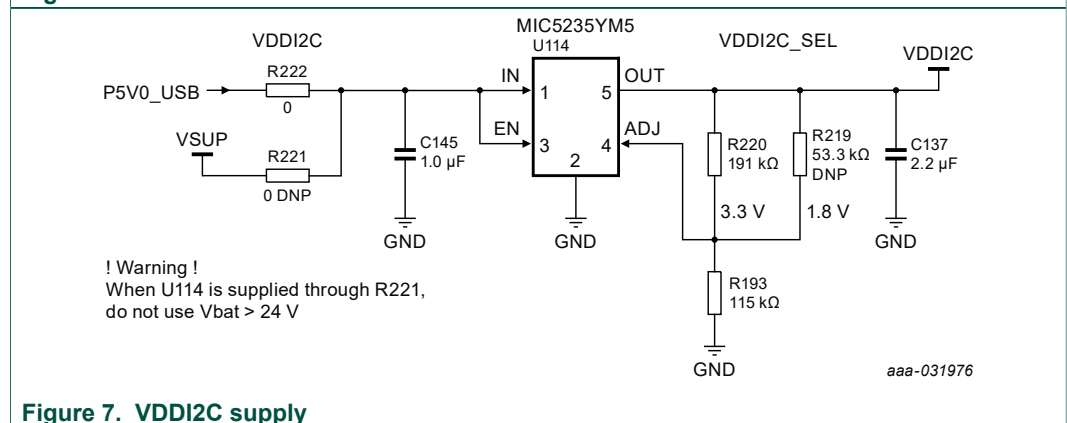


Figure 7. VDDI2C supply

4.1.7 FIN external oscillator

In order to ease the FIN evaluation, a standalone oscillator is installed on the board. It supplies either 425 kHz or 2.4 MHz to the FIN input. The configuration is shown in [Figure 8](#).

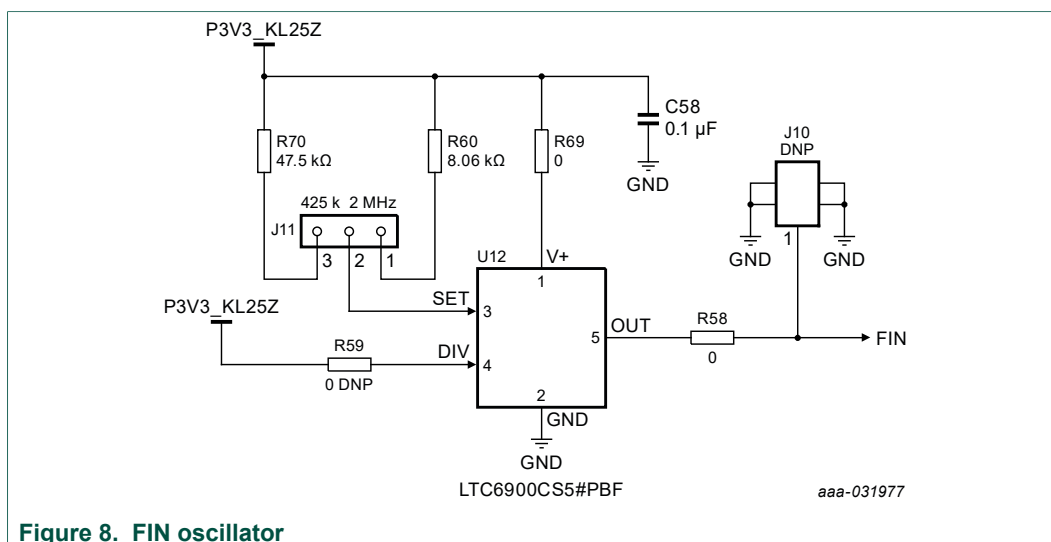


Figure 8. FIN oscillator

4.2 Device OTP user configuration

It is recommended to learn about OTP before operating with the device. The device has a high level of flexibility due to parameter configuration available in the OTP. This impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers and the FS85 SoC.

The OTP-related operations can be performed either in Emulation mode, where the product uses a given configuration as long as power supply is not switched Off or from OTP fuse content that is valid even after a power down/power up sequence.

4.2.1 OTP and mirrors registers

There are two OTP blocks in the device. One is for the main section, and the other for the fail-safe. During configuration, each of them are using dedicated sectors. The OTP configuration scheme is shown in [Figure 9](#) (same implementation for main and fail-safe).

The device can be fused three times using mirror registers. The user can first load the mirror register content with the desired contents, then decide either to use the device in Emulation mode or to burn the next sector. The first sector to be burned is S1, the second S1bis, and the third S1ter. FlexGUI automatically manages the next sector to be burned. It is not possible to revert to the previous sector. When the user reaches the sector S1ter, there no other possibility for burn, however emulation mode is still available.

Note: When device is operating in Emulation mode using configuration from mirror registers, few parameters must be overwritten by SPI/I2C. This concerns regulator TSD behaviors; VPRE slew rate high-side and low-side VBOOST slew rate. See [Section 8.4.10 "TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe"](#) for additional details.

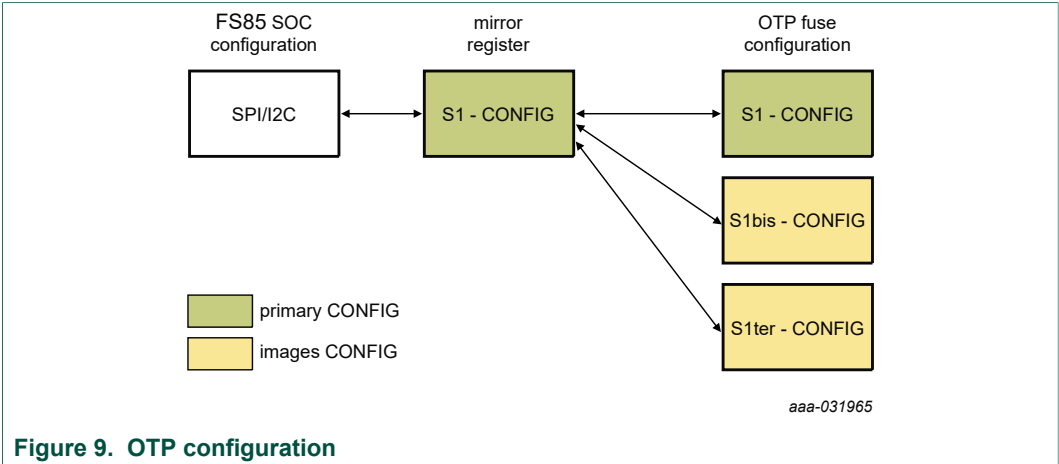


Figure 9. OTP configuration

At boot, the content of the valid sector is loaded into the Mirror Register Sector 1. The mirror register content is accessible from FlexGUI by using specific SPI/I2C commands. The mirror configuration is managed by the FlexGUI, which eases the access.

4.2.2 OTP hardware implementation

To work in OTP emulation or OTP programming, it is required to start the device in Debug mode.

Figure 10 shows the sequence to be followed to enter in Debug mode. The voltage sequence on the kit is done using switches installed on the board, while the OTP registers configuration is managed by the FlexGUI GUI. This is described in detail in the following sections.

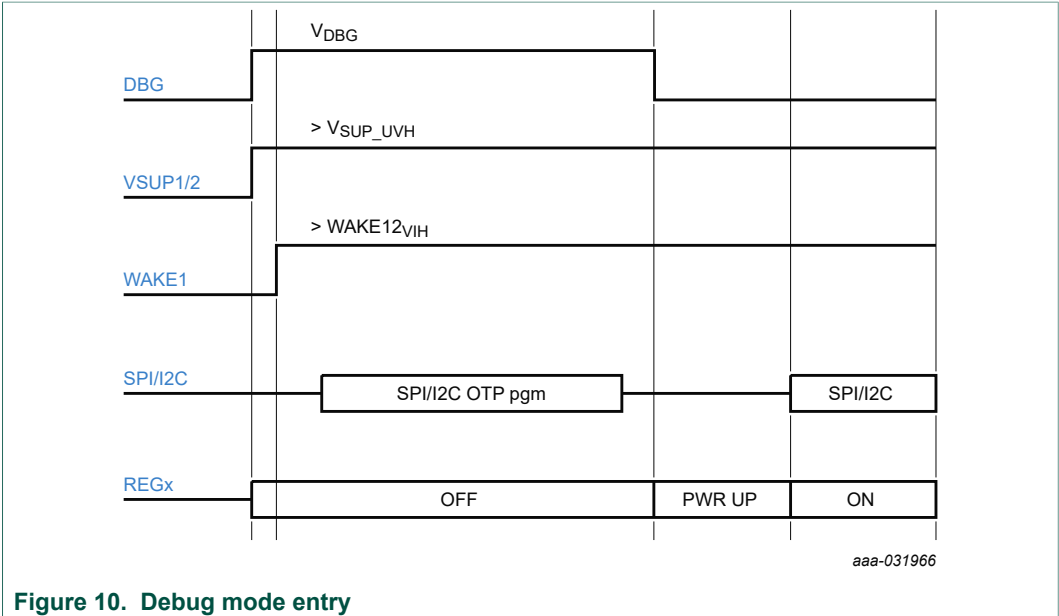


Figure 10. Debug mode entry

Figure 11 shows the hardware kit implementation.

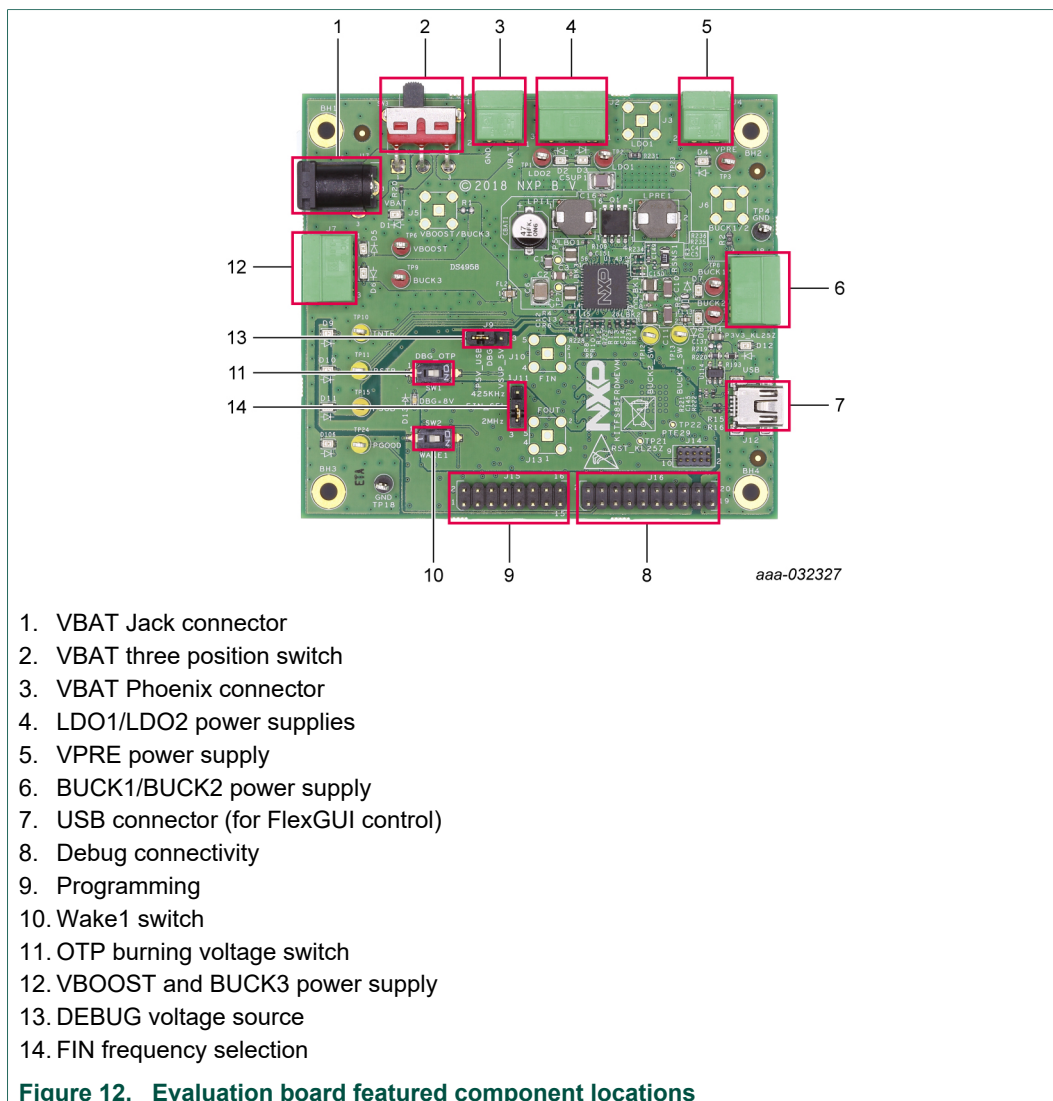


Table 3. Evaluation board component descriptions

Number	Description
1	VBAT Jack connector
2	VBAT three position switch <ul style="list-style-type: none"> Left position: board supplied by Jack connector Middle position: board not supplied Right position: board supplied by Phoenix connector
3	VBAT Phoenix connector
4	LDO1/LDO2 power supply
5	VPRE power supply
6	BUCK1/BUCK2 power supply
7	USB connector (for FlexGUI control)

Number	Description
8	Debug connectivity. Access to: <ul style="list-style-type: none"> • VSUP, GND • FOUT/FIN • PGOOD/RSTB/FS0B • FCCUx • WAKE2 • PSYNC, ERRMON, AMUX • VMONx
9	Programming <ul style="list-style-type: none"> • SPI bus • I2C bus • Debug pin • VPRE, VSUP, GND
10	WAKE1 switch
11	OTP burning voltage switch
12	VBOOST and BUCK3 power supply
13	Debug voltage source either from USB (recommended) or from VSUP
14	FIN frequency selection

4.3.1 FS8500/FS8400: Fail-safe system basis chip with multiple SMPS and LDO

4.3.1.1 General description

This device family is part of a global platform FS84 (fit for ASIL B) and FS85 (fit for ASIL D), pin to pin and software compatible. The FS85/FS84 is an automotive functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS domain controller, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

The FS85/FS84 includes enhanced safety features, with fail-safe output, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity level. It is developed in compliance with ISO 26262 standard. Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

4.3.1.2 Features

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- **Based on part number:** low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
- **Based on part number:** low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 2.5 A typical peak.

- BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- 2x linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- Standby OFF mode with very low sleep current (10 μ A typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via 32 bits SPI or I2C interface with CRC
- Power synchronization pin to operate 2x FS85 devices or FS85 plus an external PMIC
- Scalable portfolio from ASIL B to ASIL D with independent monitoring circuitry, dedicated interface for MCU monitoring, simple and challenger watchdog function, power good, reset and interrupt, built-in self-test, fail-safe output
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.

4.3.2 Indicators

The following LEDs are provided as visual output devices for the evaluation board:

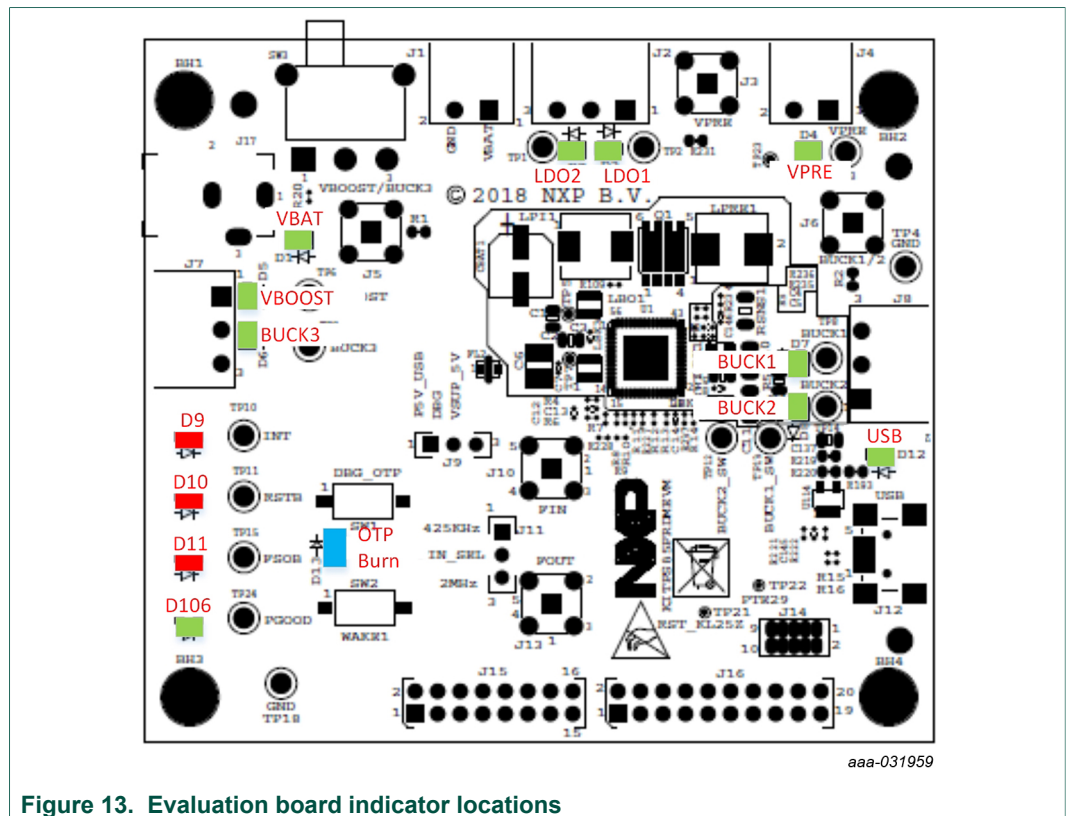


Figure 13. Evaluation board indicator locations

Table 4. Evaluation board indicator descriptions

Label	Name	Color	Description
D1	VBAT	Green	VBAT On
D2	LDO1	Green	LDO1 On
D3	LDO2	Green	LDO2 On

Label	Name	Color	Description
D4	BUCK1	Green	BUCK1 On
D6	BUCK2	Green	BUCK2 On
D7	BUCK3	Green	BUCK3 On
D8	VBOOST	Green	VBOOST On
D9	VPRE	Green	VPRE On
D12	DBG > 8.0 V	Blue	DBG pin voltage > 8.0 V (OTP programming)
D13	RSTB	Red	RSTB asserted (logic level = 0)
D14	INTB	Red	INTB asserted (logic level = 0)
D15	FS0B	Red	FS0B asserted (logic level = 0)
D16	P3V3_KL25	Green	P3V3_KL25 On

4.3.3 Connectors

Figure 14 shows the location of connectors on the board.

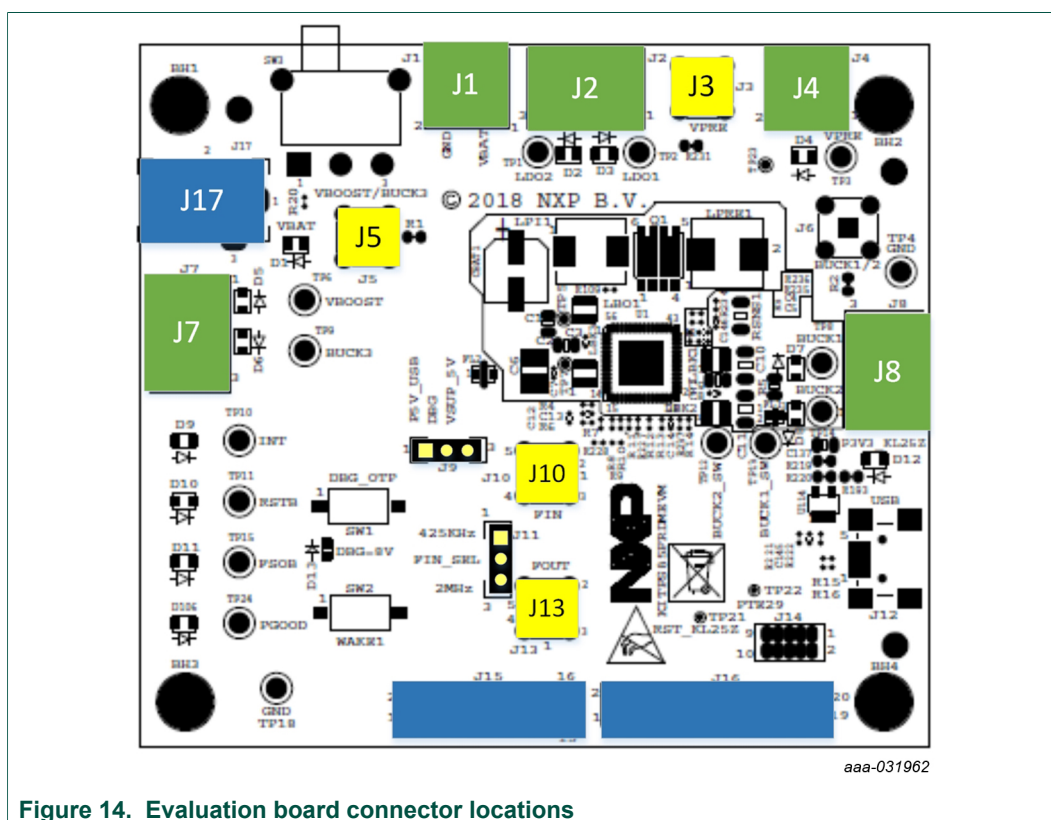


Figure 14. Evaluation board connector locations

4.3.3.1 VBAT connector (J1)

VBAT connects to the board through Phoenix connector (J1).

Table 5. V_{BAT} Phoenix connector (J1)

Schematic label	Signal name	Description
J1-1	VBAT	Battery voltage supply input
J1-2	GND	Ground

4.3.3.2 Output power supply connectors

Table 6. BUCK1/BUCK2 connector (J8)

Schematic label	Signal name	Description
J8-1	BUCK2	BUCK2 power supply output
J8-2	BUCK1	BUCK1 power supply output
J8-3	GND	Ground

Table 7. VBOOST/BUCK3 connector (J7)

Schematic label	Signal name	Description
J7-1	VBOOST	VBOOST output
J7-2	BUCK3	BUCK3 power supply output
J7-3	GND	Ground

Table 8. LDO1/LDO2 connector (J2)

Schematic label	Signal name	Description
J2-1	LDO1	LDO1 power supply output
J2-2	LDO2	LDO2 power supply output
J2-3	GND	Ground

Table 9. VPRE connector (J4)

Schematic label	Signal name	Description
J4-1	VPRE	VPRE power supply output
J4-2	GND	Ground

4.3.3.3 Debug connector (J16)

Table 10. Debug connector (J16)

Schematic label	Signal name	Description
J16-1	FOUT	Frequency synchronization output
J16-2	FIN	Frequency synchronization input
J16-3	PGOOD	Power GOOD
J16-4	VMON1_EXT	Voltage monitoring 1, from external reference
J16-5	INTB	Interrupt, active low
J16-6	VMON2_EXT	Voltage monitoring 2, from external reference
J16-7	RSTB	Reset, active low
J16-8	VMON3_EXT	Voltage monitoring 3, from external reference
J16-9	ERRMON	Error monitoring
J16-10	VMON4_EXT	Voltage monitoring 4, from external reference
J16-11	AMUX	Analog multiplexer
J16-12	FS0B_Out	Fail-safe, active low
J16-13	VDDIO_EXT	VDDIO external reference

Schematic label	Signal name	Description
J16-14	PSYNC	Power synchronization
J16-15	VDDIO	VDDIO used by FS85
J16-16	WAKE2_IN	WAKE2 input
J16-17	FCCU1	Fault collector control unit 1
J16-18	VSUP	VSUP power supply
J16-19	FCCU2	Fault collector control unit 2
J16-20	GND	Ground

4.3.3.4 Program connector (J15)

Table 11. Program connector (J15)

Schematic label	Signal name	Description
J15-1	WAKE1	WAKE1 input
J15-2	MOSI	SPI master output slave input
J15-3	VDDI2C	VDDI2C voltage
J15-4	MISO	SPI master input slave output
J15-5	I2C_SDA	I2C serial data
J15-6	SCLK	SPI clock
J15-7	I2C_SCL	I2C serial clock
J15-8	CSB	SPI chip select
J15-9	n.c.	not connected
J15-10	VPRE	VPRE output
J15-11	DBG	Connected to Debug pin
J15-12	GND	Ground
J15-13	n.c.	not connected
J15-14	VSUP	Connected to VSUP pin
J15-15	GND	Ground
J15-16	GND	Ground

4.3.4 Test points

The following test points provide access to various signals to and from the board.

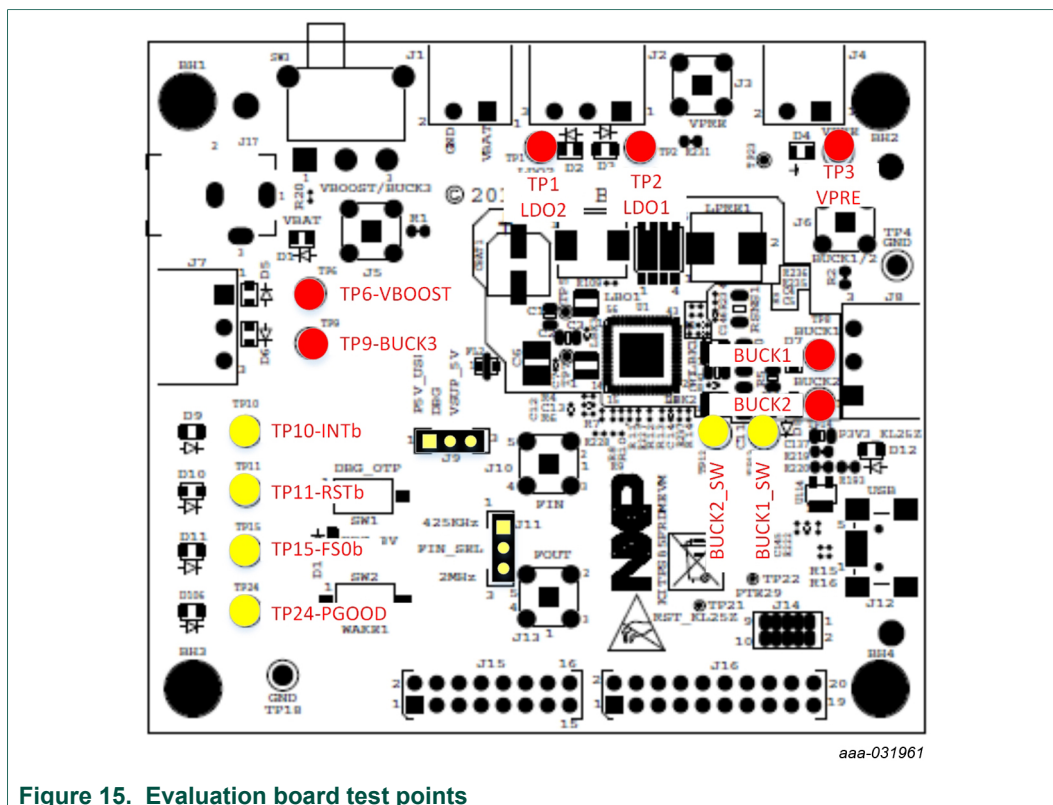


Figure 15. Evaluation board test points

Table 12. Evaluation board test point descriptions

Test point name	Signal name	Description
TP1	LDO2	LDO2 regulator output
TP2	LDO1	LDO1 regulator output
TP3	VPRE	VPRE DC/DC regulator output
TP4	GND	Ground
TP6	VBOOST	VBOOS DC/DC output
TP8	BUCK1	BUCK1 DC/DC regulator output
TP9	BUCK3	BUCK3 DC/DC regulator output
TP10	INTB	Interruption signal, active low
TP11	RSTB	Reset signal, active low
TP14	BUCK2	BUCK2 DC/DC regulator output
TP15	FS0B	Fail-safe output, active low
TP18	GND	Ground
TP24	PGOOD	Power GOOD output, active low

4.3.5 Jumpers

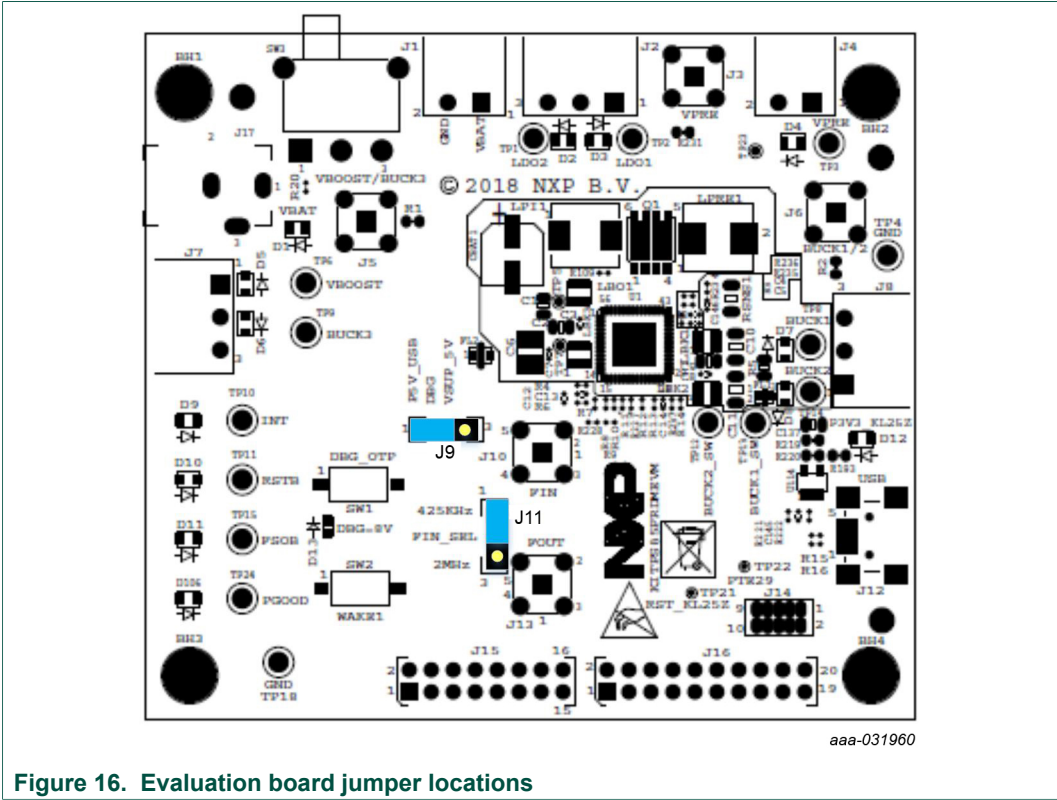


Table 13. Evaluation board jumper descriptions

Name	Function	Pin number	Jumper/pin function
J9	VBAT shunt	1-2	DBG voltage produced from VBAT
		2-3	DBG voltage produced from USB 5.0 V
J11	FIN clock selection	1-2	FIN set to 2.0 MHz
		2-3	FIN set to 425 kHz

4.3.6 Switches

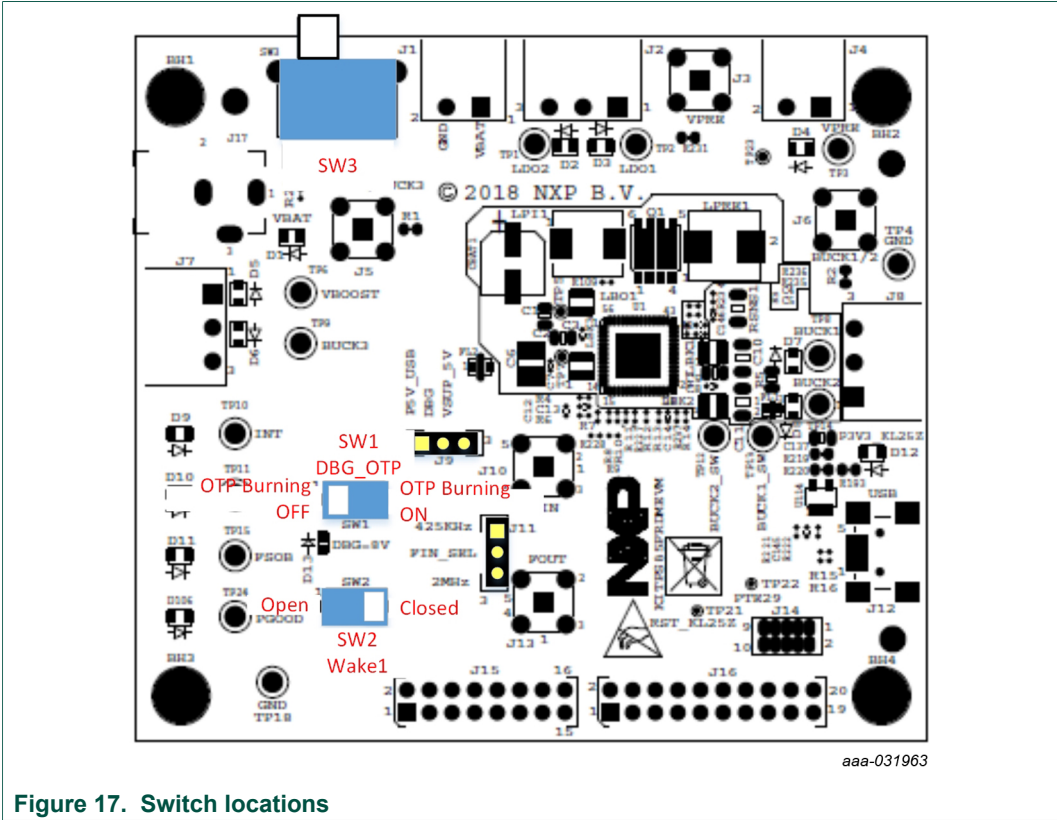


Figure 17. Switch locations

Table 14. SW1

Position	Function	Description
LEFT	OTP programming Off	OTP burning not possible
RIGHT	OTP programming On	8.0 V on DBG pin allows OTP burning (blue LED turns On to indicate this state)

Table 15. SW2

Position	Function	Description
OPEN	WAKE1 open	Wake1 pin not connected to V _{SUP}
CLOSED	WAKE1 closed	Wake1 pin connected to V _{SUP}

Table 16. SW3

Position	Function	Description
LEFT	VBAT On	VBAT from J17
MIDDLE	VBAT Off	Board not supplied
RIGHT	VBAT On	VBAT from J1

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITFS85FRDMEVM evaluation board are available at <http://www.nxp.com/KITFS85FRDMEVM>.

5 Installing and configuring software and tools

This development kit uses FlexGUI software. FlexGUI software is based on Java JRE.

Preparing the Windows PC workstation consists of three steps.

1. Install the appropriate Java SE Runtime Environment (JRE).
2. Install Windows 7 FlexGUI driver.
3. Install FlexGUI software package.

5.1 Installing the Java JRE

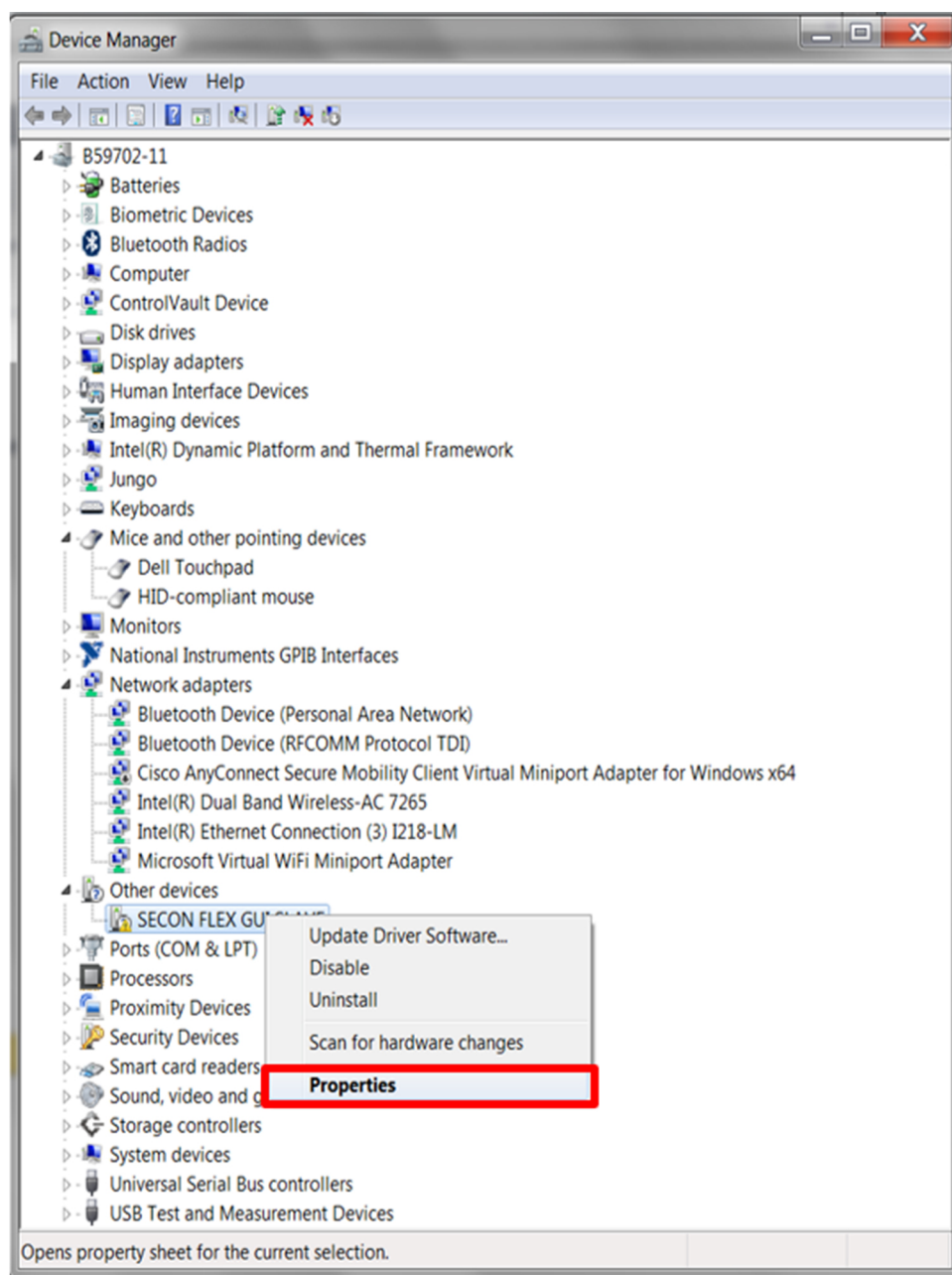
1. Download Java JRE (Java SE Runtime Environment), available at <http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html> (8u162 or newer).
2. Open the installer and follow the installation instructions.
3. Following the successful installation, restart the computer.

5.2 Installing Windows 7 FlexGUI driver

On Windows 7 PCs, a virtual COM port installation is required. Install the Windows 7 FlexGUI driver using the following procedure.

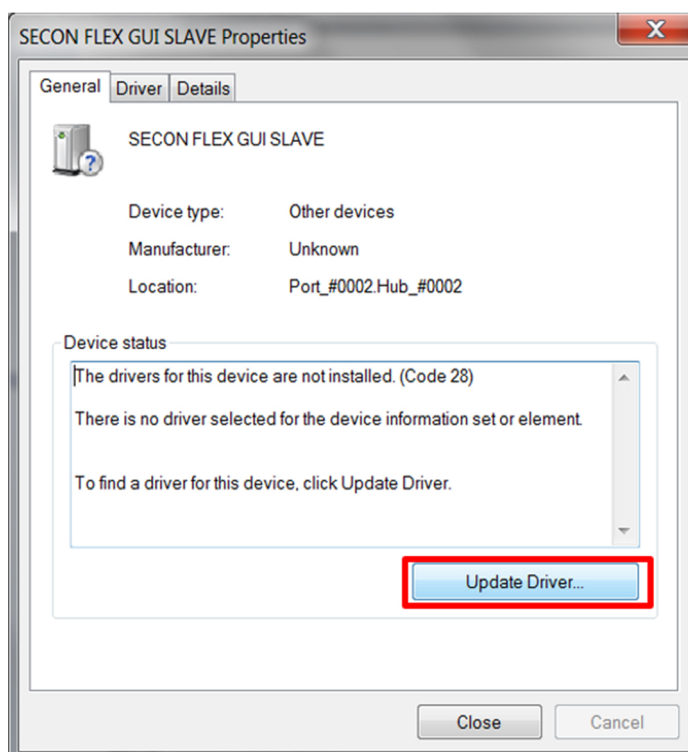
Note: On Windows 10, it is not necessary to install virtual com port as Windows 10 uses a generic COM port driver.

1. Connect the kit to the computer as described in [Section 6 "Configuring the hardware for startup"](#)
2. On the Windows PC, open the **Device Manager**.
3. In the **Device Manager** window, right-click on **SECON FLEX GUI SLAVE**, and then select **Properties**.



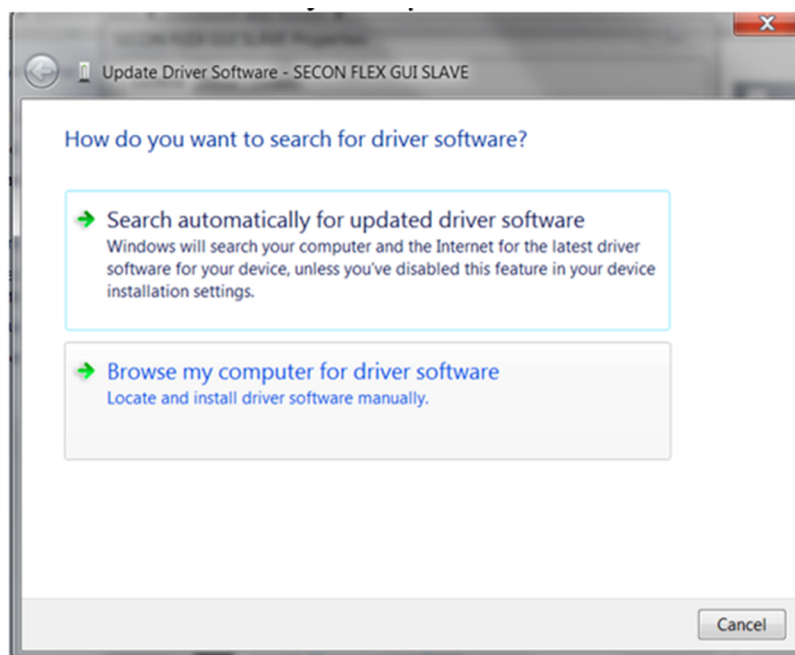
aaa-031982

4. In the **SECON FLEX GUI SLAVE Properties** window, click **Update Driver**.



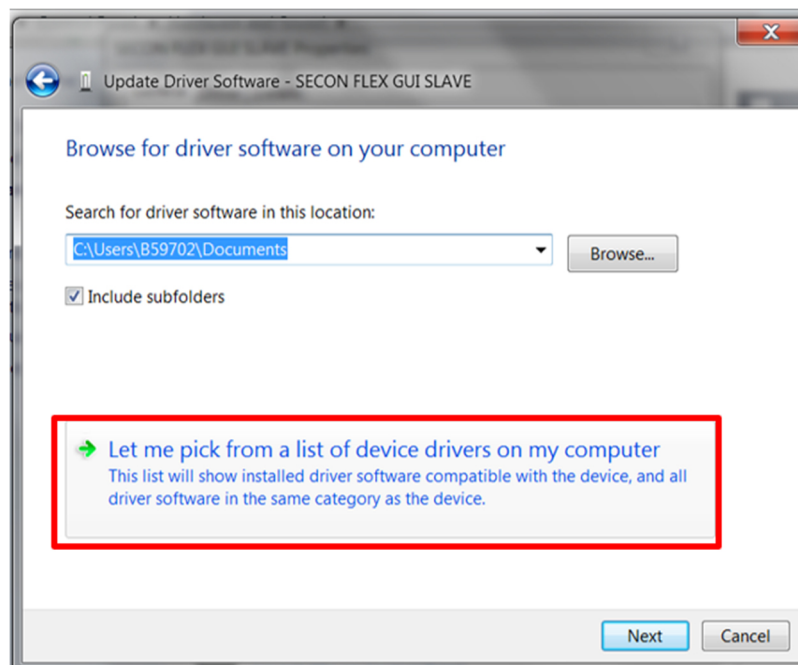
aaa-031983

5. in the **Update Software Driver** window, select **Browse my computer for driver software**.



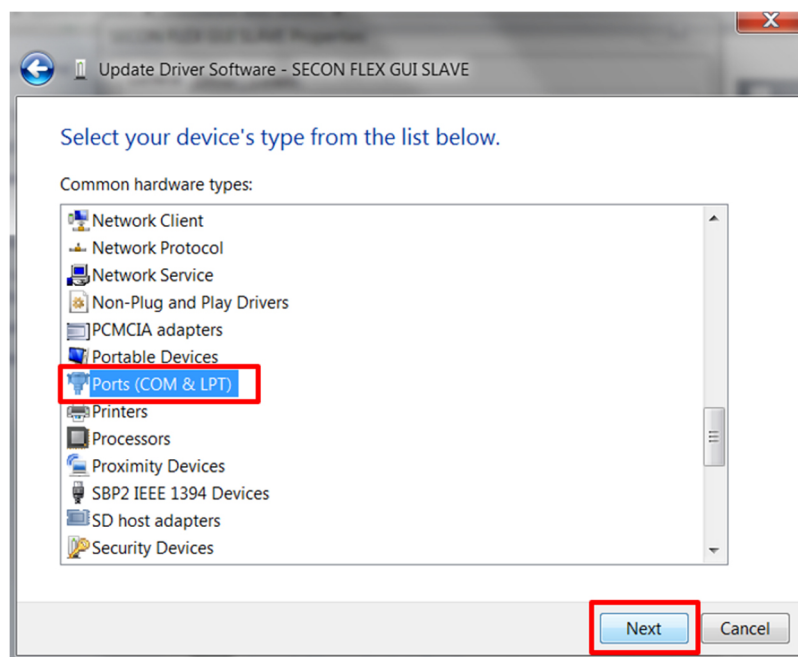
aaa-031984

6. Select **Let me pick from a list of device drivers on my computer**, and then click **Next**.



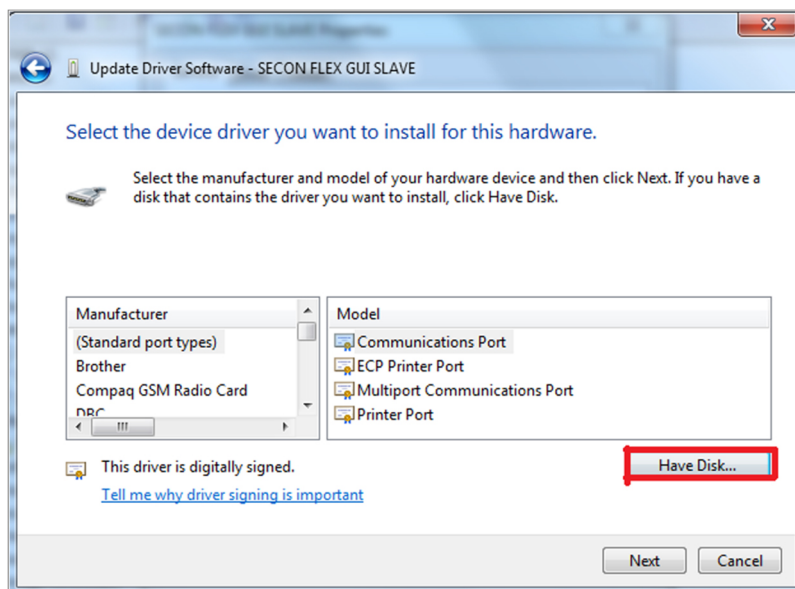
aaa-031985

7. Select **Ports (COM & LPT)** from the list, and then click **Next**.



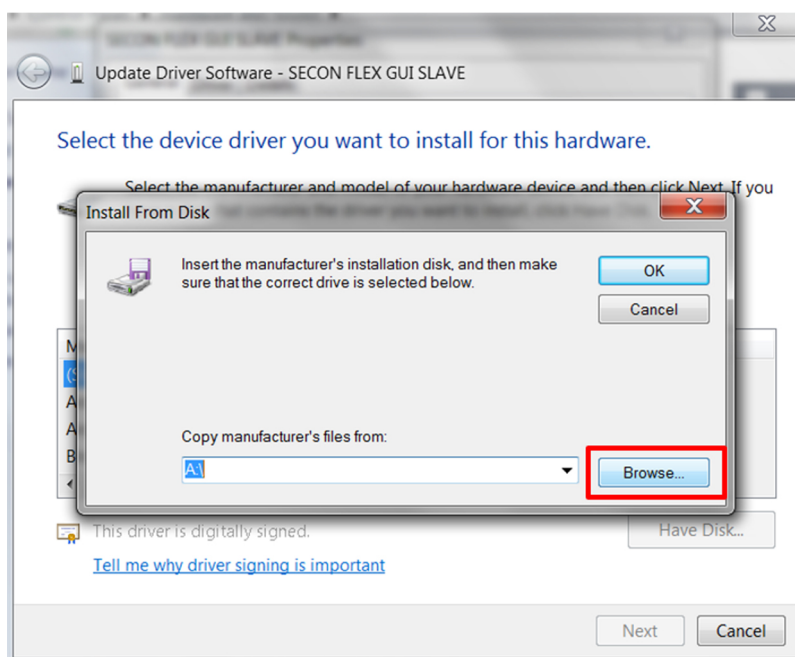
aaa-031986

8. Click **Have Disk**.



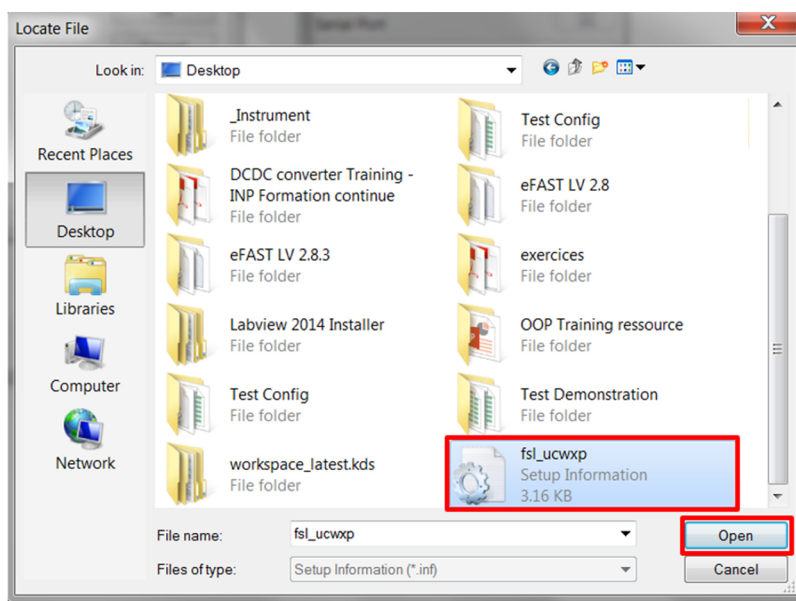
aaa-031987

9. Click **Browse**.



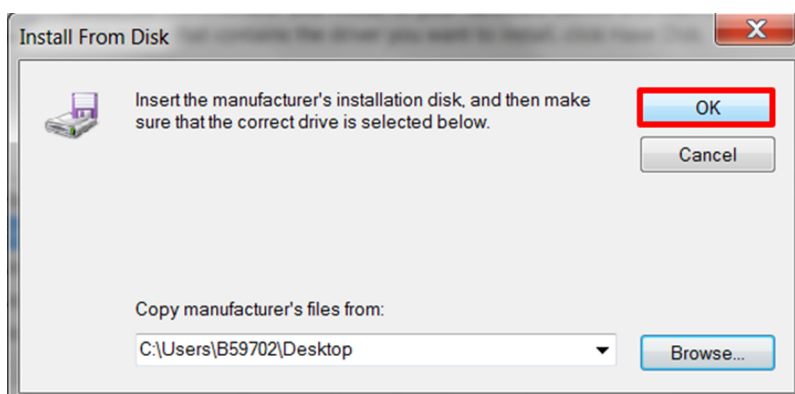
aaa-031988

10. In the **Locate File** window, locate and select **fsl_ucwxp**, and then click **Open**.



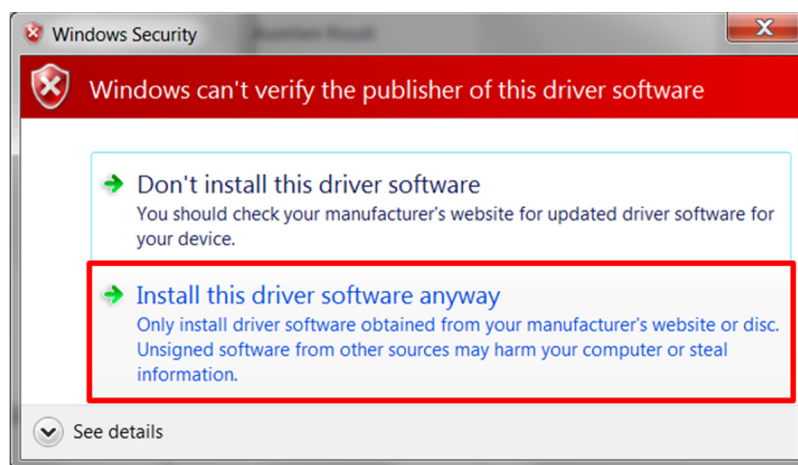
aaa-031989

11. In the **Install from Disk** window, click **OK**.



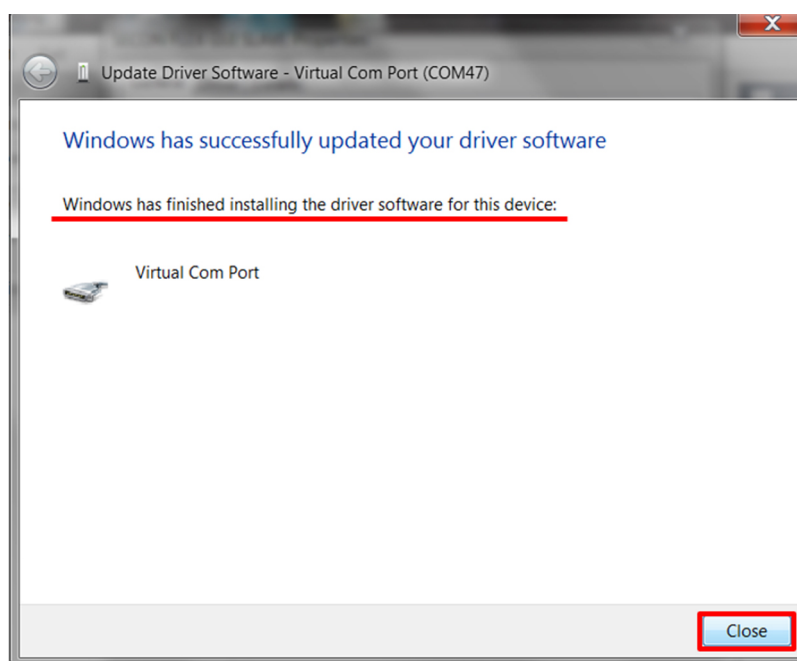
aaa-031990

12. If prompted, in the **Windows Security** window, click **Select this driver software anyway**.



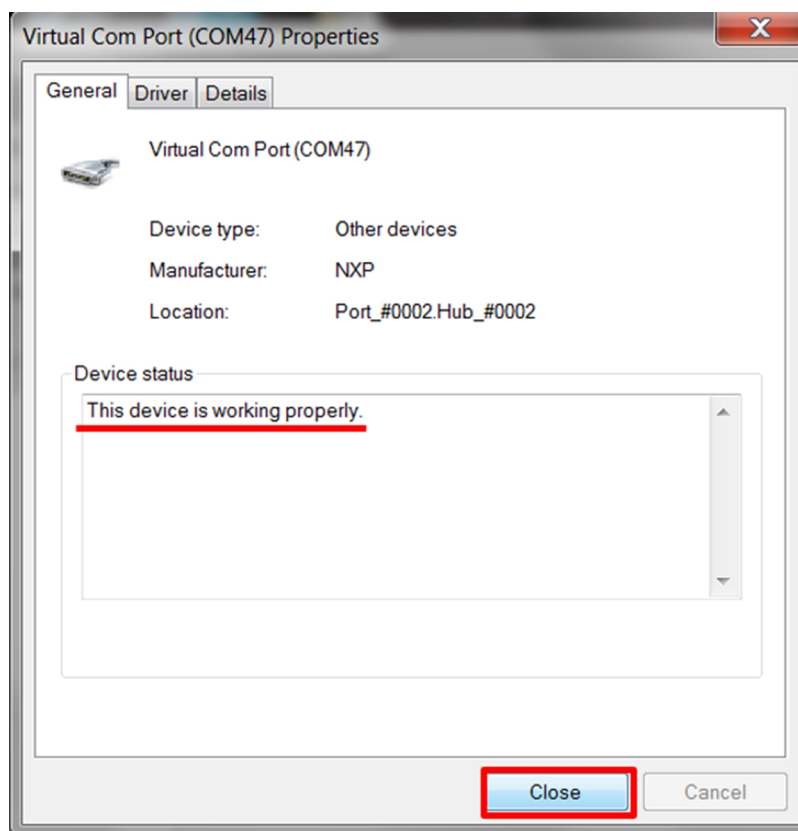
aaa-031991

13. Close the window when the installation is complete.



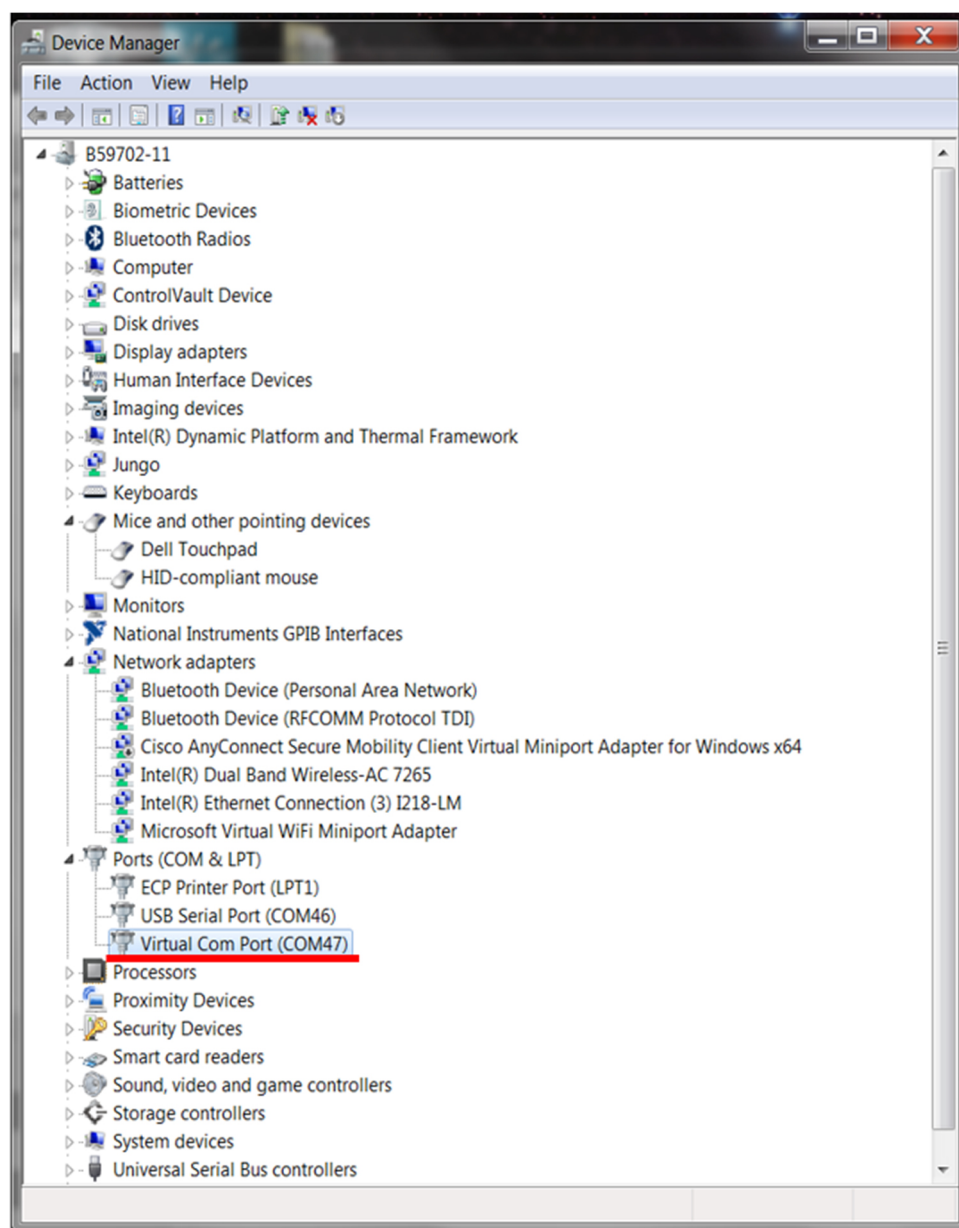
aaa-031992

14. In the **Virtual Com Port Properties** window, verify that the device is working properly, and then click **Close**.



aaa-031993

The Virtual Com Port appears in the Device Manager window.



aaa-031994

5.3 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
2. Download the latest FlexGUI (32-bit or 64-bit) version, available at <http://www.nxp.com/KITFS85FRDMEVM>.
3. Extract all the files to a desired location on your PC.
FlexGUI is started by running the batch file, `bin\flexgui-app-fs85.bat`.

6 Configuring the hardware for startup

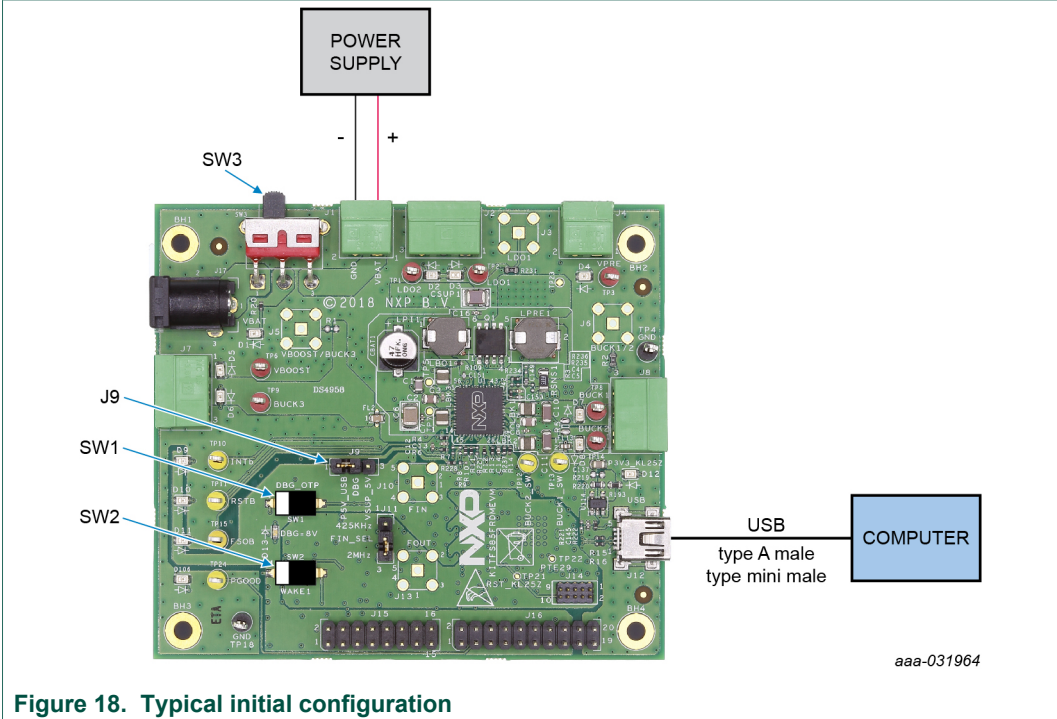


Figure 18 presents a typical hardware configuration incorporating the development board, power supply, and Windows PC workstation.

To configure the hardware and workstation as illustrated in Figure 18, complete the following procedure:

- 1. Install jumpers for the configuration.

Table 17. Jumper configuration

Jumper	Configuration
J9	connect 1-2 (connect 5.0 V on DBG pin from the USB)

- 2. Configure switches for the configuration.

Table 18. Switch configuration

Switch	Configuration
SW3	middle position (VBAT off)
SW1	open (OTP programming Off)
SW2	open (WAKE1)

- 3. Connect the Windows PC USB port to the KITFS85FRDMEVM development board using the provided USB 2.0 cable.
Set the DC power supply to 12 V and current limit to 1.0 A. With power turned off, attach the DC power supply positive and negative output to KITFS85FRDMEVM VBAT Phoenix connector (J1).
- 4. Turn on the power supply.
- 5. Close SW2.

Note: At this step, the product is in debug mode and all regulators are turned Off. The user can then power up with OTP configuration or configure the mirror registers before power up. Power up is effective as soon as J9 jumper is removed.

7 Using the KITFS85FRDMEVM evaluation board

This section summarizes the overall setup. Detailed description is provided in the following sections.

Before starting the process, choose the mode you want to run the device.

- In Normal mode, the configuration comes from OTP fuses.
- In Debug mode, you can either use the current configuration from OTP fuse, if any, or use the OTP emulation mode to write in the mirror register.

The Normal mode or Debug mode is defined at startup depending on the DBG pin level.

- Normal mode is set by tying DBG to ground.
- Debug mode is set by setting DBG voltage to 5.0 V.

In OTP emulation, you can overwrite the mirror registers from a given OTP fuse configuration. See [Section 4.2.1 "OTP and mirrors registers"](#) and [Section 8.3 "Working with the Script editor"](#) to define your configuration.

In OTP fuse configuration, use the configuration fused in the OTP. So, if a valid OTP fuse configuration exists, then it is copied to the mirror registers at startup.

7.1 Generating the OTP configuration file

Define and generate your OTP configuration using the excel file *FS85_FS84_OTP_Config.xlsm*. This file allows configuring the device for parameters controlled by the main state machine and the fail-safe state machine.

To generate the script:

1. Fill data in the **OTP_conf_main_reg** sheet.

MAIN OTP_REGISTERS											
Register Name	DDRES	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Data_Bin	Data_Hex
OTP_CFG_VPRE_1	14	-	-	-	-	VPRE[V5:0]	-	-	-	00100000	0x20
OTP_CFG_VPRE_2	15	-	-	-	-	VPRE[S6:0]	-	-	-	00000111	0x07
OTP_CFG_VPRE_3	16	-	-	-	-	VPRESLS[10]	-	-	-	10101100	0xAC
OTP_CFG_BOOST_1	17	-	-	-	-	VPRETIME[10]	-	-	-	00001101	0x0D
OTP_CFG_BOOST_2	18	-	-	-	-	VPREMODE	-	-	-	10001100	0x8C
OTP_CFG_BOOST_3	19	-	-	-	-	VPRETIME[10]	-	-	-	00000111	0x07
OTP_CFG_BUCK1_1A	1A	-	-	-	-	VBSTTIME[10]	-	-	-	10001000	0x88
OTP_CFG_BUCK1_1B	1B	-	-	-	-	VBSTTIME[10]	-	-	-	00000110	0x06
OTP_CFG_BUCK1_1C	1C	-	-	-	-	VBSTTIME[10]	-	-	-	10100001	0x81
OTP_CFG_BUCK1_1D	1D	-	-	-	-	VBSTTIME[10]	-	-	-	00011100	0x8C
OTP_CFG_BUCK1_1E	1E	-	-	-	-	VBSTTIME[10]	-	-	-	10010101	0x85
OTP_CFG_BUCK1_1F	1F	-	-	-	-	VBSTTIME[10]	-	-	-	10010011	0x83
OTP_CFG_LDO_1	20	-	-	-	-	LDOLIM	-	-	-	11111111	0x7F
OTP_CFG_SEQ_1	21	-	-	-	-	VB2S[2:0]	-	-	-	00000000	0x00
OTP_CFG_SEQ_2	22	-	-	-	-	LDOS[2:0]	-	-	-	00110000	0x38
OTP_CFG_SEQ_3	23	-	-	-	-	DVS_BUCK[10]	-	-	-	00000000	0x00
OTP_CFG_CLOCK_1	24	-	-	-	-	VPRE_pH[2:0]	-	-	-	00000100	0x04
OTP_CFG_CLOCK_2	25	-	-	-	-	BUCK1_pH[2:0]	-	-	-	00100000	0x30
OTP_CFG_CLOCK_3	26	-	-	-	-	BUCK2_pH[2:0]	-	-	-	00010000	0x18
OTP_CFG_CLOCK_4	27	-	-	-	-	BUCK3_pH[2:0]	-	-	-	00000000	0x00
OTP_CFG_SM_1	28	-	-	-	-	BUCK3_clk_sel	-	-	-	00000100	0x04
OTP_CFG_SM_2	29	-	-	-	-	otp_spares[2:0]	-	-	-	00000100	0x04
OTP_CFG_VSUP_U1	2A	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00
OTP_CFG_I2C	2B	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00
OTP_CFG_OV	2C	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00
OTP_CFG_DEVID	2D	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00
OTP_CFG_CRC_LS	2E	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00
OTP_CFG_CRC_MS	2F	-	-	-	-	otp_spares[2:0]	-	-	-	00000000	0x00

Figure 19. OTP_conf_main_reg spreadsheet example

- Fill data in the OTP_conf_failsafe_reg sheet.

FAIL-SAFE OTP_REGISTERS											
Register Name	ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Data_Bin	Data_Hex
OTP_CFG_UVUV_1	0A	-	-	-	-	VCORE_V[7:0]	-	-	-	10001000	0x88
OTP_CFG_UVUV_2	0B	-	-	-	-	VDDIOVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_UVUV_3	0C	-	-	-	-	VDDIO_V	-	-	-	00000000	0x00
OTP_CFG_UVUV_4	0D	-	-	-	-	VMON3OVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_UVUV_5	0E	-	-	-	-	VMON4OVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_UVUV_6	0F	-	-	-	-	VDDIOVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_UVUV_7	10	-	-	-	-	VMON2OVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_UVUV_8	11	-	-	-	-	VMON4OVTH[3:0]	-	-	-	11111111	0xFF
OTP_CFG_PGOOD	12	-	-	-	-	PGOOD_VMON4	-	-	-	00000000	0x00
OTP_CFG_ABIST1	13	-	-	-	-	ABIST1_VMON4	-	-	-	00000000	0x00
OTP_CFG_ASIL	14	-	-	-	-	ERRMON_EN	-	-	-	00000000	0x00
OTP_CFG_I2C	15	-	-	-	-	FLT_RECOVERY_EN	-	-	-	00000000	0x00
OTP_CFG_DGLT_DUR_1	16	-	-	-	-	VCORE_UV_DGLT[1:0]	-	-	-	00101101	0x2D
OTP_CFG_DGLT_DUR_2	17	-	-	-	-	VCORE_OV_DGLT	-	-	-	00000101	0x05
OTP_CFG_F5_S1_CRC_LSB	18	-	-	-	-	OTP_F5_S1_CRC_LSB[7:0]	-	-	-	00000000	0x00
OTP_CFG_F5_S1_CRC_MSB	19	-	-	-	-	OTP_F5_S1_CRC_MSB[7:0]	-	-	-	00000000	0x00

Figure 20. OTP_conf_failsafe_reg spreadsheet example

- See the OTP_conf_summary sheet to review the complete configuration (main and fail-safe).

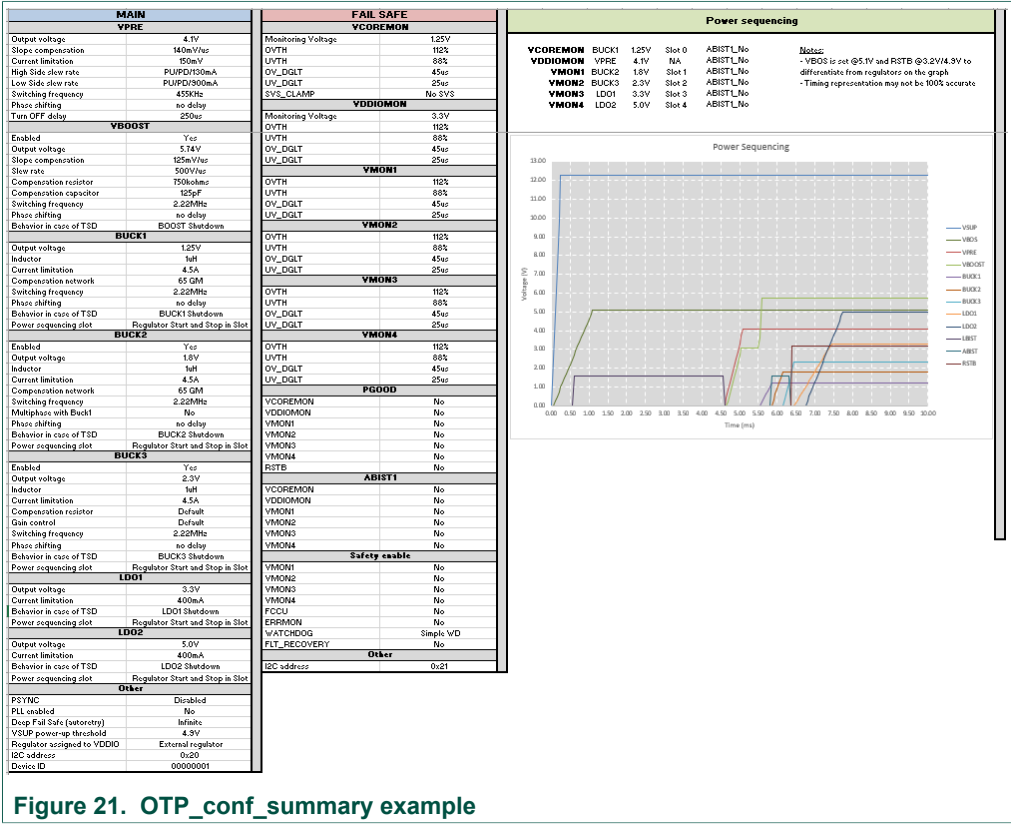


Figure 21. OTP_conf_summary example

4. Generate script in the **OTP_conf_file_generation** sheet.
- Once the configuration is ready, the user can generate the script file. Go to **OTP_conf_file_generation**, enter the path in the **File repository**, and then click **Write_OTP_File_GUI**.

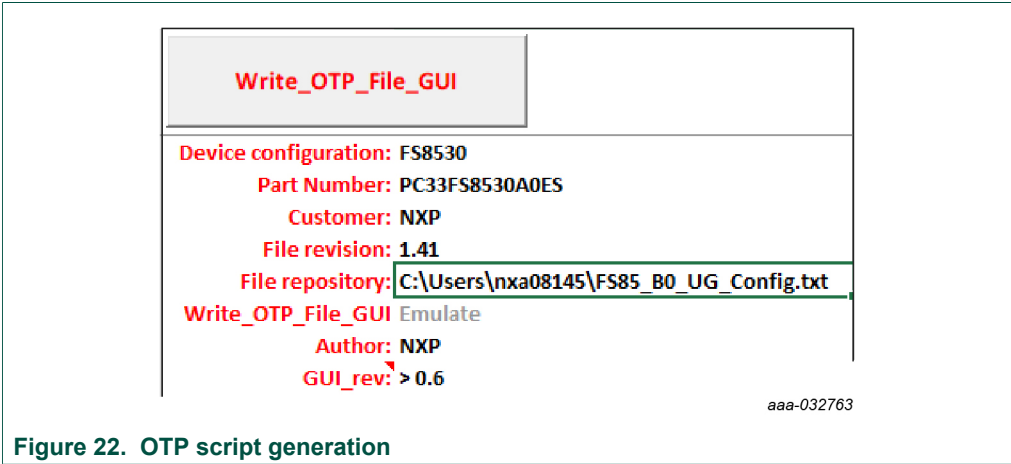


Figure 22. OTP script generation

7.2 Working in OTP emulation mode

At startup, the device always uses the content from the mirror register. This content can come from OTP fuse or from configuration written directly in the mirror register. OTP emulation means that the user can emulate the OTP writing in the mirror register. This allows trials before burning the OTP.

1. Configure the hardware. See [Section 6 "Configuring the hardware for startup"](#).
2. Launch the FlexGUI software.
3. Switch to Debug mode:
 - a. Place SW3 in the right direction (VBAT switched On).
 - b. Close SW2 (WAKE1).While in Debug mode, all regulators are turned Off.
4. Load the mirror registers to work in OTP emulation mode. See [Section 8.3 "Working with the Script editor"](#).
5. Unplug jumper J9 1-2 to start the device with the mirror configuration setting.
 - a. If the mirror registers are filled (with a configuration using the Script editor), that configuration is used in the emulation session.
 - b. If the mirror registers are not filled (with a configuration using the Script editor), the currently-programmed OTP fuse configuration is used, if it exists.
 - c. Otherwise, the mirror registers are not filled and the OTP fuse is not burned, and the device will not start up.

As long as initialization phase is not closed by a first good WD_Answer, the WD does not start and regulators do not stay alive. Also, as long as Debug mode is not exited by writing FS_STATES:[DBG_EXIT] bit to 1, the FS0B pin cannot be released.

6. Use the FlexGUI software to evaluate the device configured. See [Section 8 "Using FlexGUI"](#).

7.2.1 Example script: Closing initialization phase, disabling FCCU monitoring, and releasing FS0B

The following script can be used to:

- Disable the WD.
- Disable the FCCU monitoring.
On the hardware kit, the FCCU1 is pulled to GND and FCCU2 is pulled to VDDIO. Disabling the FCCU by SPI/I2C avoids safety issue at startup.
- Close the initialization phase.
- Exit the Debug mode.
- Release FS0B pin. This is valid only if WD is activated in OTP.
Seven good consecutive WD answers are required to have the FLT_ERR_CNTR back to 0. This is one of the conditions to allow FS0B release.

Table 19. FS85 starting sequence example

Step	Register name	Value	Description
1	FS_WD_WINDOW	0x0200	WDW_WINDOWS[3:0] = 0x0 => Watchdog disabled
2	FS_NOT_WD_WINDOW	0xF50F	NOT of FS_WD_WINDOW
3	FS_I_SAFE_INPUTS	0x51C6	FCCU_CFG[1:0] = 0x0 => 0x1 => Monitoring by pair FCCU12_FLT_POL[0] = 1 => FCCU1 or 2 = 0 is a fault
4	FS_I_NOT_SAFE_INPUTS	0xAC18	NOT of FS_I_SAFE_INPUTS
5	FS_WD_ANSWER	0x5AB2	First good WD answer (for simple WD selection in OTP) Close the initialization phase
6	FS_STATES	0x4000	DBG_EXIT[0]=1 => Exit Debug mode
7	FS_WD_ANSWER	0x5AB2	Second good WD answer
8	FS_WD_ANSWER	0x5AB2	Third good WD answer
9	FS_WD_ANSWER	0x5AB2	Fourth good WD answer
10	FS_WD_ANSWER	0x5AB2	Fifth good WD answer
11	FS_WD_ANSWER	0x5AB2	Sixth good WD answer
12	FS_WD_ANSWER	0x5AB2	Seventh good WD answer
13	FS_RELEASE_FS0B	0xB2A5	FS0B pin released (pulled to high level)
14	MFLAG2	0x40F1	Clear flags VSUPUV7; VPREUVL, VSUPUVL, WAKE1FLG
15	FS_OVUVREG_STATUS	0x4550	Clear UV status flags

This sequence can be sent using a script built with FlexGUI. See [Section 8.3.2 "Script sequence files"](#).

7.3 Programming the device with an OTP configuration

The device configuration can be changed three times (see [Section 4.2.1 "OTP and mirrors registers"](#)). The programming steps are the same as the OTP emulation mode up to step 6.

Then, the user has to burn the part with FlexGUI. See [Section 8.4.8 "OTP programming"](#). Follow the instructions on the screen to proceed.

8 Using FlexGUI

To follow the steps in this section, make sure that the board is connected using the appropriate hardware configuration (see [Section 7.2 "Working in OTP emulation mode"](#)).

Note: It is recommended to use the latest version of FlexGUI.

8.1 Starting the FlexGUI application

After FlexGUI is launched with the `flexgui-app.bat` file, the FlexGUI launcher displays available kits.

Communication bus, SPI, or I2C can be selected at this level. It is also possible to switch from one to the other using the communication tab from the main panel (see [Section 8.2 "Establishing the connection between FlexGUI and the hardware"](#)).

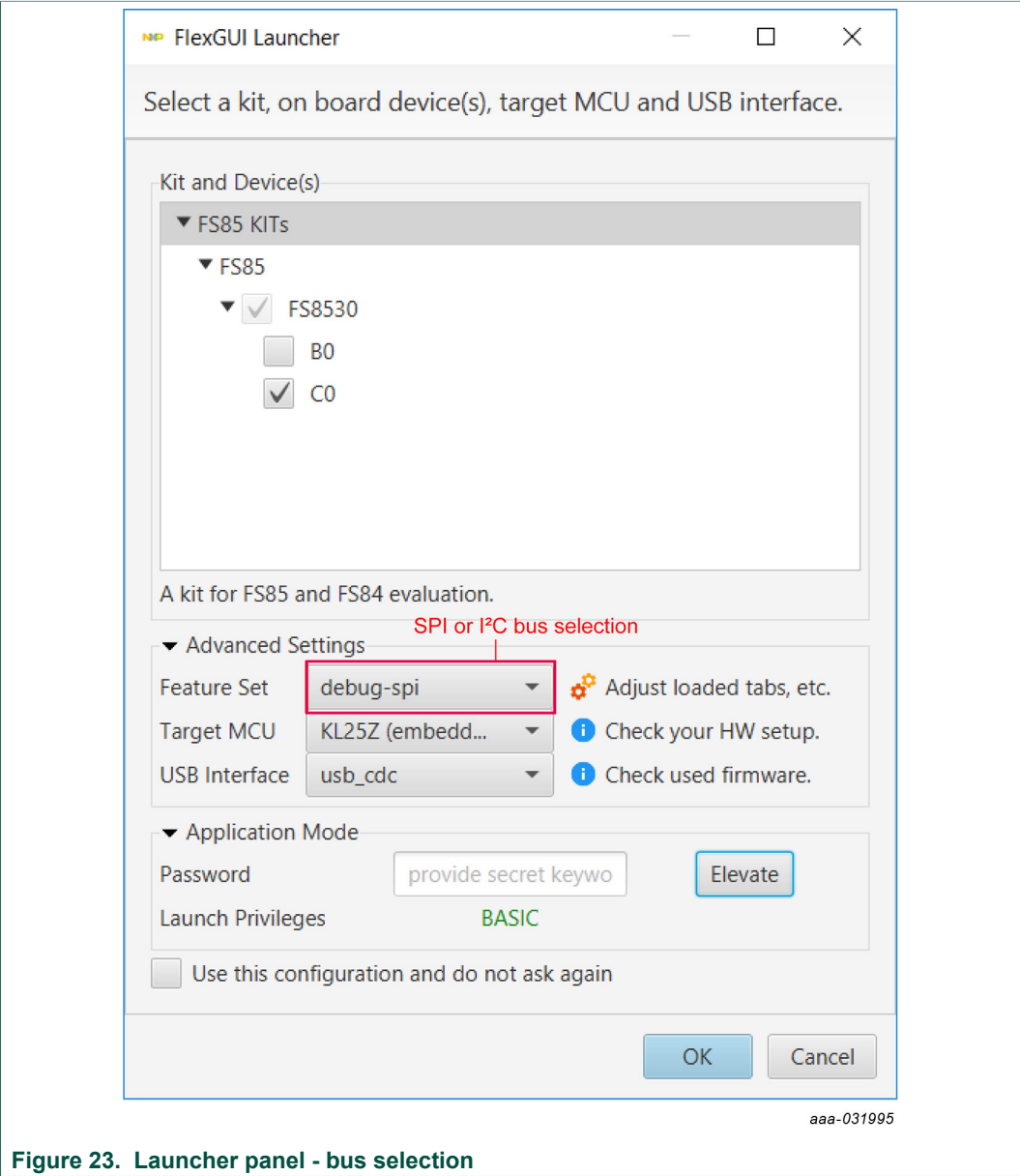


Figure 23. Launcher panel - bus selection

When the configuration is selected, click **OK**.

8.2 Establishing the connection between FlexGUI and the hardware

The board must be connected to the USB before establishing a connection.

- Click **Search** to detect the COM port of the board.
- Click **Start** to enable the connection.

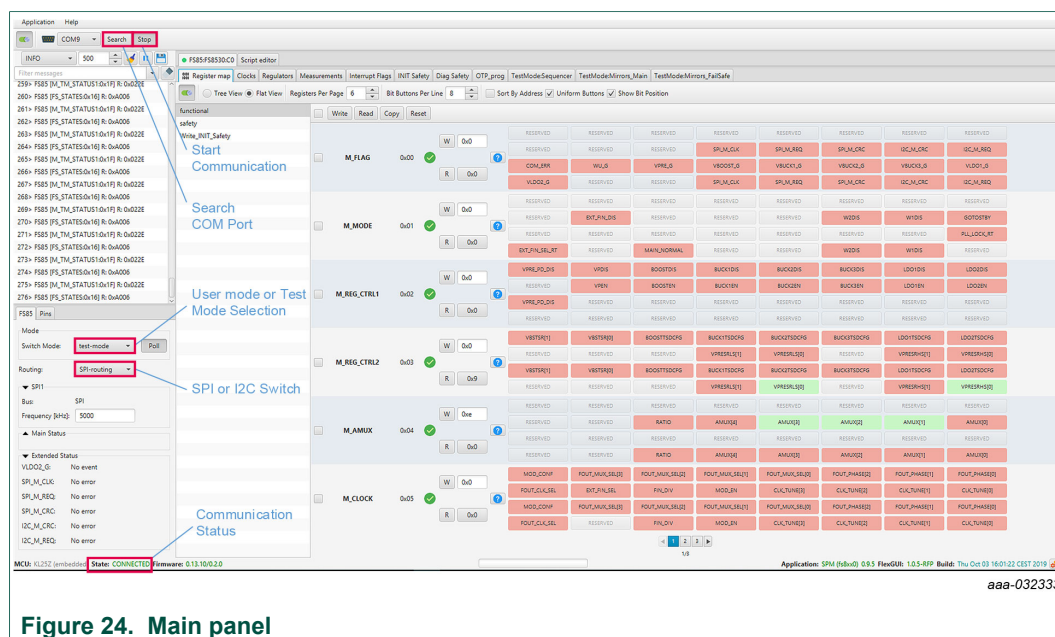


Figure 24. Main panel

Figure 24 shows the mode selection. At first launch, the FlexGUI starts in User mode. The user can then decide to switch to Test mode using the Switch mode drop-down list followed by clicking **Apply**.

The **GUI-Device Status** field checks the connection from MCU to the device. The **ONLINE** status indicates a good connection, while **ERROR** status indicates an issue (for example, V_{SUP} is not provided to the device).

The SPI/I2C communication bus can be changed at any time using the drop-down list. This change is managed by the onboard MCU to communicate with the desired bus.

It is also possible to change the clock frequency using this panel.

Note that in the case of I2C, most of the time, the default address used by the device are 0x20 for main and 0x21 for the fail-safe.

The I2C address is managed differently in Debug and Normal mode.

- Debug mode:
 - I2C address when debug mode pin is set to 5.0 V are 0x20 for main and 0x21 for fail-safe.
 - The user can change this address in the mirror register. The new address is taken into account only after debug pin is released to 0 V.
- Normal mode:
 - The address is burned in the OTP.

The user can read in which mode the device is operating. It is also possible to switch from user mode to test mode (and vice-versa).

The current mode is refreshed only when Poll button is activated. If required, this has to be done at startup (Poll button is disabled by default). See [Figure 25](#).

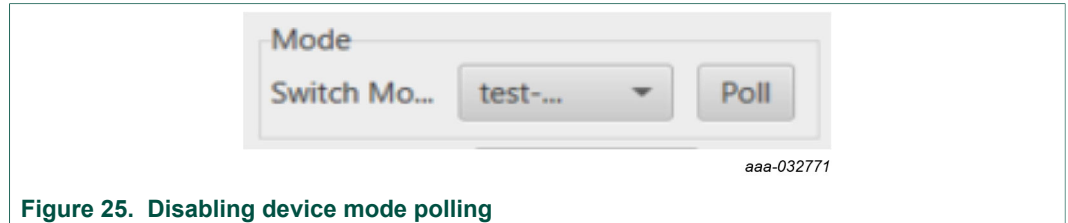


Figure 25. Disabling device mode polling

To move from one mode to the other, select the mode with switch mode drop-down button. If the requested mode is not confirmed by the device (if debug pin is not set, for instance), the drop-down menu switches back to the previous mode.

8.3 Working with the Script editor

The register and OTP emulation can be configured with the script editor. This is particularly useful to try various OTP configurations in Emulation mode.

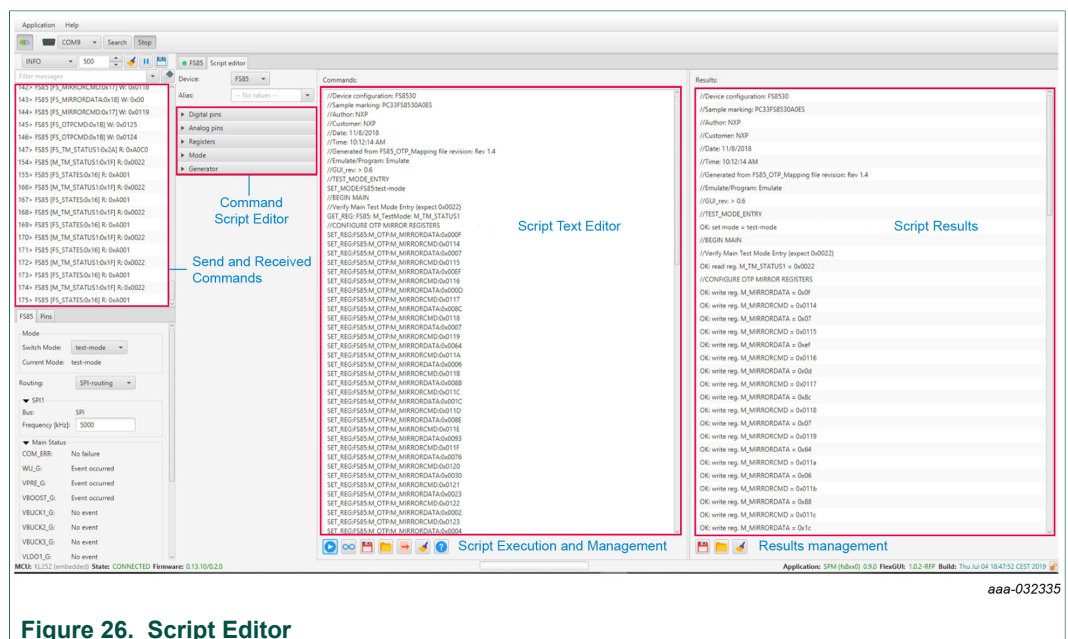


Figure 26. Script Editor

The main subareas of this panel are:

- **Send and receive command:** displays a summary of commands sent and received from the device
- **Command script editor:** builds commands to be sent to the device
- **Script text editor:** sends a sequence of register configurations from a text file or from command edited directly in this area
- **Script results:** displays result status of each command sent to the device

8.3.1 Script text editor

Using Script editor, you can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if needed.

All commands have to follow a specific syntax. The Help menu describes commands available in the script editor and their syntax.

This help page describes commands available in the script editor and their format.

List of commands

- **SET_REG**: sets value of a selected register.
- **READ_REG**: reads value of a selected register.
- **SET_DPIN**: sets value of a selected digital pin.
- **GET_DPIN**: gets value of a selected digital pin.
- **GET_APIN**: gets value of a selected analog pin. Returned value is in mV.
- **PAUSE**: shows a dialog with user defined message. The script is paused until the user confirms the dialog.
- **EXIT**: stops execution of the script.
- **SET_MODE**: sets device mode. List of modes depends on a device.

Command format

The following table describes command parameters. All parameters are mandatory.

	1st parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Pin name	Dig. pin value	-	-
GET_DPIN	Device	Pin name	-	-	-
GET_APIN	Device	Pin name	-	-	-
PAUSE	Message	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

- **Device**: device name (alias used in application).
- **Reg. set**: register set name. Register sets allows to associate registers which have similar function.
- **Reg. name**: register name as defined in datasheet.
- **Reg. address**: register address in decimal or hexadecimal (with 0x prefix) format.
- **Reg. value**: register value in decimal or hexadecimal (with 0x prefix) format.
- **Pin name**: name of digital or analog pin as defined in device datasheet.
- **Dig. pin value**: value of digital pin. Allowed strings are 'low' and 'high'.
- **Message**: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of parameters.
- **Mode**: name of a device mode.

Figure 27 shows an example to build a command from the panel.

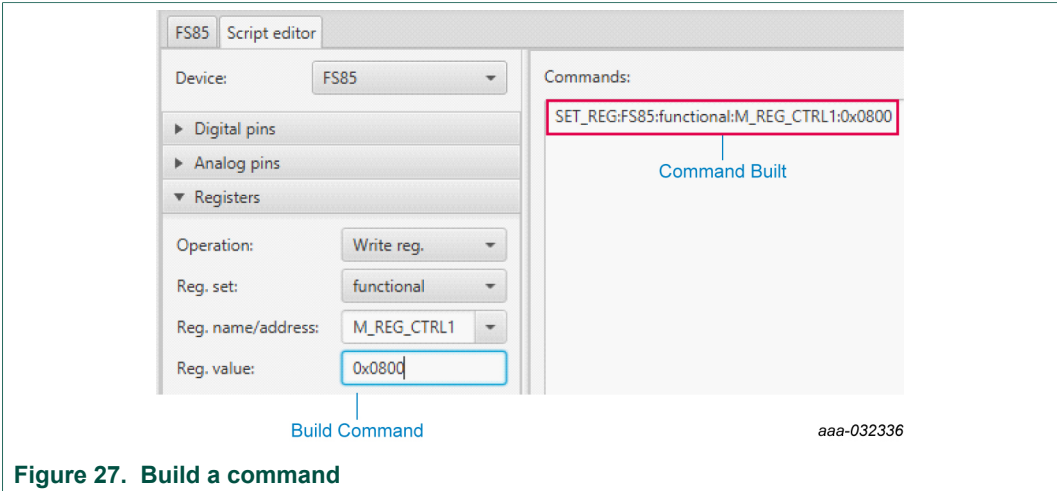


Figure 27. Build a command

The value 0x0800 is sent to the register M_REG_CTRL1 (BUCK2DIS). The user can then send it to the device by clicking the arrow (see [Figure 28](#)).

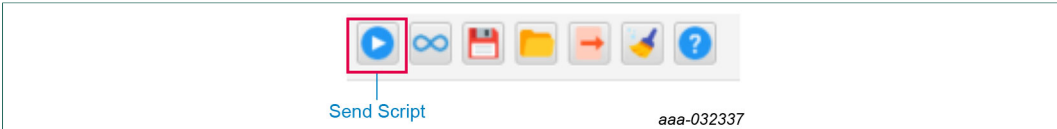


Figure 28. Send script

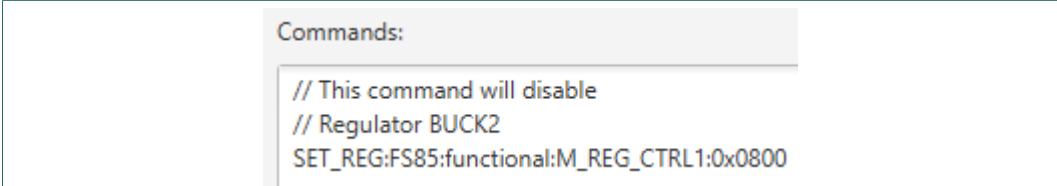


Figure 29. Correct format

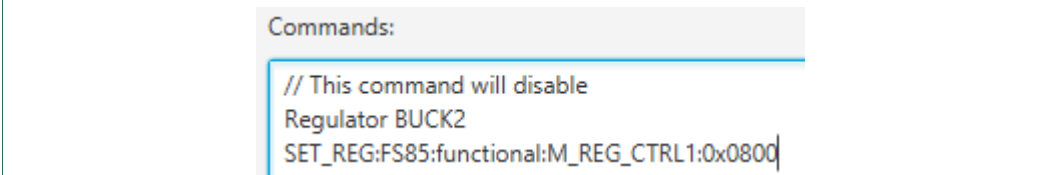


Figure 30. Wrong format (“//” missing in second line)

8.3.2 Script sequence files

The Script editor allows the user to save script sequence files. A script sequence file is text file that contains a set of commands sent to the device in the order they are written, as shown in the following example.

```
// FS85_Release_FS0b
SET_REG:FS85:safety:FS_WD_WINDOW:0x0200
SET_REG:FS85:safety:FS_NOT_WD_WINDOW:0xF50F
SET_REG:FS85:Write_INIT_Safety:FS_I_SAFE_INPUTS:0x51C6
SET_REG:FS85:Write_INIT_Safety:FS_I_NOT_SAFE_INPUTS:AC18
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_STATES:0x4000
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS85:safety:FS_RELEASE_FS0B:0xB2A5
```

Note: Comments can be added with a // prefix.

8.4 Understanding the FS85 workspace

The FS85 workspace consists of several tabs, each dedicated to a specific aspect of device functionality or configuration.

- Register map
- Clocks
- Regulators
- Measurements
- Interrupt flags
- INIT safety
- Diag safety
- OTP programming
- TestMode:Sequencer
- TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe

8.4.1 Register map

All SPI/I2C registers can be accessed in write and read mode using this tab.

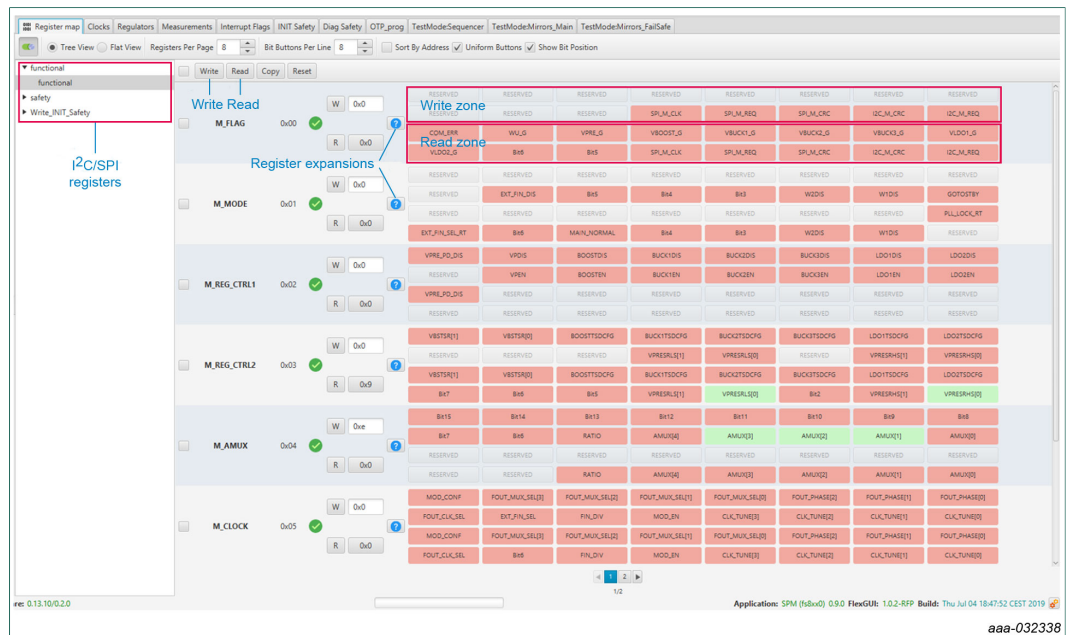


Figure 31. Register map

- **Register map:** allows access to functional register, safety register and write init register which is accessible only during initialization phase
- **Read:** allows you to read any register either individually or by bank
- **Write:** allows you to write any register either individually or by bank
- **Register expansion:** displays the value of each device parameter

8.4.2 Clocks

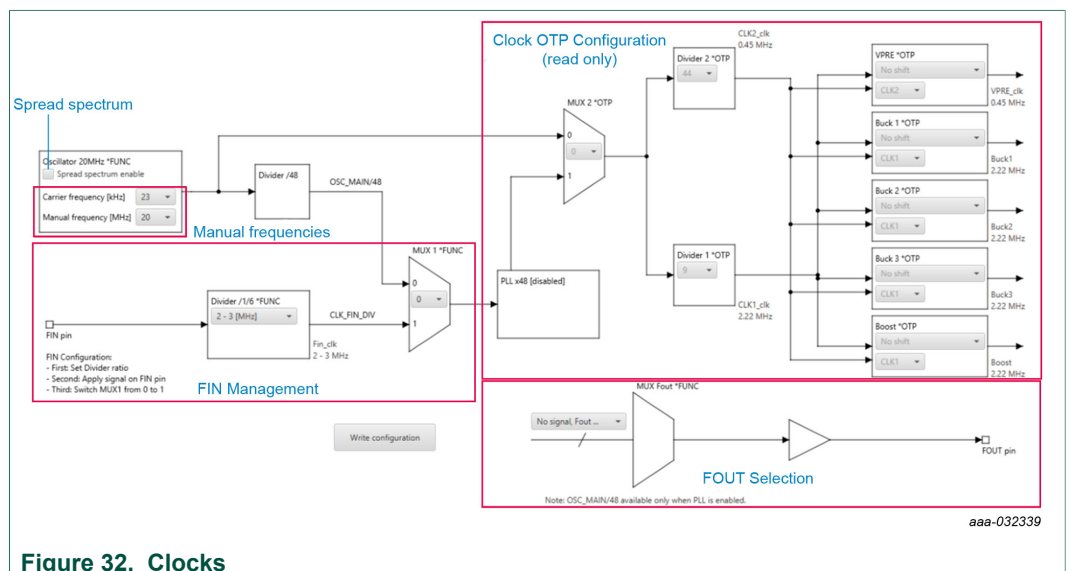


Figure 32. Clocks

This tab allows:

OTP:

- Read current OTP configuration (write operation is not possible). To display the accurate data, the device must operate in Test mode.

SPI/I2C:

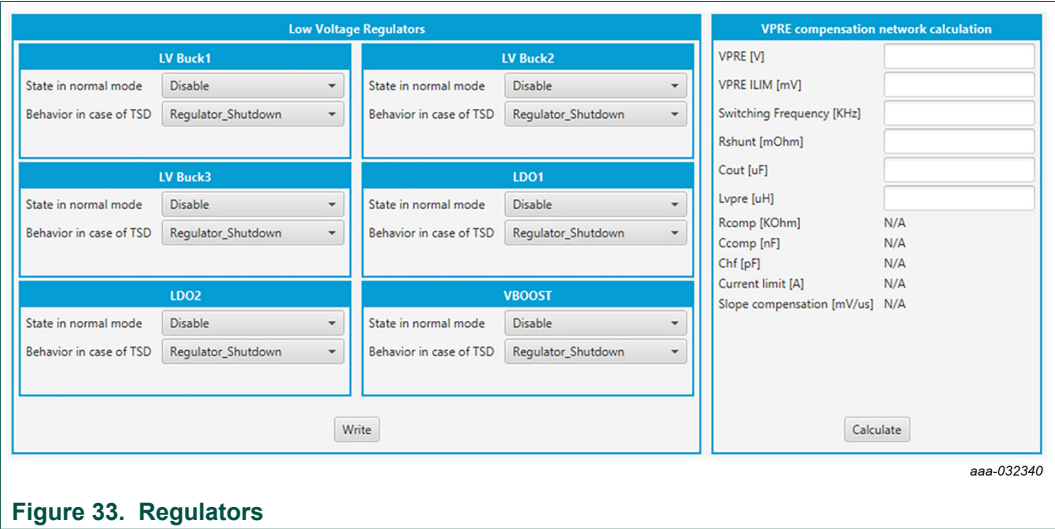
- Configure the device to work with FIN input
- Select the signal to apply on FOUT pin
- Play with manual frequencies and spread spectrum

8.4.3 Regulators

The regulator has two main areas:

- Low voltage (LV) regulators configuration
- VPRE compensation network calculation

Each regulator can either be enabled or disabled by SPI/I2C. The thermal shutdown behavior can be configured to either shutdown the regulator, or shutdown the regulator and transition to deep fail-safe. The write button applies to the entire table. The VPRE compensation network calculator helps to define the value for VPRE external compensation network.



8.4.4 Measurements

This tab enables two features:

- Read any of the AMUX signals over time
- Display regulator voltage summary

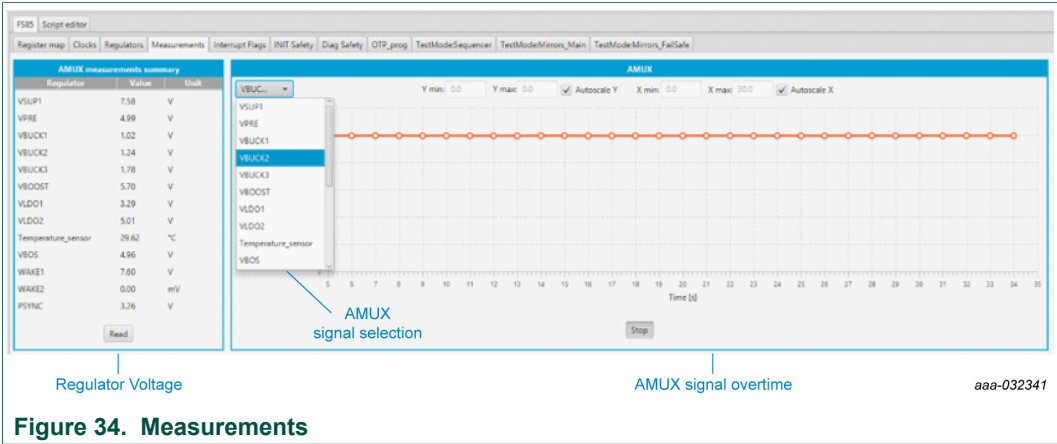


Figure 34. Measurements

8.4.5 Interrupt flags

This tab allows you to set or clear flags. It is also possible to mask the interruption.

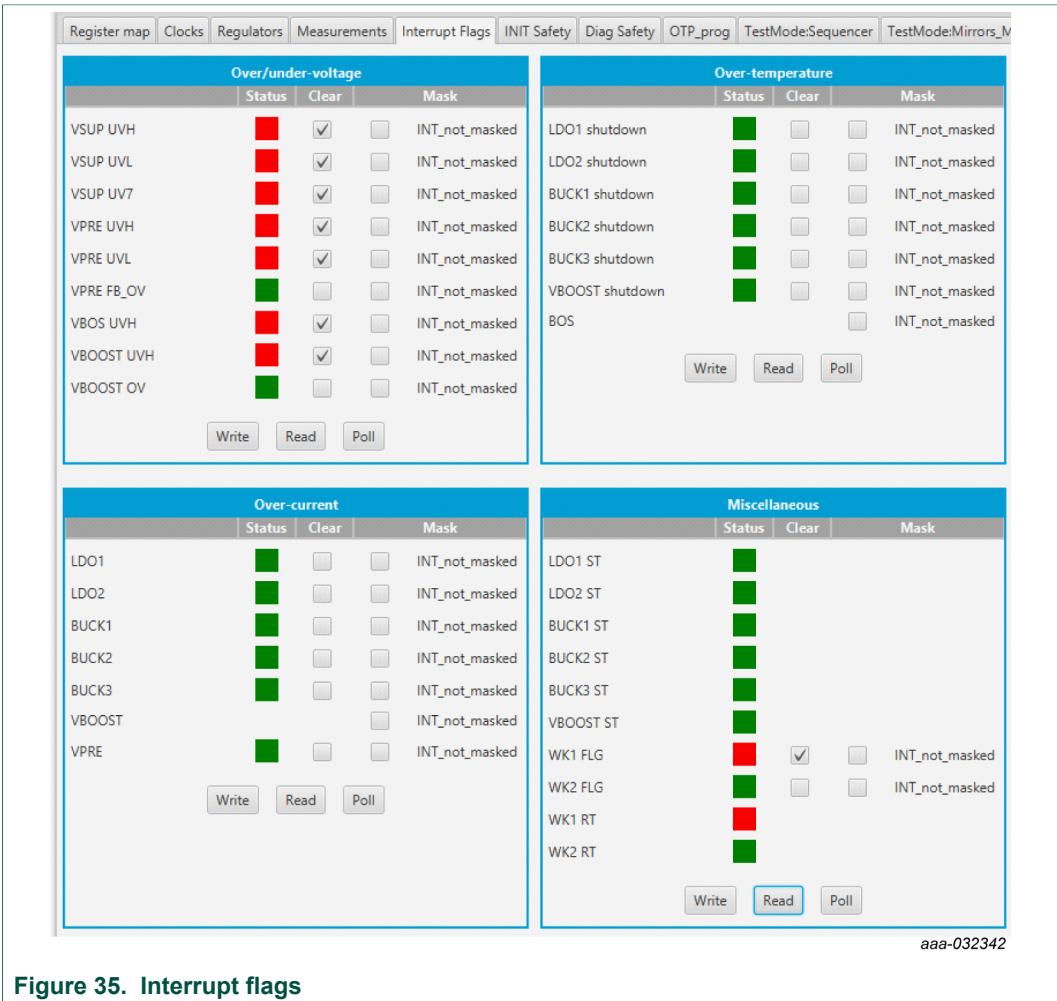


Figure 35. Interrupt flags

8.4.6 INIT safety

This tab allows you to manage all registers that can be configured to close the initialization phase. The initialization phase is closed by the first good watchdog refresh before 256 ms timeout.

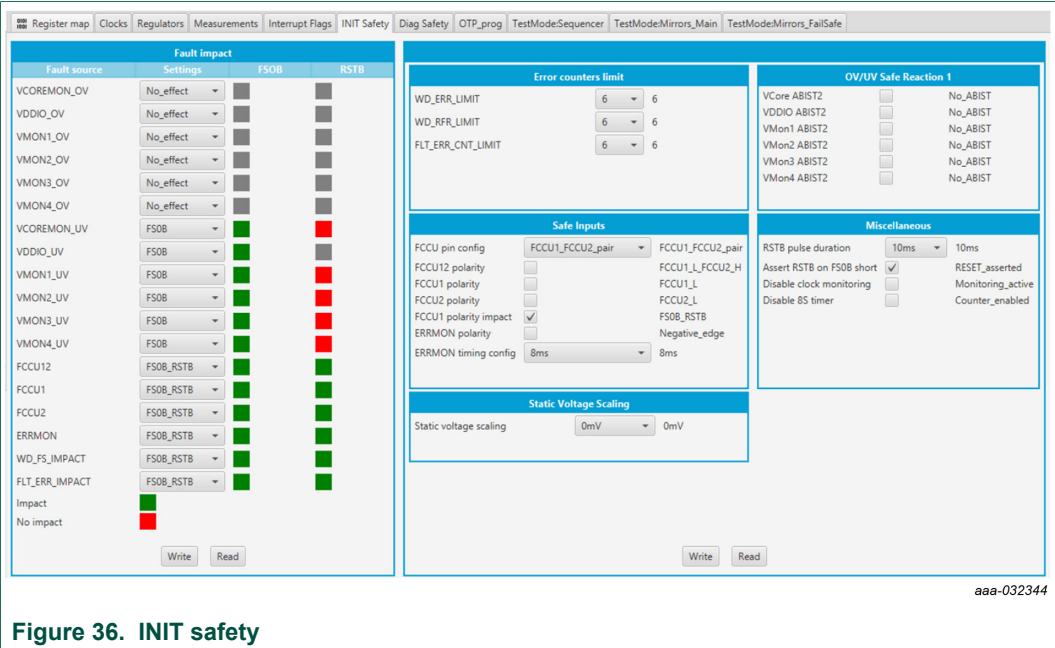
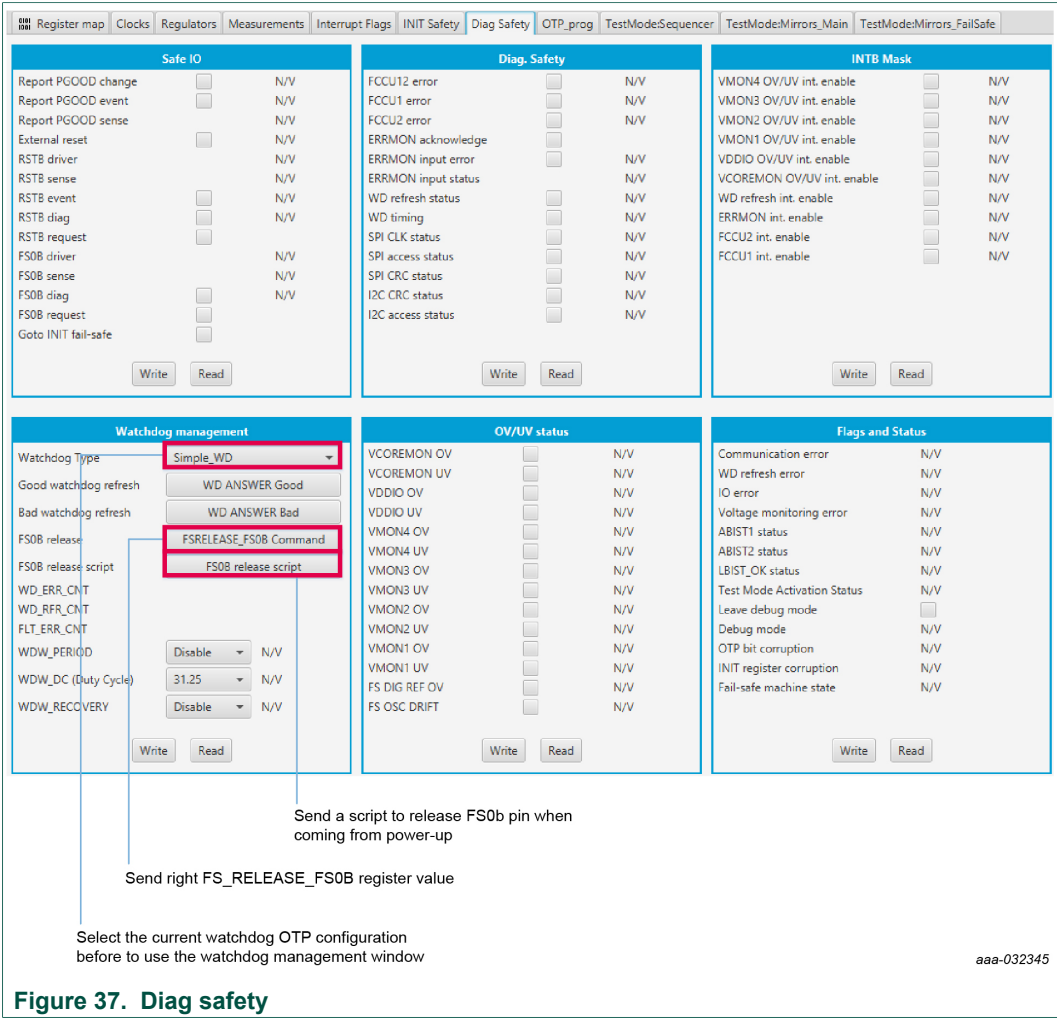


Figure 36. INIT safety

8.4.7 Diag safety

The watchdog type configured in the OTP has to be manually selected in the drop-down list to play with the watchdog features. If the user is not aware about the type of watchdog configured in the OTP, it can be found in TestMode:Mirrors_Failsafe and Miscellaneous tabs.



The FS_Release_FS0B command calculates and sends the right secure16-bit word to release FS0B.

A simplified way to release FS0B after power up is to, first, select the right type of watchdog configured in the OTP, then, hit FS0B Release script button. This sends the right sequence to close the initialization sequence, sets the error counter back to 0, then releases FS0B.

8.4.8 OTP programming

This tab allows you to burn the OTP using a script generated by the excel file OTP configuration (see [Section 7.1 "Generating the OTP configuration file "](#)).

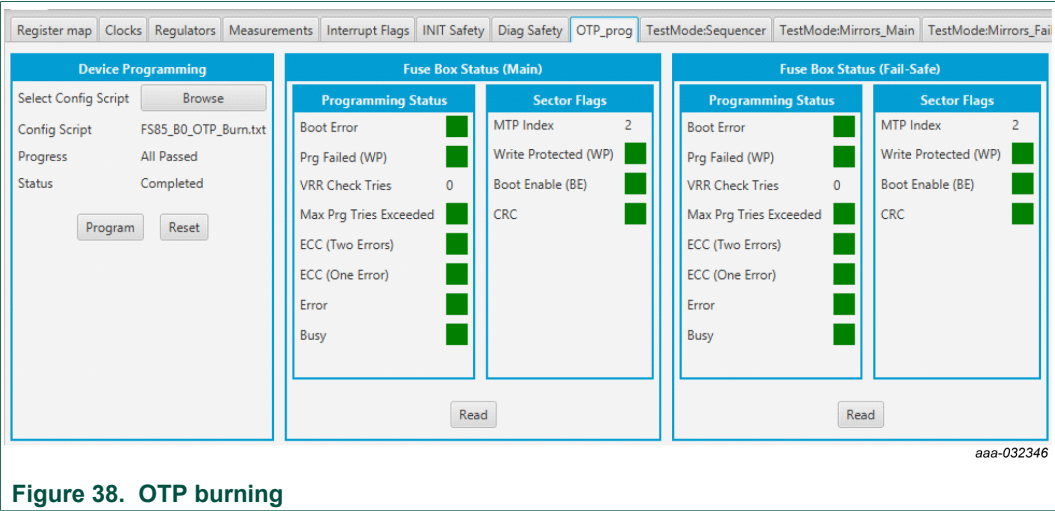


Figure 38. OTP burning

To set up the hardware before OTP burning, see [Section 7.3 "Programming the device with an OTP configuration"](#).

See [Figure 38](#) and follow the steps:

- Browse and load the script file you want to burn. The program button is then available.
- Click **Program**.

FlexGUI pops up to turn the 8.0 V On, and then turns Off. Note that the blue LED on the board indicates that an 8.0 V voltage is available on the Debug pin. This voltage is used only during the burning process, and should not be applied in any other configuration. At the end of the first OTP programming, the MTP index = 1, WP, BE, and CRC flags are green.

The Sector Flags area provides status [Table 20](#) provides the state of main flags after a read. This helps to determine how many times the part was burned.

Table 20. OTP burning flag status

OTP burning step	BE	WP	CRC	MTP Index
OTP not burn Mirrors Empty	Red	Red	Red	1
OTP not Burn Mirrors Filled	Red	Red	Green	1
1	Green	Green	Green	1
2	Green	Green	Green	2
3	Green	Green	Green	3

Example shown in [Figure 38](#) corresponds to the OTP burning step 2 from [Table 20](#).

To check if a valid OTP configuration is already burned, switch V_{BAT} Off, then On, and start the device. The device starts with the OTP configuration.

8.4.9 TestMode:Sequencer

The sequencer allows you to display the slot configuration for the device. To be able to access this tab, the device has to be in Test mode. The configuration is read from mirror register. It is possible to modify it and update the mirror register.

As an example, the slot sequence is filled at startup with the content of OTP fuses. Then the user can decide to modify any of the configurations coming from the OTP fuse. Note that all these actions are done with Debug pin at 5.0 V and in test mode.

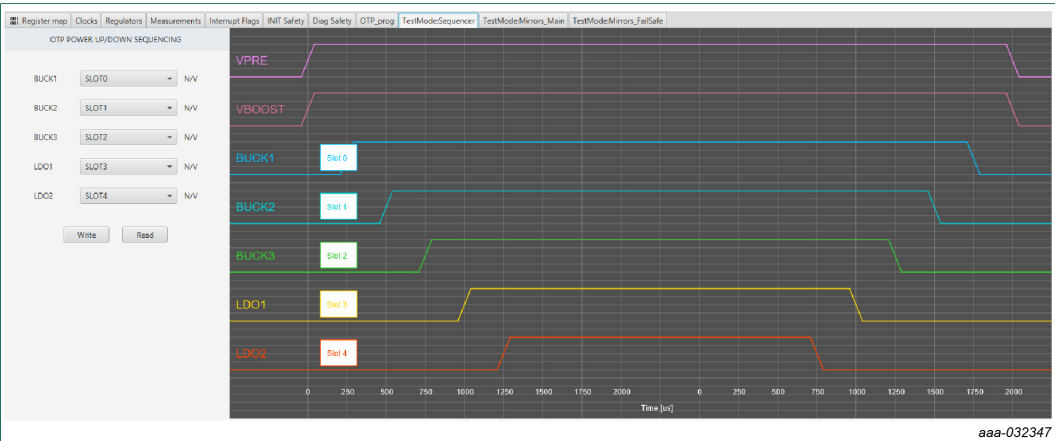


Figure 39. TestMode:Sequencer

Use the drop-down button (see [Figure 40](#)) to select the appropriate slot. The selection configuration can be sent to the device by clicking Write button. The current status can be read by using Read button.

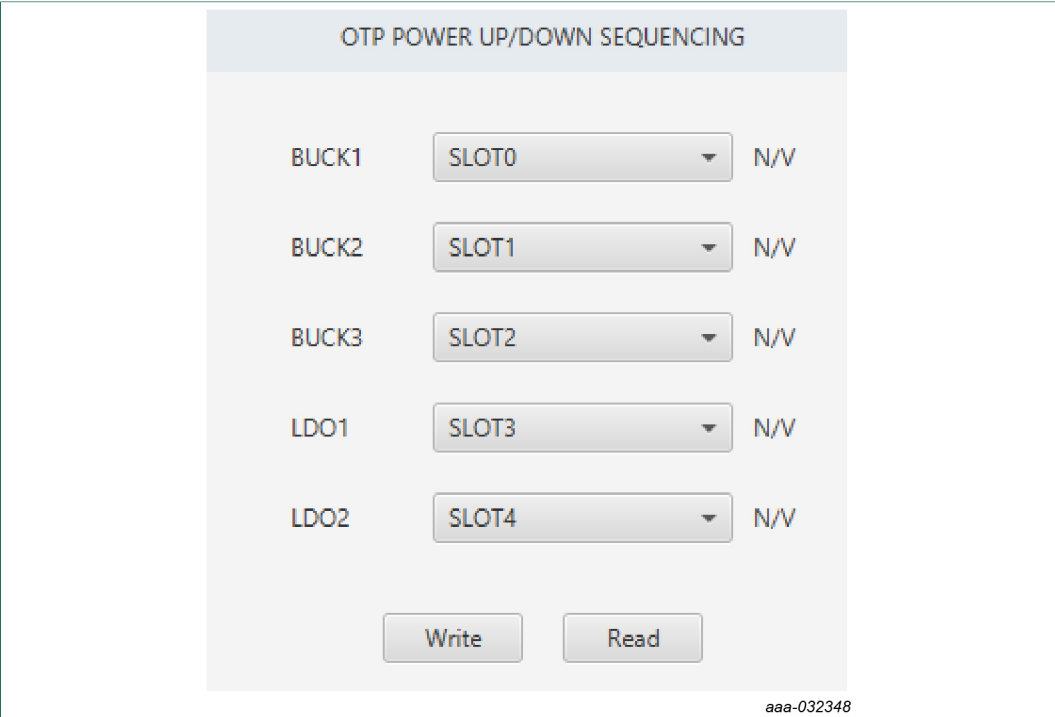


Figure 40. Slot management

8.4.10 TestMode:Mirrors_Main and TestMode:Mirrors_Failsafe

The TestModeMirrors_Main and TestModeMirrors_FailSafe tabs allow access to the OTP main mirrors and fail-safe registers. These tabs are available in Test mode.

In this panel, some parameters are highlighted in red. The red indicates that these parameters are not considered in case of emulation mode (accessible only in debug mode). The user must rewrite by SPI or I2C after startup.

This concerns only:

- VPRE and VBOOST slew rate
- All regulator behavior in case of TSD

VPRE mode

Force PWM

Force PWM

Output voltage

17

17

Slope compensation

170mV/us

170mV/us

Current limitation threshold

50mV

50mV

Low Side slew rate control

130mA

130mA

High Side slew rate control

260mA

260mA

VPRE phase (delay) selection

Delay2

Delay2

Delay to turn OFF VPRE at device power down

32ms

32ms

VPRE clock selection

CLK_DIV1

CLK_DIV1

Write

Read

BOOST

Output voltage

1

1

BOOST enable

Disabled

Disabled

BOOST minimum ON time

60ms

60ms

VBOOST slope compensation

17

17

Compensation Network Resistor Rco...

750kohms

750kohms

Compensation Network Capacitor C...

1

1

VBOOST current limitation

0

0

VBOOST Low Side slew rate control

1

1

BOOST phase (delay) selection

Delay1

Delay1

BOOST clock selection

CLK_DIV2

CLK_DIV2

BOOST shutdown

BOOST shut...

BOOST shut...

Write

Read

LDOs

VLD02 current limitation

400mA

400mA

VLD02 output voltage

1.2V

1.2V

LDO2 sequencing slot

Slot2

Slot2

Regulator behavior in case o...

LDO2 shutdown + ...

LDO2 shutdown + ...

VLD01 current limitation

400mA

400mA

VLD01 output voltage

1.2V

1.2V

LDO1 sequencing slot

Slot1

Slot1

Regulator behavior in case o...

LDO1 shutdown

LDO1 shutdown

Write

Read

BUCK1

VBUCK1 output voltage

17

17

BUCK1 inductor selection

1.5uH

1.5uH

VBUCK1 current limitation

0

0

VBUCK1 & VBUCK2 multiphase operation

Enabled

Enabled

BUCK1 Compensation Network

65GM

65GM

BUCK1 sequencing slot

Slot1

Slot1

BUCK1 phase (delay) selection

Delay2

Delay2

BUCK1 clock selection

CLK_DIV1

CLK_DIV1

Regulator behavior in case of TSD

BUCK1 shutdown + ...

BUCK1 shutdown + ...

BUCK1 and BUCK2 Soft start/stop configura...

7.81mV/us

7.81mV/us

Write

Read

BUCK2

VBUCK2 output voltage

17

17

BUCK2 inductor selection

1uH

1uH

BUCK2 enable

Enabled

Enabled

VBUCK2 current limitation

0

0

BUCK2 compensation network

0

0

BUCK2 sequencing slot

Slot2

Slot2

BUCK2 phase (delay) selection

Delay1

Delay1

BUCK2 clock selection

CLK_DIV1

CLK_DIV1

Regulator behavior in case of TSD

BUCK2 shutdown

BUCK2 shutdown

Write

Read

BUCK3

VBUCK3 output voltage

2.8V

2.8V

BUCK3 enable

Disabled

Disabled

BUCK3 inductor selection

1uH

1uH

VBUCK3 current limitation

2.6A

2.6A

BUCK3 compensation resistor

Default

Default

BUCK3 gain control

1

1

BUCK3 sequencing slot

Slot1

Slot1

BUCK3 phase (delay) selection

Delay2

Delay2

BUCK3 clock selection

CLK_DIV1

CLK_DIV1

Regulator behavior in case of ...

BUCK3 shutdown

BUCK3 shutd...

Soft start/stop configurability

3.47mV/us

3.47mV/us

Write

Read

CLOCK

PLL enable

Disabled

Disabled

Divider 1 setting

Divide8

Divide8

Divider 2 setting

Divide10

Divide10

Write

Read

SM

Deep Fail-safe infinite autoretry enable

Disabled

Disabled

Deep Fail-safe autoretry enable

Disabled

Disabled

Synchronization with 1x FS85 or 1x PF82

2xFS85

2xFS85

Synchronization with 2 devices

Enabled

Enabled

Device I2C address

D1

D1

Write

Read

VSUP UV/UV

VSUP Under Voltage Threshold Configuration

6.2V

6.2V

Regulator assigned to VDDIO (OV)

VPRE

VPRE

Write

Read

aaa-032350

Figure 41. TestMode: Mirrors_Main

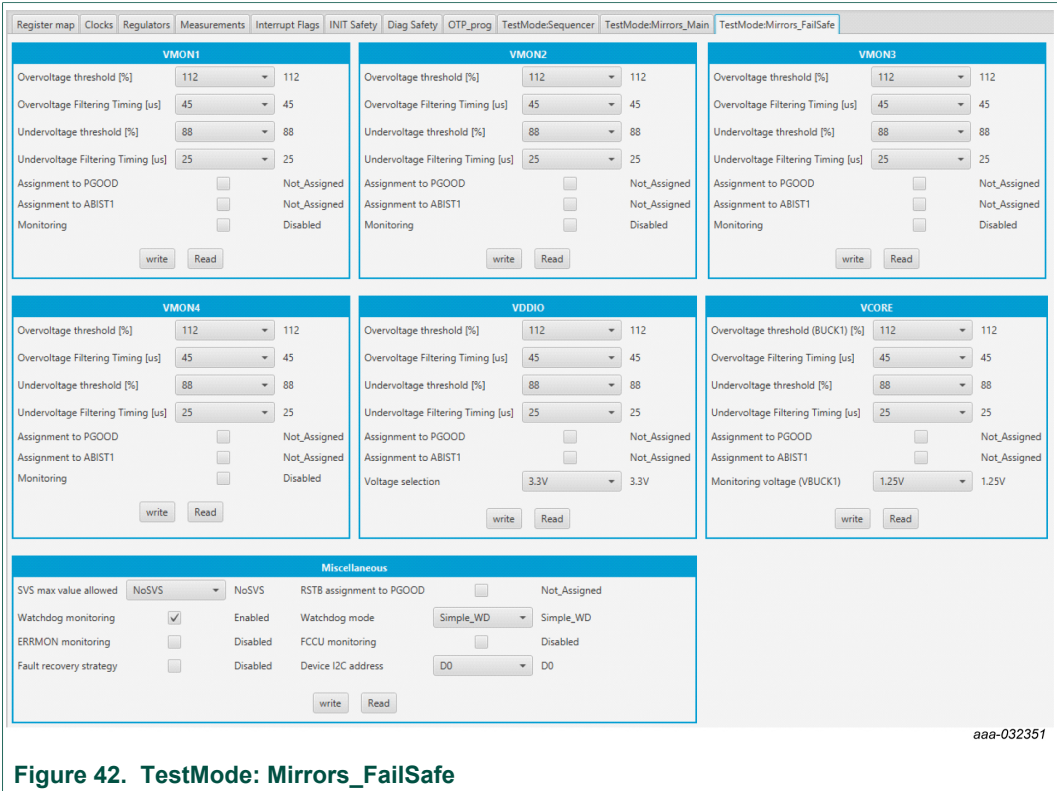


Figure 42. TestMode: Mirrors_FailSafe

The Read button provides the status. The Write button changes the configuration in mirror register. This can be useful, for example, to modify few parameters from OTP fuse to start up the board.

9 References

- [1] **KITFS85FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools
<http://www.nxp.com/KITFS85FRDMEVM>
- [2] **FS8500** — product information on FS8500, Safety system basis chip for S32 microcontrollers, fit for ASIL D
<http://www.nxp.com/FS8500>
- [3] **FS8400** — product information on FS8400, Safety system basis chip for S32 microcontroller, fit for ASIL B
<http://www.nxp.com/FS8400>
- [4] **FS85_FS84_OTP_Config.xlsm** — OTP configuration file

10 Revision history

Revision history

Rev	Date	Description
v.3	20191206	<ul style="list-style-type: none">• Section 8.1: updated Figure 23• Section 8.2: updated description and Figure 24, Figure 25• Section 8.3: updated Figure 26• Section 8.3.1: updated Figure 28• Section 8.4.1: updated Figure 31• Section 8.4.2: updated Figure 32• Section 8.4.6: updated Figure 36• Section 7.1: updated OTP_conf_main_reg spreadsheet example• Section 8.4.3: updated Figure 33• Section 8.4.10: updated Figure 41
v.2	20190220	<ul style="list-style-type: none">• Global: reorganized content to match latest template• Section 7.1: replaced FS85_OTP_Configuration.xls by FS85_FS84_OTP_Config.xlsm• Section 4.3.5: updated Table 13• Section 6: updated the configuration procedure• Section 8.4.7: updated Figure 37• Section 8.4.9: updated Figure 39 and Figure 40• Section 8.4.10: updated Figure 41
v.1	20181204	Initial version

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