Advance Information

MPC852TTS/D
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# MPC852T PowerQUICC™ Technical Summary

This document provides an overview of the MPC852T PowerQUICC™ device, describing major functions and features. The MPC852T PowerQUICC device contains a PowerPC™ processor core.



The MPC852T PowerQUICC is a 0.18 micron version of the MPC860 PowerQUICC Family and can operate up to 100 MHz on the MPC8xx Core with a 66 MHz external bus. The MPC852T has a 1.8 V core and has a 3.3 V I/O operation with 5 V TTL compatibility. The MPC852T Integrated Communications Controller is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in both communications and networking systems.

The MPC852T is a PowerPC architecture-based derivative of Motorola’s MPC860 Quad Integrated Communications Controller (PowerQUICC). The CPU on the MPC852T is the MPC8xx core, a 32-bit microprocessor which implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches.

Table 1 shows the functionality supported by the MPC852T device:

**Table 1. MPC852T**

| Part | Cache | | Ethernet | | SCC | ATM Support |
|---|---|---|---|---|---|---|
| | Instruction Cache | Data Cache | 10Base T | 10/100 | | |
| MPC852T | 4 Kbyte | 4 Kbyte | Up to 2 | 1 | 2 | No |

## 1.1 Features

The following list summarizes the key MPC852T features:

- Embedded MPC8xx core up to 100 MHz
- Maximum frequency operation of the external bus is 66 MHz
  - The 100MHz/80MHz core frequencies support 2:1 mode only
  - The 50MHz/66MHz core frequencies support both 1:1 and 2:1 modes
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with 32, 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4-Kbyte data cache and 4-Kbyte instruction cache
    - 4-Kbyte instruction cache is two-way, set-associative with 128 sets
    - 4-Kbyte data cache is two-way, set-associative with 128 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- 32 address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- Fast Ethernet controller (FEC)
- General-purpose timers
  - Two 16-bit timers or one 32-bit timer
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog

  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Interrupts
  - Seven external interrupt request (IRQ) lines
  - 7 port pins with interrupt capability
  - 18 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - 8 serial DMA (SDMA) channels
  - Three parallel I/O registers with open-drain capability
- Two baud rate generators
  - Independent (can be connected to SCC3, SCC4 or SMC1)
  - Allow changes during operation
  - Autobaud support option
- Two SCCs (serial communication controllers)
  - Ethernet/IEEE 802.3 optional on SCC3 & SCC4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC))
- One SMC (serial management channels)
  - UART.
- One SPI (serial peripheral interface)
  - Supports master and slave modes
  - Supports multimaster operation on the same bus
- PCMCIA interface

  - Master (socket) interface, release 2.1 compliant
  - Supports one independent PCMCIA sockets. 8 memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a break point internally
- Normal High and Normal Low Power Modes to conserve power
- 1.8 V Core and 3.3 V I/O operation with 5-V TTL compatibility
- 256-pin, 23mm x 23mm ball grid array (BGA) package

**Table 2. MCPC852T Possible Configurations**

| Config. | No. of Ethernet Ports | MII | 10BaseT (SCC3/SCC4) | PCMCIA | SMC1 | HDLC / Transparent / UART / Appletalk (SCC3/SCC4) | Note |
|---|---|---|---|---|---|---|---|
| 1 | 3 | Yes | Yes SCC3 & SCC4 | Yes | Yes | No | MII=portD, both SCC3 & SCC4 work as 10BaseT; parameter ram reload microcode needed for SMC1 |
| 2 | 2 | Yes | Yes, SCC4 | Yes | Yes | Yes, SCC3 | MII=portD, SCC4 works as 10BaseT while SCC3 works as HDLC/UART/etc |

The MPC852T is comprised of three modules that each use the 32-bit internal bus: the MPC8xx core, the system integration unit (SIU), and the communication processor module (CPM). The MPC852T block diagram is shown in Figure 1.

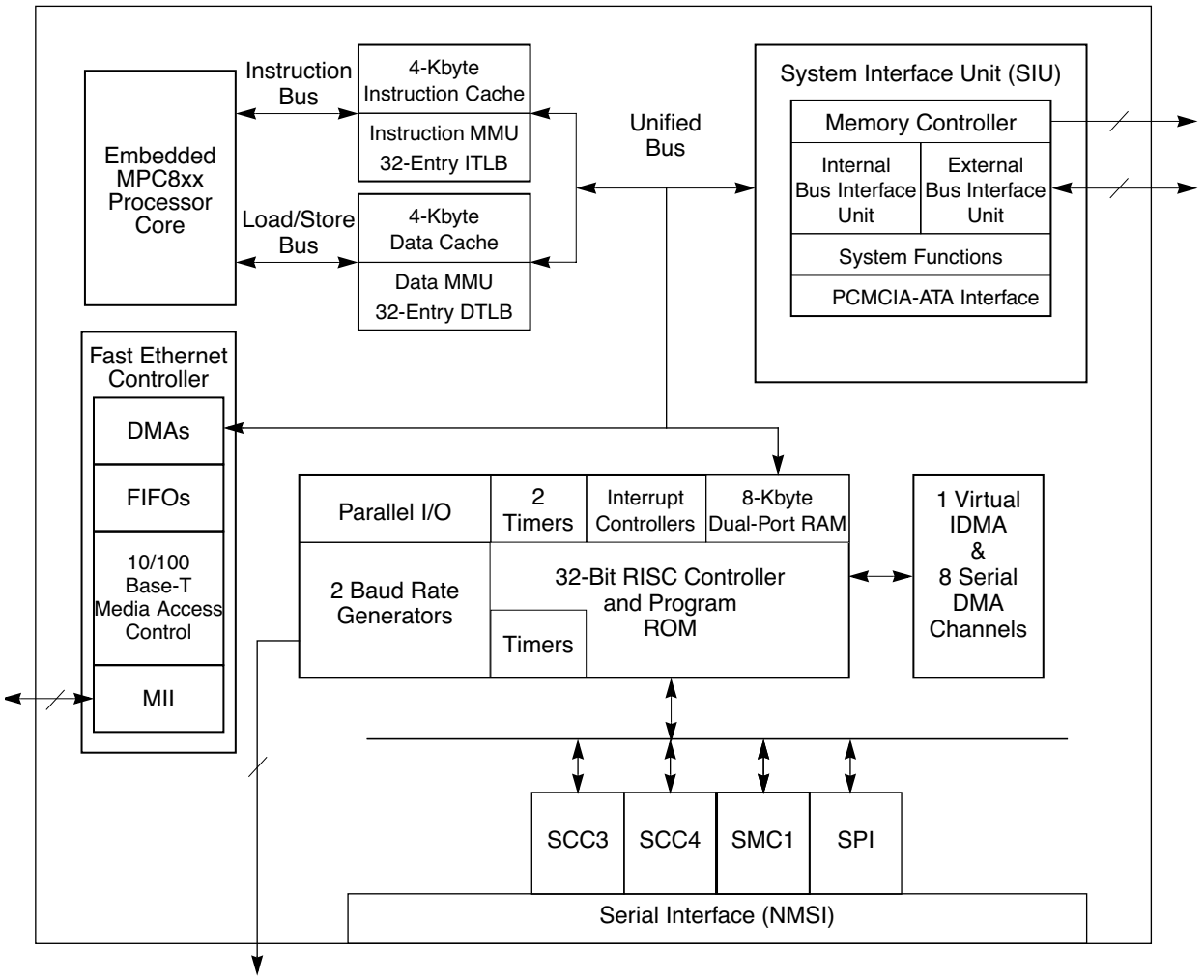


**Figure 1. MPC852T Block Diagram**

## 1.2 Embedded MPC8xx Core

The MPC852T integrates an embedded MPC8xx core with high-performance, low-power peripherals to extend the Freescale data communications family of embedded processors farther into high-end communications and networking products.

The core is compliant with the UISA (user instruction set architecture) portion of the PowerPC architecture. It has an integer unit (IU) and a load/store unit (LSU) that execute all integer and load/store operations in hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits.

The IU uses 32, 32-bit GPRs for source and target operands. Typically, it can execute one integer instruction each clock cycle. Each element in the integer block is clocked only when valid data is in the data queue and is ready for operation. This holds power consumption of the device to the absolute minimum.

The core is integrated with MMUs as well as instruction and data caches. Each MMU provides a 32-entry, fully associative instruction and data TLB, with multiple page sizes of 4, 16, 512, and 256 Kbytes and 8

Mbytes. It supports 16 virtual address spaces with 8 protection groups. Three special scratch registers support software table search and update operations.

The instruction cache is four-way, set associative with physical addressing. It allows single-cycle access on hits with no added latency for misses. It has four words per block, supporting a four-beat burst line fill using an LRU (least recently used) replacement algorithm. The cache can be locked on a per cache block basis for application-critical routines.

The data cache is two-way, set associative with physical addressing. It allows single-cycle accesses on hits with one added clock latency for misses. It has four words per cache block, supporting burst line fill using LRU replacement. The cache can be locked on a per block basis for application critical routines. The data cache can be programmed through the MMU to support copy-back or write-through. Cache-inhibit mode can be programmed per MMU page.

The debug interface provides debug capabilities without degrading operation speed. This interface supports six watchpoint pins that are used to detect software events. Four of its eight internal comparators operate on the effective address on the address bus, two operate on the effective address on the data address bus, and two operate on the data bus. The core can make =, ≠, <, and > comparisons to generate watchpoints. Each watchpoint can then generate a break point that can be configured to trigger in a programmable number of events.

## 1.3 System Interface Unit (SIU)

The SIU on the MPC852T integrates general-purpose features useful in almost any 32-bit processor system. Dynamic bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, reset control, decrementer, and timebase.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SDRAM, EDO, and other peripherals with 2-clock-cycle access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–30 wait states for each memory bank and can use address type matching to qualify each memory bank access. It provides four byte-enable signals, an output-enable signal. and a boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256 or 512 Kbytes or 1, 2, 4, 8, 16, 32, or 64 Mbytes for all port sizes. The memory depth can be 64 and 128 Kbytes for 8-bit memory or 128 and 256 Mbytes for 32-bit memory. The DRAM controller supports page-mode access for successive transfers within bursts. The MPC852T supports a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh mode, and stacking up to 7 refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

## 1.4 PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports one independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides eight memory or I/O windows where each window can be allocated to a particular socket. If only one PCMCIA port is used, the unused port may be used as general-purpose input with interrupt capability.

## 1.5 Power Management

The MPC852T supports two power management features including Normal High and Normal Low Power Modes. Full on mode leaves the MPC866 processor fully powered with all internal units operating at the full processor speed. A gear mode is determined by a clock divider, allowing the operating system to reduce the processor's operational frequency and operate in Normal Low Mode.

## 1.6 Communications Processor Module (CPM)

The MPC852T Family is the next generation MPC8xx family of devices. Like its predecessor it implements a dual-processor architecture, which provides both a high-performance, general-purpose processor for application programming use as well as a special-purpose communication processor (CPM) uniquely designed for communications applications.

The CPM contains features that, like its predecessor, allow the MPC852T to excel in communications and networking products. These features are grouped as follows:

- Communications processor (CP)
- Eight serial DMA (SDMA) controllers
- Two general-purpose timers
- One independent DMA (IDMA) controller

The CP provides the communication features of the MPC852T. Included are a RISC processor, two serial communication controllers (SCCs), one serial management controllers (SMC), a serial peripheral interface (SPI), 8-Kbytes of dual-port RAM, an interrupt controller, two independent baud rate generators, and eight serial DMA channels to support the SCCs, SMC, and SPI.

The two general-purpose timers on the CPM are identical to the timers found on all of the MPC8xx devices, and supporting the internal cascading of two timers to form a 32-bit timer.

The IDMA provides one channel of general-purpose DMA capability for each communications channel. It offers high speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

## 1.7 Document Revision History

Table 3 provides a revision history for the technical summary.

**Table 3. Revision History**

| Revision | Date | Change |
|---|---|---|
| 0 | 07/2002 | Initial document |
| 1 | 11/2002 | Took out the low power modes |
| 1.1 | 12/2002 | Added Fast Ethernet Controller to the Features |
| 1.2 | 3/2003 | Took the TSA out of the 1.6 Communication Processor Module |
| 1.3 | 4/2003 | Changed 5 Port C pins with interrupt capability to 7 Port C pins. |

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