

# Qorivva MPC5744P Evaluation Board 144LQFP Expansion Board User's Guide

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## 1 Introduction

This document describes the Qorivva MPC5744P evaluation board (EVB) expansion board for the 144LQFP (part number MPC5744P-144DC). The EVB is targeted at providing a platform for the evaluation and development of the MPC5744P automotive MCU, facilitating hardware and software development as well as debugging. Settings for switches, jumpers, LEDs, and push-buttons are shown for basic operation of the prototype version of the EVB.

This document is preliminary and is subject to change without notice.

## 2 Features

The expansion board provides the following primary features listed below:

- Standalone operation or use with the optional MPC5746MMB main board

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## Modular concept

- Socketed MPC5744P in 144-pin LQFP package
- Power options
  - Power supplied via the two interface connectors when using the EVB with the optional MPC5746MMB main board
  - Power supplied via terminal block when using the EVB in standalone configuration
  - Power supplied by the multi-output MC33907 PwrSBC power supply when using the EVB in standalone configuration
- Debug and trace
  - JTAG connector
  - Nexus parallel connector
- Clocks
  - 40 MHz crystal
  - 8 MHz crystal oscillator
  - SMA connector for external clock
- I/O connectivity
  - Access to port pins when using the EVB with the optional MPC5746MMB main board
  - Access to SCI, CAN, and LIN physical interfaces when using the EVB with the optional MPC5746MMB main board
  - On-board CAN and LIN interfaces
- Switches
  - Main power on/off
  - Power-on reset
  - Reset
- LEDs for power indication
- Test points

## 3 Modular concept

The MPC5744P-144DC is part of a modular EVB hardware system that consists of:

- A common main board that provides power and access to common communication interfaces and the MCU I/O port pins. MPC5744P-144DC is compatible with the MPC5746MMB main board.
- A package-specific expansion board to support available package types of the MPC5744P. The MPC5744P-144DC supports the 144-pin LQFP package.

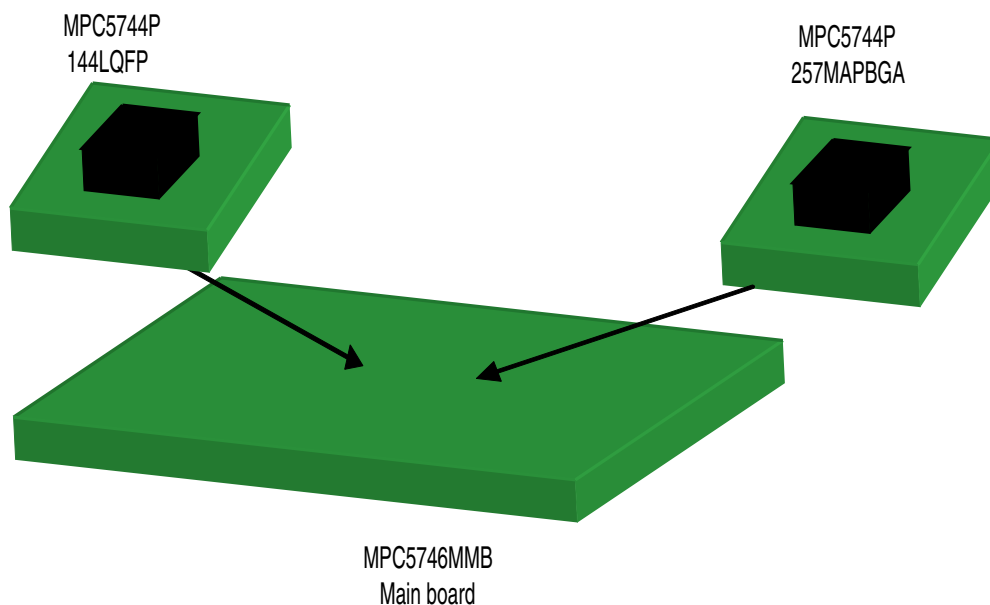


Figure 1. MPC5744P expansion board and main board system

### 3.1 Methods of operation

Power to the expansion board is supplied via three options:

1. The MPC5746MMB main board generates the 5 V/3.3 V/1.25 V supplies to the expansion board via the interface connectors.
2. In standalone configuration, external 5 V/3.3 V/1.25 V supplies are provided to the expansion board via the terminal block.
3. In standalone configuration, a single 12 V supply is input to the expansion board via the 2.1 mm power connector. The PwrSBC generates the 5 V/3.3 V high-voltage power. The NPN transistor drives the core supply using internal regulation.<sup>1</sup>

## 4 EVB configuration

This section provides information on how to configure the jumper settings on the EVB. Default settings are marked as such. [Figure 5](#) provides a top view of the EVB and shows the location of each jumper.

### 4.1 Power source

The default jumper settings are configured for using the EVB with the MPC5746MMB main board as shown in [Figure 2](#). Power is supplied from the main board to the EVB via the two interface connectors.

1. Not all expansion boards include the PwrSBC device. Check whether the PwrSBC (U3) is installed on the expansion board to determine whether standalone operation using a single 12 V supply can be used. Refer to [Figure 5](#) for the location of U3.

## EVb configuration

The EVB can also operate as a standalone device, in which power can be supplied from an external power source or from the on-board PwrSBC device.

Table 1 summarizes the switch settings for the three power options.

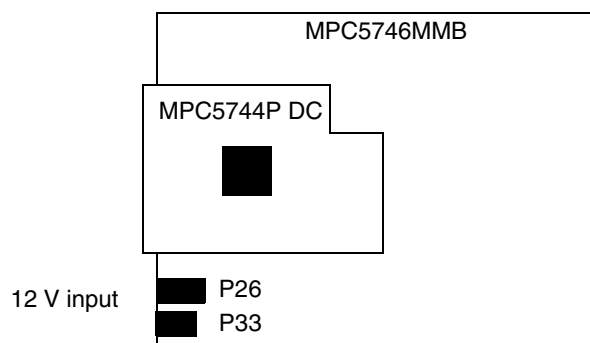
**Table 1. Switch settings — power options**

| Jumper | Setting                                                        | Description                                                                                                                                                                                                                                             |
|--------|----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| J1     | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>High voltage I/O power</b><br>VDD_HV_IO — 3.3 V from PwrSBC<br>VDD_HV_IO — 3.3 V from main board (default)<br>VDD_HV_IO — 3.3 V from external supply                                                                                                 |
| J3     | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>High voltage flash power</b><br>VDD_HV_FLAO — 3.3 V from PwrSBC<br>VDD_HV_FLAO — 3.3 V from main board (default)<br>VDD_HV_FLAO — 3.3 V from external supply                                                                                         |
| J19    | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>High voltage oscillator power</b><br>VDD_HV_OSC0 — 3.3 V from PwrSBC<br>VDD_HV_OSC0 — 3.3 V from main board (default)<br>VDD_HV_OSC0 — 3.3 V from external supply                                                                                    |
| J20    | Choose one:<br>2–4 ON<br>3–4 ON<br>7–8 ON<br>6–8 ON<br>8–10 ON | <b>High voltage ADC0/2 reference</b><br>VDD_HV_ADR0 — from PwrSBC, see J24<br>VDD_HV_ADR0 — 3.3 V from main board (default)<br>VDD_HV_ADR0 — 5 V from main board<br>VDD_HV_ADR0 — 3.3 V from external supply<br>VDD_HV_ADR0 — 5 V from external supply  |
| J21    | Choose one:<br>2–4 ON<br>3–4 ON<br>7–8 ON<br>6–8 ON<br>8–10 ON | <b>High voltage ADC1/3 reference</b><br>VDD_HV_ADR1 — from PwrSBC (see J24)<br>VDD_HV_ADR1 — 3.3 V from main board (default)<br>VDD_HV_ADR1 — 5 V from main board<br>VDD_HV_ADR1 — 3.3 V from external supply<br>VDD_HV_ADR1 — 5 V from external supply |
| J24    | Choose one:<br>2–4 ON<br>1–3 ON                                | <b>5 V/3.3 V select for ADC reference</b><br>VDD_HV_ADR0 and VDD_HV_ADR1 — 3.3 V from PwrSBC (default)<br>VDD_HV_ADR0 and VDD_HV_ADR1 — 5 V from PwrSBC                                                                                                 |
| J22    | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>High voltage ADC power</b><br>VDD_HV_ADV0/1 — 3.3 V from PwrSBC<br>VDD_HV_ADV0/1 — 3.3 V from main board (default)<br>VDD_HV_ADV0/1 — 3.3 V from external supply                                                                                     |
| J23    | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>High voltage PMU supply</b><br>VDD_HV_PMU — 3.3 V from PwrSBC<br>VDD_HV_PMU — 3.3 V from main board (default)<br>VDD_HV_PMU — 3.3 V from external supply                                                                                             |
| J16    | Choose one:<br>2–4 ON<br>3–4 ON<br>4–6 ON                      | <b>Low voltage supply</b><br>VDD_LV_CORE — use NPN transistor, internal regulation<br>VDD_LV_CORE — 1.25 V from main board, external regulation (default)<br>VDD_LV_CORE — 1.25 V from external supply, external regulation                             |

### 4.1.1 Option 1: Power from the MPC5746MMB main board

The default configuration for the EVB power source is the main board.

In this configuration, the EVB is connected to the main board. The main board must be supplied with a 12 V input via the 2.1 mm barrel connector (P26) or the terminal block (P33). Voltage regulators on the main board provide 5 V, 3.3 V, and 1.25 V to the MCU via the high-density expansion connectors. The MCU core supply can be externally regulated or internally regulated using the NPN transistor.



**Figure 2. Power from the main board**

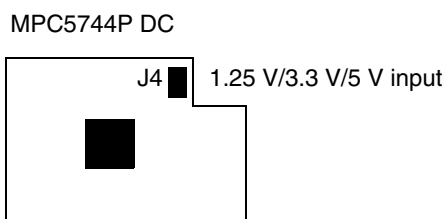
Table 2 shows the switch settings when power is sourced from the main board.

**Table 2. Switch settings — power from main board**

| Jumper | Setting                         | Description                                                                                                                  |
|--------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| J1     | 3–4 ON                          | VDD_HV_IO — 3.3 V from main board (default)                                                                                  |
| J3     | 3–4 ON                          | VDD_HV_FLA0 — 3.3 V from main board (default)                                                                                |
| J19    | 3–4 ON                          | VDD_HV_OSC0 — 3.3 V from main board (default)                                                                                |
| J20    | Choose one:<br>3–4 ON<br>7–8 ON | VDD_HV_ADR0 — 3.3 V from main board (default)<br>VDD_HV_ADR0 — 5 V from main board                                           |
| J21    | Choose one:<br>3–4 ON<br>7–8 ON | VDD_HV_ADR1 — 3.3 V from main board (default)<br>VDD_HV_ADR1 — 5 V from main board                                           |
| J22    | 3–4 ON                          | VDD_HV_ADV0/1 — 3.3 V from main board (default)                                                                              |
| J23    | 3–4 ON                          | VDD_HV_PMU— 3.3 V from main board (default)                                                                                  |
| J16    | Choose one:<br>2–4 ON<br>3–4 ON | VDD_LV_CORE — use NPN transistor, internal regulation<br>VDD_LV_CORE — 1.25 V from main board, external regulation (default) |

## 4.1.2 Option 2: Power from external supply

This configuration allows the EVB to operate in standalone configuration using external power supplies, as shown in [Figure 3](#). Power to the EVB is supplied via the terminal block J4 as shown in [Table 4](#). The core supply can be externally regulated or internally regulated using the NPN transistor.



**Figure 3. Power from external supplies**

[Table 3](#) shows the switch settings when power is sourced externally via the terminal block.

**Table 3. Switch settings — power from external supply**

| Jumper | Setting                          | Description                                                                                                             |
|--------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------|
| J1     | 4–6 ON                           | VDD_HV_IO — 3.3 V from external supply                                                                                  |
| J3     | 4–6 ON                           | VDD_HV_FLA0 — 3.3 V from external supply                                                                                |
| J19    | 4–6 ON                           | VDD_HV_OSC0 — 3.3 V from external supply                                                                                |
| J20    | Choose one:<br>6–8 ON<br>8–10 ON | VDD_HV_ADR0 — 3.3 V from external supply<br>VDD_HV_ADR0 — 5 V from external supply                                      |
| J21    | Choose one:<br>6–8 ON<br>8–10 ON | VDD_HV_ADR1 — 3.3 V from external supply<br>VDD_HV_ADR1 — 5 V from external supply                                      |
| J22    | 4–6 ON                           | VDD_HV_ADV0/1 — 3.3 V from external supply                                                                              |
| J23    | 4–6 ON                           | VDD_HV_PMU — 3.3 V from external supply                                                                                 |
| J16    | Choose one:<br>2–4 ON<br>4–6 ON  | VDD_LV_CORE — use NPN transistor, internal regulation<br>VDD_LV_CORE — 1.25 V from external supply, external regulation |

**Table 4. External power input**

| J4    | Description |
|-------|-------------|
| Pin 1 | 1.25 V      |
| Pin 2 | 3.3 V       |
| Pin 3 | 5 V         |
| Pin 4 | GND         |

### 4.1.3 Option 3: Power from PwrSBC

This configuration allows the EVB to operate standalone, using the MC33907 PwrSBC device on the EVB as shown in Figure 4. The PwrSBC is a multi-output power supply with built-in CAN and LIN transceivers. It generates the 5 V and 3.3 V power to the MCU. In this configuration, the core supply is regulated internally using the NPN transistor. Power to the EVB is supplied via the 2.1 mm power connector (P2).

Table 5 shows the switch settings when power is sourced from the PwrSBC.

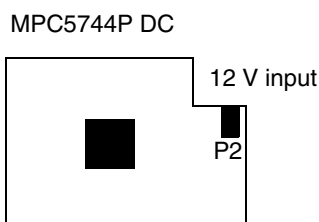


Figure 4. Power from the PwrSBC

Table 5. Switch settings — power from PwrSBC

| Jumper | Setting                         | Description                                                                                                |
|--------|---------------------------------|------------------------------------------------------------------------------------------------------------|
| J1     | 2–4 ON                          | VDD_HV_IO — 3.3 V from PwrSBC                                                                              |
| J3     | 2–4 ON                          | VDD_HV_FLA0 — 3.3 V from PwrSBC                                                                            |
| J19    | 2–4 ON                          | VDD_HV_OSC0 — 3.3 V from PwrSBC                                                                            |
| J20    | 2–4 ON                          | VDD_HV_ADR0 — from PwrSBC, see J24                                                                         |
| J21    | 2–4 ON                          | VDD_HV_ADR1 — from PwrSBC, see J24                                                                         |
| J24    | Choose one:<br>2–4 ON<br>1–3 ON | VDD_HV_ADR0 and VDD_HV_ADR1 — 3.3 V from PwrSBC (default)<br>VDD_HV_ADR0 and VDD_HV_ADR1 — 5 V from PwrSBC |
| J22    | Choose one:<br>2–4 ON           | VDD_HV_ADV0/1 — 3.3 V from PwrSBC                                                                          |
| J23    | Choose one:<br>2–4 ON           | VDD_HV_PMU — 3.3 V from PwrSBC                                                                             |
| J16    | 2–4 ON                          | VDD_LV_CORE — use NPN transistor, internal regulation                                                      |

## 4.2 VPP\_TEST

The VPP\_TEST switch (J6) must be pulled low to allow Debug mode to be entered.

**Table 6. Switch settings —VPP\_TEST**

| J6                              | Description                                       |
|---------------------------------|---------------------------------------------------|
| Choose one:<br>1–2 ON<br>2–3 ON | Pull VPP_TEST high<br>Pull VPP_TEST low (default) |

## 4.3 Boot configuration

Table 7 shows the J7 switch settings to configure the boot configuration. When booting from UART or CAN, connect the expansion board to the main board and use the interface connectors described below.

**Table 7. Switch settings — Boot configuration**

| J7                           | Description                   |                                                                                                  |
|------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------|
| 1–2 ON<br>3–4 ON<br>5–6 ON   | FAB:ABS2:ABS1 = 000 (default) | Normal boot                                                                                      |
| 1–2 OFF<br>3–4 ON<br>5–6 ON  | FAB:ABS2:ABS1 = 100           | Boot from UART<br>Connect expansion board to main board.<br>Use main board RS-232 connector J19. |
| 1–2 OFF<br>3–4 ON<br>5–6 OFF | FAB:ABS2:ABS1 = 10            | Boot from CAN<br>Connect expansion board to main board.<br>Use main board CAN connector J5.      |

## 4.4 Clocks

The EVB provides the following options for clock sources:

- Default: 40 MHz crystal (Y200)
- 8 MHz crystal oscillator (Y201)
- External clock input via SMA connector (J11)

The default clock source is the 40 MHz crystal. Changing the clock source to the 8 MHz crystal oscillator or the external clock input requires removing and replacing resistors, as shown in Table 8.

Figure 8 shows the bottom-side view of the EVB and the location of each of the relevant resistors.

**Table 8. Clock source configuration**

| Clock Source     | Configuration                                                                                                                                   |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 40 MHz crystal   | 0 $\Omega$ resistors R234 and R235 are installed (default).                                                                                     |
| 8 MHz oscillator | Remove 0 $\Omega$ resistors R234 and R235.<br>Install 0 $\Omega$ resistor to R238 and R233.<br>Remove jumper J12 pins 1–2 to enable the output. |



**Table 8. Clock source configuration (continued)**

| Clock Source   | Configuration                                                                                                                         |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------|
| External clock | Remove 0 $\Omega$ resistors R234 and R235.<br>Install 0 $\Omega$ resistors to R239 and R233.<br>Install 50 $\Omega$ resistor to R236. |

Table 9 shows the configuration to enable the 8 MHz oscillator.

**Table 9. 8 MHz oscillator output enable/disable**

| J12     | Description                                |
|---------|--------------------------------------------|
| 1–2 ON  | 8 MHz oscillator output disabled (default) |
| 1–2 OFF | 8 MHz oscillator output enabled            |

## 4.5 I/O connectivity

Some of the MCU's I/Os are routed to the main board and the PwrSBC.

### 4.5.1 DSPI0 connectivity

Jumper J18 allows the DSPI0 signals to be routed to the main board or to the PwrSBC.

When the expansion board is powered by the main board, J18 should be configured to connect the DSPI0 signals to the main board. The DSPI0 signals can be accessed on the main board from the port pin connectors as shown in Table 25.

When the expansion board is powered by the PwrSBC, J18 should be configured to connect the DSPI0 signals to the PwrSBC to allow communication between the MCU and the PwrSBC via SPI.

Table 10 shows the J18 switch settings.

**Table 10. Switch settings — DSPI and ADC0 connectivity**

| J18                                 | Description                                                                                                              |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| Choose one:<br>1–2 ON<br>2–6 ON     | <b>DSPI0 SOUT connectivity</b><br>Connect DSPI0 SOUT (PC6) to PwrSBC<br>Connect DSPI0 SOUT (PC6) to main board (default) |
| Choose one:<br>4–5 ON<br>5–3 ON     | <b>DSPI0 SIN connectivity</b><br>Connect DSPI0 SIN (PC7) to PwrSBC<br>Connect DSPI0 SIN (PC7) to main board (default)    |
| Choose one:<br>7–8 ON<br>8–9 ON     | <b>DSPI0 SCK connectivity</b><br>Connect DSPI0 SCK (PC5) to PwrSBC<br>Connect DSPI0 SCK (PC5) to main board (default)    |
| Choose one:<br>10–11 ON<br>11–12 ON | <b>DSPI0 CS0 connectivity</b><br>Connect DSPI0 CS0 (PC4) to PwrSBC<br>Connect DSPI0 CS0 (PC4) to main board (default)    |

## 4.5.2 FlexCAN\_0 connectivity

Jumper J17 allows the FlexCAN\_0 TXD/RXD (PB0/PB1) signals to be routed to the main board or to the PwrSBC.

When the EVB is powered by the main board, J17 should be configured to connect to the CAN interface of the main board. The FlexCAN\_0 signals are connected to the main board CAN transceiver that is accessed via the J5 DB9 connector on the main board. The FlexCAN\_0 signals can be accessed on the main board from the port pin connectors as shown in [Table 25](#).

When the EVB is powered by the PwrSBC, J17 should be configured to connect the FlexCAN\_0 TXD/RXD (PB0/PB1) signals to the PwrSBC as shown in [Table 11](#). The PwrSBC's built-in CAN transceiver connects to the J8 DB9 interface connector on the expansion board.

[Table 11](#) shows the switch settings for J17. Note the jumper settings for J17 require diagonal connections, in other words, pins 1–5 instead of pins 1–2.

**Table 11. Switch settings — CAN0 and LIN0 connectivity**

| J17                    | Description                                                                                                                   |
|------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| Choose one:<br>2–4 ON  | <b>FlexCAN0_TXD Connectivity</b><br>Connect FlexCAN_0 TXD (PB0) to PwrSBC. Use J8 DB9 connector on the expansion board.       |
| 2–6 ON                 | Connect FlexCAN_0 TXD (PB0) to main board. Use J5 DB9 connector on main board. (default)                                      |
| Choose one:<br>5–1 ON  | <b>FlexCAN0_RXD Connectivity</b><br>Connect FlexCAN_0 RXD (PB1) to PwrSBC. Use J8 DB9 connector on the expansion board.       |
| 5–3 ON                 | Connect FlexCAN_0 RXD (PB1) to main board. Use J5 DB9 connector on main board. (default)                                      |
| Choose one:<br>8–10 ON | <b>LINFlexD_0 TXD Connectivity</b><br>Connect LINFlexD_0 TXD (PB2) to PwrSBC. Use J15 Molex connector on the expansion board. |
| 8–12 ON                | Connect LINFlexD_0 TXD (PB2) to main board. Use J19 DB9 connector on the main board. (default)                                |
| Choose one:<br>11–7 ON | <b>LINFlexD_0 RXD Connectivity</b><br>Connect LINFlexD_0 RXD (PB3) to PwrSBC. Use J15 Molex connector on the expansion board. |
| 11–9 ON                | Connect LINFlexD_0 RXD (PB3) to main board. Use J19 DB9 connector on the main board. (default)                                |

## 4.5.3 LINFlexD\_0 connectivity

Jumper J17 allows the LINFlexD\_0 TXD/RXD (PB2/PB3) signals to be routed to the main board or the PwrSBC.

When the EVB is powered by the main board, J17 should be configured to connect to the LIN interface on the main board. The LINFlexD\_0 signals are connected to the main board eSCI/RS-232 transceiver that is accessed via the J19 DB9 connector on the main board. The LINFlexD\_0 signals can be accessed on the main board from the port pin connectors as shown in [Table 25](#).

When the EVB is powered by the PwrSBC, J17 should be configured to connect the LINFlexD\_0 signals to the PwrSBC as shown in [Table 11](#). The PwrSBC's built-in LIN transceiver connects to the J16 Molex connector on the expansion board.

[Table 11](#) shows the switch settings for J17. Note the jumper settings for J17 require diagonal connections, in other words, pins 1–5 instead of pins 1–2.

#### 4.5.4 FlexCAN\_1 connectivity

The FlexCAN\_1 TXD/RXD (PA14/PA15) signals are routed to the main board via the interface connectors. The FlexCAN\_1 signals are connected to the main board CAN transceiver that is accessed via the J6 DB9 connector on the main board.

#### 4.5.5 LINFlexD\_1 connectivity

The LINFlexD\_1 TXD/RXD (PF14/PF15) signals are routed to the main board via the interface connectors. The LINFlexD\_1 signals are connected to the main board LIN transceiver that is accessed via the J4 Molex connector on the main board. The LINFlexD\_1 signals can be accessed on the main board from the port pin connectors as shown in [Table 25](#).

#### 4.5.6 FlexRay\_A connectivity

The FlexRay\_A TX/RX/TXEN (PD3/PD2/PD4) signals are routed to the main board via the interface connectors. The FlexRay\_A signals are connected to the main board FlexRay transceiver that is accessed via the J2 DB9 connector on the main board.

#### 4.5.7 FlexRay\_B connectivity

The FlexRay\_B TX/RX/TXEN (PD0/PD1/PC15) signals are routed to the main board via the interface connectors. The FlexRay\_B signals are connected to the main board FlexRay transceiver that is accessed via the J2 DB9 connector on the main board.

### 4.6 Main board I/O power

Jumper J13 on the EVB selects between 3.3 V and 5 V for power to the main board transceivers. The main board transceivers are powered by VDD\_HV\_IO\_MAIN. The default power to VDD\_HV\_IO\_MAIN is 3.3 V.

**Table 12. Switch settings — main board VDD\_HV\_IO\_MAIN**

| J13                             | Description                                                |
|---------------------------------|------------------------------------------------------------|
| Choose one:<br>1–2 ON<br>2–3 ON | VDD_HV_IO_MAIN is 5 V<br>VDD_HV_IO_MAIN is 3.3 V (default) |

## 4.7 PwrSBC settings

This section includes settings related to the PwrSBC. Jumper settings in this section have no effect when the EVB is powered by the main board or by external supplies. These settings only apply when the EVB is powered by the PwrSBC.

### 4.7.1 CAN termination

When the CAN interface on the expansion board is used, jumper J9 provides termination resistors to the CANH and CANL pins of the PwrSBC transceiver.

[Table 13](#) shows the J9 switch settings to enable or disable the PwrSBC CAN termination resistors.

**Table 13. Switch settings — PwrSBC CAN termination resistors**

| J9                | Description                                                                                   |
|-------------------|-----------------------------------------------------------------------------------------------|
| 1–3 ON<br>1–3 OFF | Enable PwrSBC CANL termination resistor (default)<br>Disable PwrSBC CANL termination resistor |
| 2–4 ON<br>2–4 OFF | Enable PwrSBC CANH termination resistor (default)<br>Disable PwrSBC CANH termination resistor |

### 4.7.2 LIN master/slave configuration

[Table 14](#) shows the J15 switch settings to configure the PwrSBC LIN interface in master or slave configuration.

**Table 14. Switch settings — PwrSBC LIN master/slave configuration**

| J15               | Description                                                                             |
|-------------------|-----------------------------------------------------------------------------------------|
| 1–2 ON<br>1–2 OFF | PwrSBC LIN is in master configuration (default)<br>PwrSBC LIN is in slave configuration |

### 4.7.3 NMI\_B and RESET\_B

Jumper J2 allows the MCU's NMI\_B and RESET\_B signals to be routed to the PwrSBC. [Table 15](#) shows the J2 switch settings.

**Table 15. Switch settings — NMI\_B and RESET\_B connectivity**

| J2                | Description                                                               |
|-------------------|---------------------------------------------------------------------------|
| 1–2 ON<br>1–2 OFF | Connect NMI_B to PwrSBC.<br>Do not connect NMI_B to PwrSBC (default).     |
| 3–4 ON<br>3–4 OFF | Connect RESET_B to PwrSBC.<br>Do not connect RESET_B to PwrSBC (default). |

#### 4.7.4 PwrSBC IO\_0:5

Table 16 shows the J10 jumper which allows access to the PwrSBC IO\_x pins. The IO\_x pins are inputs to the PwrSBC for monitoring various signals.

J10 also provides connection between the FCCU\_F[0:1] and PwrSBC IO\_2:3 pins to allow the PwrSBC to monitor the status of the MCU's FCCU error output pins.

**Table 16. Switch settings — PwrSBC IO\_0:5**

| J10               | Description                                                                         |
|-------------------|-------------------------------------------------------------------------------------|
| 2                 | PwrSBC IO_0                                                                         |
| 4                 | PwrSBC IO_1                                                                         |
| 6                 | PwrSBC IO_2                                                                         |
| 8                 | PwrSBC IO_3                                                                         |
| 10                | PwrSBC IO_4                                                                         |
| 12                | PwrSBC IO_5                                                                         |
| 5–6 ON<br>5–6 OFF | Connect FCCU_F0 to PwrSBC IO_2.<br>Do not connect FCCU_F0 to PwrSBC IO_2 (default). |
| 7–8 ON<br>7–8 OFF | Connect FCCU_F1 to PwrSBC IO_3.<br>Do not connect FCCU_F1 to PwrSBC IO_3 (default). |

## 5 Reset switches

The push-button switches (SW1 and SW2) provide external power-on-reset and reset to the MCU.

Table 17 shows the reset switches.

**Table 17. Reset switches**

| Switches | Description                           |
|----------|---------------------------------------|
| SW1      | EXT_POR_B for external power-on reset |
| SW2      | RESET_B for functional reset          |

## 6 Connectors

Table 18 lists the connectors available on the EVB.

**Table 18. Connectors**

| Connector | Description                                                            |
|-----------|------------------------------------------------------------------------|
| P1        | 38-pin Nexus parallel trace                                            |
| P2        | 2.1 mm barrel connector for standalone configuration using PwrSBC      |
| J4        | 4-pin terminal block for standalone configuration using external power |
| J5        | 14-pin JTAG                                                            |

**Table 18. Connectors (continued)**

| Connector | Description                  |
|-----------|------------------------------|
| J8        | DB-9 PwrSBC CAN interface    |
| J11       | SMA external clock           |
| J14       | Molex PwrSBC LIN interface   |
| J200      | 240-pin main board interface |
| J201      | 240-pin main board interface |

## 6.1 JTAG connector

The JTAG port is accessed via the 14-pin BERG connector (J5).

**Table 19. JTAG connector**

| Pin | Signal    | Pin | Signal    |
|-----|-----------|-----|-----------|
| 1   | TDI       | 2   | GND       |
| 3   | TDO       | 4   | GND       |
| 5   | TCK       | 6   | GND       |
| 7   | EVTI      | 8   | EXT_POR_B |
| 9   | RESET_B   | 10  | TMS       |
| 11  | VDD_HV_IO | 12  | GND       |
| 13  | RDY_B     | 14  | JCOMP     |

## 6.2 Nexus parallel trace connector

Nexus parallel trace is supported via the 38-pin MICTOR connector (P1).

**Table 20. Nexus parallel trace connector**

| Pin | Signal  | Pin | Signal    |
|-----|---------|-----|-----------|
| 1   | NC      | 2   | NC        |
| 3   | NC      | 4   | NC        |
| 5   | NC      | 6   | NC        |
| 7   | FAB     | 8   | NC        |
| 9   | RESET_B | 10  | EVTI      |
| 11  | TDO     | 12  | VDD_HV_IO |
| 13  | NC      | 14  | RDY_B     |
| 15  | TCK     | 16  | NC        |
| 17  | TMS     | 18  | NC        |
| 19  | TDI     | 20  | NC        |

Table 20. Nexus parallel trace connector (continued)

| Pin | Signal | Pin | Signal  |
|-----|--------|-----|---------|
| 21  | JCOMP  | 22  | NC      |
| 23  | NC     | 24  | MDO3    |
| 25  | NC     | 26  | MDO2    |
| 27  | NC     | 28  | MDO1    |
| 29  | NC     | 30  | MDO0    |
| 31  | 12V    | 32  | EVTO_B  |
| 33  | 12V    | 34  | MCKO    |
| 35  | NC     | 36  | MSEO1_B |
| 37  | NC     | 38  | MSEO0_B |

## 6.3 Main board interface

The two high-density interface connectors on the expansion board (J201 and J200) card allow connection to the main board's matching connectors (J56 and J43).

Table 21. Main board interface connector J201

| J201A connector |            |     |            | J201B |         |     |        |
|-----------------|------------|-----|------------|-------|---------|-----|--------|
| Pin             | Signal     | Pin | Signal     | Pin   | Signal  | Pin | Signal |
| 1               | 1.25 V     | 2   | 1.25 V     | 121   | 5 V     | 122 | 5 V    |
| 3               | 1.25 V     | 4   | 1.25 V     | 123   | 5 V     | 124 | 5 V    |
| 5               | PA0        | 6   | PA1        | 125   | NC      | 126 | NC     |
| 7               | PA2        | 8   | PA3        | 127   | NC      | 128 | NC     |
| 9               | PA4        | 10  | PA5        | 129   | NC      | 130 | NC     |
| 11              | PA6        | 12  | PA7        | 131   | NC      | 132 | NC     |
| 13              | PA8        | 14  | PA9        | 133   | NC      | 134 | NC     |
| 15              | PA10       | 16  | PA11       | 135   | NC      | 136 | NC     |
| 17              | PA12       | 18  | PA13       | 137   | NC      | 138 | NC     |
| 19              | NC         | 20  | NC         | 139   | NC      | 140 | NC     |
| 21              | NC         | 22  | NC         | 141   | RESET_B | 142 | NC     |
| 23              | NC         | 24  | NC         | 143   | NC      | 144 | NC     |
| 25              | PC0        | 26  | PC1        | 145   | NC      | 146 | NC     |
| 27              | PC2        | 28  | NC         | 147   | NC      | 148 | NC     |
| 29              | PC4        | 30  | MB_PTC5    | 149   | NC      | 150 | NC     |
| 31              | PC6        | 32  | MB_PTC7    | 151   | NC      | 152 | NC     |
| 33              | MB_CAN_RXD | 34  | MB_CAN_TXD | 153   | NC      | 154 | NC     |

Table 21. Main board interface connector J201 (continued)

| J201A connector |        |     |        | J201B |        |     |        |
|-----------------|--------|-----|--------|-------|--------|-----|--------|
| Pin             | Signal | Pin | Signal | Pin   | Signal | Pin | Signal |
| 35              | PC10   | 36  | PC11   | 155   | NC     | 156 | NC     |
| 37              | PC12   | 38  | PC13   | 157   | NC     | 158 | NC     |
| 39              | PC14   | 40  | NC     | 159   | NC     | 160 | NC     |
| 41              | 3.3 V  | 42  | 3.3 V  | 161   | 1.25 V | 162 | 1.25 V |
| 43              | 3.3 V  | 44  | 3.3 V  | 163   | 1.25 V | 164 | 1.25 V |
| 45              | NC     | 46  | NC     | 165   | NC     | 166 | NC     |
| 47              | NC     | 48  | NC     | 167   | NC     | 168 | NC     |
| 49              | NC     | 50  | PA14   | 169   | NC     | 170 | NC     |
| 51              | PF15   | 52  | PF14   | 171   | NC     | 172 | NC     |
| 53              | NC     | 54  | PG8    | 173   | NC     | 174 | NC     |
| 55              | PG9    | 56  | PG10   | 175   | NC     | 176 | NC     |
| 57              | PG11   | 58  | NC     | 177   | NC     | 178 | NC     |
| 59              | NC     | 60  | NC     | 179   | NC     | 180 | NC     |
| 61              | 1.25 V | 62  | 1.25 V | 181   | 5 V    | 182 | 5 V    |
| 63              | 1.25 V | 64  | 1.25 V | 183   | 5 V    | 184 | 5 V    |
| 65              | NC     | 66  | NC     | 185   | NC     | 186 | NC     |
| 67              | PG2    | 68  | PG3    | 187   | NC     | 188 | NC     |
| 69              | PG4    | 70  | PG5    | 189   | NC     | 190 | NC     |
| 71              | PG6    | 72  | PG7    | 191   | NC     | 192 | NC     |
| 73              | NC     | 74  | NC     | 193   | NC     | 194 | NC     |
| 75              | NC     | 76  | NC     | 195   | NC     | 196 | NC     |
| 77              | NC     | 78  | NC     | 197   | NC     | 198 | NC     |
| 79              | PA15   | 80  | NC     | 199   | NC     | 200 | NC     |
| 81              | NC     | 82  | NC     | 201   | 3.3 V  | 202 | 3.3 V  |
| 83              | NC     | 84  | NC     | 203   | 3.3 V  | 204 | 3.3 V  |
| 85              | NC     | 86  | NC     | 205   | NC     | 206 | NC     |
| 87              | NC     | 88  | NC     | 207   | NC     | 208 | NC     |
| 89              | NC     | 90  | NC     | 209   | NC     | 210 | NC     |
| 91              | NC     | 92  | NC     | 211   | NC     | 212 | NC     |
| 93              | NC     | 94  | NC     | 213   | NC     | 214 | NC     |
| 95              | NC     | 96  | NC     | 215   | NC     | 216 | NC     |
| 97              | NC     | 98  | NC     | 217   | NC     | 218 | NC     |
| 99              | NC     | 100 | NC     | 219   | NC     | 220 | NC     |



Table 21. Main board interface connector J201 (continued)

| J201A connector |        |     |        | J201B |                |     |                |
|-----------------|--------|-----|--------|-------|----------------|-----|----------------|
| Pin             | Signal | Pin | Signal | Pin   | Signal         | Pin | Signal         |
| 101             | NC     | 102 | NC     | 221   | VDD_HV_IO_MAIN | 222 | VDD_HV_IO_MAIN |
| 103             | NC     | 104 | NC     | 223   | VDD_HV_IO_MAIN | 224 | VDD_HV_IO_MAIN |
| 105             | PE0    | 106 | NC     | 225   | NC             | 226 | NC             |
| 107             | PE2    | 108 | NC     | 227   | NC             | 228 | NC             |
| 109             | PE4    | 110 | PE5    | 229   | NC             | 230 | NC             |
| 111             | PE6    | 112 | PE7    | 231   | NC             | 232 | NC             |
| 113             | NC     | 114 | PE9    | 233   | NC             | 234 | NC             |
| 115             | PE10   | 116 | PE11   | 235   | NC             | 236 | NC             |
| 117             | PE12   | 118 | PE13   | 237   | NC             | 238 | NC             |
| 119             | PE14   | 120 | PE15   | 239   | NC             | 240 | NC             |

Table 22. Main board interface connector J200

| J201A connector |        |     |        | J201B |        |     |        |
|-----------------|--------|-----|--------|-------|--------|-----|--------|
| Pin             | Signal | Pin | Signal | Pin   | Signal | Pin | Signal |
| 120             | 5 V    | 119 | 5 V    | 240   | 1.25 V | 239 | 1.25 V |
| 118             | 5 V    | 117 | 5 V    | 238   | 1.25 V | 237 | 1.25 V |
| 116             | NC     | 115 | NC     | 236   | PB7    | 235 | PB8    |
| 114             | NC     | 113 | NC     | 234   | PB13   | 233 | PB14   |
| 112             | NC     | 111 | NC     | 232   | PB9    | 231 | PB10   |
| 110             | NC     | 109 | NC     | 230   | PB5    | 229 | PB4    |
| 108             | NC     | 107 | NC     | 228   | PB11   | 227 | PB6    |
| 106             | NC     | 105 | NC     | 226   | PB15   | 225 | PB12   |
| 104             | NC     | 103 | NC     | 224   | NC     | 223 | NC     |
| 102             | NC     | 101 | NC     | 222   | NC     | 221 | NC     |
| 100             | NC     | 99  | NC     | 220   | 5 V    | 219 | 5 V    |
| 98              | NC     | 97  | NC     | 218   | 5 V    | 217 | 5 V    |
| 96              | NC     | 95  | NC     | 216   | NC     | 215 | NC     |
| 94              | NC     | 93  | NC     | 214   | NC     | 213 | NC     |
| 92              | NC     | 91  | NC     | 212   | NC     | 211 | PD5    |
| 90              | NC     | 89  | NC     | 210   | PD6    | 209 | PD7    |
| 88              | NC     | 87  | NC     | 208   | PD8    | 207 | PD9    |
| 86              | NC     | 85  | NC     | 206   | PD10   | 205 | PD11   |

Table 22. Main board interface connector J200 (continued)

| J201A connector |                |     |                | J201B |            |     |            |
|-----------------|----------------|-----|----------------|-------|------------|-----|------------|
| Pin             | Signal         | Pin | Signal         | Pin   | Signal     | Pin | Signal     |
| 84              | NC             | 83  | NC             | 204   | PD12       | 203 | NC         |
| 82              | NC             | 81  | NC             | 202   | MB_LIN_TXD | 201 | MB_LIN_RXD |
| 80              | 1.25 V         | 79  | 1.25 V         | 200   | 3.3 V      | 199 | 3.3 V      |
| 78              | 1.25 V         | 77  | 1.25 V         | 198   | 3.3 V      | 197 | 3.3 V      |
| 76              | NC             | 75  | NC             | 196   | PF0        | 195 | NC         |
| 74              | NC             | 73  | NC             | 194   | NC         | 193 | PF3        |
| 72              | NC             | 71  | NC             | 192   | PF4        | 191 | PF5        |
| 70              | NC             | 69  | NC             | 190   | PF6        | 189 | PF7        |
| 68              | NC             | 67  | NC             | 188   | PF8        | 187 | PF9        |
| 66              | NC             | 65  | NC             | 186   | PF10       | 185 | PF11       |
| 64              | NC             | 63  | NC             | 184   | PF12       | 183 | PF13       |
| 62              | NC             | 61  | NC             | 182   | NC         | 181 | NC         |
| 60              | NC             | 59  | NC             | 180   | 1.25       | 179 | 1.25       |
| 58              | NC             | 57  | NC             | 178   | 1.25       | 177 | 1.25       |
| 56              | NC             | 55  | NC             | 176   | PD14       | 175 | NC         |
| 54              | NC             | 53  | NC             | 174   | NC         | 173 | PD3        |
| 52              | NC             | 51  | NC             | 172   | PD4        | 171 | NC         |
| 50              | NC             | 49  | NC             | 170   | NC         | 169 | PD0        |
| 48              | NC             | 47  | NC             | 168   | PC15       | 167 | PD1        |
| 46              | NC             | 45  | NC             | 166   | PD2        | 165 | NC         |
| 44              | NC             | 43  | NC             | 164   | NC         | 163 | NC         |
| 42              | NC             | 41  | NC             | 162   | NC         | 161 | NC         |
| 40              | 3.3 V          | 39  | 3.3 V          | 160   | 3.3 V      | 159 | 3.3 V      |
| 38              | 3.3 V          | 37  | 3.3 V          | 158   | 3.3 V      | 157 | 3.3 V      |
| 36              | NC             | 35  | NC             | 156   | NC         | 155 | NC         |
| 34              | NC             | 33  | NC             | 154   | NC         | 153 | NC         |
| 32              | NC             | 31  | NC             | 152   | NC         | 151 | NC         |
| 30              | NC             | 29  | NC             | 150   | NC         | 149 | NC         |
| 28              | NC             | 27  | NC             | 148   | PJ8        | 147 | PJ9        |
| 26              | NC             | 25  | NC             | 146   | NC         | 145 | NC         |
| 24              | NC             | 23  | NC             | 144   | NC         | 143 | NC         |
| 22              | NC             | 21  | NC             | 142   | NC         | 141 | NC         |
| 20              | VDD_HV_IO_MAIN | 19  | VDD_HV_IO_MAIN | 140   | NC         | 139 | NC         |

**Table 22. Main board interface connector J200 (continued)**

| J201A connector |                |     |                | J201B |        |     |        |
|-----------------|----------------|-----|----------------|-------|--------|-----|--------|
| Pin             | Signal         | Pin | Signal         | Pin   | Signal | Pin | Signal |
| 18              | VDD_HV_IO_MAIN | 17  | VDD_HV_IO_MAIN | 138   | NC     | 137 | NC     |
| 16              | NC             | 15  | NC             | 136   | NC     | 135 | NC     |
| 14              | NC             | 13  | NC             | 134   | NC     | 133 | NC     |
| 12              | NC             | 11  | NC             | 132   | NC     | 131 | NC     |
| 10              | NC             | 9   | NC             | 130   | NC     | 129 | NC     |
| 8               | NC             | 7   | NC             | 128   | NC     | 127 | NC     |
| 6               | NC             | 5   | NC             | 126   | NC     | 125 | NC     |
| 4               | NC             | 3   | NC             | 124   | NC     | 123 | NC     |
| 2               | NC             | 1   | NC             | 122   | NC     | 121 | NC     |

## 7 LEDs

LEDs shown in [Table 23](#) provide indicators for:

- Power from externally-supplied voltages
- Power output from the PwrSBC
- Reset states
- Fail-safe signals from the PwrSBC

**Table 23. LEDs**

| LED | Description                  |
|-----|------------------------------|
| D1  | PwrSBC FS0                   |
| D2  | EXT_POR_B                    |
| D3  | RESET_B                      |
| D4  | External power supply 5 V    |
| D5  | External power supply 3.3 V  |
| D6  | External power supply 1.25 V |
| D7  | PwrSBC VSUP                  |
| D10 | PwrSBC VCAN                  |
| D12 | PwrSBC FS1                   |
| D15 | PwrSBC VAUX                  |
| D16 | PwrSBC VCCA                  |
| D17 | PwrSBC VCORE                 |
| D18 | PwrSBC VPRE                  |

## 8 Test points

Test points shown in [Table 24](#) are available to allow probing of various voltages.

**Table 24. Test points**

| Test Point | Description                          |
|------------|--------------------------------------|
| TP1        | VDD_HV_FLA0                          |
| TP2        | GND                                  |
| TP3        | GND                                  |
| TP4        | VSUP3 — PwrSBC supply                |
| TP5        | VDD_HV_IO                            |
| TP6        | VDD_HV_OSC0                          |
| TP7        | GND                                  |
| TP8        | VCAN — PwrSBC VCAN output            |
| TP9        | FS1 — PwrSBC fail-safe output 1      |
| TP10       | VSUP1/2 — PwrSBC supply              |
| TP11       | VSUW1/VSUW2 — PwrSBC switching point |
| TP12       | VDD_LV_PLL                           |
| TP13       | VDD_LV_CORE                          |
| TP14       | FB_CORE — PwrSBC feedback core       |
| TP16       | COMP_CORE — PwrSBC compensation      |
| TP17       | VSUW_CORE PwrSBC switching core      |
| TP18       | VPRE — PwrSBC preregulator           |
| TP19       | VDD_HV_ADR0                          |
| TP20       | VDD_HV_ADR1                          |
| TP21       | VDD_HV_ADV0/1                        |
| TP22       | VDD_HV_PMU                           |
| TP23       | VAUX — PwrSBC VAUX output            |
| TP24       | VCCA — PwrSBC VCCA output            |
| TP25       | VCORE — PwrSBC VCORE output          |
| TP26       | CLK_OUT                              |

## 9 Port pin to main board mapping

When the expansion board is connected to the main board, the port pins are routed to the main board via the interface connectors. [Table 25](#) shows the port pin mapping to the main board connectors.

For example, port pin PB4 can be accessed on the main board from connector P9 pin 8.

Table 25. Port pin mapping to main board connectors

| MPC5744P<br>port pin | MPC5746MMB<br>port pin connectors                    | MPC5746MMB<br>communication interface |
|----------------------|------------------------------------------------------|---------------------------------------|
| PA0                  | P8.1                                                 |                                       |
| PA1                  | P8.2                                                 |                                       |
| PA2                  | P8.3                                                 |                                       |
| PA3                  | P8.4                                                 |                                       |
| PA4                  | P8.5                                                 |                                       |
| PA5                  | P8.6                                                 |                                       |
| PA6                  | P8.7                                                 |                                       |
| PA7                  | P8.8                                                 |                                       |
| PA8                  | P8.9                                                 |                                       |
| PA9                  | P8.10                                                |                                       |
| PA10                 | P8.11                                                |                                       |
| PA11                 | P8.12                                                |                                       |
| PA12                 | P8.13                                                |                                       |
| PA13                 | P8.14                                                |                                       |
| PA14                 | P12.6                                                | J6 CAN DB9 connector                  |
| PA15                 | P14.15                                               |                                       |
| PB0                  | P10.10<br>(Must connect J17 2–6 on expansion board)  | J5 CAN DB9 connector                  |
| PB1                  | P10.9<br>(Must connect J17 5–3 on expansion board)   |                                       |
| PB2                  | P11.15<br>(Must connect J17 8–12 on expansion board) | J19 RS-232 DB9 connector              |
| PB3                  | P11.16<br>(Must connect J17 9–11 on expansion board) |                                       |
| PB4                  | P9.8                                                 |                                       |
| PB5                  | P9.7                                                 |                                       |
| PB6                  | P9.10                                                |                                       |
| PB7                  | P9.1                                                 |                                       |
| PB8                  | P9.2                                                 |                                       |
| PB9                  | P9.5                                                 |                                       |
| PB10                 | P9.6                                                 |                                       |
| PB11                 | P9.9                                                 |                                       |
| PB12                 | P9.12                                                |                                       |
| PB13                 | P9.3                                                 |                                       |
| PB14                 | P9.4                                                 |                                       |

Table 25. Port pin mapping to main board connectors (continued)

| MPC5744P<br>port pin | MPC5746MMB<br>port pin connectors                    | MPC5746MMB<br>communication interface |
|----------------------|------------------------------------------------------|---------------------------------------|
| PB15                 | P9.11                                                |                                       |
| PC0                  | P10.1                                                |                                       |
| PC1                  | P10.2                                                |                                       |
| PC2                  | P10.3                                                |                                       |
| PC3                  | Not implemented                                      |                                       |
| PC4                  | P10.5<br>(Must connect J18 11–12 on expansion board) |                                       |
| PC5                  | P10.6 (Must connect J18 8–9 on expansion board)      |                                       |
| PC6                  | P10.7 (Must connect J18 2–3 on expansion board)      |                                       |
| PC7                  | P10.8 (Must connect J18 5–6 on expansion board)      |                                       |
| PC8                  | Not implemented                                      |                                       |
| PC9                  | Not implemented                                      |                                       |
| PC10                 | P10.11                                               |                                       |
| PC11                 | P10.12                                               |                                       |
| PC12                 | P10.13                                               |                                       |
| PC13                 | P10.14                                               |                                       |
| PC14                 | P10.15                                               |                                       |
| PC15                 | P15.9                                                | J2 FlexRay DB9 connector              |
| PD0                  | P15.8                                                |                                       |
| PD1                  | P15.10                                               |                                       |
| PD2                  | P15.11                                               | J2 FlexRay DB9 connector              |
| PD3                  | P15.4                                                |                                       |
| PD4                  | P15.5                                                |                                       |
| PD5                  | P11.6                                                |                                       |
| PD6                  | P11.7                                                |                                       |
| PD7                  | P11.8                                                |                                       |
| PD8                  | P11.9                                                |                                       |
| PD9                  | P11.10                                               |                                       |
| PD10                 | P11.11                                               |                                       |
| PD11                 | P11.12                                               |                                       |
| PD12                 | P11.13                                               |                                       |
| PD13                 | Not implemented                                      |                                       |
| PD14                 | P15.1                                                |                                       |
| PD15                 | Not implemented                                      |                                       |

Table 25. Port pin mapping to main board connectors (continued)

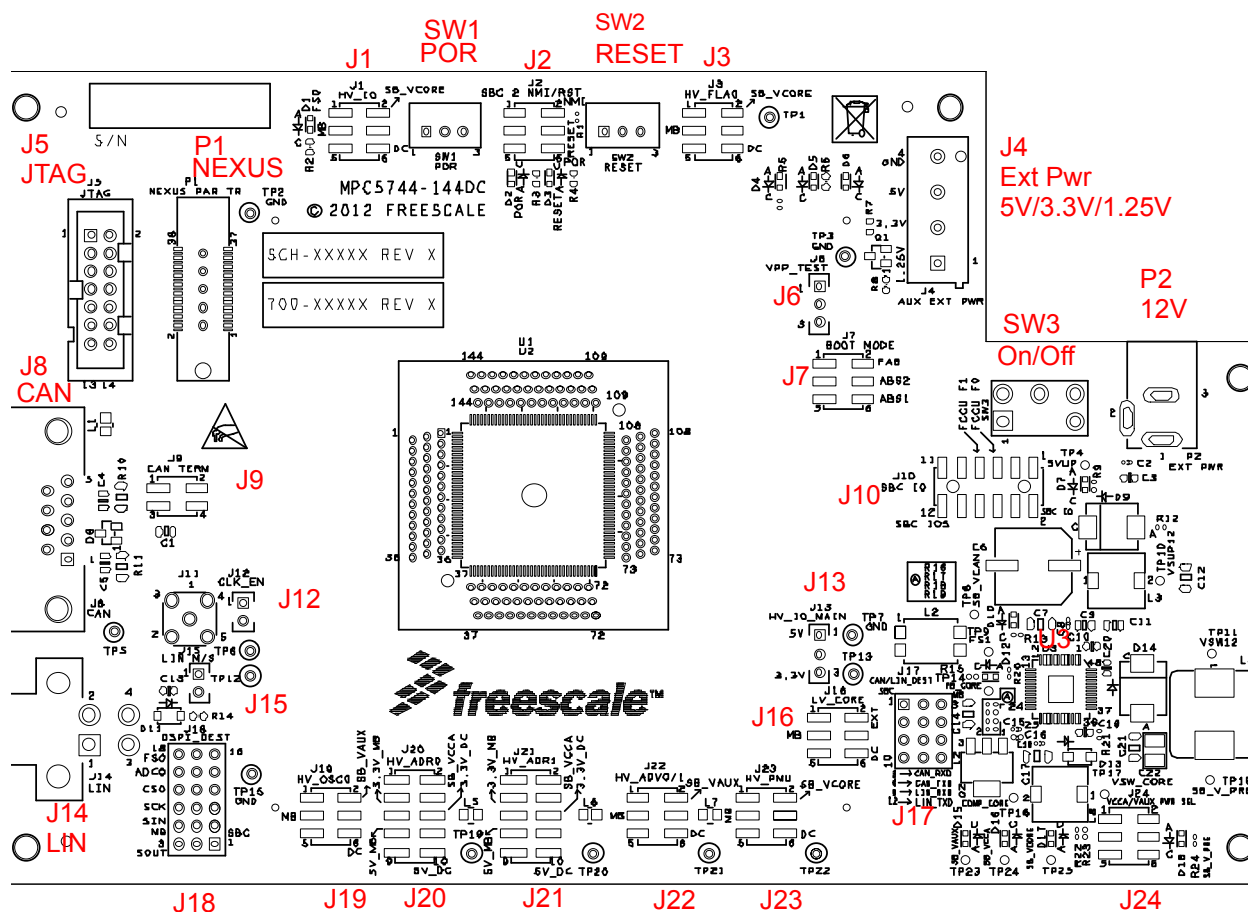
| MPC5744P<br>port pin | MPC5746MMB<br>port pin connectors | MPC5746MMB<br>communication interface |
|----------------------|-----------------------------------|---------------------------------------|
| PE0                  | P18.1                             |                                       |
| PE1                  | P18.2                             |                                       |
| PE2                  | P18.3                             |                                       |
| PE3                  | P18.4                             |                                       |
| PE4                  | P18.5                             |                                       |
| PE5                  | P18.6                             |                                       |
| PE6                  | P18.7                             |                                       |
| PE7                  | P18.8                             |                                       |
| PE8                  | P18.9                             |                                       |
| PE9                  | P18.10                            |                                       |
| PE10                 | P18.11                            |                                       |
| PE11                 | P18.12                            |                                       |
| PE12                 | P18.13                            |                                       |
| PE13                 | P18.14                            |                                       |
| PE14                 | P18.15                            |                                       |
| PE15                 | P18.16                            |                                       |
| PF0                  | P13.1                             |                                       |
| PF1                  | Not implemented                   |                                       |
| PF2                  | Not implemented                   |                                       |
| PF3                  | P13.4                             |                                       |
| PF4                  | P13.5                             |                                       |
| PF5                  | P13.6                             |                                       |
| PF6                  | P13.7                             |                                       |
| PF7                  | P13.8                             |                                       |
| PF8                  | P13.9                             |                                       |
| PF9                  | P13.10                            |                                       |
| PF10                 | P13.11                            |                                       |
| PF11                 | P13.12                            |                                       |
| PF12                 | P13.13                            |                                       |
| PF13                 | P13.14                            |                                       |
| PF14                 | P12.8                             | J4 LIN Molex connector                |
| PF15                 | P12.7                             |                                       |
| PG0                  | Not implemented                   |                                       |
| PG1                  | Not implemented                   |                                       |

Table 25. Port pin mapping to main board connectors (continued)

| MPC5744P<br>port pin | MPC5746MMB<br>port pin connectors | MPC5746MMB<br>communication interface |
|----------------------|-----------------------------------|---------------------------------------|
| PG2                  | P14.3                             |                                       |
| PG3                  | P14.4                             |                                       |
| PG4                  | P14.5                             |                                       |
| PG5                  | P14.6                             |                                       |
| PG6                  | P14.7                             |                                       |
| PG7                  | P14.8                             |                                       |
| PG8                  | P12.10                            |                                       |
| PG9                  | P12.11                            |                                       |
| PG10                 | P12.12                            |                                       |
| PG11                 | P12.13                            |                                       |
| PG12                 | Not implemented                   |                                       |
| PG13                 | Not implemented                   |                                       |
| PG14                 | Not implemented                   |                                       |
| PG15                 | Not implemented                   |                                       |
| PJ0                  | Not implemented                   |                                       |
| PJ1                  | Not implemented                   |                                       |
| PJ2                  | Not implemented                   |                                       |
| PJ3                  | Not implemented                   |                                       |
| PJ4                  | Not implemented                   |                                       |
| PJ5                  | Not implemented                   |                                       |
| PJ6                  | Not implemented                   |                                       |
| PJ7                  | Not implemented                   |                                       |
| PJ8                  | P17.9                             |                                       |
| PJ9                  | P17.10                            |                                       |
| PJ10                 | Not implemented                   |                                       |
| PJ11                 | Not implemented                   |                                       |
| PJ12                 | Not implemented                   |                                       |
| PJ13                 | Not implemented                   |                                       |
| PJ14                 | Not implemented                   |                                       |
| PJ15                 | Not implemented                   |                                       |

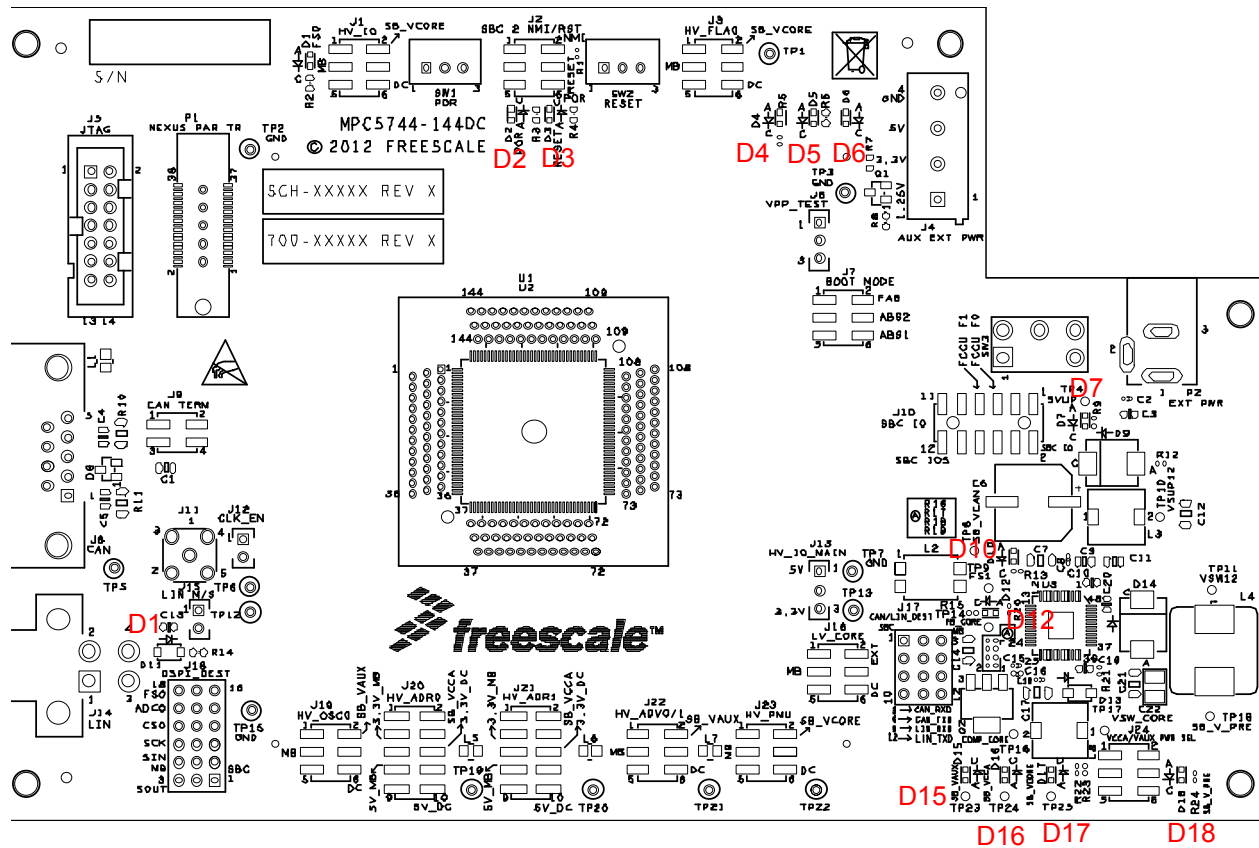


# 10 Diagrams



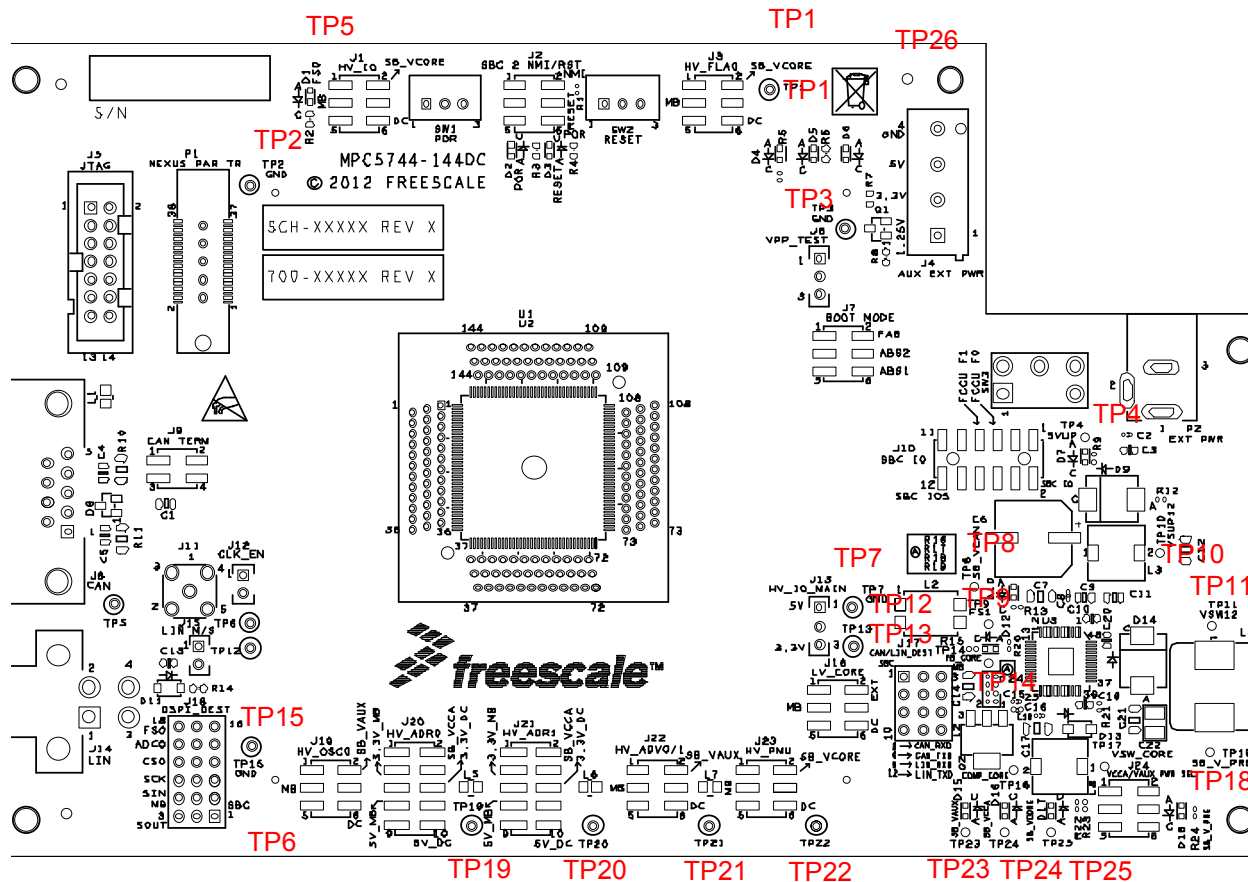
|                                                                                                                                                                                                          |                           |                                                                                                                         |                           |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-------------------------------------------------------------------------------------------------------------------------|---------------------------|
| FREESCALE                                                                                                                                                                                                |                           | NAME                                                                                                                    |                           |
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| SHEET<br>2 OF 12                                                                                                                                                                                         | FLM<br>PRIMARY SILKSCREEN | DATE<br>06-17-12                                                                                                        | NUMBER<br>170-27513 REV A |

Figure 5. Jumpers, connectors, and switches



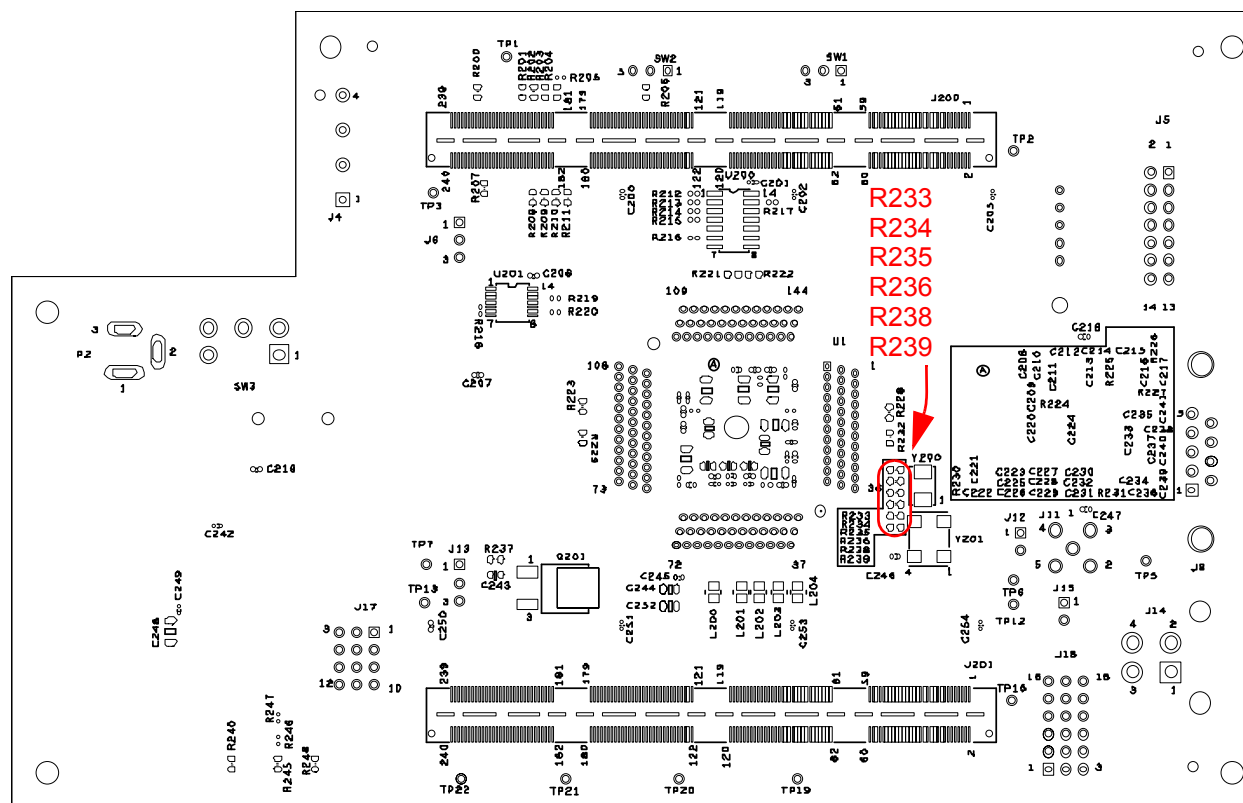
|                                                                                                                                                                                                          |                            |                  |                                          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------------------|------------------------------------------|
| FREESCALE                                                                                                                                                                                                |                            | NAME             | MPC5744-144DC                            |
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|                                                                                                                                                                                                          |                            | ---              | FCP (FREESCALE CONFIDENTIAL PROPRIETARY) |
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Figure 6. LEDs



|                                                                                                                                                                                                          |                            |                                              |                     |       |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|----------------------------------------------|---------------------|-------|
| FREESCALE                                                                                                                                                                                                |                            | NAME                                         |                     |       |
| 5501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78736 USA                                                                                                                                                |                            | MPC5744-144DC                                |                     |       |
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|                                                                                                                                                                                                          |                            | -X- FIU0 (FREESCALE INTERNAL USE ONLY)       |                     |       |
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| SHEET<br>2 OF 12                                                                                                                                                                                         | FILM<br>PRIMARY SILKSCREEN | DATE<br>06-17-12                             | NUMBER<br>170-27513 | REV A |

Figure 7. Test points



|                                                                                |                                                                                                                                                                                                                                                            |                                                                 |                          |
|--------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------------|
| SHEET<br>1 OF 14<br>FILM<br>00-17-15<br>DATE<br>170-2513<br>NUMBER<br>REV<br>A | PRESCAL<br>PRESCAL WITHOUT THE CONSENT OF<br>PROPRIETARY OR MANUFACTURE IN WHOLE<br>OR PART FOR ENGINEERING DESIGN<br>PROPRIETARY TO PRESCAL AND SHALL<br>THIS DOCUMENT CONTAINING INFORMATION<br>(PUB) (PUBLIC INFORMATION)<br>(PUB) (PUBLIC INFORMATION) | NAME<br>WILLIAM LANNON DRIVE WEST<br>TEXAS 75135 USA<br>PRESCAL | 144D-144C<br>MP5344-144C |
|--------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|--------------------------|

### Figure 8. Bottom view

## 11 Revision history

### Table 26. Revision history

| Revision number | Date    | Description                                                                                                                              |
|-----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------|
| 0               | 08/2012 | Initial version.                                                                                                                         |
| 1               | 11/2012 | Correct values in table 10, “Switch settings— DSPI and ADC0 connectivity,” and in table 25, “Port pin mapping to main board connectors.” |

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