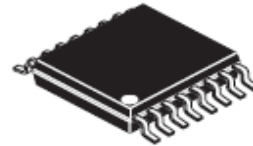


# MC9S08SC4 8-Bit Microcontroller Data Sheet

## MC9S08SC4



948F-01

### 8-Bit HCS08 Central Processor Unit (CPU)

- Up to 40 MHz HCS08 CPU (central processor unit); up to 20 MHz bus frequency
- HC08 instruction set with added BGND instruction

### On-Chip Memory

- 4 KB of FLASH with read/program/erase over full operating voltage and temperature
- 256 bytes of Random-access memory (RAM)

### Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode

### Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 32 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2 % resolution and 2.0 % deviation over temperature and voltage; supports bus frequencies from 2 MHz to 20 MHz.

### System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect
- Reset on loss of clock

### Development Support

- Single-wire background debug interface

- Breakpoint capability to allow single breakpoint setting during in-circuit debugging

### Peripherals

- **SCI** — Serial Communication Interface
  - Full-duplex non-return to zero (NRZ)
  - LIN master extended break generation
  - LIN slave extended break detection
  - Wake-up on active edge
- **TPMx** — Two 2-channel Timer/PWM modules (TPM1 and TPM2)
  - 16-bit modulus or up/down counters
  - Input capture, output compare, buffered edge-aligned or center-aligned PWM
- **ADC** — Analog to Digital Converter
  - 8-channel, 10-bit resolution
  - 2.5  $\mu$ s conversion time
  - Automatic compare function
  - Temperature sensor
  - Internal bandgap reference channel

### Input/Output

- 12 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.

### Package Options

- 16-TSSOP

### Operating Parameters

- 4.5-5.5 V operation
- C, V, M temperature ranges available, covering -40 - 125 °C operation

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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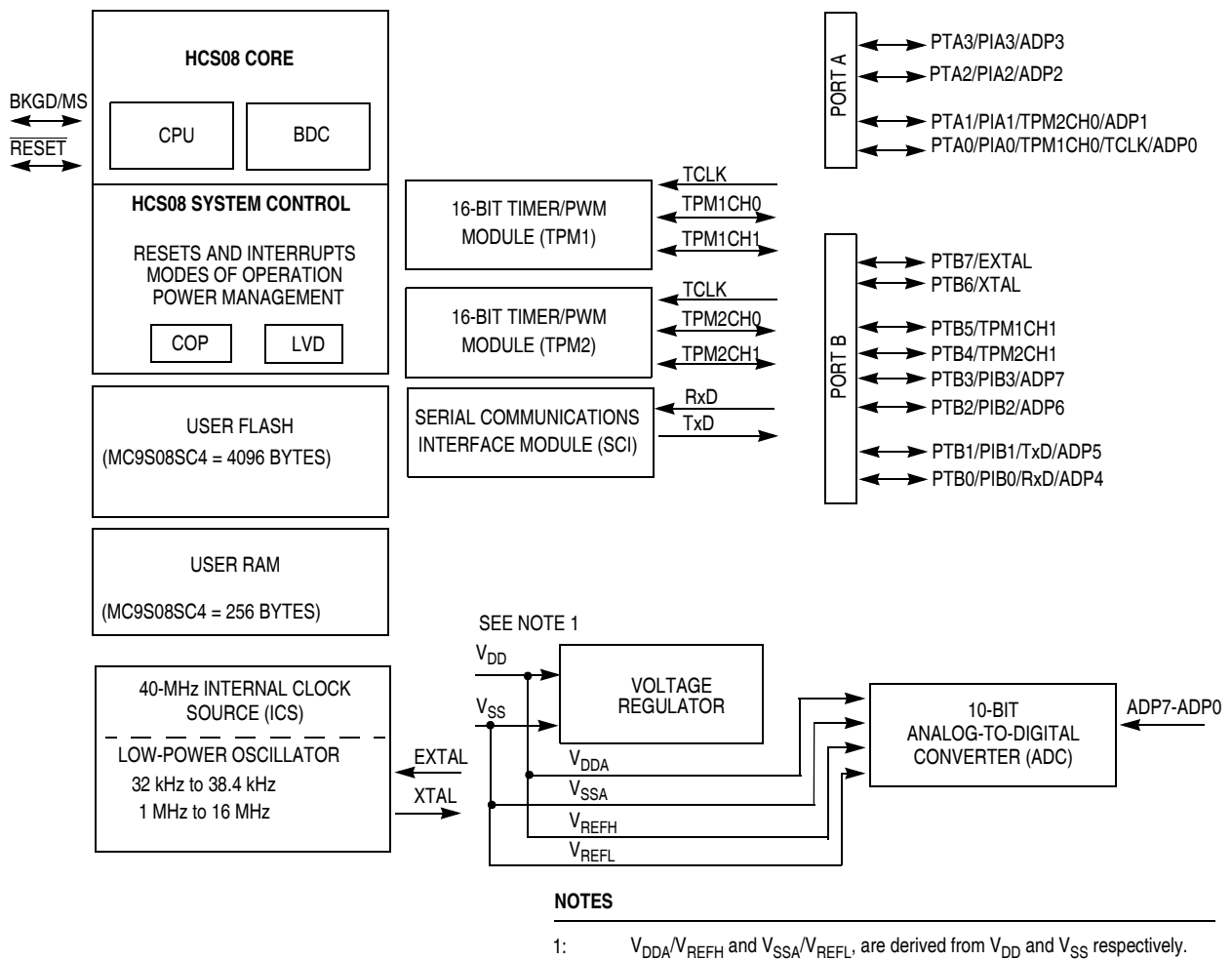
# Chapter 1

## Device Overview

The MC9S08SC4 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). The MC9S08SC4 uses the enhanced HCS08 core.

### 1.1 MCU Block Diagram

The block diagram in [Figure 1-1](#) shows the structure of the MC9S08SC4 MCU.



**Figure 1-1. MC9S08SC4 Block Diagram**







# Chapter 3

## Electrical Characteristics

### 3.1 Introduction

This section contains electrical and timing specifications for the MC9S08SC4 Series of microcontrollers available at the time of publication.

### 3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 3-1. Parameter Classifications**

<b>P</b>	Those parameters are guaranteed during production testing on each individual device.
<b>C</b>	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
<b>T</b>	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
<b>D</b>	Those parameters are derived mainly from simulations.

#### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3-2](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pull-up resistor associated with the pin is enabled.

**Table 3-2. Absolute Maximum Ratings**

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD}$	-0.3 to +5.8	V
Maximum current into $V_{DD}$	$I_{DD}$	120	mA
Digital input voltage	$V_{In}$	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) <sup>1, 2, 3</sup>	$I_D$	$\pm 25$	mA
Storage temperature range	$T_{stg}$	-55 to 150	°C

- <sup>1</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive ( $V_{DD}$ ) and negative ( $V_{SS}$ ) clamp voltages, then use the larger of the two resistance values.
- <sup>2</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .
- <sup>3</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{In} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

## 3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 3-3. Thermal Characteristics**

Num	C	Rating	Symbol	Value	Unit	
1	—	Operating temperature range (packaged)	$T_A$	$T_L$ to $T_H$	°C	
				C		-40 to 85
				V		-40 to 105
				M		-40 to 125
2	D	Maximum junction temperature	$T_{JM}$	—	°C	
				C		95
				V		115
				M		135
3	D	Thermal resistance <sup>1,2</sup> Single-layer board	$\theta_{JA}$	16-pin TSSOP	130	°C/W
				4	D	Thermal resistance <sup>1,2</sup> Four-layer board



- <sup>1</sup> Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- <sup>2</sup> Junction to Ambient Natural Convection

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{Eqn. 3-1}$$

where:

- $T_A$  = Ambient temperature, °C
- $\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W
- $P_D = P_{int} + P_{I/O}$
- $P_{int} = I_{DD} \times V_{DD}$ , Watts — chip internal power
- $P_{I/O}$  = Power dissipation on input and output pins — user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \tag{Eqn. 3-2}$$

Solving Equation 3-1 and Equation 3-2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \tag{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of  $T_A$ .

### 3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 3-4. ESD and Latch-up Test Conditions**

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	-2.5	V
	Maximum input voltage limit	—	7.5	V

**Table 3-5. ESD and Latch-Up Protection Characteristics**

No.	Rating <sup>1</sup>	Symbol	Min	Max	Unit
1	Human body model (HBM)	$V_{\text{HBM}}$	$\pm 2000$	—	V
2	Charge device model (CDM)	$V_{\text{CDM}}$	$\pm 500$	—	V
3	Latch-up current at $T_A = 125^\circ\text{C}$	$I_{\text{LAT}}$	$\pm 100$	—	mA

<sup>1</sup> Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 3-6. DC Characteristics**

Num	C	Characteristic	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit	
4	—	Operating voltage	$V_{\text{DD}}$	—	4.5	—	5.5	V	
5	C	Output high voltage All I/O pins, low-drive strength	$V_{\text{OH}}$	5 V, $I_{\text{Load}} = -4$ mA	$V_{\text{DD}} - 1.5$	—	—	V	
	P			5 V, $I_{\text{Load}} = -2$ mA	$V_{\text{DD}} - 0.8$	—	—		
	C			All I/O pins, high-drive strength	5 V, $I_{\text{Load}} = -20$ mA	$V_{\text{DD}} - 1.5$	—		—
	P				5 V, $I_{\text{Load}} = -10$ mA	$V_{\text{DD}} - 0.8$	—		—
6	C	Output high current Max total $I_{\text{OH}}$ for all ports	$I_{\text{OHT}}$	$V_{\text{OUT}} < V_{\text{DD}}$	0	—	-100	mA	
7	C	Output low voltage All I/O pins, low-drive strength	$V_{\text{OL}}$	5 V, $I_{\text{Load}} = 4$ mA	—	—	1.5	V	
	P			5 V, $I_{\text{Load}} = 2$ mA	—	—	0.8		
	C			All I/O pins, high-drive strength	5 V, $I_{\text{Load}} = 20$ mA	—	—		1.5
	P				5 V, $I_{\text{Load}} = 10$ mA	—	—		0.8
8	C	Output low current Max total $I_{\text{OL}}$ for all ports	$I_{\text{OLT}}$	$V_{\text{OUT}} > V_{\text{SS}}$	0	—	100	mA	
9	P	Input high voltage; all digital inputs	$V_{\text{IH}}$	5V	$0.65 \times V_{\text{DD}}$	—	—	V	
10	P	Input low voltage; all digital inputs	$V_{\text{IL}}$	5V	—	—	$0.35 \times V_{\text{DD}}$	V	
11	C	Input hysteresis	$V_{\text{hys}}$	—	$0.06 \times V_{\text{DD}}$	—	—	V	
12	P	Input leakage current (per pin)	$ I_{\text{In}} $	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	0.1	1	$\mu\text{A}$	
13	P	Hi-Z (off-state) leakage current (per pin) input/output port pins PTB6/XTAL, RESET	$ I_{\text{OZ}} $	$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$ ,	—	0.1	1	$\mu\text{A}$	
				$V_{\text{In}} = V_{\text{DD}}$ or $V_{\text{SS}}$	—	0.2	2	$\mu\text{A}$	
14	P	Pull-up or Pull-down <sup>2</sup> resistors; when enabled I/O pins	$R_{\text{PU}}, R_{\text{PD}}$	—	17	37	52	k $\Omega$	
	C				RESET <sup>3</sup>	$R_{\text{PU}}$	17	37	52

Table 3-6. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
15	D	DC injection current <sup>4, 5, 6, 7</sup> Single pin limit	$I_{IC}$	$V_{IN} > V_{DD}$	0	—	2	mA
				$V_{IN} < V_{SS}$ ,	0	—	-0.2	mA
		Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA
				$V_{IN} < V_{SS}$ ,	0	—	-5	mA
16	D	Input Capacitance, all pins	$C_{In}$	—	—	—	8	pF
17	D	RAM retention voltage	$V_{RAM}$	—	—	0.6	1.0	V
18	D	POR re-arm voltage <sup>8</sup>	$V_{POR}$	—	0.9	1.4	2.0	V
19	D	POR re-arm time <sup>9</sup>	$t_{POR}$	—	10	—	—	μs
20	P	Low-voltage detection threshold — high range  $V_{DD}$ falling $V_{DD}$ rising	$V_{LVD1}$	—	3.85	4.0	4.15	V
					3.95	4.1	4.25	
21	P	Low-voltage warning threshold — high range 1  $V_{DD}$ falling $V_{DD}$ rising	$V_{LVW3}$	—	4.45	4.6	4.75	V
					4.55	4.7	4.85	
22	P	Low-voltage warning threshold — high range 0  $V_{DD}$ falling $V_{DD}$ rising	$V_{LVW2}$	—	4.15	4.3	4.45	V
					4.25	4.4	4.55	
23	T	Low-voltage inhibit reset/recover hysteresis	$V_{hys}$	—	—	100	—	mV
24	P	Bandgap Voltage Reference <sup>10</sup>	$V_{BG}$	—	1.17	1.20	1.22	V

<sup>1</sup> Typical values are measured at 25°C. Characterized, not tested.

<sup>2</sup> When a pin interrupt is configured to detect rising edges, pull-down resistors are used in place of pull-up resistors.

<sup>3</sup> The specified resistor value is the actual value internal to the device. The pull-up value may measure higher when measured externally on the pin.

<sup>4</sup> Power supply must maintain regulation within operating  $V_{DD}$  range during instantaneous and operating maximum current conditions. If positive injection current ( $V_{IN} > V_{DD}$ ) is greater than  $I_{DD}$ , the injection current may flow out of  $V_{DD}$  and could result in external power supply going out of regulation. Ensure external  $V_{DD}$  load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

<sup>5</sup> All functional non-supply pins are internally clamped to  $V_{SS}$  and  $V_{DD}$ .

<sup>6</sup> Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

<sup>7</sup> The  $\overline{RESET}$  pin does not have a clamp diode to  $V_{DD}$ . Do not drive this pin above  $V_{DD}$ .

<sup>8</sup> Maximum is highest voltage that POR will occur.

<sup>9</sup> Simulated, not tested

<sup>10</sup> Factory trimmed at  $V_{DD} = 5.0$  V, Temp = 25°C

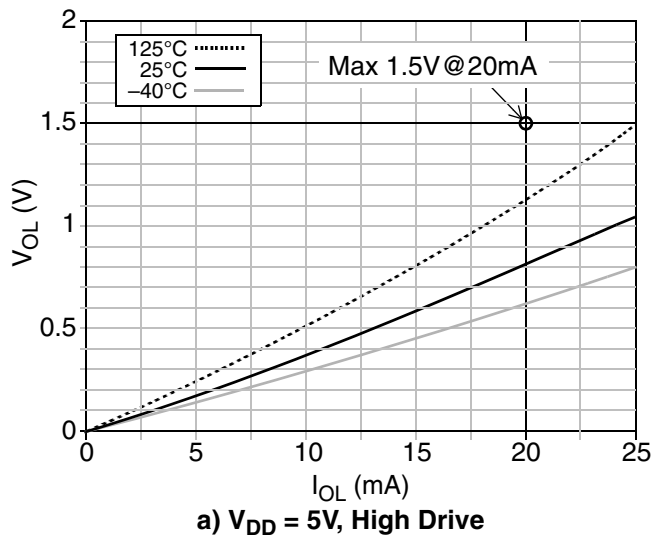


Figure 3-1. Typical  $V_{OL}$  vs  $I_{OL}$ , High Drive Strength

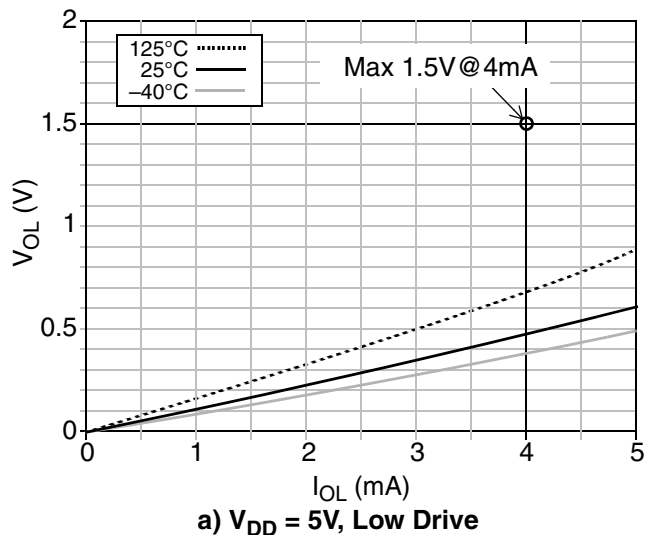
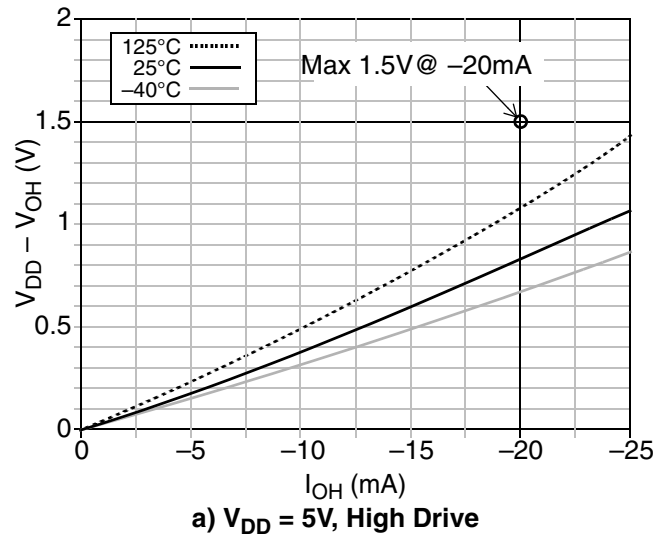
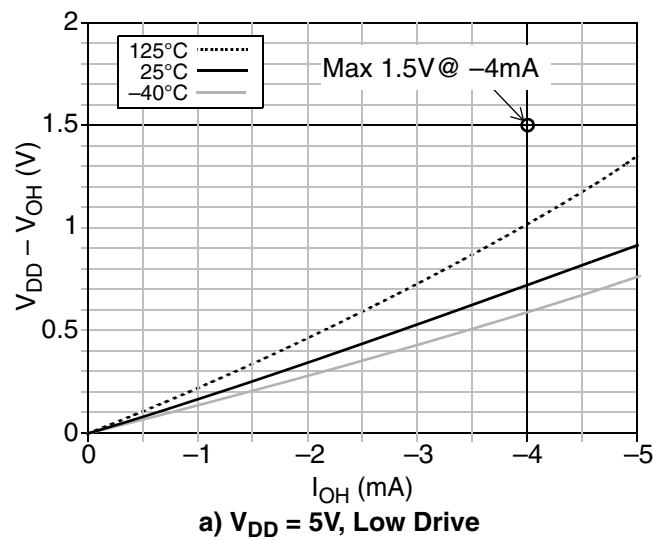


Figure 3-2. Typical  $V_{OL}$  vs  $I_{OL}$ , Low Drive Strength


 Figure 3-3. Typical  $V_{DD} - V_{OH}$  vs  $I_{OH}$ , High Drive Strength

 Figure 3-4. Typical  $V_{DD} - V_{OH}$  vs  $I_{OH}$ , Low Drive Strength

### 3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

**Table 3-7. Supply Current Characteristics**

Num	C	Parameter	Symbol	V <sub>DD</sub> (V)	Typ <sup>1</sup>	Max <sup>2</sup>	Unit	
1	C	Run supply current <sup>3</sup> measured at (CPU clock = 4 MHz, f <sub>BUS</sub> = 2 MHz)	R <sub>I</sub> DD	5	1.9	2.4	mA	
2	P	Run supply current <sup>3</sup> measured at (CPU clock = 16 MHz, f <sub>BUS</sub> = 8 MHz)	R <sub>I</sub> DD	5	4.6	5.6	mA	
3	C	Run supply current <sup>4</sup> measured at (CPU clock = 32 MHz, f <sub>BUS</sub> = 16 MHz)	R <sub>I</sub> DD	5	7.8	8.9	mA	
4	C	Stop3 mode supply current	S3I <sub>DD</sub>	5	-40 °C (C & M suffix)	0.71	—	μA
	P				25 °C (All parts)	0.93	—	
	C <sup>5</sup>				85 °C (C suffix only)	4	11	
	C <sup>5</sup>				105 °C (V suffix only)	9	30	
	P <sup>5</sup>				125 °C (M suffix only)	28	60	
5	C	Stop2 mode supply current	S2I <sub>DD</sub>	5	-40 °C (C & M suffix)	0.70	—	μA
	P				25 °C (All parts)	0.89	—	
	C <sup>5</sup>				85 °C (C suffix only)	3	8	
	C <sup>5</sup>				105 °C (V suffix only)	6	22	
	P <sup>5</sup>				125 °C (M suffix only)	17	41	
6	C	LVD adder to stop3 (LVDE = LVDSE = 1)	S3I <sub>DDLVD</sub>	5	110	165	μA	
7	C	Adder to stop3 for oscillator enabled <sup>6</sup> (EREFSTEN = 1)	S3I <sub>DDOSC</sub>	5	5	8	μA	

<sup>1</sup> Typical values are based on characterization data at 25 °C. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

<sup>2</sup> Max values in this column apply for the full operating temperature range of the device unless otherwise noted.

<sup>3</sup> All modules except ADC active, ICS configured for FBE, and does not include any dc loads on port pins.

<sup>4</sup> All modules except ADC active, ICS configured for FEI, and does not include any dc loads on port pins.

<sup>5</sup> Stop currents are tested in production for 25 °C on all parts. Tests at other temperatures depend upon the part number suffix and maturity of the product. Freescale may eliminate a test insertion at a particular temperature from the production test flow once sufficient data has been collected and is approved.

<sup>6</sup> Values given under the following conditions: low range operation (RANGE = 0) with a 32.768 kHz crystal and low power mode (HGO = 0).

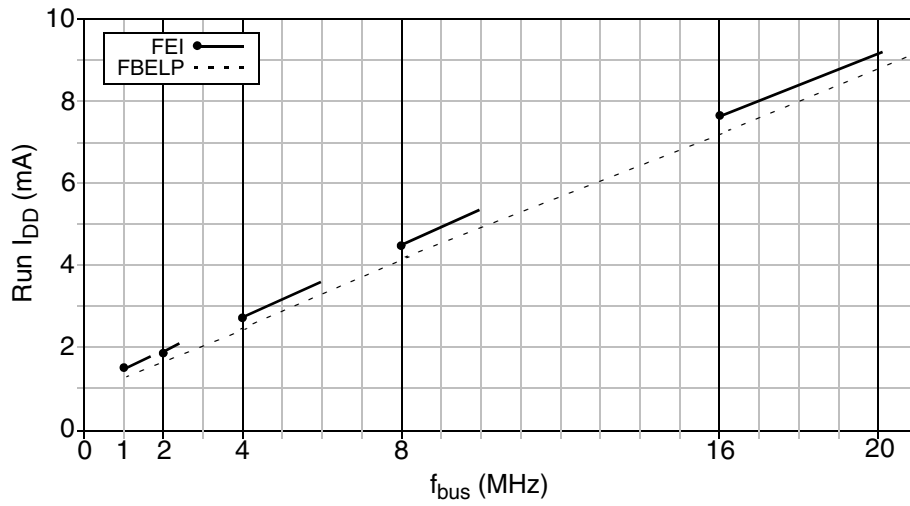
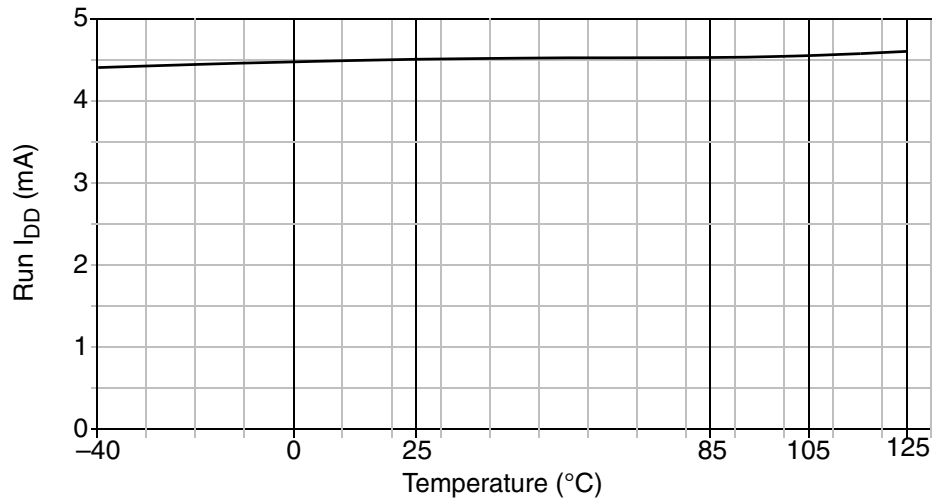


Figure 3-5. Typical Run I<sub>DD</sub> vs. Bus Frequency (V<sub>DD</sub> = 5V)



Note: ICS is configured to FEI.

Figure 3-6. Typical Run I<sub>DD</sub> vs. Temperature (V<sub>DD</sub> = 5V; f<sub>bus</sub> = 8MHz)

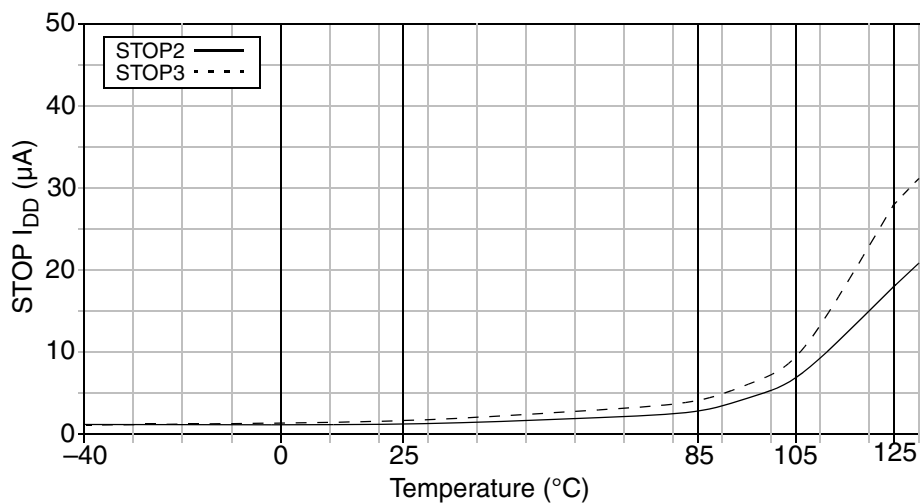


Figure 3-7. Typical Stop I<sub>DD</sub> vs. Temperature (V<sub>DD</sub> = 5V)

### 3.8 External Oscillator (XOSC) Characteristics

#### NOTE

The MC9S08SC4 series supports a narrower low frequency external reference range than the standard ICS specification. All references to range "31.25 kHz to 39.0625 kHz" in this section should be limited to "32.0 kHz to 38.4 kHz".



**Table 3-8. Oscillator Electrical Specifications (Temperature Range = –40 to 125°C Ambient)**

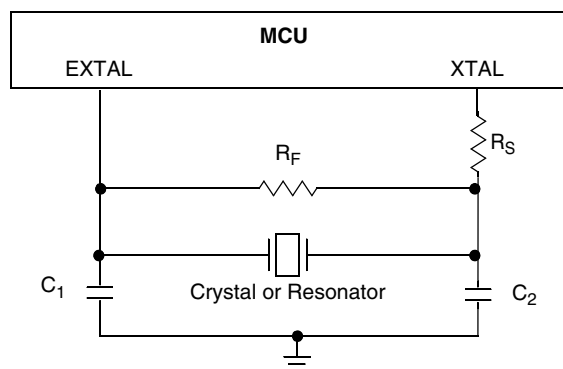
Num	C	Rating	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	$f_{lo}$	32	—	38.4	kHz
		High range (RANGE = 1) FEE or FBE mode <sup>2</sup>	$f_{hi}$	1	—	5	MHz
		High range (RANGE = 1, HGO = 1) FBELP mode	$f_{hi-hgo}$	1	—	16	MHz
		High range (RANGE = 1, HGO = 0) FBELP mode	$f_{hi-lp}$	1	—	8	MHz
2	—	Load capacitors	$C_1, C_2$	See crystal or resonator manufacturer's recommendation			
3	—	Feedback resistor	$R_F$				$M\Omega$
		Low range (32 kHz to 100 kHz)		—	10	—	
		High range (1 MHz to 16 MHz)		—	1	—	
4	—	Series resistor	$R_S$				$k\Omega$
		Low range, low gain (RANGE = 0, HGO = 0)		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low gain (RANGE = 1, HGO = 0)		—	0	—	
		High range, high gain (RANGE = 1, HGO = 1)					
≥ 8 MHz	—	0	0				
4 MHz	—	0	10				
1 MHz	—	0	20				
5	T	Crystal start-up time <sup>3</sup>					ms
		Low range, low gain (RANGE = 0, HGO = 0)	$t_{CSTL-LP}$	—	200	—	
		Low range, high gain (RANGE = 0, HGO = 1)	$t_{CSTL-HGO}$	—	400	—	
		High range, low gain (RANGE = 1, HGO = 0) <sup>4</sup>	$t_{CSTH-LP}$	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1) <sup>4</sup>	$t_{CSTH-HGO}$	—	15	—	
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)					
		FEE or FBE mode <sup>2</sup>	$f_{extal}$	0.03125	—	5	MHz
		FBELP mode		0	—	40	MHz

<sup>1</sup> Typical data was characterized at 5.0 V, 25°C or is recommended value.

<sup>2</sup> The input clock source must be divided using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

<sup>3</sup> This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications. This data will vary based upon the crystal manufacturer and board design. The crystal should be characterized by the crystal manufacturer.

<sup>4</sup> 4 MHz crystal.



### 3.9 Internal Clock Source (ICS) Characteristics

Table 3-9. ICS Frequency Specifications (Temperature Range = -40 to 125°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	P	Internal reference frequency - factory trimmed at $V_{DD} = 5\text{ V}$ and temperature = 25°C	$f_{int\_ft}$	—	31.25	—	kHz
2	T	Internal reference frequency - untrimmed <sup>1</sup>	$f_{int\_ut}$	25	36	41.66	kHz
3	P	Internal reference frequency - user trimmed	$f_{int\_t}$	31.25	—	39.0625	kHz
4	T	Internal reference startup time	$t_{irefst}$	—	—	6	μs
5	—	DCO output frequency range - untrimmed <sup>1</sup> value provided for reference assumes: $f_{dco\_ut} = 1024 \times f_{int\_ut}$	$f_{dco\_ut}$	25.6	36.86	42.66	MHz
6	D	DCO output frequency range - trimmed	$f_{dco\_t}$	32	—	40	MHz
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	% $f_{dco}$
8	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	% $f_{dco}$
9	D	Total deviation from actual trimmed DCO output frequency over voltage and temperature	$\Delta f_{dco\_t}$	—	+ 0.5 - 1.0	± 2.0	% $f_{dco}$
10	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	$\Delta f_{dco\_t}$	—	± 0.5	± 1	% $f_{dco}$
11	D	FLL acquisition time <sup>2</sup>	$t_{acquire}$	—	—	1	ms
12	D	DCO output clock long term jitter (over 2mS interval) <sup>3</sup>	$C_{jitter}$	—	0.02	0.2	% $f_{dco}$

<sup>1</sup> TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

<sup>2</sup> This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

<sup>3</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{BUS}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{DD}$  and  $V_{SS}$  and variation in crystal oscillator frequency increase the  $C_{jitter}$  percentage for a given interval.

### 3.10 ADC Characteristics

**Table 3-10. ADC Operating Conditions**

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}^2$	2.7	—	5.5	V	—
Input Voltage	—	$V_{ADIN}$	$V_{REFL}^2$	—	$V_{REFH}^2$	V	—
Input Capacitance	—	$C_{ADIN}$	—	4.5	5.5	pF	—
Input Resistance	—	$R_{ADIN}$	—	3	5	k $\Omega$	—
Analog Source Resistance	10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	$R_{AS}$	—	—	5	k $\Omega$	External to MCU
	8 bit mode (all valid $f_{ADCK}$ )		—	—	10		
ADC Conversion Clock Frequency	High Speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	—
	Low Power (ADLPC=1)		0.4	—	4.0		

<sup>1</sup> Typical values assume  $V_{DDA} = 5.0\text{ V}$ ,  $\text{Temp} = 25^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup>  $V_{DDA}/V_{REFH}$  and  $V_{SSA}/V_{REFL}$ , are derived from  $V_{DD}$  and  $V_{SS}$  respectively.

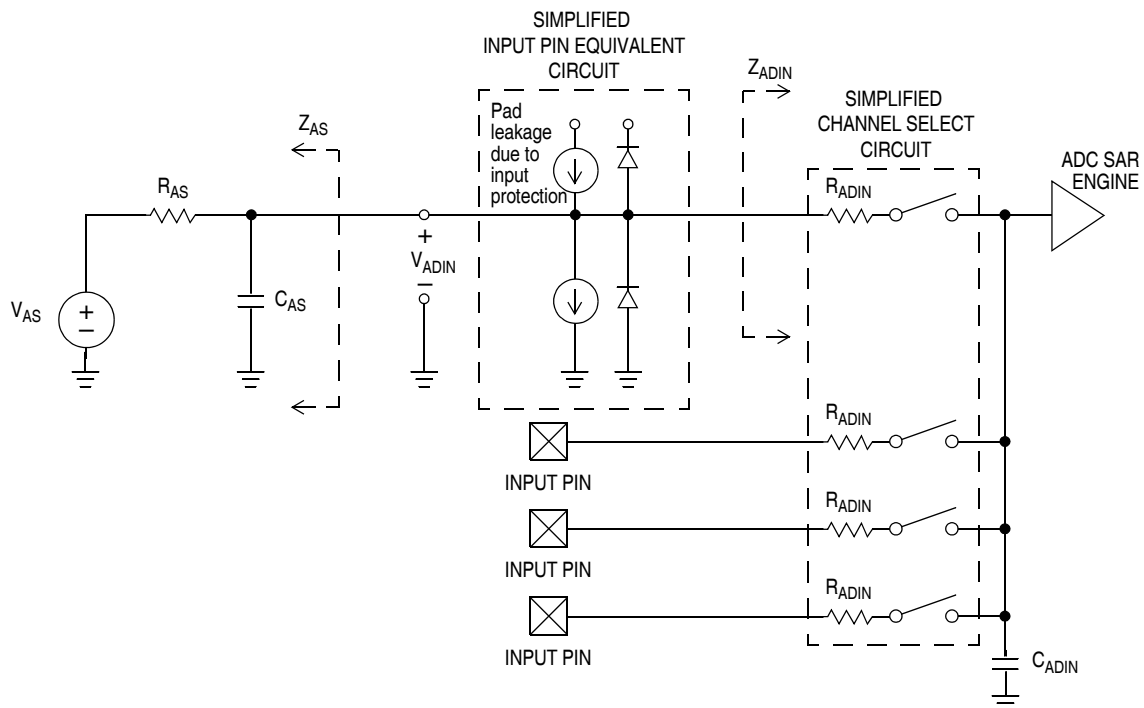

**Figure 3-8. ADC Input Impedance Equivalency Diagram**

Table 3-11. ADC Characteristics

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1	—	T	I <sub>DDA</sub>	—	133	—	μA	—
Supply Current ADLPC=1 ADLSMP=0 ADCO=1	—	T	I <sub>DDA</sub>	—	218	—	μA	—
Supply Current ADLPC=0 ADLSMP=1 ADCO=1	—	T	I <sub>DDA</sub>	—	327	—	μA	—
Supply Current ADLPC=0 ADLSMP=0 ADCO=1	—	T	I <sub>DDA</sub>	—	0.582	1	mA	—
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f <sub>ADACK</sub>	2	3.3	5	MHz	t <sub>ADACK</sub> = 1/f <sub>ADACK</sub>
	Low Power (ADLPC=1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t <sub>ADC</sub>	—	20	—	ADCK cycles	See ADC chapter in MC9S08SC4 Reference Manual for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t <sub>ADS</sub>	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	10 bit mode	P	E <sub>TUE</sub>	—	±1.5	±3.5	LSB	Includes quantization
	8 bit mode			—	±0.7	±1.5		
Differential Non-Linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB	Monotonicity and No-Missing-Codes guaranteed
	8 bit mode			—	±0.3	±0.5		
Integral Non-Linearity	10 bit mode	C	INL	—	±0.5	±1.0	LSB	
	8 bit mode			—	±0.3	±0.5		
Zero-Scale Error	10 bit mode	P	E <sub>ZS</sub>	—	±1.5	±2.5	LSB	V <sub>ADIN</sub> = V <sub>SSA</sub>
	8 bit mode			—	±0.5	±0.7		
Full-Scale Error	10 bit mode	P	E <sub>FS</sub>	—	±1	±1.5	LSB	V <sub>ADIN</sub> = V <sub>DDA</sub>
	8 bit mode			—	±0.5	±0.5		

Table 3-11. ADC Characteristics

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Quantization Error	10 bit mode	D	$E_Q$	—	—	±0.5	LSB	—
	8 bit mode			—	—	±0.5		
Input Leakage Error	10 bit mode	D	$E_{IL}$	—	±0.2	±2.5	LSB	Pad leakage <sup>2</sup> * $R_{AS}$
	8 bit mode			—	±0.1	±1		
Temp Sensor Slope	−40°C– 25°C	D	m	—	3.266	—	mV/°C	—
	25°C– 125°C			—	3.638	—		
Temp Sensor Voltage	25°C	D	$V_{TEMP2}$ 5	—	1.396	—	V	—

<sup>1</sup> Typical values assume  $V_{DDA} = 5.0V$ , Temp = 25C,  $f_{ADCK} = 1.0MHz$  unless otherwise stated. Typical values are for reference only and are not tested in production.

<sup>2</sup> Based on input pad leakage current. Refer to pad electricals.

## 3.11 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

### 3.11.1 Control Timing

Table 3-12. Control Timing

Num	C	Rating	Symbol	Min	Typ <sup>1</sup>	Max	Unit
1	D	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	dc	—	20	MHz
2	P	Internal low power oscillator period	$t_{LPO}$	700	975	1500	μs
3	D	External reset pulse width <sup>2</sup>	$t_{extrst}$	100	—	—	ns
4	D	Reset low drive <sup>3</sup>	$t_{rstdrv}$	$66 \times t_{cyc}$	—	—	ns
5	D	Pin interrupt pulse width Asynchronous path <sup>2</sup> Synchronous path <sup>4</sup>	$t_{ILIH}$ , $t_{IHIL}$	100 $1.5 \times t_{cyc}$	—	—	ns
6	C	Port rise and fall time — Low output drive ( $PTxDS = 0$ ) (load = 50 pF) <sup>5</sup> Slew rate control disabled ( $PTxSE = 0$ ) Slew rate control enabled ( $PTxSE = 1$ )	$t_{Rise}$ , $t_{Fall}$	— —	40 75	—	ns
		Port rise and fall time — High output drive ( $PTxDS = 1$ ) (load = 50 pF) <sup>6</sup> Slew rate control disabled ( $PTxSE = 0$ ) Slew rate control enabled ( $PTxSE = 1$ )	$t_{Rise}$ , $t_{Fall}$	— —	11 35	—	ns

<sup>1</sup> Typical values are based on characterization data at  $V_{DD} = 5.0V$ , 25°C unless otherwise stated.

- 2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources. Refer to [Figure 3-9](#).
- 3 When any reset is initiated, internal circuitry drives the reset pin low for about 66 cycles of  $t_{CYC}$ . After POR reset the bus clock frequency changes to the untrimmed DCO frequency ( $f_{reset} = (f_{dco\_ut})/4$ ) because TRIM is reset to 0x80 and FTRIM is reset to 0, and there is an extra divide-by-two because BDIV is reset to 0:1. After other resets trim stays at the pre-reset value.
- 4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 5 Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range  $-40^{\circ}C$  to  $125^{\circ}C$ .

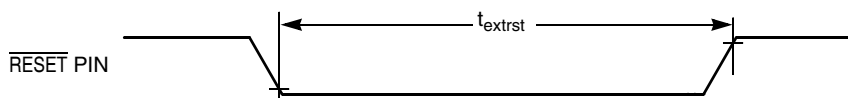


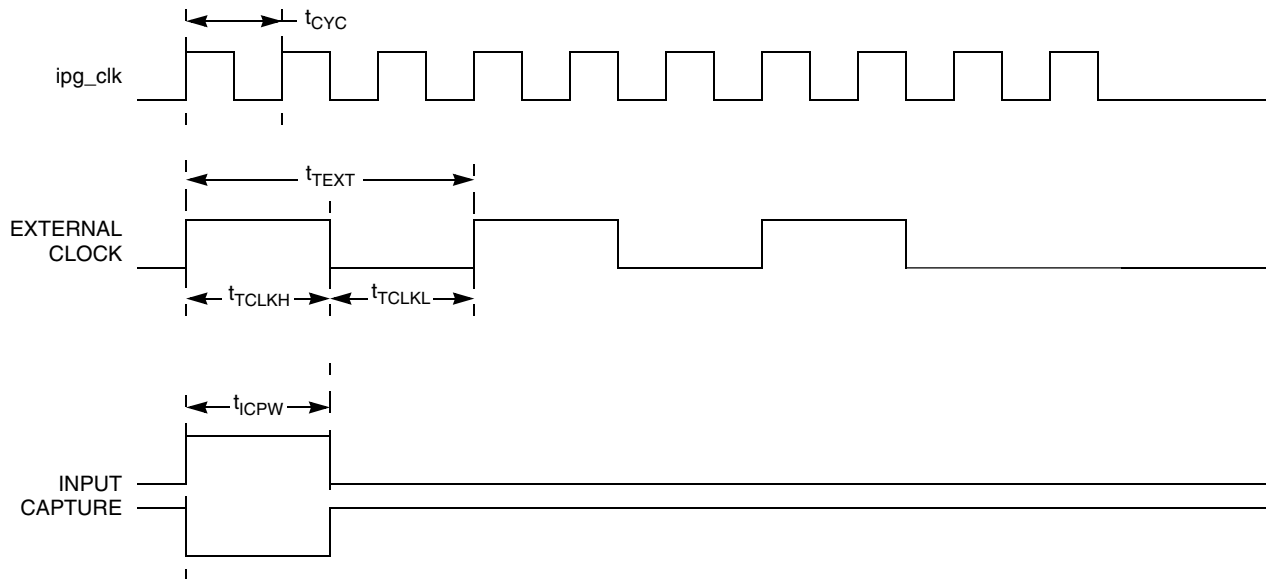
Figure 3-9. Reset Timing

### 3.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 3-13. TPM Input Timing

Num	C	Rating	Symbol	Min	Max	Unit
1	—	External clock frequency	$f_{TEXT}$	dc	$1/4 f_{op}$	MHz
2	—	External clock period	$t_{TEXT}$	4	—	$t_{CYC}$
3	—	External clock high time	$t_{TCLKH}$	1.5	—	$t_{CYC}$
4	—	External clock low time	$t_{TCLKL}$	1.5	—	$t_{CYC}$
5	—	Input capture pulse width	$f_{ICPW}$	1.5	—	$t_{CYC}$



## 3.12 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the FLASH memory.

Program and erase operations do not require any special power sources other than the normal  $V_{DD}$  supply. For more detailed information about program/erase operations, see the Memory section.

**Table 3-14. FLASH Characteristics**

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	4.5	—	5.5	V
2	—	Supply voltage for read operation	$V_{Read}$	4.5	—	5.5	V
3	—	Internal FCLK frequency <sup>1</sup>	$f_{FCLK}$	150	—	200	kHz
4	—	Internal FCLK period ( $1/f_{FCLK}$ )	$t_{FcyC}$	5	—	6.67	$\mu$ s
5	—	Byte program time (random location) <sup>2</sup>	$t_{prog}$	9			$t_{FcyC}$
6	—	Byte program time (burst mode) <sup>2</sup>	$t_{Burst}$	4			$t_{FcyC}$
7	—	Page erase time <sup>2</sup>	$t_{Page}$	4000			$t_{FcyC}$
8	—	Mass erase time <sup>2</sup>	$t_{Mass}$	20,000			$t_{FcyC}$
9	C	Program/erase endurance <sup>3</sup> $T_L$ to $T_H = -40^\circ\text{C}$ to $+125^\circ\text{C}$ $T = 25^\circ\text{C}$	$n_{FLPE}$	10,000 —	— 100,000	— —	cycles
10	C	Data retention <sup>4</sup>	$t_{D\_ret}$	15	100	—	years

<sup>1</sup> The frequency of this clock is controlled by a software setting.

<sup>2</sup> These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

<sup>3</sup> Typical endurance for FLASH is based on the intrinsic bit cell performance. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619/D, Typical Endurance for Nonvolatile Memory.

<sup>4</sup> Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to  $25^\circ\text{C}$  using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618/D, Typical Data Retention for Nonvolatile Memory.

### 3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

#### 3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

**Table 3-15. Radiated Emissions, Electric Field**

Parameter	Symbol	Conditions	Frequency	$f_{osc}/f_{BUS}$	Level <sup>1</sup> (Max)	Unit	
Radiated emissions, electric field	$V_{RE\_TEM}$	$V_{DD} = 5\text{ V}$ $T_A = +25^\circ\text{C}$ package type 16-TSSOP	0.15 – 50 MHz	4 MHz crystal 8 MHz bus	-7	dB $\mu$ V	
			50 – 150 MHz		-11		
			150 – 500 MHz		-11		
			500 – 1000 MHz		-10		
			IEC Level		N		—
			SAE Level		1		—

<sup>1</sup> Data based on qualification test results.



# Chapter 4

## Ordering Information and Mechanical Drawings

### 4.1 Ordering Information

This section contains ordering information for MC9S08SC4 device.

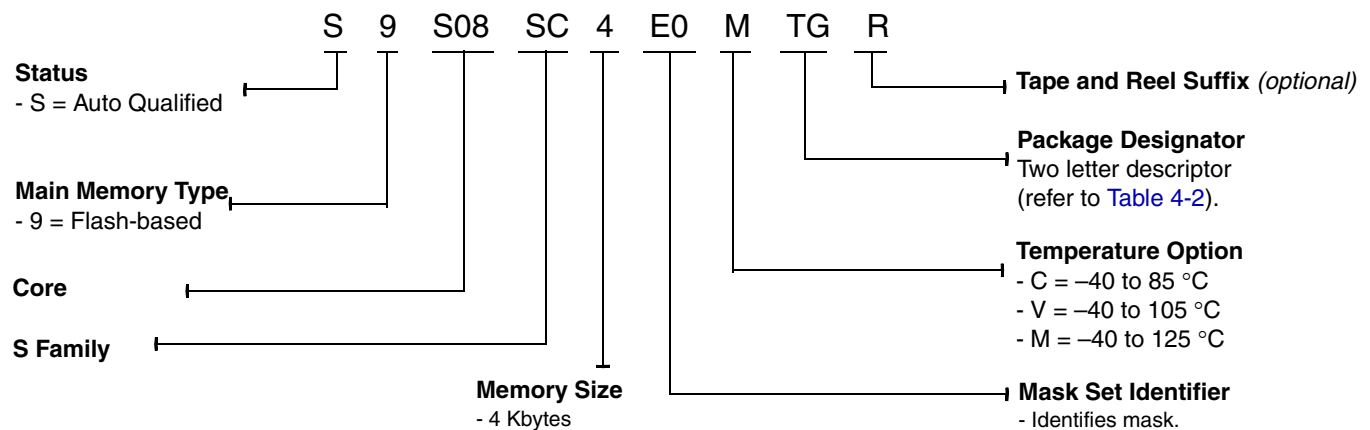
**Table 4-1. Device Numbering System**

Device Number <sup>1</sup>	Memory		Available Packages <sup>2</sup>
	FLASH	RAM	
S9S08SC4E0MTG	4K	256	16 TSSOP

<sup>1</sup> See MC9S08SC4 Reference Manual for a complete description of modules included on each device.

<sup>2</sup> See [Table 4-2](#) for package information.

#### 4.1.1 Device Numbering Scheme



### 4.2 Package Information

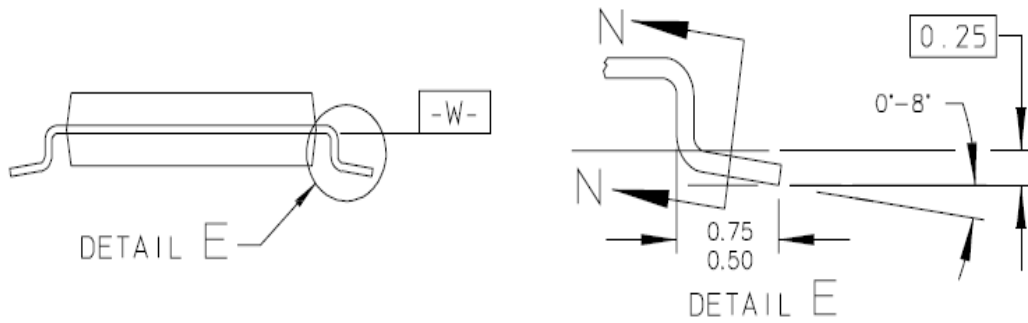
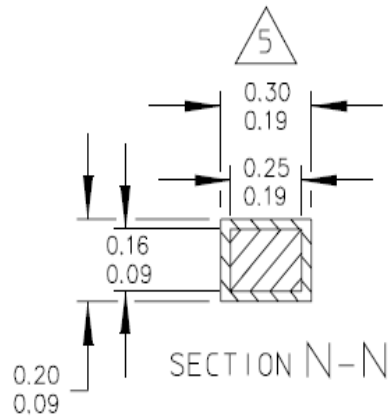
**Table 4-2. Package Information**

Pin Count	Type	Designator	Case Number	Document No.
16	TSSOP	TG	948F-01	98ASH70247A

### 4.3 Mechanical Drawings

The following pages are mechanical drawings for the package described in [Table 4-2](#).





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TITLE:  16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B	
	CASE NUMBER: 948F-01	19 MAY 2005	
	STANDARD: JEDEC		

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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	CASE NUMBER: 948F-01	19 MAY 2005	
	STANDARD: JEDEC		

# Chapter 5

## Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:  
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The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	9/2008	<ul style="list-style-type: none"> <li>Initial Release.</li> </ul>
2	7/2009	<ul style="list-style-type: none"> <li>Incorporated editing updates.</li> <li>Added C and V temperature ranges at page 1.</li> <li>Updated Section 3.10, "ADC Characteristics".</li> <li>Updated Table 3-3, Table 3-6, Table 3-7, Table 3-9, Table 3-12, Table 3-15 and Section 4.1.1, "Device Numbering Scheme".</li> <li>Added actual package mechanical drawings.</li> <li>Updated Figure 3-5, Figure 3-6.</li> <li>Removed Transient Susceptibility Section.</li> <li>Updated disclaimer page.</li> </ul>
3	3/2010	<ul style="list-style-type: none"> <li>Updated TSSOP-16 package diagram, clarified ICS deviation, SCI LIN features at page 1.</li> <li>Updated Table 3-6, Table 3-7, Table 3-9, Table 3-12, Table 4-1.</li> <li>Updated Figure 3-5 and Figure 3-7.</li> </ul>
4	6/2010	<ul style="list-style-type: none"> <li>Document changed from Advance Information to Technical Data</li> <li>Updated footnotes in Table 3-7</li> <li>Updated Figure 3-5</li> </ul>



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