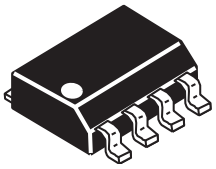
Document Number: MC33399
Rev. 10.0, 4/2013

Local Interconnect Network (LIN) Physical Interface

33399

LIN PHYSICAL INTERFACE



EF SUFFIX (PB-FREE)
98ASB42564B
8 PIN SOICN

Local interconnect network (LIN) is a serial communication protocol designed to support automotive networks in conjunction with controller area network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required. This device is powered by SMARTMOS technology.

The 33399 is a physical layer component dedicated to automotive sub-bus applications. It offers communication speed from 1.0 kbps to 20 kbps, and up to 60 kbps for programming mode. It has two operating modes: Normal and Sleep.

The 33399 supports LIN protocol specification 1.3.

Features

- Nominal operation from V_{SUP} 7.0 to 18 V DC, functional up to 27 V DC battery voltage and capable of handling 40 V during load dump
- Active bus waveshaping to minimize radiated emission
- ±5.0 kV ESD on LIN Bus Pin, ±4.0 kV ESD on other pins
- 30 kΩ internal pull-up resistor
- Ground shift operation and ground disconnection Fail-safe at module level
- An unpowered node does not disturb the network
- 20 µA in Sleep mode
- Wake-up capability from LIN Bus, MCU command and dedicated high voltage wake-up input (interface to external switch)
- Interface to MCU with CMOS compatible I/O pins
- Control of external voltage regulator

ORDERING INFORMATION		
Device (Add R2 Suffix for Tape and Reel)	**Temperature Range (T_A)**	**Package**
MC33399PEF	-40 to 125 °C	8 SOICN

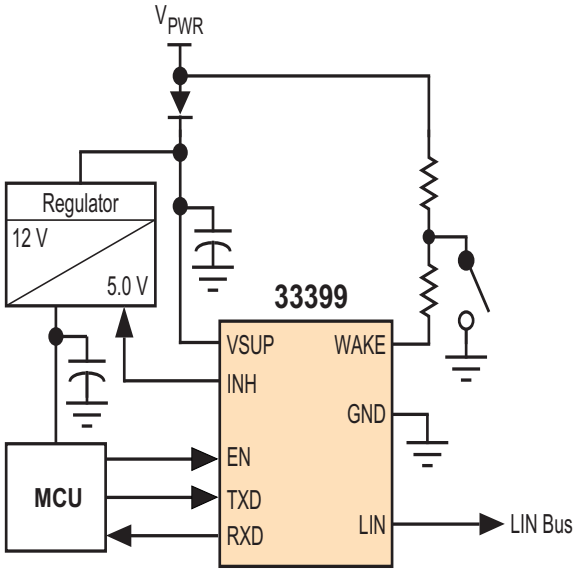


Figure 1. 33399 Simplified Application Diagram

INTERNAL BLOCK DIAGRAM

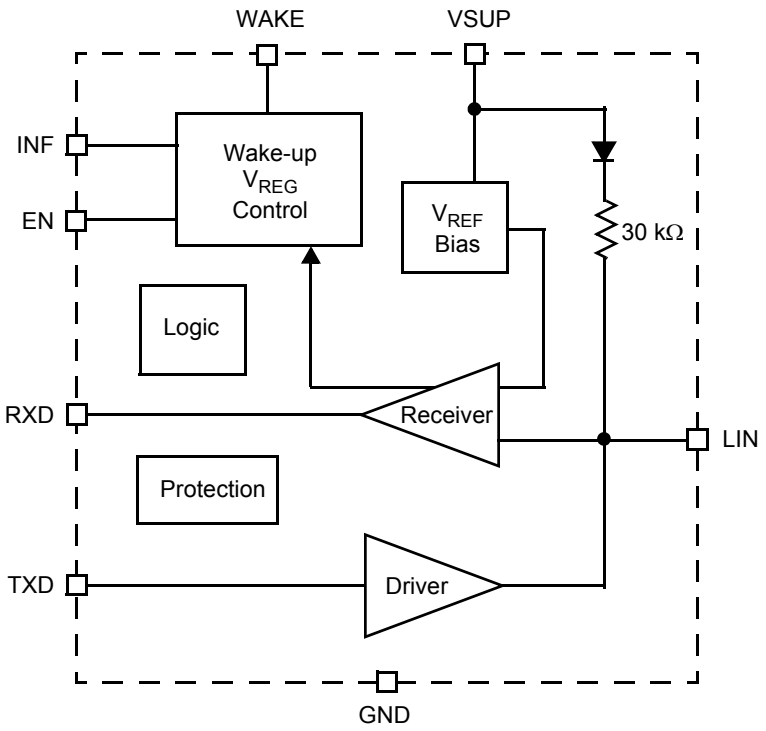


Figure 2. 33399 Simplified Internal Block Diagram

PIN CONNECTIONS

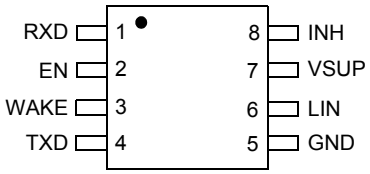


Figure 3. 33399 8-SOICN Pin Connections

Table 1. 8-SOICN Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 10.

Pin	Pin Name	Formal Name	Definition
1	RXD	Data Output	MCU interface that reports the state of the LIN bus voltage.
2	EN	Enable Control	Controls the operation mode of the interface.
3	WAKE	Wake Input	High voltage input used to wake up the device from the Sleep mode.
4	TXD	Data Input	MCU interface that controls the state of the LIN output.
5	GND	Ground	Device ground pin.
6	LIN	LIN Bus	Bidirectional pin that represents the single-wire bus transmitter and receiver.
7	VSUP	Power Supply	Device power supply pin.
8	INH	Inhibit Output	Controls an external switchable voltage regulator having an inhibit input.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage Continuous Supply Voltage Transient Voltage (Load Dump)	V_{SUP}	 27 40	V
WAKE DC and Transient Voltage (Through a 33 kΩ Serial Resistor)	V_{WAKE}	-18 to 40	V
Logic Voltage (RXD, TXD, EN Pins)	V_{LOG}	-0.3 to 5.5	V
LIN Pin DC Voltage Transient (Coupled Through 1.0 nF Capacitor)	V_{BUS}	 -18 to 40 -150 to 100	V
INH Voltage/Current DC Voltage	V_{INH}	-0.3 to V_{SUP} + 0.3	V
ESD Voltage, Human Body Model (1) All Pins LIN Bus Pin with Respect to Ground	V_{ESD1}	 ±4000 ±5000	V
ESD Voltage, Machine Model All Pins	V_{ESD2}	 ±200	V
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	150	°C/W
Peak Package Reflow Temperature During Reflow (2), (3)	T_{PPRT}	Note 3.	°C
Thermal Shutdown	T_{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis	T_{HYST}	8.0 to 20	°C

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 220 pF, R_{ZAP} = 0 Ω).
2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSUP PIN (DEVICE POWER SUPPLY)					
Supply Voltage Range	V_{SUP}	7.0	13.5	18	V
Supply Current in Sleep Mode V_{LIN} > V_{SUP} -0.5 V, V_{SUP} < 14 V 14 V < V_{SUP} < 18 V	 I_{S1} I_{S2}	 — —	 20 —	 50 150	µA
Supply Current in Normal Mode Recessive State Dominant State, Total Bus Load > 500 Ω	 $I_{S(REC)}$ $I_{S(DOM)}$	 — —	 — —	 2.0 3.0	mA
Supply Undervoltage Threshold	V_{SUP_UV}	5.5	6.4	6.8	V
RXD OUTPUT PIN (LOGIC)					
Low-Level Output Voltage I_{IN} ≤ 1.5 mA	V_{OL}	0.0	—	0.9	V
High-Level Output Voltage I_{OUT} ≤ 250 µA	V_{OH}	3.75	—	5.25	V
TXD INPUT PIN (LOGIC)					
Low-Level Input Voltage	V_{IL}	—	—	1.5	V
High-Level Input Voltage	V_{IH}	3.5	—	—	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	550	800	mV
Pullup Current Source 1.0 V < V_{TXD} < 4.0 V, V_{EN} = 5.0 V	I_{PU}	-50	—	-25	µA
EN INPUT PIN (LOGIC)					
Low-Level Input Voltage	V_{IL}	—	—	1.5	V
High-Level Input Voltage	V_{IH}	3.5	—	—	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	480	800	mV
EN Low-Level Input Current V_{IN} = 1.0 V	I_{IL}	5.0	20	30	µA
High-Level Input Current V_{IN} = 4.0 V	I_{IH}	—	20	40	µA
Pulldown Current 1.0 V < EN < 4.0 V	I_{PD}	—	20	—	µA

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PIN (VOLTAGE EXPRESSED VERSUS VSUP VOLTAGE)					
Low Level Bus Voltage (Dominant State) TXD LOW, V_{LIN} = 40 mA	V_{DOM}	 0.0	 —	 1.4	V
High Level Voltage (Recessive State) TXD HIGH, I_{OUT} = 1.0 µA	V_{REC}	 0.85 V_{SUP}	 —	 —	V
Internal Pullup Resistor to VSUP (4) -40 °C ≤ T_A ≤ 70 °C 70 °C < T_A ≤ 125 °C	R_{PU}	 20 35	 30 49	 47 60	kΩ
Current Limitation TXD LOW, V_{LIN} = V_{SUP}	I_{LIM}	 50	 150	 200	mA
Leakage Current to GND Recessive State, V_{SUP} - 0.3 V ≤ V_{LIN} ≤ V_{SUP} (4) V_{SUP} Disconnected, -18 V ≤ V_{LIN} ≤ 18 V (Excluding Internal Pull-up Source) V_{SUP} Disconnected, V_{LIN} = -18 V (Including Internal Pull-up Source) V_{SUP} Disconnected, V_{LIN} = +18 V (Including Internal Pull-up Source)	I_{LEAK}	 0.0 -40 — —	 — — -600 15	 10 40 — —	µA
LIN Receiver, Low Level Input Voltage TXD HIGH, RXD LOW	V_{LINL}	 0 V_{SUP}	 —	 0.4 V_{SUP}	V
LIN Receiver, High Level Input Voltage TXD HIGH, RXD HIGH	V_{LINH}	 0.6 V_{SUP}	 —	 V_{SUP}	V
LIN Receiver Threshold Center (V_{LINH} - V_{LINL}) / 2	V_{LINTH}	 —	 V_{SUP}/2	 —	V
LIN Receiver Input Voltage Hysteresis V_{LINH} - V_{LINL}	V_{LINHYS}	 0.05 V_{SUP}	 —	 0.15 V_{SUP}	V
LIN Wake-up Threshold Voltage	V_{LINWU}	3.5	4.5	6.0	V
INH OUTPUT PIN					
High Level Voltage (Normal Mode)	V_{WUH}	V_{SUP} -0.8	—	V_{SUP}	V
Leakage Current (Sleep Mode) 0 < V_{INH} < V_{SUP}	I_{LEAK}	 0.0	 —	 5.0	µA
WAKE INPUT PIN					
Typical Wake-Up Threshold (EN = 0 V, 7.0 V ≤ V_{SUP} ≤ 18 V) (5) HIGH-to-LOW Transition LOW-to-HIGH Transition	V_{WUTH}	 0.3 V_{SUP} 0.4 V_{SUP}	 0.43 V_{SUP} 0.55 V_{SUP}	 0.55 V_{SUP} 0.65 V_{SUP}	V
Wake-up Threshold Hysteresis	V_{WUHYS}	0.1 V_{SUP}	0.16 V_{SUP}	0.2 V_{SUP}	V
WAKE Input Current V_{WAKE} ≤ 14 V V_{WAKE} > 14 V	I_{WU}	 — —	 1.0 —	 5.0 100	µA

Notes
4. A diode structure is inserted with the pullup resistor to avoid parasitic current path from LIN to VSUP.
5. When V_{SUP} is greater than 18 V, the wake-up voltage thresholds remain identical to the wake-up thresholds at 18 V.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING					
LIN Slew Rate (6), (7)					V/µs
Falling Edge	t_{FALL}	0.75	2.0	3.0	
Rising Edge	t_{RISE}	0.75	2.0	3.0	
LIN Rise/Fall Symmetry (t_{RISE}-t_{FALL})	t_{SYM}	-2.0	—	2.0	µs
Driver Propagation Delay (8), (9)					µs
TXD LOW-to-LIN LOW	$t_{TXDLINL}$	0.0	—	4.0	
TXD HIGH-to-LIN HIGH	$t_{TXDLINH}$	0.0	—	4.0	
Receiver Propagation Delay (9), (10)					µs
LIN LOW to RXD LOW	$t_{RXDLINL}$	2.0	4.0	6.0	
LIN HIGH to RXD HIGH	$t_{RXDLINH}$	2.0	4.0	6.0	
Receiver Propagation Delay Symmetry	t_{RECSYM}	-2.0	—	2.0	µs
Transmitter Propagation Delay Symmetry	t_{TRSYM}	-2.0	—	2.0	µs
Propagation Delay (11)	t_{PROPWL}				µs
LIN Bus Wake-up to INH HIGH		45	70	130	

Notess

6. Measured between 20 and 80 percent of bus signal for 10 V < V_{SUP} < 18 V. Between 30 and 70 percent of signal for 7.0 V < V_{SUP} < 10 V.
7. See Figure 5, page 8.
8. $t_{TXDLINL}$ is measured from TXD (HIGH-to-LOW) and LIN (V_{REC} -0.2 V). $t_{TXDLINH}$ is measured from TXD (LOW-to-HIGH) and LIN (V_{DOM} + 0.2 V).
9. See Figure 4, page 8.
10. Measured between LIN receiver thresholds and RXD pin.
11. See Figure 6, page 8.

TIMING DIAGRAMS

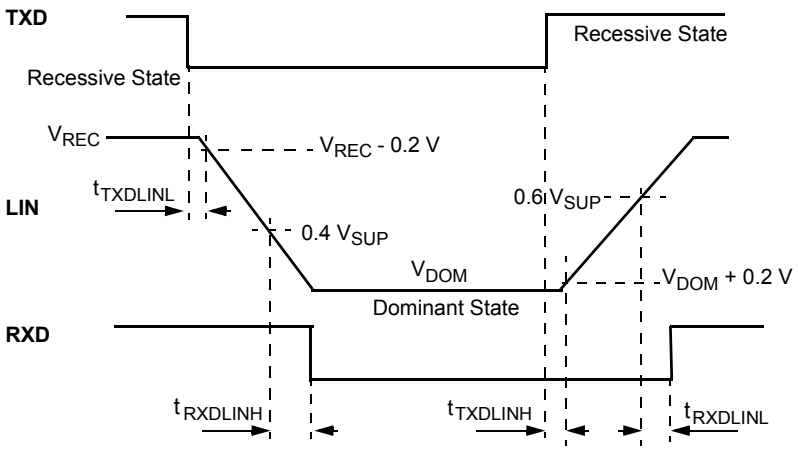


Figure 4. Normal Mode Bus Timing Characteristics

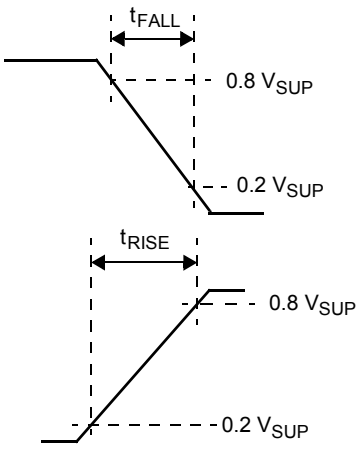


Figure 5. LIN Rise and Fall Time

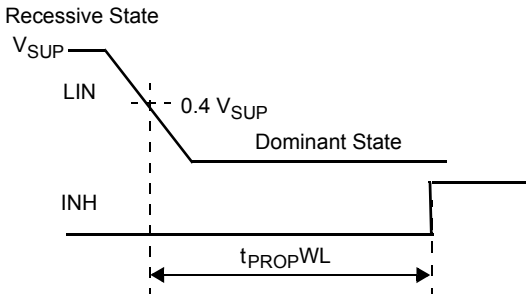


Figure 6. LIN Bus Wake-up

FUNCTIONAL DIAGRAMS

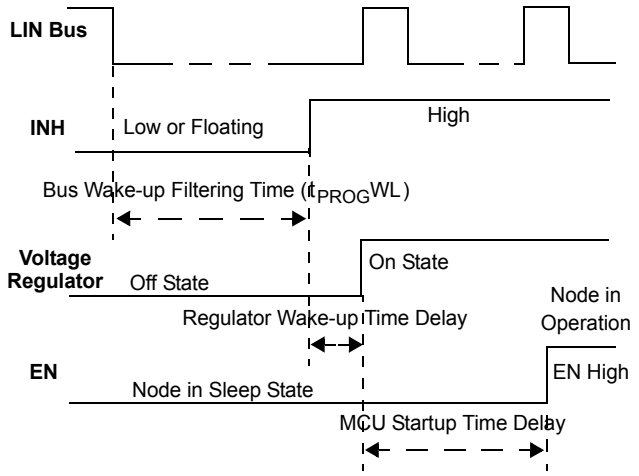


Figure 7. LIN Wake-up with INH Option

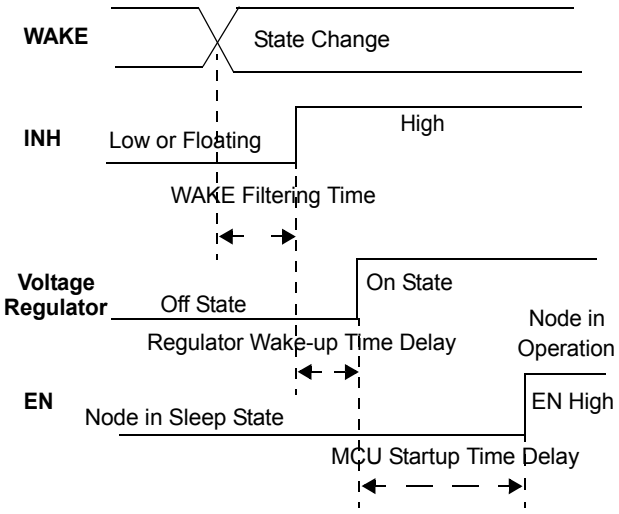


Figure 8. LIN Wake-Up from Wake-up Switch

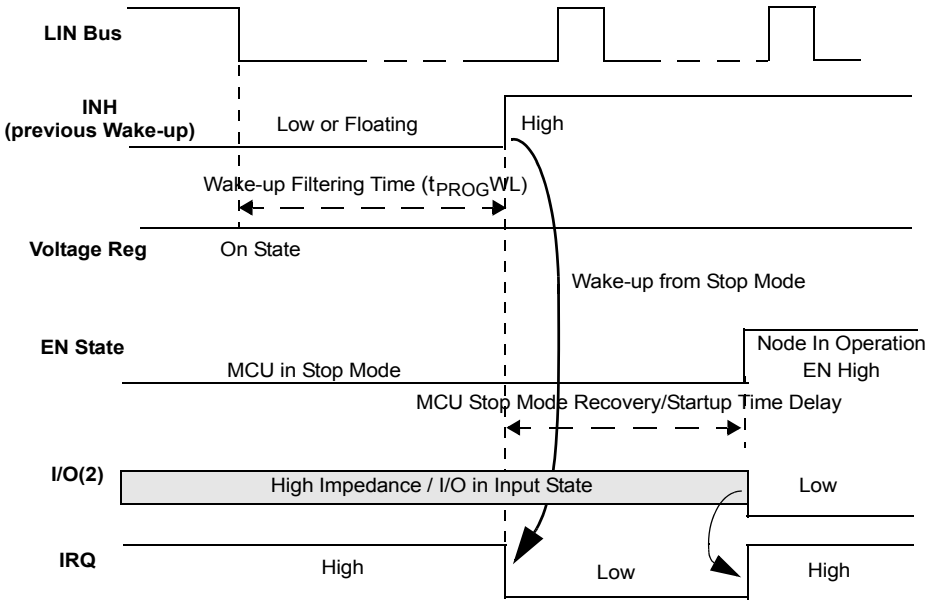


Figure 9. LIN Wake-up with MCU in Stop Mode

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33399 is a Physical Layer component dedicated to automotive LIN sub-bus applications.

The 33399 features include speed communication from 1.0 kbps to 20 kbps, up to 60 kbps for Programming mode, and active bus waveshaping to minimize radiated emission.

The device offers three different wake-up capabilities: wake-up from LIN bus, wake-up from the MCU command, and dedicated high voltage wake-up input.

The INH output may be used to control an external voltage regulator.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP power supply pin is connected to a battery through a serial diode for reverse battery protection. The DC operating voltage is from 7.0 to 27 V. This pin sustains standard automotive voltage conditions such as 27 V DC during jump-start conditions and 40 V during load dump. To avoid a false bus message, an undervoltage reset circuitry disables the transmission path (from TXD to LIN) when V_{SUP} falls below 7.0 V. Supply current in the Sleep mode is typically 20 μA.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33399 does not have significant current consumption on the LIN bus pin when in the recessive state. (Less than 100 μA is sourced from LIN bus pin, which creates 100 mV drop voltage from the 1.0 kΩ LIN bus pull-up resistor.) For the dominant state, the pull-up resistor should always be active.

The 33399 handles a ground shift up to 3.0 V when V_{SUP} > 9.0 V. Below 9.0 V V_{SUP}, a ground shift can reduce V_{SUP} value below the minimum V_{SUP} operation of 7.0 V.

LIN BUS PIN (LIN)

The LIN bus pin represents the single-wire bus transmitter and receiver.

Transmitter Characteristics

The LIN driver is a low side MOSFET with internal current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the master node.

Voltage can go from -18 to 40 V without current other than the pull-up resistance. The LIN pin exhibits no reverse current from the LIN bus line to VSUP, even in the event of GND shift or V_{PWR} disconnection. LIN thresholds are compatible with the LIN protocol specification.

The fall time from recessive to dominant and the rise time from dominant to recessive are controlled to typically 2.0 V/μs. The symmetry between rise and fall time is also guaranteed.

When going from dominant to recessive, the bus impedance parasitic capacitor must be charged up to V_{SUP}. This charge-up is achieved by the total system pull-up current resistors. In order to guarantee that the rise time is within specification, maximum bus capacitance should not exceed 10 nF with bus total pull-up resistance less than 1.0 kΩ.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin. Typical threshold is 50%, with a hysteresis between 5% and 10% of V_{SUP}.

DATA INPUT PIN (TXD)

The TXD input pin is the MCU interface that controls the state of the LIN output. When TXD is LOW, LIN output is LOW; when TXD is HIGH, the LIN output transistor is turned OFF.

This pin has an internal 5.0 V internal pull-up current source to set the bus in a recessive state in case the MCU is not able to control it; for instance, during system power-up/power-down. During the Sleep mode, the pull-up current source is turned OFF.

DATA OUTPUT PIN (RXD)

The RXD output pin is the MCU interface that reports the state of the LIN bus voltage. LIN HIGH (recessive) is reported by a high level on RXD; LIN LOW (dominant) is reported by a low voltage on RXD. RXD output structure is a CMOS-type push-pull output stage.

ENABLE INPUT PIN (EN)

The EN pin controls the operation mode of the interface. If EN = logic [1], the interface is in normal mode, with the transmission path from TXD to LIN and from LIN to RXD both active. If EN = logic [0], the device is in Sleep mode or low power mode, and no transmission is possible.

In Sleep mode, the LIN bus pin is held at V_{SUP} through the bus pull-up resistors and pull-up current sources. The device can transmit only after being awakened. Refer to the INHIBIT OUTPUT PIN (INH) description on page 11.

During Sleep mode, the device is still supplied from the battery voltage (through VSUP pin). Supply current is 20 μA typical. Setting the EN pin to LOW will turn the INH to high-impedance. The EN pin has an internal 20 μA pull-down current source to ensure the device is in Sleep mode if EN floats.

INHIBIT OUTPUT PIN (INH)

The INH pin controls an external switchable voltage regulator having an inhibit input. This pin is a high side switch structure to V_{SUP}. When the device is in the Normal mode, the inhibit high side switch is turned ON and the external voltage regulator is activated. When the device is in Sleep mode, the inhibit switch is turned OFF and disables the voltage regulator (if this feature is used).

A wake-up event on the LIN bus line will switch the INH pin to V_{SUP} level. Wake-up output current capability is limited to 280 µA. INH can also drive an external MOSFET connected to an MCU IRQ or XIRQ input to generate an interrupt. See the typical application illustrated in Figure 13, page 15.

WAKE INPUT PIN (WAKE)

The WAKE pin is a high voltage input used to wake up the device from Sleep mode. WAKE is usually connected to an external switch in the application. The typical WAKE thresholds are $V_{SUP}/2$.

The WAKE pin has a special design structure and allows wake-up from both HIGH-to-LOW or LOW-to-HIGH transitions. When entering the Sleep mode, the LIN monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to re-enter Normal mode.

An internal filter is implemented (50 µs typical filtering time delay). The WAKE pin input structure exhibits a high impedance with extremely low input current when voltage at this pin is below 14 V. When voltage at the WAKE pin exceeds 14 V, input current starts to sink into the device. A series resistor should be inserted in order to limit the input current, mainly during transient pulses. Recommended resistor value is 33 kΩ.

Important The WAKE pin should *not* be left open. If the wake-up function is not used, WAKE should be connected to GND to avoid false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described below and depicted in Figure 10 and Table 5 on page 13, the 33399 has two operational modes, normal and sleep, and one transitional mode, Awake.

NORMAL MODE

This is the normal transmitting and receiving mode. All features are available.

SLEEP MODE

In this mode the transmission path is disabled and the device is in low power mode. Supply current from VSUP is 20 µA typical. Wake-up can occur from LIN bus activity, as well as from node internal wake-up through the EN pin and the WAKE input pin.

DEVICE POWER-UP (AWAKE TRANSITIONAL MODE)

At system power-up (V_{SUP} rises from zero), the 33399 automatically switches into the "Awake" mode (refer to Figure 10 below and Table 5 on page 13. It switches the INH pin in HIGH state to V_{SUP} level. The microcontroller of the application then confirms the Normal mode by setting the EN pin HIGH.

DEVICE WAKE-UP EVENTS

The device can be awakened from Sleep mode by three wake-up events:

- LIN bus activity
- Internal node wake-up (EN pin)
- Wake-up from WAKE pin

Figures 7, 8, and 9 on page 9 show device application circuit and detail of wake-up operations.

Wake-up from LIN Bus (Awake Transitional Mode)

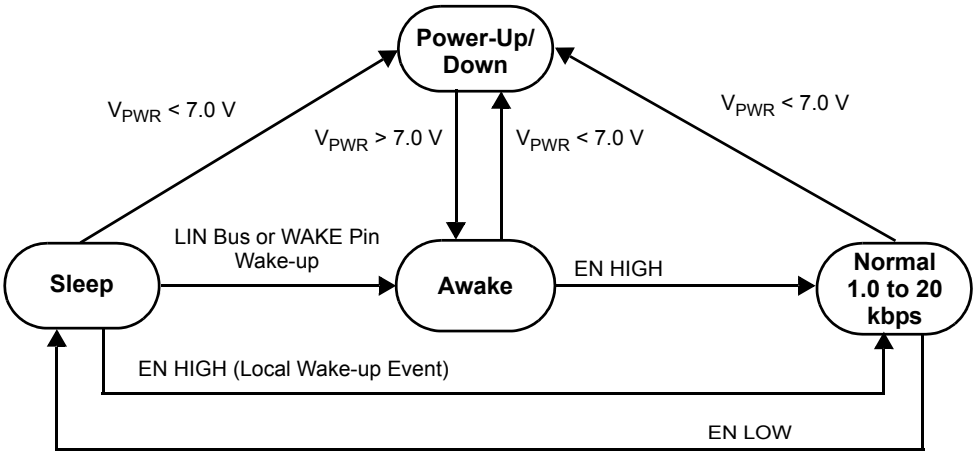
A wake-up from the LIN pin switching from recessive to dominant state (switch from VSUP to GND) can occur. This is achieved by a node sending a wake-up frame on the bus. This condition internally wakes up the interface, which switches the INH pin to a HIGH level to enable the voltage regulator. The device switches into the Awake mode. The microcontroller and the complete application power up. The microcontroller must switch the EN pin to a HIGH level to allow the device to leave the Awake mode and turn it into Normal mode in order to allow communication on the bus.

Wake-up from Internal Node Activity (Normal Mode)

The application can internally wake-up. In this case, the microcontroller of the application sets the EN pin in the HIGH state. The device switches into Normal mode.

Wake-up from WAKE Pin (Awake Transitional Mode)

The application can wake up with the activation of an external switch. Refer to Table 1, 8-SOICN Pin Definitions on page 3.



Note Refer to Table 5 for explanation.

Figure 10. Operational and Transitional Modes State Diagram

Table 5. Explanation of Operational and Transitional Modes State Diagram

Operational/ Transitional	LIN	INH	EN	TXD	RXD
Sleep Mode	Recessive state, driver off. 20 μA pull-up current source.	LOW	LOW	X	High-impedance.
Awake	Recessive state, driver off.	HIGH	LOW	X	LOW.
Normal Mode	Driver active. 30 kΩ pullup active.	HIGH	HIGH	LOW to drive LIN bus in dominant. HIGH to drive LIN bus in recessive.	Report LIN bus level: • LOW LIN bus dominant • HIGH LIN bus recessive

X = Don't care.

PROTECTION AND DIAGNOSIS FEATURES

ELECTROSTATIC DISCHARGE (ESD)

The 33399 has two Human Body Model ESD values. All pins can handle ±4.0 kV. The LIN bus pin, with respect to ground, can handle ±5.0 kV.

ELECTROMAGNETIC COMPATIBILITY

RADIATED EMISSION ON LIN BUS OUTPUT LINE

Radiated emission level on the LIN bus output line is internally limited and reduced by active slew rate control of the output bus driver. Figure 11 shows the results in the frequency range 100 kHz to 2.0 MHz.

ELECTROMAGNETIC IMMUNITY (EMI)

On the LIN bus pin, the 33399 offers high EMI level from external disturbance occurring at the LIN bus pin in order to guarantee communication during external disturbance.

On the WAKE input pin, an internal filter is implemented to reduce false wake-up during external disturbance.

NOISE FILTERING

Noise filtering is used to protect the electronic module against illegal wake-up spikes on the bus. Integrated receiver filters suppress any high-frequency (HF) noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression.

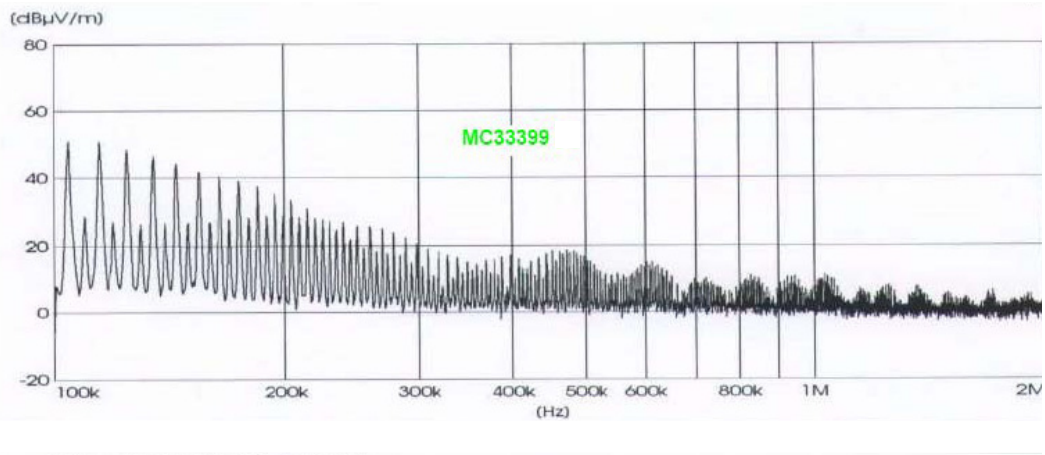


Figure 11. Radiated Emission in Normal Mode

TYPICAL APPLICATIONS

The 33399 can be configured in several applications. Figures 12 and 13 show slave and master node applications. An additional pull-up resistor of 1.0 kΩ in series with a diode must be added when the device is used in the master node.

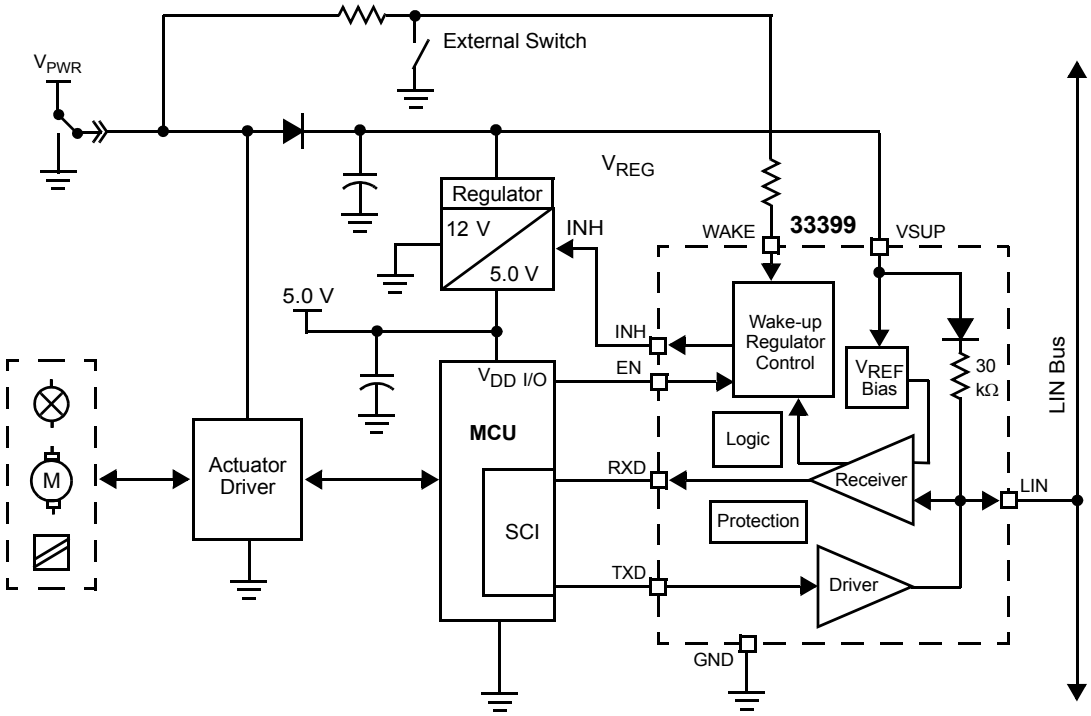


Figure 12. Slave Node Typical Application with WAKE Input Switch and INH (Switchable 5.0 V Regulator)

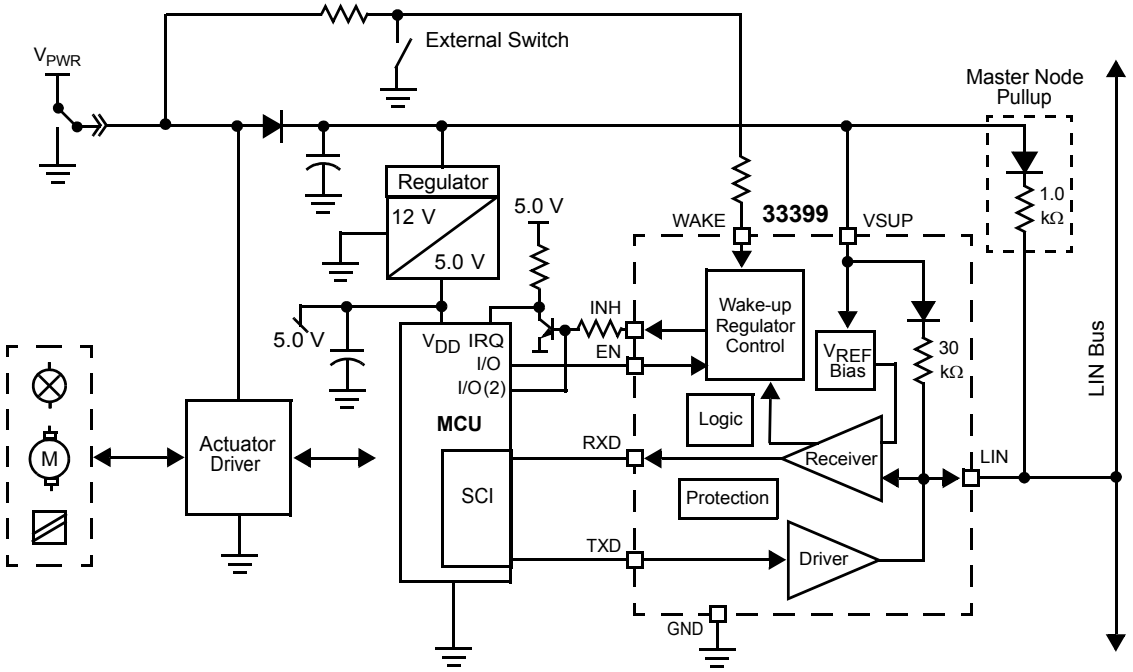


Figure 13. Master Node Typical Device Application with MCU Wake-Up from Stop Mode (Non-Switchable 5.0 V Regulator, MCU Stop Mode)

REFERENCE DOCUMENTS

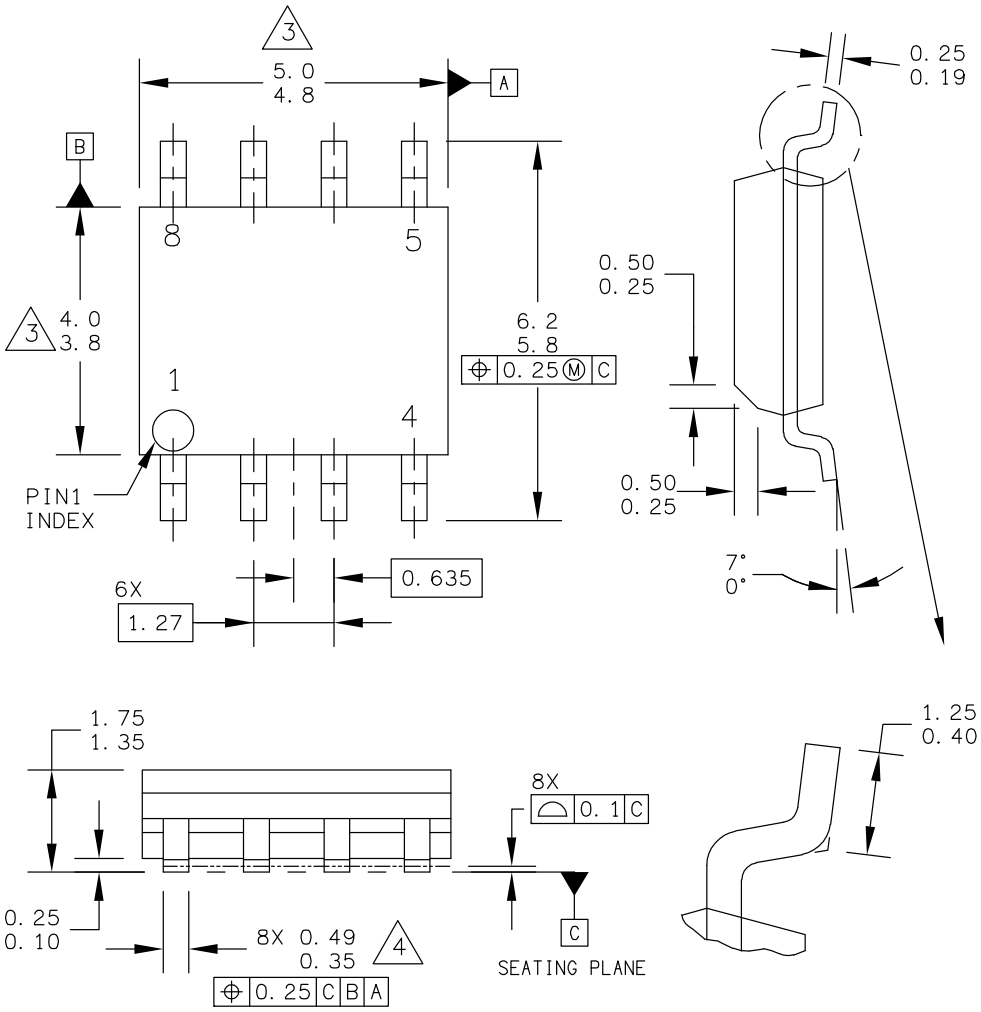
Table 6. Reference Documents

Title	LIterature Order Number
Local Interconnect Network (LIN) Physical Interface: Difference Between MC33399 and MC33661	EB215

PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98ASB42564B drawing number below. Dimensions shown are provided for reference ONLY.



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TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U
	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

EF SUFFIX (Pb-FREE)
8-PIN SOIC NARROW BODY
98ASB42564B
ISSUE U

33399

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	7/2006	• Implemented Revision History page • Added Pb-Free suffix code EF • Added EPP ordering part number MCZ33399EF/R2 • Adjusted to the Freescale prevailing form and style
8.0	10/2006	• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS on page 4. Added note with instructions to obtain this information from www.freescale.com.
9.0	6/2012	• Removed MC33399D from the ordering information. • Removed D Suffix • Updated orderable part number from MCZ33399EF to MC33399PEF. • Updated Freescale form and style
10.0	4/2013	• Change T_{STG} to -55 to 150 • No other technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.

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