LPC55S6x

32-bit Arm Cortex®-M33; M33 coprocessor

Rev. 2.5 — 29 August 2024 Data sheet

1 General description

The LPC55S6x is an ARM Cortex-M33 based microcontroller for embedded applications. These devices include an ARM Cortex-M33 coprocessor, CASPER Crypto/FFT engine, PowerQuad hardware accelerator for DSP functions, up to 320 KB of on-chip SRAM, up to 640 KB on-chip flash, PRINCE module for on-the-fly flash encryption/decryption, high-speed and full-speed USB host and device interface with crystal-less operation for full-speed, SD/MMC/SDIO interface, five general-purpose timers, one SCTimer/PWM, one RTC/alarm timer, one 24-bit Multi-Rate Timer (MRT), a Windowed Watchdog Timer (WWDT), nine flexible serial communication peripherals (which can be configured as a USART, SPI, high speed SPI, I^2C, or I^2S interface), Programmable Logic Unit (PLU), one 16-bit 1.0 Msamples/sec ADC capable of simultaneous conversions.

The ARM Cortex-M33 provides a security foundation, offering isolation to protect valuable IP and data with TrustZone® technology. It simplifies the design and software development of digital signal control systems with the integrated digital signal processing (DSP) instructions. To support security requirements, the LPC55S6x also offers support for secure boot, HASH, AES, RSA, UUID, DICE, dynamic encrypt and decrypt, debug authentication, and TBSA compliance.

2 Features and benefits

- ARM Cortex-M33 core (CPU0, r0p3):
  - Running at a frequency of up to 150 MHz (device revision 1B only).
  - TrustZone®, Floating Point Unit (FPU) and Memory Protection Unit (MPU).
  - ARM Cortex M33 built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with eight breakpoints and four watch points. Includes Serial Wire Output for enhanced debug capabilities.
  - System tick timer.
  - The configuration of this instance includes MPU, FPU, DSP, ETM, and Trustzone.
- ARM Cortex-M33 co-processor (CPU1, r0p3):
  - Running at a CPU frequency of up to 150 MHz (device revision 1B only).
  - The configuration of this instance does not include MPU, FPU, DSP, ETM, and Trustzone.
  - System tick timer.
- CASPER Crypto co-processor is provided to enable hardware acceleration for various functions required for certain asymmetric cryptographic algorithms, such as, Elliptic Curve Cryptography (ECC).
- PowerQuad hardware accelerator for (fixed and floating point unit) CMSIS DSP functions with support of SDK software API faster execution of ARM CMSIS instruction set.
- On-chip memory:
  - Up to 640 KB on-chip flash program memory with flash accelerator and 512 byte page erase and write.
  - Up to 320 KB total SRAM consisting of 32 KB SRAM on Code Bus, 272 KB SRAM on System Bus (272 KB is contiguous), and additional 16 KB USB SRAM on System Bus which can be used by the USB interface or for general purpose use.

- PRINCE module for real-time encryption of data being written to on-chip flash and decryption of encrypted flash data during read to allow asset protection, such as securing application code, and enabling secure flash update.
- On-chip ROM bootloader supports:
  - Booting of images from on-chip flash
  - Supports CRC32 image integrity checking.
  - Supports flash programming through In System Programming (ISP) commands over following interfaces: USB0/1 interfaces using HID Class device, UART interface (Flexcomm 0) with auto baud, SPI slave interfaces (Flexcomm 3 or 9) using mode 3 (CPOL = 1 and CPHA = 1), and I2C slave interface (Flexcomm 1)
  - ROM API functions: Flash programming API, Power control API, and Secure firmware update API using NXP Secure Boot file format, version 2.0 (SB2 files).
  - Supports booting of images from PRINCE encrypted flash regions.
  - Support NXP Debug Authentication Protocol version 1.0 (RSA-2048) and 1.1 (RSA-4096).
  - Supports setting a sealed part to Fault Analysis mode through Debug authentication.
- Secure Boot support:
  - Uses RSASSA-PKCS1-v1_5 signature of SHA256 digest as cryptographic signature verification.
  - Supports RSA-2048 bit public keys (2048 bit modulus, 32-bit exponent).
  - Supports RSA-4096 bit public keys (4096 bit modulus, 32-bit exponent).
  - Uses x509 certificate format to validate image public keys.
  - Supports up to four revocable Root of Trust (RoT) or Certificate Authority keys, Root of Trust establishment by storing the SHA-256 hash digest of the hashes of four RoT public keys in protected flash region (PFR).
  - Supports anti-rollback feature using image key revocation and supports up to 16 Image key certificates revocations using Serial Number field in x509 certificate.
  - Supports Device Identifier Composition Engine (DICE) Specification (version Family 2.0, Level 00 Revision 69) specified by Trusted Computing Group.
- Serial interfaces:
  - Flexcomm Interface contains up to nine serial peripherals (Flexcomm Interface 0-7 and Flexcomm Interface 8). Each Flexcomm Interface (except flexcomm 8, which is dedicated for high-speed SPI) can be selected by software to be a USART, SPI, I^2C, and I^2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I^2S. A variety of clocking options are available to each Flexcomm Interface, including a shared fractional baud-rate generator, and time-out feature.Flexcomm interfaces 0 to 7 each provide one channel pair of I^2S.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I^2C pads also support high-speed Mode (3.4 Mbit/s) as a slave.
  - USB 2.0 full speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library example in technical note (TN00063).
  - USB 2.0 high-speed host/device controller with on-chip high-speed PHY.
- Digital peripherals:
  - DMA0 controller with 23 channels and up to 22 programmable triggers, able to access all memories and DMA-capable peripherals.
  - DMA1 controller with 10 channels and up to 15 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Secured digital input/output (SD/MMC and SDIO) card interface with DMA support. SDIO with support for up to two cards. Supported card types are MMC, SDIO, and CE-ATA. Supports SD2.0, and SDR25 (52MHz).
  - CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
  - Up to 64 General-Purpose Input/Output (GPIO) pins.
  - GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.

- Up to eight GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- I/O pin configuration with support for up to 16 function options.
- Programmable Logic Unit (PLU) to create small combinatorial and/or sequential logic networks including state machines.

- Security Features:
  - ARM TrustZone® enabled.
  - AES-256 encryption/decryption engine with keys fed directly from PUF or a software supplied key
  - Secure Hash Algorithm (SHA2) module supports secure boot with dedicated DMA controller.
  - Physical Unclonable Function (PUF) using dedicated SRAM for silicon fingerprint. PUF can generate, store, and reconstruct key sizes from 64 to 4096 bits. Includes hardware for key extraction.
  - True Random Number Generator (TRNG).
  - 128 bit unique device serial number for identification (UUID).
  - Secure GPIO.
- Timers:
  - Five 32-bit standard general purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
  - One SCTimer/PWM with 8 input and 10 output functions (including 16 capture and match registers). Inputs and outputs can be routed to or from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 16 captures/matches, 16 events, and 32 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. Another timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution. The RTC is clocked by the 32 kHz FRO or 32.768 kHz external crystal.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT) with FRO 1 MHz as clock source.
  - The Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from sleep and deep-sleep modes. Includes 4 capture registers with pin inputs.
  - 42-bit free running OS Timer as continuous time-base for the system, available in any reduced power modes. It runs on 32kHz clock source, allowing a count period of more than 4 years.
- Analog peripherals:
  - 16-bit ADC with five differential channel pair (or 10 single-ended channels), and with multiple internal and external trigger inputs and sample rates of up to 1.0 MSamples/sec. The ADC supports simultaneous conversions, on two ADC input channels belonging to a differential pair.
  - Integrated temperature sensor connected to the ADC.
  - Comparator with five input pins and external or internal reference voltage.
- Clock generation:
  - Internal Free Running Oscillator (FRO). This oscillator provides a selectable 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to +/- 2% accuracy over the entire voltage and -40 C to 105 C. For devices with date code 2041 (yyww)and onwards, the FRO is trimmed to +/- 1% accuracy over the entire voltage and 0 C to 85 C.
  - 32 kHz Internal Free Running Oscillator FRO. The FRO is trimmed to +/- 2% accuracy over the entire voltage and temperature range.
  - Internal low power oscillator (FRO 1 MHz) trimmed to +/- 15% accuracy over the entire voltage and temperature range.

- Crystal oscillator with an operating frequency of 16 MHz to 32 MHz. Option for external clock input (bypass mode) for clock frequencies of up to 25 MHz.
- Crystal oscillator with 32.768 KHz operating frequency. Option for external clock input (bypass mode) for clock frequencies of up to 100 kHz.
- PLL0 and PLL1 allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. PLL0 and PLL1 can run from the internal FRO 12 MHz output, the external oscillator, internal FRO 1 MHz output, or the 32.768 KHz RTC oscillator.
- Clock output function with divider to monitor internal clocks.
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Each crystal oscillator has one embedded capacitor bank which can be used as an integrated load capacitor. Using APIs, the capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) which conserves board space and reduces costs.

- Power-saving modes and wake-up:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep, deep-sleep with RAM retention, power-down with RAM retention and CPU0 retention, and deep power-down with RAM retention.
  - Configurable wake-up options from peripherals interrupts.
  - The Micro-Tick Timer running from the watchdog oscillator, and the Real-Time Clock (RTC) running from the 32.768 kHz clock, can be used to wake-up the device from sleep and deep-sleep modes.
  - Power-On Reset (POR, around 0.8 V).
  - Brown-Out Detectors (BOD) for VBAT_DCDC for forced reset or interrupt.
- Operating from internal DC-DC converter.
- Single power supply 1.8 V to 3.6 V.
- JTAG boundary scan supported.
- Operating temperature range -40 °C to +105 °C.
- Available in HLQFP100, HTQFP64, VFBGA98, and VFBGA59 packages.

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC55S66JBD100	HLQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 0.5mm pitch	SOT1570-3
LPC55S69JBD100	HLQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 0.5mm pitch	SOT1570-3
LPC55S66JEV98	VFBGA98	thin fine-pitch ball grid array package; 98 balls; body 7‘ 7‘ 0.5 mm	SOT1982-1
LPC55S69JEV98	VFBGA98	thin fine-pitch ball grid array package; 98 balls; body 7‘ 7‘ 0.5 mm	SOT1982-1
LPC55S66JBD64	HTQFP64	plastic low profile quad flat package; 64 leads; body 10 x10 x 0.5mm pitch	SOT855-5
LPC55S69JBD64	HTQFP64	plastic low profile quad flat package; 64 leads; body 10 x10 x 0.5mm pitch	SOT855-5
LPC55S69JEV59	VFBGA59	Thin fine-pitch ball grid array package; 59 balls; body 4 × 4 × 0.4 mm pitch	SOT2162-1
LPC55S66JEV59	VFBGA59	Thin fine-pitch ball grid array package; 59 balls; body 4 × 4 × 0.4 mm pitch	SOT2162-1

3.1 Ordering options

Table 2. Ordering options

Type number	Max CPU Frequency (MHz)	Primary core (CPU0)	Secondary core (CPU1)	Power Quad	CASPER	Flash/KB	Total SRAM/KB	Secure boot	TrustZone	PRINCE	PUF Controller	HASH-AES	SDIO	USB	GPIO
LPC55S66JBD100	150 [1]	yes	yes	yes	yes	256	144	yes	yes	yes	yes	yes	yes	FS + HS	64
LPC55S69JBD100	150 [1]	yes	yes	yes	yes	640	320	yes	yes	yes	yes	yes	yes	FS + HS	64
LPC55S66JEV98	150 [1]	yes	yes	yes	yes	256	144	yes	yes	yes	yes	yes	yes	FS + HS	64
LPC55S69JEV98	150 [1]	yes	yes	yes	yes	640	320	yes	yes	yes	yes	yes	yes	FS + HS	64
LPC55S66JBD64	150 [1]	yes	yes	yes	yes	256	144	yes	yes	yes	yes	yes	yes	FS + HS	36
LPC55S69JBD64	150 [1]	yes	yes	yes	yes	640	320	yes	yes	yes	yes	yes	yes	FS + HS	36
LPC55S69JEV59	150 [1]	yes	yes	yes	yes	640	320	yes	yes	yes	yes	yes	yes	HS	37
LPC55S66JEV59	150 [1]	yes	yes	yes	yes	256	144	yes	yes	yes	yes	yes	yes	HS	37

[1] Device revision 1B operates at a maximum CPU frequency of up to 150 MHz. Device revision 0A operates at a maximum CPU frequency of up to 100 MHz.

4 Marking

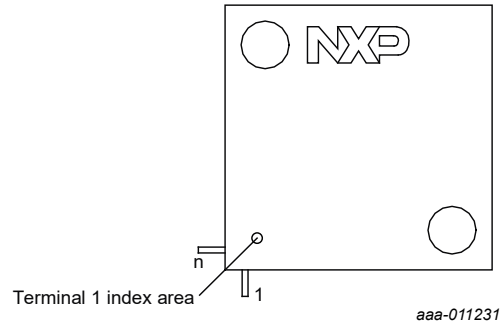


Figure 1. HLQFP100 package marking

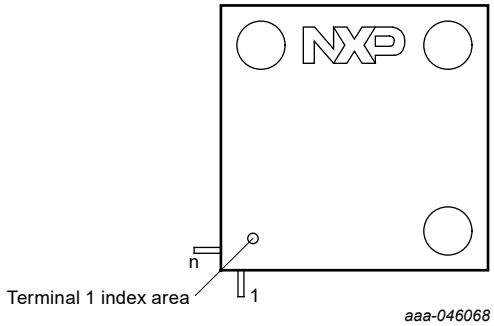


Figure 2. HTQFP64 package marking

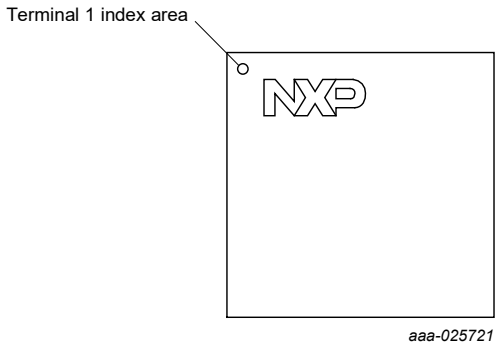


Figure 3. VFBGA98 package marking

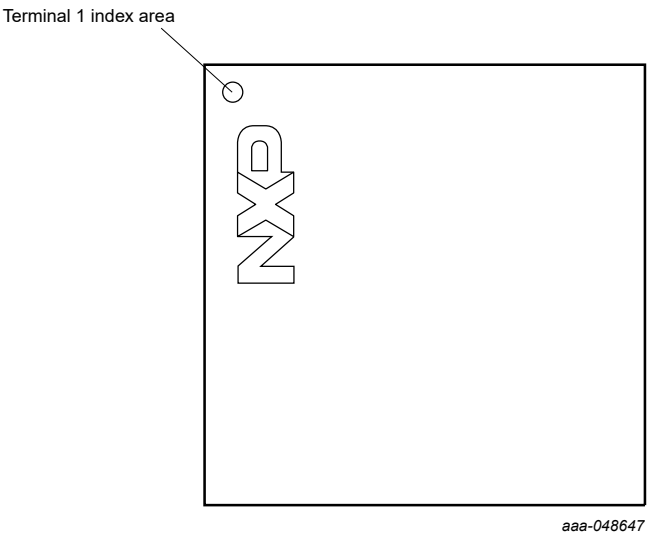


Figure 4. VFBGA59 package marking

The LPC55S6x HLQFP100 package has the following top-side marking:

- First line: LPC55S6xJBD100
- Second line: xxxxxxxx
- Third line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 0A or Device revision 1B

The LPC55S6x HTQFP64 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Fifth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S6x VFBGA98 package has the following top-side marking:

- First line: LPC55S6x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: zzzyywwxR
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S69 and LPC55S66 VFBGA59 package has the following top-side marking:

- First line: S69 or S66
- Second line: xxxx
- Third line: zzywwxR
  - yww: Date code with y = year and ww = week.
  - xR: Device revision 1B

5 Block diagram

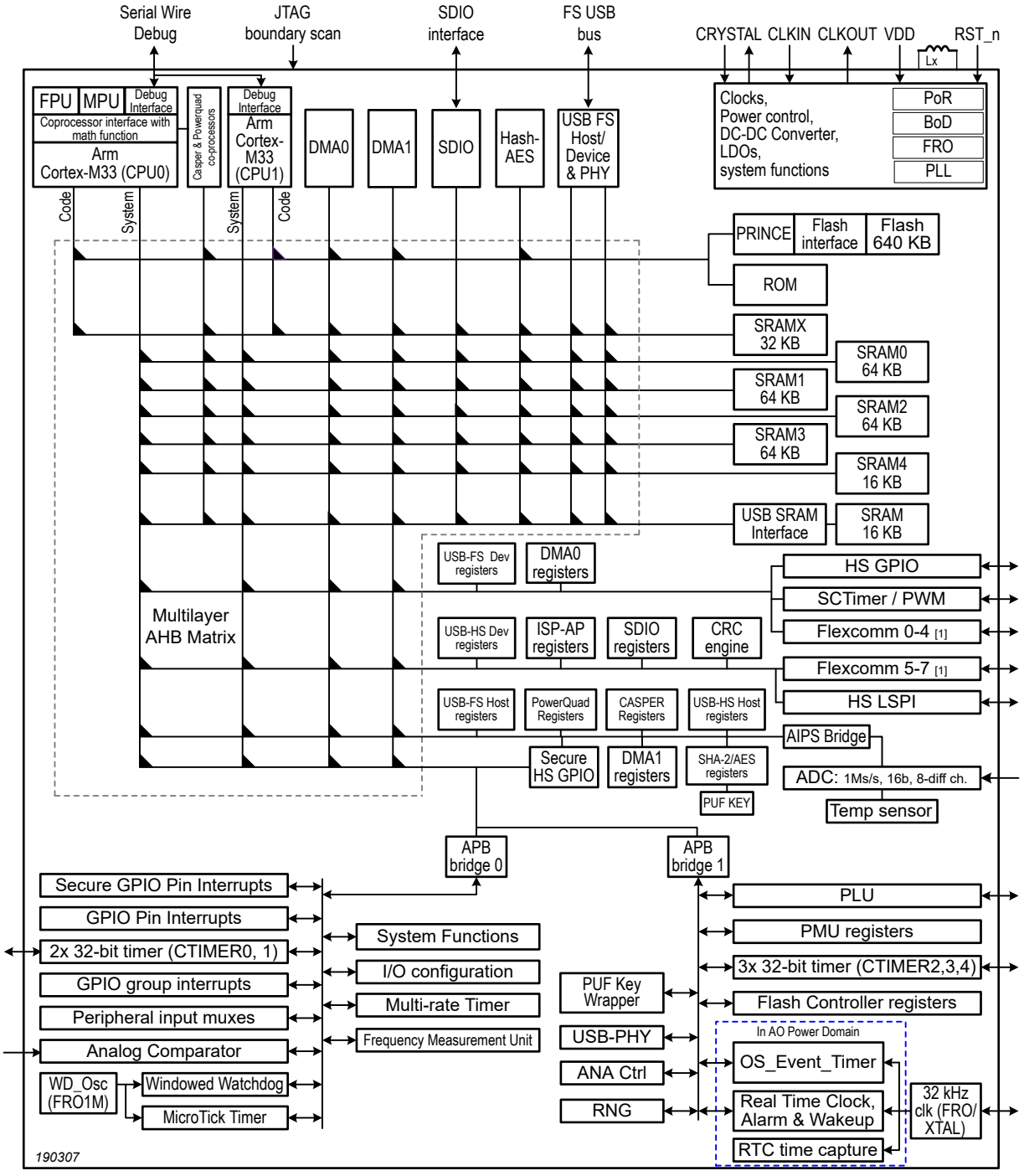


Figure 5. LPC55S6x Block diagram

6 Pinning information

6.1 Pin description

Table 4 shows the pin functions available on each pin, and for each package. These functions are selectable using the IOCON control registers.

Some functions, such as ADC or comparator inputs, are available only on specific pins when digital functions are disabled on those pins. By default, the GPIO function is selected except on pins PIO0_11 an PIO0_12, which are the serial wire debug pins. This allows debug to operate through reset.

All pins have all pull-ups, pull-downs, and inputs turned off at reset except PIO0_2, PIO0_5, PIO0_11, PIO0_12, PIO0_13 and PIO0_14 pins. This prevents power loss through pins prior to software configuration. Due to special pin functions, some pins have a different reset configuration. PIO0_5 and PIO0_12 pins have internal pull-up enabled by default, and PIO0_2 and PIO0_11 have internal pull-down enabled by default. PIO0_13 and PIO0_14 are true open drain pins. Refer to pin description table for default reset configuration.

The state of port pin PIO0_5 at Reset determines the boot source of the part or if the handler is invoked.

The external reset pin or 3 wake-up pins can trigger a wake-up from deep power-down mode. For the wake-up pins, do not assign any function to this pin if it will be used as a wake-up input when using deep power-down mode. If not in deep power-down mode, a function can be assigned to this pin. If the pin is used for wake-up, it should be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode wakes up the part.

The JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_2 to PIO0_6 by hardware when the part is in boundary scan mode. The JTAG functions cannot be used for debug mode.

Table 3. Pin description

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
PIO0_0/ ACMP0_A	J8	36	L12	54	[2]	Z	I/O; AI	0	**PIO0_0/ACMP0_A** General-purpose digital input/output pin. Comparator 0, input A if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin.
								1	**R** Reserved.
							I/O	2	**FC3_SCK** Flexcomm 3: USART, SPI, or I2S clock.
							O	3	**CTIMER0_MAT0** 32-bit CTimer0 match output 0.
							I	4	**SCT0_GPI0** Pin input 0 to SCTimer/PWM.
								5	**R** Reserved.
							I	6	**SD1_CARD_INT_N** SD/MMC 1 card interrupt.
								7	**R** Reserved.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_0** Secure GPIO pin.
PIO0_1	A1	2	F5	7	[3]	Z	I/O	0	**PIO0_1** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**FC3_CTS_SDA_SSEL0** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	3	**CTIMER_INP0** Capture input to CTIMER input muxes.
							I	4	**SCT0_GPI1** Pin input 1 to SCTimer/PWM.
								5	**R** Reserved.
							O	6	**SD1_CLK** SD/MMC 1 card clock.
							O	7	**CMP0_OUT** Analog comparator 0 output.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_1** Secure GPIO pin.
PIO0_2/ TRST	B7	52	B11	81	[3][4]	PD	I/O	0	**PIO0_2** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
							I/O	1	**FC3_TXD_SCL_MISO_WS** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	2	**CTIMER_INP1** Capture input to CTIMER input multiplexers.
							O	3	**SCT0_OUT0**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									SCTimer/PWM output 0.
							I	4	**SCT0_GPI2** Pin input 2 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_2** Secure GPIO pin.
PIO0_3/ TCK	B6	53	F8	83	[3][4]	Z	I/O	0	**PIO0_3** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
							I/O	1	**FC3_RXD_SDA_MOSI_DATA** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	2	**CTIMER0_MAT1** 32-bit CTimer0 match output 1.
							O	3	**SCT0_OUT1** SCTimer/PWM output 1.
							I	4	**SCT0_GPI3** Pin input 3 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_3** Secure GPIO pin.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
PIO0_4/ TMS	A6	55	E7	86	[3][4]	Z	I/O	0	**PIO0_4** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SSEL0 function.
								1	**R** Reserved.
							I/O	2	**FC4_SCK** Flexcomm 4: USART, SPI, or I2S clock.
							I	3	**CTIMER_INP12** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI4** Pin input 4 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
							I/O	8	**FC3_CTS_SDA_SSEL0** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_4** Secure GPIO pin.
PIO0_5/ TDI	C6	56	A7	88	[3][4]	PU	I/O	0	**PIO0_5** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset determines the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM11126 for more details.
								1	**R** Reserved.
							I/O	2	**FC4_RXD_SDA_MOSI_DATA** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	3	**CTIMER3_MAT0** 32-bit CTimer3 match output 0.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I	4	**SCT0_GPI5** Pin input 5 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
							I/O	8	**FC3_RTS_SCL_SSEL1** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	9	**MCLK** MCLK input or output for I2S.
							I/O	10	**SEC_PIO0_5** Secure GPIO pin.
PIO0_6/ TDO	C5	57	B7	89	[3][4]	Z	I/O	0	**PIO0_6** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
							I/O	1	**FC3_SCK** Flexcomm 3: USART, SPI, or I2S clock.
							I	2	**CTIMER_INP13** Capture input to CTIMER input multiplexers.
							O	3	**CTIMER4_MAT0** 32-bit CTimer4 match output 0.
							I	4	**SCT0_GPI6** Pin input 6 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_6** Secure GPIO pin.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
PIO0_7	A2	1	G5	6	[3]	Z	I/O	0	**PIO0_7** General-purpose digital input/output pin.
							I/O	1	**FC3_RTS_SCL_SSEL1** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							O	2	**SD0_CLK** SD/MMC 0 card clock.
							I/O	3	**FC5_SCK** Flexcomm 5: USART, SPI, or I2S clock.
							I/O	4	**FC1_SCK** Flexcomm 1: USART, SPI, or I2S clock.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_7** Secure GPIO pin.
PIO0_8	H1	17	M2	26	[3]	Z	I/O	0	**PIO0_8** General-purpose digital input/output pin.
							I/O	1	**FC3_SSEL3** Flexcomm 3: SPI slave select 3.
							I/O	2	**SD0_CMD** SD/MMC 0 card command I/O.
							I/O	3	**FC5_RXD_SDA_MOSI_DATA** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	4	**SWO** Serial Wire Debug trace output.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_8** Secure GPIO pin.
PIO0_9/ ACMP0_B	J9	37	L13	55	[2]	Z	I/O; AI	0	**PIO0_9/ACMP0_B** General-purpose digital input/output pin. Comparator 0, input B if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin.
							I/O	1	**FC3_SSEL2** Flexcomm 3: SPI slave select 2.
							O	2	**SD0_POW_EN** SD/MMC 0 card power enable.
							I/O	3	**FC5_TXD_SCL_MISO_WS** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
								4	**R** Reserved.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_9** Secure GPIO pin.
PIO0_10/ ADC0_1	F1	13	F2	21	[2]	Z	I/O; AI	0	**PIO0_10/ADC0_1** General-purpose digital input/output pin. ADC single ended input channel 1A - CH1A. Can optionally be paired with CH1B as the positive differential input on ADC1 channel 1.
							I/O	1	**FC6_SCK** Flexcomm 6: USART, SPI, or I2S clock.
							I	2	**CTIMER_INP10**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Capture input to CTIMER input multiplexers.
							O	3	**CTIMER2_MAT0** 32-bit CTimer2 match output 0.
							I/O	4	**FC1_TXD_SCL_MISO_WS** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	5	**SCT0_OUT2** SCTimer/PWM output 2.
							O	6	**SWO** Serial Wire Debug trace output.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_10** Secure GPIO pin.
PIO0_11/ ADC0_9	D2	6	F1	13	[2]	PD	I/O; AI	0	**PIO0_11/ADC0_9** General-purpose digital input/output pin. ADC single ended input channel 1B - CH1B. Can optionally be paired with CH1A as the negative differential input on ADC1 channel 1.
							I/O	1	**FC6_RXD_SDA_MOSI_DATA** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	2	**CTIMER2_MAT2** 32-bit CTimer2 match output 2.
							I	3	**FREQME_GPIO_CLK_A** Frequency Measure pin clock input A.
								4	**R** Reserved.
								5	**R** Reserved.
							I	6	**SWCLK** Serial Wire Debug clock. This is the default function after booting.
								7	**R** Reserved.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_11** Secure GPIO pin.
PIO0_12/ ADC0_10	C2	5	E2	12	[2]	PU	I/O; AI	0	**PIO0_12/ADC0_10** General-purpose digital input/output pin. ADC single ended input channel 2B - CH2B. Can optionally be paired with CH2A as the negative differential input on ADC1 channel 2.
							I/O	1	**FC3_TXD_SCL_MISO_WS** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	2	**SD1_BACKEND_PWR** SD/MMC 1 back-end power supply for embedded device.
							I	3	**FREQME_GPIO_CLK_B** Frequency Measure pin clock input B.
							I	4	**SCT0_GPI7** Pin input 7 to SCTimer/PWM.
							O	5	**SD0_POW_EN** SD/MMC 0 card power enable.
							I/O	6	**SWDIO** Serial Wire Debug I/O. This is the default function after booting.
							I/O	7	**FC6_TXD_SCL_MISO_WS** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_12** Secure GPIO pin.
PIO0_13	D9	46	C12	71	[5]	Z	I/O	0	**PIO0_13** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	1	**FC1_CTS_SDA_SSEL0**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	2	**UTICK_CAP0** Micro-tick timer capture input 0.
							I	3	**CTIMER_INP0** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI0** Pin input 0 to SCTimer/PWM.
							I/O	5	**FC1_RXD_SDA_MOSI_DATA** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
							I	9	**PLU_INPUT0** PLU input 0.
							I/O	10	**SEC_PIO0_13** Secure GPIO pin.
PIO0_14	D8	47	C13	72	[5]	Z	I/O	0	**PIO0_14** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	1	**FC1_RTS_SCL_SSEL1** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	2	**UTICK_CAP1** Micro-tick timer capture input 1.
							I	3	**CTIMER_INP1** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI1** Pin input 1 to SCTimer/PWM.
								5	**R** Reserved.
							I/O	6	**FC1_TXD_SCL_MISO_WS** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								7	**R** Reserved.
								8	**R** Reserved.
							I	9	**PLU_INPUT1** PLU input 1.
							I/O	10	**SEC_PIO0_14** Secure GPIO pin.
PIO0_15/ ADC0_2	F2	14	L2	22	[2]	Z	I/O; AI	0	**PIO0_15/ADC0_2** General-purpose digital input/output pin. ADC single ended input channel 2A - CH2A. Can optionally be paired with CH2B as the positive differential input on ADC1 channel 2.
							I/O	1	**FC6_CTS_SDA_SSEL0** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	2	**UTICK_CAP2** Micro-tick timer capture input 2.
							I	3	**CTIMER_INP16** Capture input to CTIMER input multiplexers.
							O	4	**SCT0_OUT2** SCTimer/PWM output 2.
							I	5	**SD0_WR_PRT** SD/MMC 0 write protect.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_15** Secure GPIO pin.
PIO0_16/ ADC0_8	D1	7	J2	14	[2]	Z	I/O; AI	0	**PIO0_16/ADC0_8** General-purpose digital input/output pin. ADC single ended input channel 0B - CH0B. Can optionally be paired with CH0A as the negative differential input on ADC1 channel 0.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I/O	1	**FC4_TXD_SCL_MISO_WS** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	2	**CLKOUT** Output of the CLKOUT function.
							I	3	**CTIMER_INP4** Capture input to CTIMER input multiplexers.
								4	**R** Reserved.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_16** Secure GPIO pin.
PIO0_17	B1	3	G3	8	[3]	Z	I/O	0	**PIO0_17** General-purpose digital input/output pin.
							I/O	1	**FC4_SSEL2** Flexcomm 4: SPI slave select 2.
							I	2	**SD0_CARD_DET_N** SD/MMC 0 card detect (active low).
							I	3	**SCT0_GPI7** Pin input 7 to SCTimer/PWM.
							O	4	**SCT0_OUT0** SCTimer/PWM output 0.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
							I	8	**SD0_CARD_INT_N** SD/MMC 0 card interrupt.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I	9	**PLU_INPUT2** PLU input 2.
							I/O	10	**SEC_PIO0_17** Secure GPIO pin.
PIO0_18/ ACMP0_C	H9	38	H9	56	[2]	Z	I/O; AI	0	**PIO0_18/ACMP0_C** General-purpose digital input/output pin. Comparator 0, input C if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin.
							I/O	1	**FC4_CTS_SDA_SSEL0** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	2	**SD0_WR_PRT** SD/MMC 0 write protect.
							O	3	**CTIMER1_MAT0** 32-bit CTimer1 match output 0.
							O	4	**SCT0_OUT1** SCTimer/PWM output 1.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
							I	9	**PLU_INPUT3** PLU input 3.
							I/O	10	**SEC_PIO0_18** Secure GPIO pin.
PIO0_19	C4	58	E6	90	[3]	Z	I/O	0	**PIO0_19** General-purpose digital input/output pin.
							I/O	1	**FC4_RTS_SCL_SSEL1** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	2	**UTICK_CAP0** Micro-tick timer capture input 0.
							O	3	**CTIMER0_MAT2** 32-bit CTimer0 match output 2.
							O	4	**SCT0_OUT2** SCTimer/PWM output 2.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								5	**R** Reserved.
								6	**R** Reserved.
							I/O	7	**FC7_TXD_SCL_MISO_WS** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
								8	**R** Reserved.
							I	9	**PLU_INPUT4** PLU input 4.
							I/O	10	**SEC_PIO0_19** Secure GPIO pin.
PIO0_20	C8	48	B12	74	[3]	Z	I/O	0	**PIO0_20** General-purpose digital input/output pin.
							I/O	1	**FC3_CTS_SDA_SSEL0** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	2	**CTIMER1_MAT1** 32-bit CTimer1 match output 1.
							I	3	**CTIMER_INP15** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI2** Pin input 2 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
							I/O	7	**FC7_RXD_SDA_MOSI_DATA** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	8	**HS_SPI_SSEL0** Slave Select 0 for high speed SPI.
							I	9	**PLU_INPUT5** PLU input 5.
							I/O	10	**SEC_PIO0_20** Secure GPIO pin.
							I/O	11	**FC4_TXD_SCL_MISO_WS**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_21	B8	49	A12	76	[3]	Z	I/O	0	**PIO0_21** General-purpose digital input/output pin.
							I/O	1	**FC3_RTS_SCL_SSEL1** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	2	**UTICK_CAP3** Micro-tick timer capture input 3.
							O	3	**CTIMER3_MAT3** 32-bit CTimer3 match output 3.
							I	4	**SCT0_GPI3** Pin input 3 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
							I/O	7	**FC7_SCK** Flexcomm 7: USART, SPI, or I2S clock.
								8	**R** Reserved.
							I	9	**PLU_CLKIN** PLU clock input. Maximum frequency on PLU clock input is 25 MHz.
							I/O	10	**SEC_PIO0_21** Secure GPIO pin.
PIO0_22	B9	50	E9	78	[3][6]	Z	I/O	0	**PIO0_22** General-purpose digital input/output pin.
							I/O	1	**FC6_TXD_SCL_MISO_WS** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	2	**UTICK_CAP1** Micro-tick timer capture input 1.
							I	3	**CTIMER_INP15** Capture input to CTIMER input multiplexers.
							O	4	**SCT0_OUT3** SCTimer/PWM output 3.
								5	**R** Reserved.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								6	**R** Reserved.
							I	7	**USB0_VBUS** Monitors the presence of USB0 bus power.
							I/O	8	**SD1_D[0]** SD/MMC 1 data 0.
							O	9	**PLU_OUT7** PLU output 7.
							I/O	10	**SEC_PIO0_22** Secure GPIO pin.
PIO0_23/ ADC0_0	F3	12	J1	20	[2]	Z	I/O; AI	0	**PIO0_23/ADC0_0** General-purpose digital input/output pin. ADC single ended input channel 0A - CH0A. Can optionally be paired with CH0B as the positive differential input on ADC1 channel 0.
							I/O	1	**MCLK** MCLK input or output for I2S.
							O	2	**CTIMER1_MAT2** 32-bit CTimer1 match output 2.
							O	3	**CTIMER3_MAT3** 32-bit CTimer3 match output 3.
							O	4	**SCT0_OUT4** SCTimer/PWM output 4.
							I/O	5	**FC0_CTS_SDA_SSEL0** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								6	**R** Reserved.
								7	**R** Reserved.
							I/O	8	**SD1_D[1]** SD/MMC 1 data 1.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_23** Secure GPIO pin.
PIO0_24	-	45	E12	70	[3]	Z	I/O	0	**PIO0_24** General-purpose digital input/output pin.
							I/O	1	**FC0_RXD_SDA_MOSI_DATA** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I/O	2	**SD0_D[0]** SD/MMC 0 data 0.
							I	3	**CTIMER_INP8** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI0** Pin input 0 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_24** Secure GPIO pin.
PIO0_25	A9	51	A11	79	[3]	Z	I/O	0	**PIO0_25** General-purpose digital input/output pin.
							I/O	1	**FC0_TXD_SCL_MISO_WS** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	2	**SD0_D[1]** SD/MMC 0 data 1.
							I	3	**CTIMER_INP9** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI1** Pin input 1 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Reserved.
							I/O	10	**SEC_PIO0_25** Secure GPIO pin.
PIO0_26	F8	40	H12	60	[3][6]	Z	I/O	0	**PIO0_26** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the HS SPI MOSI function (Flexcomm 8)
							I/O	1	**FC2_RXD_SDA_MOSI_DATA** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	2	**CLKOUT** Output of the CLKOUT function.
							I	3	**CTIMER_INP14** Capture input to CTIMER input multiplexers.
							O	4	**SCT0_OUT5** SCTimer/PWM output 5.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**USB0_IDVALUE** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
							I/O	8	**FC0_SCK** Flexcomm 0: USART, SPI, or I2S clock.
							I/O	9	**HS_SPI_MOSI** Master-out/slave-in data for high speed SPI.
							I/O	10	**SEC_PIO0_26** Secure GPIO pin.
PIO0_27	G2	18	N2	27	[3]	Z	I/O	0	**PIO0_27** General-purpose digital input/output pin.
							I/O	1	**FC2_TXD_SCL_MISO_WS** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
								2	**R** Reserved.
							O	3	**CTIMER3_MAT2** 32-bit CTimer3 match output 2.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							O	4	**SCT0_OUT6** SCTimer/PWM output 6.
								5	**R** Reserved.
								6	**R** Reserved.
							I/O	7	**FC7_RXD_SDA_MOSI_DATA** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								8	**R** Reserved.
							O	9	**PLU_OUT0** PLU output 0.
							I/O	10	**SEC_PIO0_27** Secure GPIO pin.
PIO0_28/ WAKEUP	D7	44	F13	66	[3][6]	Z	I/O	0	**PIO0_28** General-purpose digital input/output pin. This pin can trigger a wake-up from deep power-down mode. WAKEUP pin can be configured as rising or falling edge
							I/O	1	**FC0_SCK** Flexcomm 0: USART, SPI, or I2S clock.
							I/O	2	**SD1_CMD** SD/MMC 1 card command I/O.
							I	3	**CTIMER_INP11** Capture input to CTIMER input multiplexers.
							O	4	**SCT0_OUT7** SCTimer/PWM output 7.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**USB0_OVERCURRENTN** USB0 bus overcurrent indicator (active low).
								8	**R** Reserved.
							O	9	**PLU_OUT1** PLU output 1.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I/O	10	**SEC_PIO0_28** Secure GPIO pin.
PIO0_29	A4	59	H8	92	[3]	Z	I/O	0	**PIO0_29** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART RXD function.
							I/O	1	**FC0_RXD_SDA_MOSI_DATA** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	2	**SD1_D[2]** SD/MMC 1 data 2.
							O	3	**CTIMER2_MAT3** 32-bit CTimer2 match output 3.
							O	4	**SCT0_OUT8** SCTimer/PWM output 8.
								5	**R** Reserved.
								6	**R** Reserved.
							O	7	**CMP0_OUT** Analog comparator 0 output.
								8	**R** Reserved.
							O	9	**PLU_OUT2** PLU output 2.
							I/O	10	**SEC_PIO0_29** Secure GPIO pin.
PIO0_30	B4	60	E5	94	[3]	Z	I/O	0	**PIO0_30** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	1	**FC0_TXD_SCL_MISO_WS** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	2	**SD1_D[3]** SD/MMC 1 data 3.
							O	3	**CTIMER0_MAT0** 32-bit CTimer0 match output 0.
							O	4	**SCT0_OUT9** SCTimer/PWM output 9.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_30** Secure GPIO pin.
PIO0_31/ ADC0_3	-	15	L1	23	[2]	Z	I/O; AI	0	**PIO0_31/ADC0_3** General-purpose digital input/output pin. ADC single ended input channel 3A - CH3A. Can optionally be paired with CH3B as the positive differential input on ADC1 channel 3.
							I/O	1	**FC0_CTS_SDA_SSEL0** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	2	**SD0_D[2]** SD/MMC 0 data 2.
							O	3	**CTIMER0_MAT1** 32-bit CTimer0 match output 1.
							O	4	**SCT0_OUT3** SCTimer/PWM output 3.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
								9	**R** Reserved.
							I/O	10	**SEC_PIO0_31** Secure GPIO pin.
PIO1_0/ ADC0_11	B2	4	E1	11	[2]	Z	I/O; AI	0	**PIO1_0/ADC0_11** General-purpose digital input/output pin. ADC single ended input channel 3B -

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									CH3B. Can optionally be paired with CH3A as the negative differential input on ADC1 channel 3.
							I/O	1	**FC0_RTS_SCL_SSEL1** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	2	**SD0_D[3]** SD/MMC 0 data 3.
							I	3	**CTIMER_INP2** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI4** Pin input 4 to SCTimer/PWM.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
							O	9	**PLU_OUT3** PLU output 3.
PIO1_1/ WAKEUP	G8	39	G11	59	[3][6]	Z	I/O	0	**PIO1_1** General-purpose digital input/output pin. This pin can trigger a wake-up from deep power-down mode. WAKEUP pin can be configured as rising or falling edge **Remark:** In ISP mode, this pin is set to the High Speed SPI SSEL1 function (Flexcomm 8)
							I/O	1	**FC3_RXD_SDA_MOSI_DATA** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								2	**R** Reserved.
							I	3	**CTIMER_INP3** Capture input to CTIMER input multiplexers.
							I	4	**SCT0_GPI5** Pin input 5 to SCTimer/PWM.
							I/O	5	**HS_SPI_SSEL1**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Slave Select 1 for high speed SPI.
								6	**R** Reserved.
							I	7	**USB1_OVERCURRENTN** USB1 bus overcurrent indicator (active low).
								8	**R** Reserved.
							O	9	**PLU_OUT4** PLU output 4.
PIO1_2	F9	41	G12	61	[3][6]	Z	I/O	0	**PIO1_2** General-purpose digital input/output pin. Remark: In ISP mode, this pin is set to the High Speed SPI SCK function (Flexcomm 8).
								1	**R** Reserved.
								2	**R** Reserved.
							O	3	**CTIMER0_MAT3** 32-bit CTimer0 match output 3.
							I	4	**SCT0_GPI6** Pin input 6 to SCTimer/PWM.
								5	**R** Reserved.
							I/O	6	**HS_SPI_SCK** Clock for high speed SPI.
							O	7	**USB1_PORTPWRN** USB1 VBUS drive indicator (Indicates VBUS must be driven).
								8	**R** Reserved.
							O	9	**PLU_OUT5** PLU output 5.
PIO1_3	F7	42	G13	62	[3][6]	Z	I/O	0	**PIO1_3** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the High Speed SPI MISO function (Flexcomm 8).
								1	**R** Reserved.
								2	**R**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Reserved.
								3	**R** Reserved.
							O	4	**SCT0_OUT4** SCTimer/PWM output 4.
								5	**R** Reserved.
							I/O	6	**HS_SPI_MISO** Master-in/slave-out data for high speed SPI.
							O	7	**USB0_PORTPWRN** USB0 VBUS drive indicator (Indicates VBUS must be driven).
								8	**R** Reserved.
							O	9	**PLU_OUT6** PLU output 6.
PIO1_4	B3	-	B2	1	[3]	Z	I/O	0	**PIO1_4** General-purpose digital input/output pin.
							I/O	1	**FC0_SCK** Flexcomm 0: USART, SPI, or I2S clock.
							I/O	2	**SD0_D[0]** SD/MMC 0 data 0.
							O	3	**CTIMER2_MAT1** 32-bit CTimer2 match output 1.
							O	4	**SCT0_OUT0** SCTimer/PWM output 0.
							I	5	**FREQME_GPIO_CLK_A** Frequency Measure pin clock input A.
PIO1_5	-	-	M5	31	[3]	Z	I/O	0	**PIO1_5** General-purpose digital input/output pin.
							I/O	1	**FC0_RXD_SDA_MOSI_DATA** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	2	**SD0_D[2]** SD/MMC 0 data 2.
							O	3	**CTIMER2_MAT0** 32-bit CTimer2 match output 0.
							I	4	**SCT0_GPI0** Pin input 0 to SCTimer/PWM.
PIO1_6	-	-	H5	5	[3]	Z	I/O	0	**PIO1_6**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									General-purpose digital input/output pin.
							I/O	1	**FC0_TXD_SCL_MISO_WS** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	2	**SD0_D[3]** SD/MMC 0 data 3.
							O	3	**CTIMER2_MAT1** 32-bit CTimer2 match output 1.
							I	4	**SCT0_GPI3** Pin input 3 to SCTimer/PWM.
PIO1_7	-	-	J5	9	[3]	Z	I/O	0	**PIO1_7** General-purpose digital input/output pin.
							I/O	1	**FC0_RTS_SCL_SSEL1** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	2	**SD0_D[1]** SD/MMC 0 data 1.
							O	3	**CTIMER2_MAT2** 32-bit CTimer2 match output 2.
							I	4	**SCT0_GPI4** Pin input 4 to SCTimer/PWM.
PIO1_8/ ADC0_4	-	-	A6	24	[2]	Z	I/O; AI	0	**PIO1_8/ADC0_4** General-purpose digital input/output pin. ADC single ended input channel 4A - CH4A. Can optionally be paired with CH4B as the positive differential input on ADC1 channel 4.
							I/O	1	**FC0_CTS_SDA_SSEL0** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	2	**SD0_CLK** SD/MMC 0 card clock.
								3	**R** Reserved.
							O	4	**SCT0_OUT1** SCTimer/PWM output 1.
							I/O	5	**FC4_SSEL2** Flexcomm 4: SPI slave select 2.
PIO1_9/ ADC0_12	-	-	C1	10	[2]	Z	I/O; AI	0	**PIO1_9/ADC0_12** General-purpose digital input/output pin. ADC single ended input channel 4B - CH4B. Can optionally be paired with CH4A

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									as the negative differential input on ADC1 channel 4.
								1	**R** Reserved.
							I/O	2	**FC1_SCK** Flexcomm 1: USART, SPI, or I2S clock.
							I	3	**CTIMER_INP4** Capture input to CTIMER input multiplexers.
							O	4	**SCT0_OUT2** SCTimer/PWM output 2.
							I/O	5	**FC4_CTS_SDA_SSEL0** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
PIO1_10	-	-	J7	40	[3]	Z	I/O	0	**PIO1_10** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**FC1_RXD_SDA_MOSI_DATA** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	3	**CTIMER1_MAT0** 32-bit CTimer1 match output 0.
							O	4	**SCT0_OUT3** SCTimer/PWM output 3.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
PIO1_11	-	-	G6	93	[3][6]	Z	I/O	0	**PIO1_11** General-purpose digital input/output pin.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								1	**R** Reserved.
							I/O	2	**FC1_TXD_SCL_MISO_WS** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	3	**CTIMER_INP5** Capture input to CTIMER input multiplexers.
							I	4	**USB0_VBUS** Monitors the presence of USB0 bus power.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
PIO1_12	-	-	F12	67	[3][6]	Z	I/O	0	**PIO1_12** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**FC6_SCK** Flexcomm 6: USART, SPI, or I2S clock.
							O	3	**CTIMER1_MAT1** 32-bit CTimer1 match output 1.
							O	4	**USB0_PORTPWRN** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							I/O	5	**HS_SPI_SSEL2** Slave Select 2 for high speed SPI.
PIO1_13	-	-	B3	2	[3][6]	Z	I/O	0	**PIO1_13** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**FC6_RXD_SDA_MOSI_DATA** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I	3	**CTIMER_INP6** Capture input to CTIMER input multiplexers.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I	4	**USB0_OVERCURRENTN** USB0 bus overcurrent indicator (active low).
							O	5	**USB0_FRAME** USB0 frame toggle signal.
								6	**R** Reserved.
							I	7	**SD0_CARD_DET_N** SD/MMC 0 card detect (active low).
PIO1_14/ ACMP0_D	-	-	L7	57	[2][6]	Z	I/O; AI	0	**PIO1_14/ACMP0_D** General-purpose digital input/output pin. Comparator 0, input D if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin.
								1	**R** Reserved.
							I	2	**UTICK_CAP2** Micro-tick timer capture input 2.
							O	3	**CTIMER1_MAT2** 32-bit CTimer1 match output 2.
							I/O	4	**FC5_CTS_SDA_SSEL0** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	5	**USB0_LEDN** USB0-configured LED indicator (active low).
								6	**R** Reserved.
							I/O	7	**SD1_CMD** SD/MMC 1 card command I/O.
PIO1_15	-	-	B6	82	[3]	Z	I/O	0	**PIO1_15** General-purpose digital input/output pin.
								1	**R** Reserved.
							I	2	**UTICK_CAP3** Micro-tick timer capture input 3.
							I	3	**CTIMER_INP7** Capture input to CTIMER input multiplexers.
							I/O	4	**FC5_RTS_SCL_SSEL1** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I/O	5	**FC4_RTS_SCL_SSEL1** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								6	**R** Reserved.
							I/O	7	**SD1_D[2]** SD/MMC 1 data 2.
								8	**R** Reserved.
PIO1_16	-	-	C7	87	[3]	Z	I/O	0	**PIO1_16** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**FC6_TXD_SCL_MISO_WS** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	3	**CTIMER1_MAT3** 32-bit CTimer1 match output 3.
							I/O	4	**SD0_CMD** SD/MMC 0 card command I/O.
								5	**R** Reserved.
								6	**R** Reserved.
								7	**R** Reserved.
								8	**R** Reserved.
PIO1_17	-	-	J9	43	[3]	Z	I/O	0	**PIO1_17** General-purpose digital input/output pin.
								1	**R** Reserved.
								2	**R** Reserved.
							I/O	3	**FC6_RTS_SCL_SSEL1** Flexcomm 6: USART request-to-send, I2C clock, SPI slave select 1.
							O	4	**SCT0_OUT4** SCTimer/PWM output 4.
								5	**R**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Reserved.
								6	**R** Reserved.
							I	7	**SD1_CARD_INT_N** SD/MMC 1 card interrupt.
								8	**R** Reserved.
							I	9	**SD1_CARD_DET_N** SD/MMC 1 card detect (active low).
PIO1_18/ WAKUP	-	-	G9	64	[3]	Z	I/O	0	**PIO1_18** General-purpose digital input/output pin. This pin can trigger a wake-up from deep power-down mode.
							O	1	**SD1_POW_EN** SD/MMC 1 card power enable.
								2	**R** Reserved.
								3	**R** Reserved.
							O	4	**SCT0_OUT5** SCTimer/PWM output 5.
								5	**R** Reserved.
								6	**R** Reserved.
							O	7	**PLU_OUT0** PLU output 0.
								8	**R** Reserved.
PIO1_19/ $ACMPV_{REF}$	-	-	H13	58	[2]	Z	I/O; AI	0	**PIO1_19/$ACMPV_{REF}$** General-purpose digital input/output pin. Alternate reference voltage for the analog comparator if the DIGIMODE bit is set to 0 and ANAMODE is set to 1 in the IOCON register for this pin.
								1	**R** Reserved.
							O	2	**SCT0_OUT7** SCTimer/PWM output 7.
							O	3	**CTIMER3_MAT1** 32-bit CTimer3 match output 1.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
							I	4	**SCT0_GPI7** Pin input 7 to SCTimer/PWM.
							I/O	5	**FC4_SCK** Flexcomm 4: USART, SPI, or I2S clock.
								6	**R** Reserved.
							O	7	**PLU_OUT1** PLU output 1.
								8	**R** Reserved.
PIO1_20	-	-	C2	4	[3]	Z	I/O	0	**PIO1_20** General-purpose digital input/output pin.
							I/O	1	**FC7_RTS_SCL_SSEL1** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								2	**R** Reserved.
							I	3	**CTIMER_INP14** Capture input to CTIMER input multiplexers.
								4	**R** Reserved.
							I/O	5	**FC4_TXD_SCL_MISO_WS** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
								6	**R** Reserved.
							O	7	**PLU_OUT2** PLU output 2.
								8	**R** Reserved.
PIO1_21	-	-	M7	30	[3]	Z	I/O	0	**PIO1_21** General-purpose digital input/output pin.
							I/O	1	**FC7_CTS_SDA_SSEL0** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								2	**R** Reserved.
							O	3	**CTIMER3_MAT2** 32-bit CTimer3 match output 2.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								4	**R** Reserved.
							I/O	5	**FC4_RXD_SDA_MOSI_DATA** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								6	**R** Reserved.
							O	7	**PLU_OUT3** PLU output 3.
								8	**R** Reserved.
PIO1_22	-	-	M8	41	[3]	Z	I/O	0	**PIO1_22** General-purpose digital input/output pin.
								1	**R** Reserved.
							I/O	2	**SD0_CMD** SD/MMC 0 card command I/O.
							O	3	**CTIMER2_MAT3** 32-bit CTimer2 match output 3.
							I	4	**SCT0_GPI5** Pin input 5 to SCTimer/PWM.
							I/O	5	**FC4_SSEL3** Flexcomm 4: SPI slave select 3.
								6	**R** Reserved.
							O	7	**PLU_OUT4** PLU output 4.
PIO1_23	-	-	J8	42	[3]	Z	I/O	0	**PIO1_23** General-purpose digital input/output pin.
							I/O	1	**FC2_SCK** Flexcomm 2: USART, SPI, or I2S clock.
							O	2	**SCT0_OUT0** SCTimer/PWM output 0.
							I/O	3	**SD1_D[3]** SD/MMC 1 data 3.
								4	**R** Reserved.
							I/O	5	**FC3_SSEL2** Flexcomm 3: SPI slave select 2.
								6	**R**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									Reserved.
							O	7	**PLU_OUT5** PLU output 5.
								8	**R** Reserved.
PIO1_24	-	-	F6	3	[3]	Z	I/O	0	**PIO1_24** General-purpose digital input/output pin.
							I/O	1	**FC2_RXD_SDA_MOSI_DATA** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	2	**SCT0_OUT1** SCTimer/PWM output 1.
							I/O	3	**SD1_D[1]** SD/MMC 1 data 1.
								4	**R** Reserved.
							I/O	5	**FC3_SSEL3** Flexcomm 3: SPI slave select 3.
								6	**R** Reserved.
							O	7	**PLU_OUT6** PLU output 6.
								8	**R** Reserved.
PIO1_25	-	-	B8	77	[3]	Z	I/O	0	**PIO1_25** General-purpose digital input/output pin.
							I/O	1	**FC2_TXD_SCL_MISO_WS** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	2	**SCT0_OUT2** SCTimer/PWM output 2.
							I/O	3	**SD1_D[0]** SD/MMC 1 data 0.
							I	4	**UTICK_CAP0** Micro-tick timer capture input 0.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**PLU_CLKIN**

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									PLU clock input. Maximum frequency on PLU clock input is 25 MHz.
								8	**R** Reserved.
PIO1_26	-	-	E13	68	[3]	Z	I/O	0	**PIO1_26** General-purpose digital input/output pin.
							I/O	1	**FC2_CTS_SDA_SSEL0** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	2	**SCT0_OUT3** SCTimer/PWM output 3.
							I	3	**CTIMER_INP3** Capture input to CTIMER input multiplexers.
							I	4	**UTICK_CAP1** Micro-tick timer capture input 1.
							I/O	5	**HS_SPI_SSEL3** Slave Select 3 for high speed SPI.
								6	**R** Reserved.
							I	7	**PLU_INPUT5** PLU input 5.
								8	**R** Reserved.
PIO1_27	-	-	E8	85	[3]	Z	I/O	0	**PIO1_27** General-purpose digital input/output pin.
							I/O	1	**FC2_RTS_SCL_SSEL1** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	2	**SD0_D[4]** SD/MMC 0 data 4.
							O	3	**CTIMER0_MAT3** 32-bit CTimer0 match output 3.
							O	4	**CLKOUT** Output of the CLKOUT function.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**PLU_INPUT4** PLU input 4.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
								8	**R** Reserved.
PIO1_28	-	-	A8	73	[3]	Z	I/O	0	**PIO1_28** General-purpose digital input/output pin.
							I/O	1	**FC7_SCK** Flexcomm 7: USART, SPI, or I2S clock.
							I/O	2	**SD0_D[5]** SD/MMC 0 data 5.
							I	3	**CTIMER_INP2** Capture input to CTIMER input multiplexers.
								4	**R** Reserved.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**PLU_INPUT3** PLU input 3.
								8	**R** Reserved.
PIO1_29	A8	-	G8	80	[3][6]	Z	I/O	0	**PIO1_29** General-purpose digital input/output pin.
							I/O	1	**FC7_RXD_SDA_MOSI_DATA** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	2	**SD0_D[6]** SD/MMC 0 data 6.
							I	3	**SCT0_GPI6** Pin input 6 to SCTimer/PWM.
							O	4	**USB1_PORTPWRN** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	5	**USB1_FRAME** USB1 frame toggle signal.
								6	**R** Reserved.
							I	7	**PLU_INPUT2** PLU input 2.
PIO1_30/ WAKEUP	E7	-	F9	65	[3][6]	Z	I/O	0	**PIO1_30** General-purpose digital input/output pin.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
									This pin can trigger a wake-up from deep power-down mode. WAKEUP pin can be configured as rising or falling edge.
							I/O	1	**FC7_TXD_SCL_MISO_WS** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	2	**SD0_D[7]** SD/MMC 0 data 7.
							I	3	**SCT0_GPI7** Pin input 7 to SCTimer/PWM.
							I	4	**USB1_OVERCURRENTN** USB1 bus overcurrent indicator (active low).
							O	5	**USB1_LEDN** USB1-configured LED indicator (active low).
								6	**R** Reserved.
							I	7	**PLU_INPUT1** PLU input 1.
PIO1_31	-	-	H6	91	[3]	Z	I/O	0	**PIO1_31** General-purpose digital input/output pin.
							I/O	1	**MCLK** MCLK input or output for I2S.
							O	2	**SD1_CLK** SD/MMC 1 card clock.
							O	3	**CTIMER0_MAT2** 32-bit CTimer0 match output 2.
							O	4	**SCT0_OUT6** SCTimer/PWM output 6.
								5	**R** Reserved.
								6	**R** Reserved.
							I	7	**PLU_INPUT0** PLU input 0.
								8	**R** Reserved.
FB	-	29	N9	45		-	-		Feedback node (regulated output) of DCDC converter.
LX	H6	31	N11	48		-	-		DCDC converter power stage output.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
RESETN	H2	21	J6	32	[7]	-	I		External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.
USB0_3V3	-	61	A3	96		-	-		USB0 analog 3.3 V supply.
USB0_DM	-	63	A1	98	[8][6]		I/O		USB0 bidirectional D- line.
USB0_DP	-	62	A2	97	[8][6]		I/O		USB0 bidirectional D+ line.
USB0_ VSS	-	64	B1	99					USB0 analog 3.3 V ground.
USB1_DM	J4	24	N6	35	[8][6]		I/O		USB1 bidirectional D- line.
USB1_DP	H4	23	M6	34	[8][6]		I/O		USB1 bidirectional D+ line.
USB1_ VBUS	G4	25	N8	36	[8][6]		I		VBUS pin (power on USB cable).
USB1_3V3	G5	27	N7	38	[9]	-	-		USB1 analog 3.3 V supply.
USB1_ VSS	H3	22;26	N5	33; 37		-	-		USB1 analog 3.3 V ground.
VBAT_ DCDC	H7	32	N13	49, 50	[10]	-	-		Supply of DCDC output stage. DCDC core supply (references and regulation stages).
VBAT_ PMU	H8	33	M13	51	[10]	-	-		Analog supply.
VDD	F5;E5;D5	8; 16; 43; 54	M1; A5; A9; A13	15; 25; 44; 63; 69;75; 84; 95; 100		-	-		Single 1.8 V to 3.6 V power supply powers I/Os.
VDD_PMU	G6	28	M9	39		-	-		Core supply. For applications with DCDC converter, VDD_PMU and FB are tied at PCB level.
VDDA	D3	9	G2	16		-	-		Analog supply voltage. At PCB level, has to be tied to main supply (VBAT_PMU, VBAT_ DCDC)
VREFN	-	-	H1	18		-	-		ADC negative reference voltage.
VREFP	-	10	G1	17		-	-		ADC positive reference voltage.
VSS	D4;D6;F 4;F6	exposed pad	N1; B5; B9; B13	exposed pad		-	-		Ground.
VSS_ DCDC	J6	30	N12, M12	46, 47		-	-		Star ground connection is managed to PCB ground plane.
VSS_PMU	-	-	M11	-		-	-		Star ground connection is managed to PCB ground plane.
VSSA	E3	11	H2	19		-	-		Analog ground.

Table 3. Pin description...*continued*

Symbol	59 pin VFBGA	64 pin HTQFP	98 pin VFBGA	100 pin HLQFP		Reset state [1]	Type	Function #	Description
XTAL32K_N	-	35	J12	53	[11]	-	-		RTC oscillator output.
XTAL32K_P	-	34	J13	52	[11]	-	-		RTC oscillator input.
XTAL32M_N	J1	19	M3	28	[12]	-	-		Main oscillator output. For USB HS ISP mode, 16 MHz crystal is required.
XTAL32M_P	J2	20	N3	29	[12]	-	-		Main oscillator input. For USB HS ISP mode, 16 MHz crystal is required.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls pin up towards V_{DD}). PD = input mode, pull-down enabled (pull-down resistor pulls pin down towards V_{SS}). Z = high impedance; pull-up, pull-down, and input disabled. AI = analog input. I = input. O = output. I/O = input/output. Reset state reflects the pin state at reset without boot code operation. For termination on unused pins, see Section 6.1.1 "Termination of unused pins".

[2] Pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled.

[3] Pad provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

[4] The JTAG functions TRST, TCK, TMS, TDI, and TDO are selected by hardware when the part is in boundary scan mode. The JTAG functions cannot be used for debug mode.

[5] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin. Includes a filter that can be selectively disabled by setting the FILTEROFF bit. The filter suppresses input pulses smaller than about 3 ns in GPIO mode and smaller than about 3 ns in GPIO mode and smaller than 10 ns or 50 ns in I2C mode, depending on the value of I2CFILTER field.

[6] The corresponding VBUS must be connected to supply voltage when using the USB peripheral. USB0_VBUS is not 5 V tolerant pin and is tolerant up to 3.6 V only when the VDD is at operating level (minimum: 1.8 V). USB1_VBUS is 5 V tolerant pin regardless if the VDD supply is present or not.

[7] Reset pad with glitch filter and hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[8] Transparent analog pad.

[9] If the USB1_3V3 pin is not using the same supply as the VBAT_PMU pin, the application should ensure the supply on USB1_3V3 does not drop below 2.8 V. If the USB1_3V3 pin is using separate supply and this voltage unexpectedly drops below 2.8 V, the USB PHY can go into unknown state causing USB transactions (R/W) to hang. In this case, the application can detect this event with a time-out and would have to recover by performing a USB reset..

[10] Main battery supply: Star connection at application level (PCB).

[11] Optional bypass mode is supported, xtal32K_P can be driven by an external clock with restrictions in terms of drive level See: Section 13 "Application information".

[12] Optional bypass mode is supported, xtal32M_P can be driven by an external clock with restrictions in terms of drive level. See: Section 13 "Application information".

6.1.1 Termination of unused pins

Table 4 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 4. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
All PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up or pull-down disabled by software.

Table 4. Termination of unused pins...*continued*

Pin	Default state[1]	Recommended termination of unused pins
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
XTAL32K_P	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTAL32K_N	-	Can be left unconnected.
XTAL32M_P	-	Connect to ground. When grounded, the System oscillator is disabled.
XTAL32M_N	-	Can be left unconnected.
VREFP	-	Tie to VBAT_DCDC.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VBAT_DCDC.
VSSA	-	Tie to VSS.
USBn_DP	F	Can be left unconnected.
USBn_DM	F	Can be left unconnected.
USBn_3V3	F	Tie to VBAT_DCDC. If not using USB and using 1.8 V supply, USBn_3V3 can be connected to 1.8 V. When not using USB, pin can be connected to ground as well.
USB1_VBUS	F	Can be left unconnected.
USBn_VSS	F	Tie to VSS.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled

6.1.2 Using Internal DC-DC converter

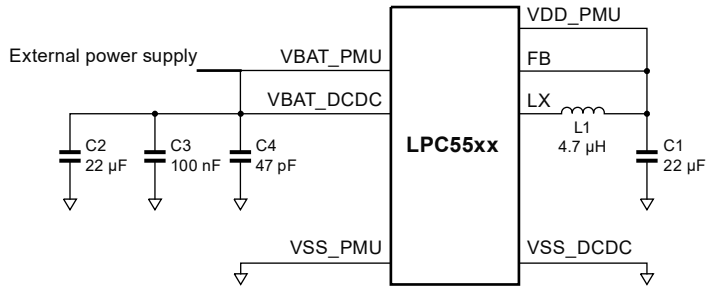


Figure 6. Using internal DC-DC converter

7 Functional description

7.1 Architectural overview

The Arm Cortex M33 includes two AHB-Lite buses, one system bus and one code and bus. The Code AHB (C-AHB) interface is used for any instruction fetch and data access to the Code region of the ARMv8-M memory map ([0x00000000 - 0x1FFFFFFF]). The System AHB (S-AHB) interface is used for instruction fetch and data access to all other regions of the ARMv8-M memory map ([0x20000000 - 0xFFFFFFFF]).

The LPC55S6x uses a multi-layer AHB matrix to connect the ARM Cortex-M33 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters. Figure 5 shows details of the available matrix connections.

7.2 Arm Cortex-M33 processor (CPU0)

The ARM Cortex-M33 is based on the ARMv8-M architecture that offers systems enhancements, such as ARM TrustZone® security, single-cycle digital signal processing, low power consumption, enhanced debug features, and a high level of support block integration. The ARM Cortex-M33 CPU employs a 7-stage instruction pipe and includes an internal prefetch unit that supports speculative branching. A hardware floating-point processor is integrated into the core. On the LPC55S6x, the Cortex-M33 is augmented with two hardware co-processors providing accelerated support for additional DSP algorithms and cryptography.

The Arm Cortex M33 provides a security foundation, offering isolation to protect valuable IP and data with TrustZone technology. It simplifies the design and software development of digital signal control systems with the integrated digital signal processing (DSP) instructions.

7.3 Arm Cortex-M33 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Arm Cortex-M33 (CPU1)

The LPC55S6x device includes a second instance of Cortex-M33. The configuration of this instance does not include MPU, FPU, DSP, ETM, Trustzone (SECEXT), Secure Attribution Unit (SAU) or co-processor interface. It supports the same debug levels and interrupt lines as the primary CPU.

7.5 Memory Protection Unit (MPU)

The Cortex-M33 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M33 (CPU0)

The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.

- 60 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using Vector Table Offset Register (VTOR).
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M33 (CPU1)

The NVIC is an integral part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 60 vectored interrupts.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using VTOR.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.8 System Tick timer (SysTick)

The ARM Cortex-M33 core include a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the system clock or the SYSTICK clock.

7.9 On-chip static RAM

The LPC55S6x support up to 320 KB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.10 On-chip flash

The LPC55S6x supports up to 640 kB of on-chip flash memory. The last 17 pages (10 KB) are reserved on the 640 KB flash devices resulting in 630 KB internal flash memory.

7.11 On-chip ROM

The on-chip ROM contains the bootloader and the following features:

- Booting of images from on-chip flash.
- Supports CRC32 image integrity checking.
- Supports flash programming through In System Programming (ISP) commands over following interfaces: USB0/1 interfaces using HID Class device, UART interface (Flexcomm 0) with auto baud, SPI slave interfaces (Flexcomm 3 or 9) using mode 3 (CPOL = 1 and CPHA = 1), and I2C slave interface (Flexcomm 1)

- ROM API functions: Flash programming API, Power control API, and Secure firmware update API using NXP Secure Boot file format, version 2.0 (SB2 files).
- Supports booting of images from PRINCE encrypted flash region.
- Supports NXP Debug Authentication Protocol version 1.0 (RSA-2048) and 1.1 (RSA-4096)
- Supports setting a sealed part to Fault Analysis mode through Debug authentication.

The on-chip ROM supports the following secure boot features:

- Uses RSASSA-PKCS1-v1_5 signature of SHA256 digest as cryptographic signature verification
- Supports RSA-2048 bit public keys (2048 bit modulus, 32-bit exponent)
- Supports RSA-4096 bit public keys (4096 bit modulus, 32-bit exponent)
- Uses x509 certificate format to validate image public keys
- Supports up to four revocable Root of Trust (or Certificate Authority) keys, Root of Trust (RoT) establishment by storing the SHA-256 hash digest of the hashes of four RoT public keys in protected flash region (PFR)
- Supports anti-rollback feature using image key revocation and supports up to 16 Image key certificates revocations using Serial Number field in x509 certificate.
- Supports Device Identifier Composition Engine (DICE) Specification (version Family 2.0, Level 00 Revision 69) specified by Trusted Computing Group.

7.12 Protected Flash Region (PFR)

The protected flash region is available to configure secure boot, debug authentication, read UUID, store PUF in key store area, and user defined fields available for specific data storage.

7.13 Memory mapping

7.14 AHB multilayer matrix

The LPC55S6x uses a multi-layer AHB matrix to connect the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters. The device block diagram in Figure 5 shows details of the available matrix connections.

7.15 Memory Protection Unit (MPU)

CPU0 has a memory protection unit (MPU) that provides fine grain memory control, enabling applications to implement security privilege levels, separating code, data and stack on a task-by-task basis. Such requirements are critical in many embedded applications.

The MPU register interface is located on the CPU private peripheral bus and is described in detail in Ref 1 "Cortex-M33 DEBUG"

7.16 TrustZone and system mapping on this device

The implementation of ARM TrustZone for CPU0 involves using address bit 28 to divide the address space into potential secure and non-secure regions. Address bit 28 is not decoded in memory access hardware, so each physical location appears in two places on whatever bus they are located on. Other hardware determines which kinds of accesses (including non-secure callable) are actually allowed for any particular address.

Table 5 shows the overall mapping of the code and data buses for secure and non-secure accesses to various device resources.

Remark: Address regions considered secure by TrustZone may also be accessible to CPU1 if it is assigned as a secure master and marked as secure by checker hardware.

Remark: In the peripheral description chapters of this manual, only the native (non-secure) base address is noted, secure base addresses can be found in this chapter or created by setting bit 28 in the address as needed.

Table 5. TrustZone and system general mapping

Start address	End address	TrustZone, CPU0 only	CPU bus	CM-33 usage (both CPUs)
0x0000 0000	0x0FFF FFFF	Non-secure	Code	Flash memory, Boot ROM, SRAM X.
0x1000 0000	0x1FFF FFFF	Secure	Code	Same as above.
0x2000 0000	0x2FFF FFFF	Non-secure	Data	SRAM 0, SRAM 1, SRAM 2, SRAM 3, SRAM 4.
0x3000 0000	0x3FFF FFFF	Secure	Data	Same as above.
0x4000 0000	0x4FFF FFFF	Non-secure	Data	AHB and APB peripherals.
0x5000 0000	0x5FFF FFFF	Secure	Data	Same as above.

1. The size shown for peripherals spaces indicates the space allocated in the memory map, not the actual space used by the peripheral or memory.
2. Selected areas of secure regions may be marked as non-secure callable.

7.17 Links to specific memory map descriptions and tables:

- Section 7.18
- Section 7.19
- Section 7.20

7.18 Memory map overview

Table 6 gives a more detailed memory map as seen by the 2 Cortex-M33 (both CPU0 and CPU1). The purpose of the four address spaces for the shared RAMs is outlined at the beginning of this chapter. The details of which shared RAM regions are on which AHB matrix slave ports can be seen here.

Table 6. Memory map overview

AHB port	Non-secure start address	Non-secure end address	Secure start address	Secure end address	Function [1]
0	0x0000 0000	0x0009 FFFF	0x1000 0000	0x1009 FFFF	Flash memory, on CM33 code bus. The last 17 pages (10 KB) are reserved on the 640 KB flash devices resulting in 630 KB internal flash memory.
	0x0300 0000	0x0301 FFFF	0x1300 0000	0x1301 FFFF	Boot ROM, on CM33 code bus.
1	0x0400 0000	0x0400 7FFF	0x1400 0000	0x1400 7FFF	SRAM X on CM33 code bus, 32 KB. SRAMX_0 (0x1400 0000 to 0x1400 0FFF) and SRAMX_1 (0x1400 4000 to 0x1400 4FFF) are used for Casper (total 8 KB). If CPU retention used in power-down mode, SRAMX_2 (0x1400 6000 to 0x1400 65FF) is used (total 1.5 KB) by default in power API and this is user configurable within SRAMX_2 and SRAMX_3.
2	0x2000 0000	0x2000 FFFF	0x3000 0000	0x3000 FFFF	SRAM 0 on CM33 data bus, 64 KB.
3	0x2001 0000	0x2001 FFFF	0x3001 0000	0x3001 FFFF	SRAM 1 on CM33 data bus, 64 KB.
4	0x2002 0000	0x2002 FFFF	0x3002 0000	0x3002 FFFF	SRAM 2 on CM33 data bus, 64 KB.
5	0x2003 0000	0x2003 FFFF	0x3003 0000	0x3003 FFFF	SRAM 3 on CM33 data bus, 64 KB.

Table 6. Memory map overview*...continued*

AHB port	Non-secure start address	Non-secure end address	Secure start address	Secure end address	Function [1]
6	0x2004 0000	0x2004 3FFF	0x3004 0000	0x3004 3FFF	SRAM 4 on CM33 data bus, 16 KB. Entire SRAM 4 is used by PowerQuad when PowerQuad is enabled.
7	0x4000 0000	0x4001 FFFF	0x5000 0000	0x5001 FFFF	AHB to APB bridge 0. See Section 7.19.
	0x4002 0000	0x4003 FFFF	0x5002 0000	0x5003 FFFF	AHB to APB bridge 1. See Section 7.19.
8	0x4008 0000	0x4008 FFFF	0x5008 0000	0x5008 FFFF	AHB peripherals. See Section 7.20.
9	0x4009 0000	0x4009 FFFF	0x5009 0000	0x5009 FFFF	AHB peripherals. See Section 7.20.
10	0x400A 0000	0x400A FFFF	0x500A 0000	0x500A FFFF	AHB peripherals. See Section 7.20.
11	0x4010 0000	0x4010 FFFF	0x5010 0000	0x5010 FFFF	AHB peripherals. See Section 7.20.

[1] Gaps between AHB matrix slave ports are not shown.

7.19 APB peripherals

Table 7 provides details of the addresses for APB peripherals. APB peripherals have both secure and non-secure access possibilities.

Table 7. APB peripherals memory map

APB bridge	Non-secure base address	Secure base address	Peripheral
0	0x4000 0000	0x5000 0000	Syscon.
	0x4000 1000	0x5000 1000	IOCON. Pin function selection and pin control setup.
	0x4000 2000	0x5000 2000	Group GPIO input interrupt 0 (GINT0)
	0x4000 3000	0x5000 3000	Group GPIO input interrupt 1 (GINT1)
	0x4000 4000	0x5000 4000	Pin interrupt and pattern match (PINT)
	0x4000 5000	0x5000 5000	Secure pin interrupt and pattern match.
	0x4000 6000	0x5000 6000	Input multiplexing 0 and frequency measure.
	0x4000 7000	0x5000 7000	Reserved.
	0x4000 8000	0x5000 8000	CT32B0 (standard counter/timer 0).
	0x4000 9000	0x5000 9000	CT32B1 (standard counter/timer 1).
	0x4000 C000	0x5000 C000	WWDT0 (windowed watchdog timer 0).
	0x4000 D000	0x5000 D000	MRT (Multi-Rate Timer).
	0x4000 E000	0x5000 E000	Utick (micro-tick timer).
	0x4001 0000	0x5001 0000	ACMP0 (analog comparator).
	0x4001 3000	0x5001 3000	Analog controls.
	0x4001 5000	0x5001 5000	Reserved.
1	0x4002 3000	0x5002 3000	Sysctl (I2S signal sharing)
	0x4002 8000	0x5002 8000	CT32B2 (standard counter/timer 2).
	0x4002 9000	0x5002 9000	CT32B3 (standard counter/timer 3).
	0x4002 A000	0x5002 A000	CT32B4 (standard counter/timer 4).

Table 7. APB peripherals memory map...*continued*

APB bridge	Non-secure base address	Secure base address	Peripheral
	0x4002 C000	0x5002 C000	RTC & Wake-up timer.
	0x4002 D000	0x5002 D000	OS_Event Timer.
	0x4003 4000	0x5003 4000	Flash controller.
	0x4003 5000	0x5003 5000	PRINCE dynamic encrypt/decrypt
	0x4003 8000	0x5003 8000	USB HS Phy.
	0x4003 A000	0x5003 A000	True Random Number Generator.
	0x4003 B000	0x5003 B000	PUF (Physical Unclonable Function).
	0x4003 D000	0x5003 D000	PLU (Programmable Logic Unit).

7.20 AHB peripherals

Table 8 provides details of the addresses for AHB peripherals. AHB peripherals have both secure and non-secure access possibilities.

Table 8. AHB peripheral memory map

AHB port	Non-secure base address	Secure base address	Peripheral
8	0x4008 2000	0x5008 2000	DMA0 registers.
	0x4008 4000	0x5008 4000	FS USB Device registers.
	0x4008 5000	0x5008 5000	SCTimer/PWM.
	0x4008 6000	0x5008 6000	Flexcomm Interface 0.
	0x4008 7000	0x5008 7000	Flexcomm Interface 1.
	0x4008 8000	0x5008 8000	Flexcomm Interface 2.
	0x4008 9000	0x5008 9000	Flexcomm Interface 3.
	0x4008 A000	0x5008 A000	Flexcomm Interface 4.
	0x4008 B000	0x5008 B000	Inter-CPU Mailbox.
	0x4008 C000	0x5008 C000	High Speed GPIO.
9	0x4009 4000	0x5009 4000	HS USB device registers.
	0x4009 5000	0x5009 5000	CRC Engine.
	0x4009 6000	0x5009 6000	Flexcomm Interface 5.
	0x4009 7000	0x5009 7000	Flexcomm Interface 6.
	0x4009 8000	0x5009 8000	Flexcomm Interface 7.
	0x4009 B000	0x5009 B000	SDIO registers.
	0x4009 C000	0x5009 C000	Debug Mailbox (DM-AP).
	0x4009 F000	0x5009 F000	High Speed SPI.
10	0x400A 0000	0x500A 0000	ADC0.
	0x400A 2000	0x500A 2000	FS USB Host registers.
	0x400A 3000	0x500A 3000	HS USB Host registers.

Table 8. AHB peripheral memory map...*continued*

AHB port	Non-secure base address	Secure base address	Peripheral
	0x400A 4000	0x500A 4000	Hash-AES registers.
	0x400A 5000	0x500A 5000	Casper
	0x400A 6000	0x500A 6000	PowerQuad
	0x400A 7000	0x500A 7000	DMA1 registers.
	0x400A 8000	0x500A 8000	Secure HS GPIO.
	0x400A C000	0x500A C000	Security Control registers.
11	0x4010 0000	0x5010 0000	USB SRAM.

7.21 RAM configuration

Table 9 describes the RAM configuration for the LPC55S6x.

Table 9. RAM Configuration

RAM Total	RAM-X (KB)	RAM0 (KB)	RAM1 (KB)	RAM2 (KB)	RAM3 (KB)	RAM4 (KB)	USB-RAM (KB)
320 KB devices	32	64	64	64	64	16	16
256 KB devices	32	64	64	64	-	16	16
144 KB devices	32	64	32	-	-	-	16

7.22 System control

7.22.1 Clock sources

The LPC55S6x supports 2 external and 3 internal clock sources:

- Internal Free Running Oscillator (FRO). This oscillator provides a selectable 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to +/- 2% accuracy over the entire voltage and -40 C to 105 C. For devices with date code 2041 (yyww)and onwards, the FRO is trimmed to +/- 1% accuracy over the entire voltage and 0 C to 85 C. The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.
- 32 kHz Internal Free Running Oscillator FRO. The FRO is trimmed to +/- 2% accuracy over the entire voltage and temperature range.
  Internal low power oscillator (FRO 1 MHz). The FRO is trimmed to +/- 15% accuracy over the entire voltage and temperature range.
- Crystal oscillator with an operating frequency of 16 MHz to 32 MHz. Option for external clock input (bypass mode) for clock frequencies of up to 25 MHz
  Crystal oscillator with 32.768 KHz operating frequency. Option for external clock input (bypass mode) for clock frequencies of up to 100 kHz
- Each crystal oscillator has one embedded capacitor bank which can be used as an integrated load capacitor. Using APIs, the capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) which conserves board space and reduces costs.

7.22.2 PLL (PLL0 and PLL1)

PLL0 and PLL1 allows CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. PLL0 and PLL1 can run from the internal FRO 12 MHz output, the external oscillator, internal FRO 1 MHz output, or the 32.768 KHz RTC oscillator.

The system PLL accepts an input clock frequency in the range of 2 kHz - 150 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The PLL can be enabled or disabled by software.

7.22.3 Clock generation

The system control block facilitates the clock generation. Many clocking variations are possible. Figure 7 gives an overview of potential clock options. Table 10 describes signals on the clocking diagram. The maximum clock frequency is 150 MHz.

Remark: The indicated clock multiplexers shown in Figure 7 are synchronized. In order to operate, the currently selected clock must be running, and the clock to be switched to must also be running. This is so that the multiplexer can gracefully switch between the two clocks without glitches. Other clock multiplexers are not synchronized. The output divider can be stopped and restarted gracefully during switching if a glitch-free output is needed.

The low-power oscillator provides a frequency in the range of 1 MHz. The accuracy of this clock is limited to +/- 15% over temperature, voltage, and silicon processing variations after trimming made during assembly. To determine the actual watchdog oscillator output, use the frequency measure block.

The part contains one system PLL that can be configured to use a number of clock inputs and produce an output clock in the range of 1.2 MHz up to the maximum chip frequency, and can be used to run most on-chip functions. The output of the PLL can be monitored through the CLKOUT pin.

Table 10. Clocking diagram signal name descriptions

Name	Description
32k_osc	The 32 kHz output of the RTC oscillator. The 32 kHz clock must be enabled in the RTCOSCCTRL register.
clk_in	This is the internal clock that comes from the external oscillator.
frg_clk	The output of each Fractional Rate Generator to Flexcomm clock. Each FRG and its source selection is shown in Figure 7.
fro_12m	12 MHz divided down from the currently selected on-chip FRO oscillator.
fro_hf	The currently selected FRO high speed output at 96 MHz.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others. The main clock and its source selection are shown in Figure 7.
mclk_in	The MCLK input function, when it is connected to a pin by selecting it in the IOCON block.
pll0_clk	The output of the PLL0. The PLL0 and its source selection is shown in Figure 7.
pll1_clk	The output of the PLL1. The PLL1 and its source selection is shown in Figure 7.
fro_1m	The output of the low power oscillator.
"none"	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.

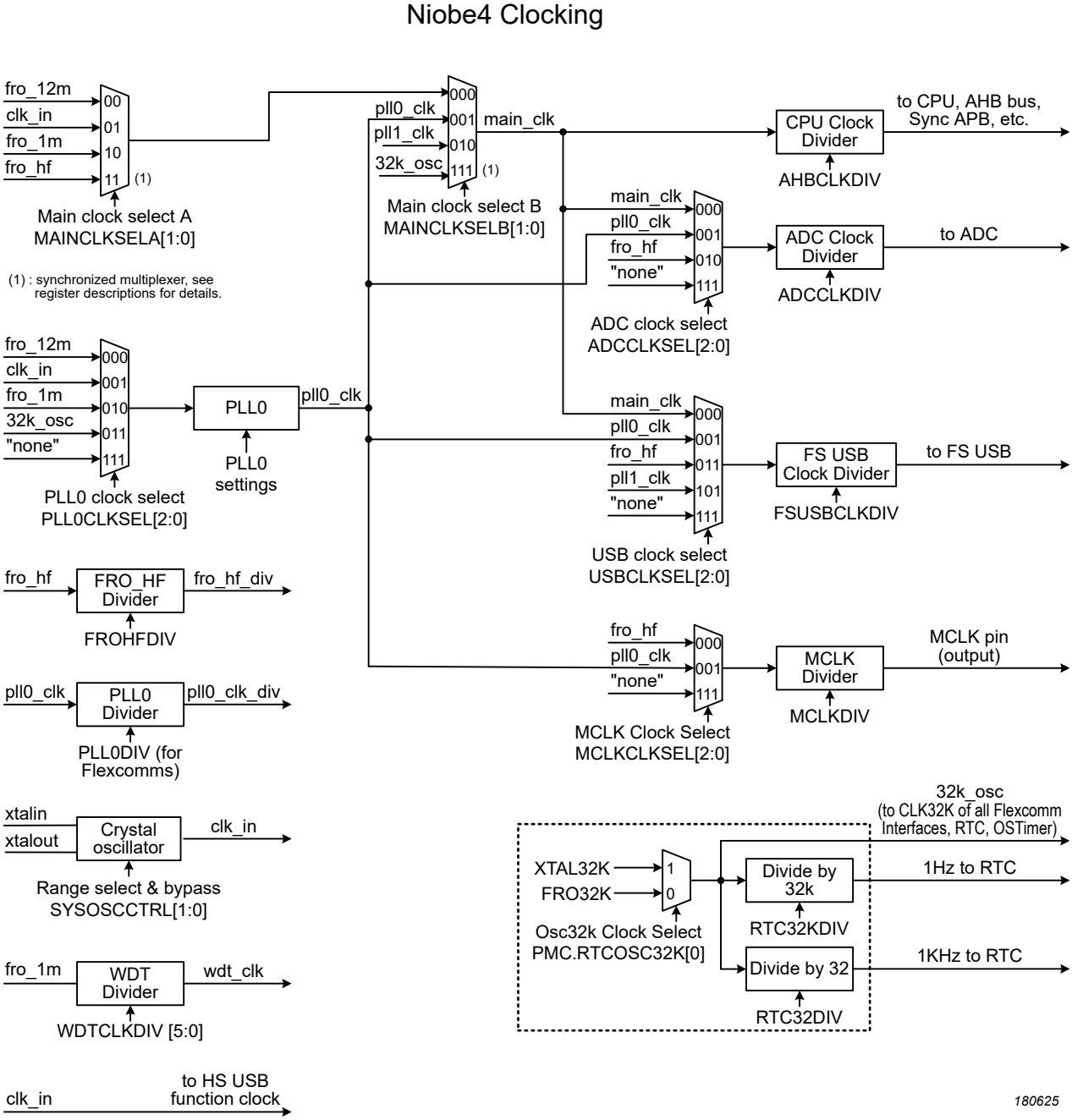


Figure 7. Clock generation (Part 1 of 2)

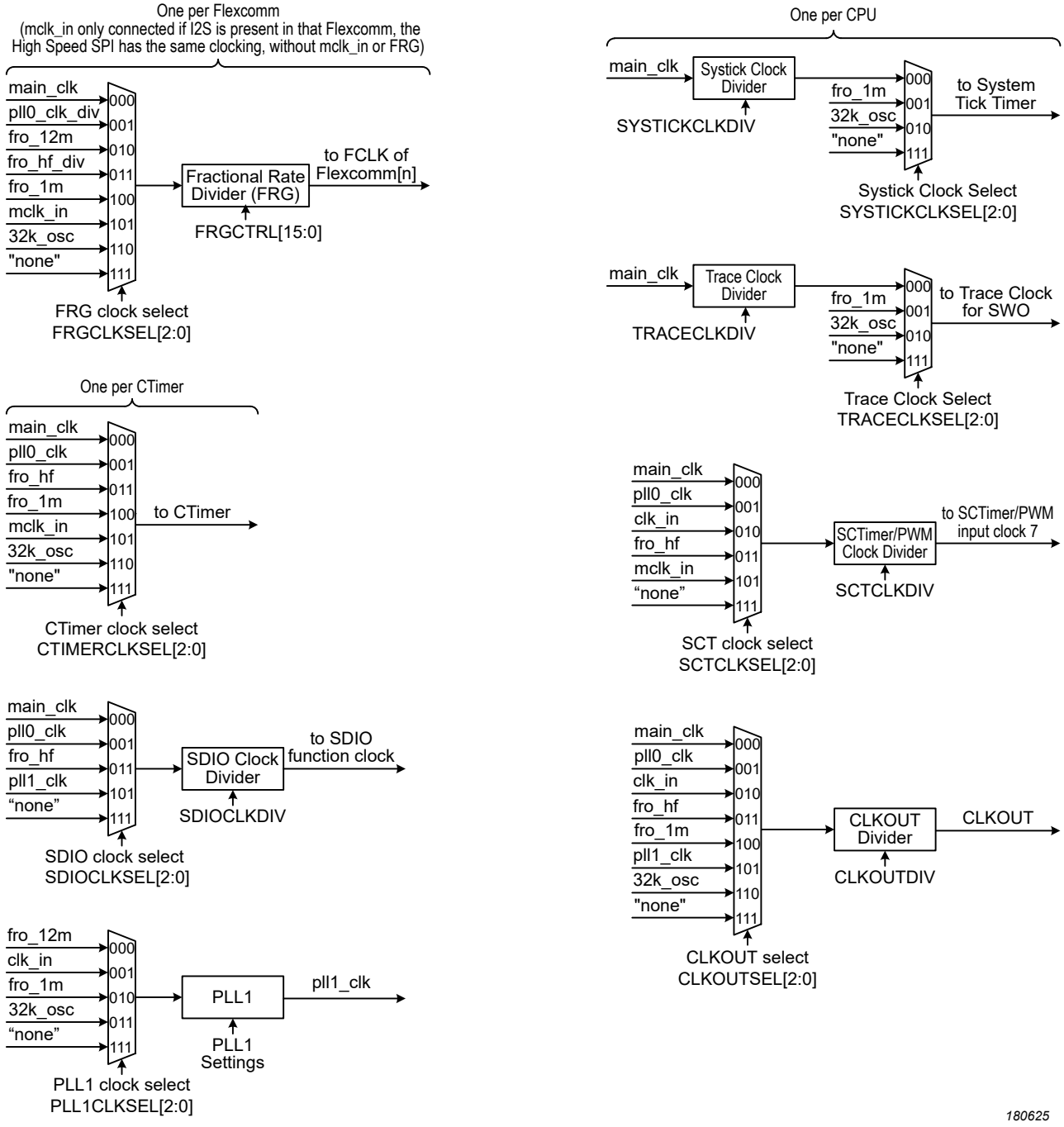


Figure 8. Clock generation (Part 2 of 2)

7.22.4 Brownout detection

The LPC55S6x includes one Brown-out detector to monitor the voltage of VBAT. If the voltage falls below one of the selected voltages, the BOD asserts an interrupt to the NVIC or issues a reset.

7.23 Power control

The LPC55S6x support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are four special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, power-down mode, and deep power-down mode which can be activated by the power mode configure API.

7.23.1 Sleep mode

In sleep mode, the system clock to both CPUs (CPU0 and CPU1) are stopped and execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals.

7.23.2 Deep-sleep mode

In deep-sleep mode, the flash is powered down. The system clock to both CPUs (CPU0 and CPU1) are stopped and if not configured, the peripherals receives no clocks. Through the power profiles API, selected peripherals such as USB0, USB1, Flexcomm interfaces 0 to 7 (SPI, I2C, USART, I2S), Flexcomm interface 10 (High Speed SPI), Micro-tick, WWDT, RTC, OSTimer, Standard Timers, comparator, and BOD can be left running in deep-sleep mode. Clock sources such as FRO12 MHz, FRO 32 KHz, FRO 1 MHz, the 32.768 kHz RTC clock, and the external oscillator can be enabled or disabled via software.

The LPC55S6x can wake up from deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block and group interrupt block, OS Timer, Standard Timers, Micro-tick, RTC alarm, a watchdog timer interrupt/reset, BOD interrupt/reset, an interrupt from the USB0, USB1, SPI, I2C, I2S, USART, comparator, and PLU. Some peripherals can have DMA service during deep-sleep mode without waking up entire device.

In deep-sleep mode, all SRAM, GPIO logic state, and registers maintain their internal states. All SRAM instances that are not configured to enter in ‘retention state’ will stay in active state. Deep-sleep mode allows for very low quiescent power and fast wake-up options.

7.23.3 Power-down mode

In power-down mode, nearly all on-chip power consumption is turned off by shutting down the internal DC-DC converter. The flash is powered down. The system clock to both CPUs (CPU0 and CPU1) are stopped and if not configured, the peripherals receives no clocks. Through the power profiles API, selected peripherals such as Flexcomm interfaces 3 (SPI, I2C, USART, I2S), RTC, OS Timer, and comparator can be left running in power-down mode. Clock sources such as FRO 32 KHz, and the 32.768 kHz RTC clock can be enabled or disabled via software.

The LPC55S6x can wake up from power-down mode via a reset, digital pins selected as inputs to the group interrupt block, OS Timer, RTC alarm, an interrupt from the Flexcomm Interface 3 (SPI, I2C, I2S, USART), and comparator.

In power-down mode, the CPU0 processor state is retained to allow resumption of code execution when a wake-up event occurs.

All SRAM can be configured to maintain their internal state as long as it is configured to do so using power API call. The GPIO logic level does not remain static in power-down mode. All GPIO pin state will be logic '0' in power- down mode.

All IOCON registers and peripheral registers related ONLY to Flexcomm3 (SPI, I2C, I2S, USART), GINTO0, RTC, OS Event timer, and analog comparator will maintain state in power-down mode.

7.23.4 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain, the $\overline{\text{RESET}}$ pin, 4 Wake-up pins, and the OT Timer if enabled. Clock sources such as FRO 32 KHz, and the 32.768 kHz RTC clock can be enabled or disabled via software. The LPC55S6x can wake up from deep power-down mode via the $\overline{\text{RESET}}$ pin, the RTC alarm, four special wake-up pins, or without an external signal, by using the time-out of the OS Timer. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. SRAM can maintain their internal states. All SRAM instances that are not configured to enter in 'retention state' will stay in active state. In deep power-down mode all functional pins are in tri-state.

7.24 General Purpose I/O (GPIO)

The LPC55S6x provide GPIO ports 0 and 1 with a total of 64 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 3 for the default state on reset.

7.24.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set, clear, and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- Two GPIO group interrupts can be triggered by a combination of any pin or pins to reflect two distinct interrupt patterns.
- The grouped interrupts can wake up the part from sleep, deep-sleep, and power-down modes.

7.25 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.25.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.

- Level-sensitive interrupt pins can be HIGH-active or LOW-active.
- Level-sensitive interrupt pins can be HIGH-active or LOW-active.
- Pin interrupts can wake up the device from sleep mode, and deep-sleep mode.

- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.26 Communication peripherals

7.26.1 Full-speed USB Host/Device Interface (USB0)

The USB is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.26.1.1 USB0 device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. Itconsists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- USB2.0 full-speed device controller supporting crystal-less operation in device mode using software library example in technical note (TN00063).
- Supports ten physical (five logical) endpoints including one control endpoint.
- Single and double-buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from Deep-sleep mode on USB activity and remote wake-up.
- Supports SoftConnect.
- Link Power Management (LPM) supported.

7.26.1.2 USB0 host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

Features

- OHCI compliant.
- Two downstream ports.

7.26.2 High-Speed USB Host/Device Interface (USB1)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.26.2.1 USB1 device controller

The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Fully compliant with USB 2.0 Specification (high speed).
- Supports 12 physical (6 logical) endpoints with up to 8 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- While USB is in the Suspend mode, the LPC55S6x can enter deep-sleep mode and wake up on USB activity.
- Double buffer implementation for Bulk and Isochronous endpoints

7.26.2.2 USB1 host controller

The host controller enables high speed data exchange with USB devices attached to the bus. It consists of register interface and serial interface engine. The register interface complies with the Enhanced Host Controller Interface (EHCI) specification

Features

- EHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.26.3 Flexcomm Interface serial communication

Each Flexcomm Interface provides a choice of peripheral functions, one of which must be chosen by the user before the function can be configured and used.

7.26.3.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Flexcomm interfaces 0 to 7 each provide one channel pair of I^2S.
- Data for USART, SPI, and I2S traffic uses the Flexcomm FIFO. The I^2C function does not use the FIFO.

7.26.3.2 SPI serial I/O (SPIO) controller

Features

- Maximum supported bit rate for SPI master mode (transmit/receive) is 32 Mbit/s. The maximum supported bit rate for SPI slave receive mode is 25 Mbit/s and for SPI slave transmit mode is 16 Mbits/s.
- Master and slave operation.
- Data frames of 4 to 16 bits supported directly. Larger frames supported by software.
- The SPI function supports separate transmit and receive FIFOs with eight entries each.
- Supports DMA transfers: SPIn transmit and receive functions can operated with the system DMA controller.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Up to Four Slave Select input/outputs with selectable polarity and flexible usage.

7.26.3.3 I^2C-bus interface

The I^2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for exanple, an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

Features

- Support standard, Fast-mode, and Fast-mode Plus (specific I2C pins) with data rates of up to 1 Mbit/s.
- Support high-speed slave mode with data rates of up to 3.4 Mbit/s (specific I2C pins).
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I^2C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I^2C-bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Separate DMA requests for master, slave, and monitor functions.
- No chip clocks are required in order to receive and compare an address as a slave, so this event can wake-up the device from deep-sleep mode.
- Automatic modes optionally allow less software overhead for some use cases.

7.26.3.4 USART

Features

- Maximum bit rates of 10 Mbit/s in asynchronous mode and 25 Mbit/s in synchronous mode for USART functions.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.

- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and deep-sleep2 modes.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.
- The USART function supports separate transmit and receive FIFO with 16 entries each.

7.26.3.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus with one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer in addition to other configurations. Each Flexcomm Interface implements one I^2S channel pair.

The I^2S interface within one Flexcomm Interface provides one channel pair that can be configured as a master or a slave. The channel pair within one Flexcomm Interface shares one set of I^2S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration, and frame configuration. All such channel pairs can participate in a Time Division Multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I^2S block in the system level clocking scheme.

Features

- A Flexcomm Interface can implement one or more I^2S channel pairs, the first of which could be a master or a slave, and the rest would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes.
- Flexcomm interfaces 0 to 7 each provide one channel pair of I^2S function.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I^2S traffic within one Flexcomm Interface uses the Flexcomm FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.

- Sampling frequencies supported depends on the specific device configuration and applications constraints (For example, system clock frequency and PLL availability) but generally supports standard audio data rates.

7.26.4 High-speed SPI serial I/O controller

7.26.4.1 Features

- Master and slave operation.
- The maximum supported bit rate for SPI master mode (transmit/receive) and slave mode (transmit/receive) is 50 Mbit/s.
- Data frames of 4 to 16 bits supported directly. Larger frames supported by software.
- The SPI function supports separate transmit and receive FIFOs with eight entries each.
- Supports DMA transfers: SPIn transmit and receive functions can operated with the system DMA controller.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Up to Four Slave Select input/outputs with selectable polarity and flexible usage.

7.27 SDIO/MMC interface

Secured digital input/output (SD/MMC and SDIO) card interface with DMA support. SDIO with support for up to two cards. Supported card types are MMC, SDIO, and CE-ATA. Supports SD2.0, and SDR25 (52MHz).

7.27.1 Features

- Secure Digital memory protocol commands.
- Secure Digital I/O protocol commands.
- Multimedia Card protocol commands.
- CE-ATA digital protocol commands.
- Two SD or MMC (4.4), CE-ATA (1.1), or eMMC (4.4) device.
- CRC 2.0 generation and error detection.
- SDIO interrupts in 1-bit and 4-bit modes.
- Block size of 1 to 65,535 bytes.
- Internal (bus mastering) DMA.
- Two FIFOs, TX and RX FIFO (FIFO depth = 32 and FIFO data width = 32 bits).

7.28 Standard counter/timers (CT32B0 to 4)

The LPC55S6x includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.28.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- The timer and prescaler may be configured to be cleared on a designated capture

event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs per timer corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.
- Up to 4 match registers can be configured for PWM operation, allowing up to 3 single edged controlled PWM outputs.WM mode using up to three match channels for PWM output.

7.28.2 SCTimer/PWM subsystem

The SCTimer/PWM is a flexible timer module capable of creating complex PWM waveforms and performing other advanced timing and control operations with minimal or no CPU intervention.

The SCTimer/PWM can operate as a single 32-bit counter or as two independent, 16-bit counters in uni-directional or bi-directional mode. It supports a selection of match registers against which the count value can be compared, and capture registers where the current count value can be recorded when some pre-defined condition is detected.

The SCTimer/PWM module supports multiple separate events that can be defined by the user based on some combination of parameters including a match on one of the match registers, and/or a transition on one of the SCTimer/PWM inputs or outputs, the direction of count, and other factors.

Every action that the SCTimer/PWM block can perform occurs in direct response to one of these user-defined events without any software overhead. Any event can be enabled to:

- Start, stop, or halt the counter.
- Limit the counter which means to clear the counter in unidirectional mode or change its direction in bi-directional mode.
- Set, clear, or toggle any SCTimer/PWM output.
- Force a capture of the count value into any capture registers.
- Generate an interrupt of DMA request.

7.28.2.1 Features

- The SCTimer/PWM Supports:
  - Eight inputs.
  - Ten outputs.
  - Sixteen match/capture registers.
  - Sixteen events.
  - Thirty two states.
- Counter/timer features:
  - Each SCTimer/PWM is configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by system clock or selected input.
  - Configurable number of match and capture registers. Up to sixteen match and capture registers total.
  - Sixteen events.

- Thirty two states.
- Upon match and/or an input or output transition create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs; change the state.
- Counter value can be loaded into capture register triggered by a match or input/output toggle.

- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to ten single-edge or eight dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.

7.28.3 Windowed WatchDog Timer (WWDT)

The purpose of the Watchdog Timer is to reset or interrupt the microcontroller within a programmable time if it enters an erroneous state. When enabled, a watchdog reset is generated if the user program fails to feed (reload) the Watchdog within a predetermined amount of time.

7.28.3.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks (TWDCLK × 256 × 4) to over 67 million watchdog clocks (TWDCLK × 224 × 4) in increments of four watchdog clocks.
- "Safe" watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog event if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the "warning interrupt" time is reached.
- Flag to indicate Watchdog reset.
- The watchdog clock (WDCLK) is generated from always on FRO_1MHz clock which can be divided by WDT clock divider register. The accuracy of this clock is limited to +/- 15% over temperature, voltage, and silicon processing variations.
- The Watchdog timer can be configured to run in Deep-sleep mode.
- Debug mode.

7.28.4 RTC timer

The RTC block to count seconds and generate an alarm interrupt to the processor whenever the counter value equals the value programmed into the associated 32-bit match register.

7.28.4.1 Features

- The RTC oscillator has the following clock outputs: 32.768 kHz clock (named as 32 kHz clock in rest of this chapter) 32 kHz clock, selectable for system clock and CLKOUT pin, 1 Hz clock for RTC timing, and 1024 Hz clock (named as 1 kHz clock in rest of this chapter) for high-resolution RTC timing.
- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- 15-bit, 32KHz sub-second counter.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests that go to one NVIC channel. Either time-out can wake up the part from any of the low power modes, including deep power-down.
- Eight 32-bit general purpose registers can retain data in deep power-down. These registers are reset only on software reset of the RTC.

7.28.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.28.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat interrupt, one-shot interrupt, and one-shot bus stall modes.

7.28.6 OS Timer

42-bit free running timer with individual match/capture and interrupt generation logic used as continuous time-base for the system, available in any reduced power modes. It runs on 32kHz clock source, allowing a count period of more than 4 years.

7.28.6.1 Features

- Central 42-bit, free-running gray-code event/timestamp timer.
  Match registers compared to the main counter to generate an interrupt and/or wake-up event.
- Capture registers triggered by CPU command, readable via the AHB/IPS bus.
- APB interface for register access.
- IRQ and wake-up.
- Reads of gray-encoded timers are accomplished with no synchronization latency.

7.28.7 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from sleep and deep-sleep modes.

7.28.7.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.
- Four capture registers that can be triggered by external pin transitions.

7.29 Digital peripherals

7.29.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

Two identical DMA controllers are provided on the LPC55S6x. The user may elect to dedicate one of these to CPU0 and the other for use by the CPU1 and/or one may be used as a secure DMA the other non-secure.

7.29.1.1 Features

- DMA0: 22 channels, 21 of which are connected to peripheral DMA requests. These come from the Flexcomm (USART, SPI, I2C, and I2S), high-speed SPI interface, ADC, AES, and SHA interfaces. 22 trigger sources are available.
- DMA1: 10 channels, 9 of which are connected to peripheral DMA requests. These come from the Flexcomm Interfaces (0, 1, and 3), high-speed SPI interface, AES, and SHA interfaces. 15 trigger sources are available.
- DMA operations can be triggered by on-chip or off-chip events.
- Priority is user selectable for each channel (up to eight priority levels).
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.29.2 Programmable Logic Unit (PLU)

The PLU is comprised of 26 5-input LUT elements. Each LUT element contains a 32-bit truth table (look-up table) register and a 32:1 multiplexer. During operation, the five LUT inputs control the select lines of the multiplexer. This structure allows any desired logical combination of the five LUT inputs.

7.29.2.1 Features

- The Programmable Logic Unit is used to create small combinatorial and/or sequential logic networks including simple state machines.
- Eight primary outputs can be selected using a multiplexer from among all of the LUT outputs and the four flip-flops.
- An external clock to drive the four flip-flops must be applied to the PLU_CLKIN pin if a sequential network is implemented.
- Programmable logic can be used to drive on-chip inputs/triggers through external pin-to-pin connections.
- A tool suite is provided to facilitate programming of the PLU to implement the logic network described in a Verilog RTL design.
- Any of the eight selected PLU outputs can be enabled to contribute to an asynchronous wake-up or an interrupt request from sleep and deep-sleep modes.

7.29.3 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.29.3.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT : $x^{16} + x^{12} + x^5 + 1$
  - CRC-16 : $x^{16} + x^{15} + x^2 + 1$
  - CRC-32 : $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write : 1-cycle operation.
  - 16-bit write : 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.30 Analog peripherals

7.30.1 16-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 16-bit and fast conversion rates of up to 1.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources.

7.30.1.1 Features

- 16-bit Linear successive approximation algorithm.
- Differential operation with 16-bit or 13-bit resolution.
- Single-ended operation with 16-bit or 12-bit resolution.
- Support for simultaneous conversions, on two ADC input channels belonging to a differential pair.
- Channel support for up to 10 analog input channels for conversion of external pin and from internal sources.
- Select external pin inputs paired for conversion as differential channel input.
- Measurement of on-chip analog sources such as DAC, temperature sensor or bandgap.
- Configurable analog input sample time.
- Configurable speed options to accommodate operation in low power modes of SoC.
- Trigger detect with up to 16 trigger sources with priority level configuration. Software or hardware trigger option for each.
- Fifteen command buffers allow independent options selection and channel sequence scanning.
- Automatic compare for less-than, greater-than, within range, or out-of-range with "store on true" and "repeat until true" options.
- Two independent result FIFOs each contains 16 entries. Each FIFO has configurable watermark and overflow detection.
- Interrupt, DMA, or polled operation.
- Linearity and gain offset calibration logic.

7.30.2 Comparator

The analog comparator can compare voltage levels on external pins and internal voltages. The comparator has five inputs multiplexed separately to its positive and negative inputs.

7.30.2.1 Features

- Selectable external inputs can be used as either the positive or negative input of the comparator.
  Voltage ladder source selectable between the supply, multiplexing between internal VBAT_PMU and ACMPVREF.
  32-stage voltage ladder can be used as either the positive or negative input of the comparator.
- Supports standard and low power modes
- Interrupt capability.

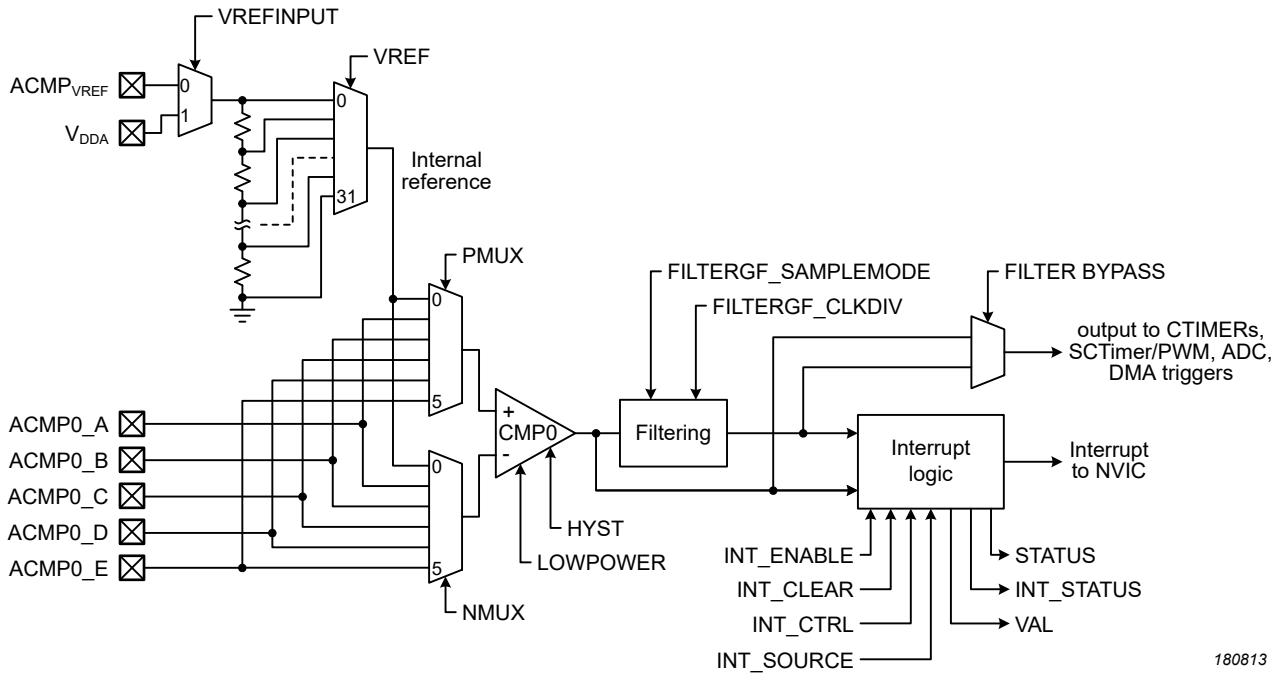


Figure 9. Comparator block diagram

7.30.3 Temperature sensor

The ADC has a dedicated input channel for an on-chip temperate sensor that is mapped on channel 26.

7.31 Security Features

The security system on LPC55S6xLPC55S6x has a set of hardware blocks and ROM code to implement the security features of the device. The hardware consists of an AES engine, a Secure Hash Algorithm (SHA) engine, a Random Number Generator (RNG), a PRINCE engine for real-time flash encryption/decryption, and a key storage block that keys from an SRAM based PUF (Physically Unclonable Function). All components of the system can be accessed by the processor or the DMA engine to encrypt or decrypt data and for hashing. The ROM is responsible for secure boot in addition to providing support for various security functions.

7.31.1 AES engine

The LPC55S6xx devices provide an on-chip hardware AES encryption and decryption engine to protect the image content and to accelerate processing for data encryption or decryption, data integrity, and proof of origin. Data can be encrypted or decrypted by the AES engine using a key from the PUF or a software supplied key. The AES engine supports 128 bit, 192 bit, or 256 bit keys for encryption and decryption operations.

7.31.1.1 Features

- Encryption and decryption of data.
- Secure storage of AES key that cannot be read.
- Supports 128 bit, 192 bit or 256 bit key in Electronic Code Book (ECB) mode, Cipher Block Chaining (CBC) mode, and Counter (CTR) mode.
- Supports 128-bit key in ICB (Indexed Code Book) mode, that offers protection against side-channel attacks.
- Compliant with the FIPS (Federal Information Processing Standard) Publication 197, Advanced Encryption Standard (AES).
- It may use the processor, DMA, or AHB Master for data movement. AHB Master may only be used to load data, DMA may be used to read-out results. DMA based result reading is a "trigger", so the application must set the size correctly.

7.31.2 HASH engine

The LPC55S6x devices provide on-chip Hash support to perform SHA-1 and SHA-2 with 256-bit digest (SHA-256). Hashing is a way to reduce arbitrarily large messages or code images to a relatively small fixed size "unique" number called a digest. The SHA-1 Hash produces a 160 bit digest (five words), and the SHA-256 hash produces a 256 bit digest (eight words).

7.31.2.1 Features

- Performs SHA-1 and SHA-2(256) based hashing.
- Used with HMAC to support a challenge/response or to validate a message.

7.31.3 PUF

The PUF controller on the LPC55S6x provides generation and secure storage for keys without storing the key. The PUF controller provides a unique key per device and exists in that device based on the unique characteristics of PUF SRAM. Instead of storing the key, a Key Code is generated, which in combination with the digital fingerprint is used to reconstruct keys that are routed to the AES engine, for use by software, and by PRINCE engine. PUF keys have a dedicated path to the AES engine and PRINCE engine. There is no other mechanism by which keys can be observed.

7.31.3.1 Features

- Key strength of 256-bits.
- The PUF constructs 256-bit strength device unique PUF root key using the digital fingerprint of a device derived from SRAM and error correction data called Activation Code (AC). The Activation Code (AC) is generated during enrollment process. The Activation Code (AC) should be stored on external non-volatile memory device in the system.
- Generation, storage, and reconstruction of keys.
- Key sizes from 64 bits to 4096 bits.
- PUF controller allows storage of keys, generated externally or on chip, of sizes 64 bits to 4096 bits.

- PUF controller combines keys with digital fingerprint of device to generate key codes. These key codes should be provided to the controller to reconstruct original key. They can be stored on external non-volatile memory device in the system.
- Key output via dedicated hardware interface or through register interface.
- PUF controller allows to assign a 4-bit index value for each key while generating key codes. Keys that are assigned index value zero are output through HW bus, accessible to AES and PRINCE engines only. Keys with non-zero index are available through APB register interface.
- 32-bit APB interface.

7.31.4 Random Number Generator

The True Random Number Generators (TRNG) module is a hardware accelerator module that generate 256-bit entropy. The purpose of the module is to generate high quality, cryptographically secure, random data.

Random number generators are used for data masking, cryptographic modeling and simulation applications that employ keys that must be generated in a random fashion. The chip embeds a hardware IP that, combined with appropriate software and the availability of a stochastic model, can be used to generate random numbers.

7.31.5 PRINCE On-the-fly encryption/decryption

LPC55S6x devices offer support for on-the-fly encryption of date being written to flash and decryption of encrypted on-chip flash data during read using the PRINCE encryption algorithm. Compared to AES, PRINCE is fast as it can decrypt and encrypt in one clock cycle. Also, it does not need extra SRAM to copy data. It operates on a block-size of 64 bits with an 128-bit key. This functionality is useful for asset protection, such as securing application code, securing stored keys and enabling secure flash update.

7.31.6 Universally Unique Identifier (UUID)

Each LPC55S6x device consists of a unique 128-bit IETF RFC4122 compliant non-sequential UUID. It can be read from the protected flash region (register location 0x0009_FC70 onwards).

7.31.7 Device Identifier Composition Engine (DICE)

The LPC55S6x (secure part) supports Device Identifier Composition Engine (DICE) to provide Composite Device Identifier (CDI). The CDI value is available at SYSCON for consumption after boot completion. It is recommended to overwrite these registers once ephemeral key-pairs are generated using this value.

7.32 Debug Mailbox and Authentication

The Debugger Mailbox (DM) AP offers a register based mailbox accessible by both CPUs and the device debug port DP of the MCU. This port is always enabled and external world can send and receive data to/from ROM. This port is used to implement NXP Debug Authentication Protocol. BootROM implements debug mailbox protocol to interact with tools over SWD interface. LPC55S6x offers a debug authentication protocol as a tool to authenticate the debugger and grant it access to the device. The debug authentication scheme on LPC55S6x is a challenge-response scheme and assures that debugger in possession of required debug credentials only can successfully authenticate over debug interface and access restricted parts of the device. This protocol provides a mechanism for a device and its debug interface to authenticate the identity and credentials of the debugger (or user). Access right settings can be pre-configured and gets loaded into register above upon successful debug authentication. Until debug authentication process is successfully completed, secure part of the device is non-accessible to the debugger.

7.33 Emulation and debugging

Debug and trace functions are integrated into the Arm Cortex-M33 (CPU0 and CPU1) Serial wire debug and trace function (Serial Wire Output) are supported. Eight breakpoints and four watch points are supported. In addition, JTAG boundary scan mode is provided.

The Arm SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

8 Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	Main IO supply		[2]	-0.3	3.96	V
VBAT_DCDC	Supply of DCDC output stage. DCDC core supply (references and regulation stages)		[2]	-0.3	3.96	V
VBAT_PMU	Analog supply		[2]	-0.3	3.96	V
VDD_PMU	Analog supply for Core. DCDC output		[2]	-0.3	1.26	V
USB0_3V3	USB0 analog 3.3 V supply.		[2]	-0.3	3.96	V
USB1_3V3	USB1 analog 3.3 V supply.		[2]	-0.3	3.96	V
V_{DDA}	Analog supply voltage for ADC		[2]	-0.3	3.96	V
V_{refp}	ADC positive reference voltage		[2]	-0.3	3.96	V
V_I	input voltage	only valid when the $V_{DD} \geq 1.8$ V		-0.5	V_{DD} + 0.5	V
V_I	input voltage	on I2C open-drain pins	[3]	-0.5	V_{DD} + 0.5	V
		USB_DM, USB_DP pins		-0.3	USB_3V3 + 0.5	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[4][5]	-0.3	3.96	V
I_{DD}	total supply current	per supply pin (HLQFP100, VFBGA98, and VFBGA59)		-	256	mA
I_{SS}	total ground current	per ground pin (HLQFP100, VFBGA98, and VFBGA59)		-	256	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature			-65	+150	°C

Table 11. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[6]		2000	V
V_{ESD}	electrostatic discharge voltage	charge device model; all pins	[6]		500	V

[1] The following applies to the limiting values:
1. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 24.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 24) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[4] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[5] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

9 Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:–

$$T_j = T_{amb} + \left(P_D \times R_{th(j-a)}\right) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 12. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
HLQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient [1]	JESD51-9, 2s2p[2]	27	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case [3]	JESD51-9[2]	2.0	°C/W
VFBGA98 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient [1]	JESD51-9, 2s2p[2]	56	°C/W
$R_{th(j-c)}$	Junction-to-Top of Package Thermal Characterization Parameter [3]	JESD51-9[2]	0.7	°C/W
HTQFP 64 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient [1]	JESD51-9, 2s2p[2]	28	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case [3]	JESD51-9[2]	0.3	°C/W

Table 12. Thermal resistance*...continued*

Symbol	Parameter	Conditions	Max/Min	Unit
VFBGA 59 Package				
$R_{th(j-a)}$	Thermal resistance from junction to ambient	JESD51-9, 2s2p[2]	47.9	°C/W
Ψ_{JT}	Junction-to-Top of Package Thermal Characterization Parameter	JESD51-9, 2s2p	0.2	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
[2] Thermal test board meets JEDEC specification for this package (JESD51-9).
[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. Case is defined as the bottom of the packages (exposed pad)

Table 13. Maximum Junction Temperature

Symbol	Parameter	Conditions	Max	Unit
T_{jmax} (Device)	maximum junction temperature for Device	Device operating per datasheet spec	+ 107	°C
T_{jmax} (Silicon Process)	maximum junction temperature for Silicon Process	Device operating, datasheet specifications not guaranteed	+ 125	°C

10 Static characteristics

10.1 General operating conditions

Table 14. General operating conditions

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{clk}	clock frequency	internal CPU/system clock	-	-	150 [2] [3]	MHz
f_{clk}	clock frequency	For USB high-speed device and host operations	90	-	150 [2] [3]	MHz
f_{clk}	clock frequency	For USB full-speed device and host operations	12	-	150 [2] [3]	MHz
V_{DD}	Main IO supply		1.8	-	3.6	V
VBAT_DCDC	Supply of DCDC output stage. DCDC core supply (references and regulation stages)		1.8	-	3.6	V
VBAT_PMU	Analog supply		1.8	-	3.6	V
VDD_PMU [4]	Analog supply for Core. DCDC output		1.0	-	1.2	V
USB0_3V3	USB0 analog 3.3 V supply.		3.0	-	3.6	V
USB1_3V3	USB1 analog 3.3 V supply.		3.0	-	3.6	V
V_{DDA}	Analog supply voltage for ADC		1.8	-	3.6	V
V_{refp}	ADC positive reference voltage		0.985	-	V_{DDA}	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Device revision 1B operates at a maximum CPU frequency of up to 150 MHz. Device revision 0A operates at a maximum CPU frequency of up to 100 MHz.
[3] Flash operations (erase, blank check, program) and reading single word can only be performed for CPU frequencies of up to 100 MHz. Cannot be performed for frequencies above 100 MHz.
[4] For device revision 1B, power library in SDK sets the DCDC output based on the frequency selected. For frequencies 100 MHz or below, DCDC output is set between 1.0 V to 1.075 V, for frequencies between 101 MHz to 130 MHz, DCDC output is set between 1.025 V to 1.150 V and for frequencies above 130 MHz, DCDC output is set between 1.050 V to 1.2 V. For device revision 0A, the default typical DCDC output is 1.1 V and for device revision 1B, the typical default DCDC output is 1.0 V.

10.2 CoreMark data

Table 15. CoreMark score [1]

T_{amb} = 25°C, VBAT_PMU = VBAT_DCDC = VDD = 3.0 V

Parameter	Conditions		Typ [2]	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[3][4]	4.0	(Iterations/s) / MHz
	CCLK = 48 MHz	[3][4]	4.0	(Iterations/s) / MHz
	CCLK = 60 MHz	[3][4]	4.0	(Iterations/s) / MHz
	CCLK = 96 MHz	[3][4]	4.0	(Iterations/s) / MHz
	CCLK = 100 MHz	[4][5]	4.0	(Iterations/s) / MHz
	CCLK = 150 MHz	[4][5]	4.0	(Iterations/s) / MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 2 system clock flash access time.	[3][4][6]	3.6	(Iterations/s) / MHz
	CCLK = 48 MHz, 5 system clock flash access time.	[3][4][6]	3.0	(Iterations/s) / MHz
	CCLK = 60 MHz, 6 system clock flash access time.	[3][4][6]	2.5	(Iterations/s) / MHz
	CCLK = 96 MHz, 8 system clock flash access time.	[3][4][6]	2.3	(Iterations/s) / MHz
	CCLK = 100 MHz, 8 system clock flash access time.	[4][6][5]	2.3	(Iterations/s) / MHz
	CCLK = 150 MHz, 12 system clock flash access time.	[4][6][5]	2.0	(Iterations/s) / MHz

[1] For device revision 1B, power library in SDK sets the DCDC output based on the frequency selected. For frequencies 100 MHz or below, DCDC output is set between 1.0 V to 1.075 V, for frequencies between 101 MHz to 130 MHz, DCDC output is set between 1.025 V to 1.150 V and for frequencies above 130 MHz, DCDC output is set between 1.050 V to 1.2 V. For device revision 0A, the default typical DCDC output is 1.1 V and for device revision 1B, the typical default DCDC output is 1.0 V.
[2] Characterized through bench measurements using typical samples.
[3] Clock source FRO. PLL disabled
[4] Compiler settings: Keil v.5.28, optimization level 3, optimized for time on.
[5] PLL enabled
[6] See the FLASHCFG register in the LPC55S6x User Manual for system clock flash access time settings. Power Library in SDK sets the flash wait states based on the frequency selected.

10.3 Power consumption

Table 16. Static characteristics: Power consumption in active mode [1]

T_{amb} = -40 °C to +105 °C, unless otherwise specified. VBAT_PMU = VBAT_DCDC = VDD = 3.0 V

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down CCLK = 12 MHz	[3][4]	-	0.9	-	mA
		CCLK = 48 MHz	[3][4]	-	2.1	-	mA
		CCLK = 60 MHz	[3][4]	-	2.3	-	mA
		CCLK = 96 MHz	[3][4]	-	3.4	-	mA
		CCLK = 100 MHz	[4][5]	-	3.5	-	mA
		CCLK = 150 MHz	[4][5]	-	6.2	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 2 system clock flash access time.	[3][4][6]	-	0.95	-	mA
		CCLK = 48 MHz, 5 system clock flash access time.	[3][4][6]	-	2.4	-	mA
		CCLK = 60 MHz, 6 system clock flash access time.	[3][4][6]	-	2.6	-	mA
		CCLK = 96 MHz, 8 system clock flash access time.	[3][4][6]	-	3.4	-	mA
		CCLK = 100 MHz, 8 system clock flash access time.	[4][5][6]	-	3.5	-	mA
		CCLK = 150 MHz, 12 system clock flash access time.	[4][5][6]	-	5.9	-	mA

[1] For device revision 1B, power library in SDK sets the DCDC output based on the frequency selected. For frequencies 100 MHz or below, DCDC output is set between 1.0 V to 1.075 V, for frequencies between 101 MHz to 130 MHz, DCDC output is set between 1.025 V to 1.150 V and for frequencies above 130 MHz, DCDC output is set between 1.050 V to 1.2 V. For device revision 0A, the default typical DCDC output is 1.1 V and for device revision 1B, the typical default DCDC output is 1.0 V.
[2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[3] Clock source FRO. PLL disabled
[4] Compiler settings: IAR v.8.20.2., optimization level 0, optimized for time off.
[5] PLL enabled.
[6] See the FLASHCFG register in the LPC55S6x User Manual for system clock flash access time settings. Power Library in SDK sets the flash wait states based on the frequency selected.

Table 17. Static characteristics: Power consumption in active mode [1]

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[2]	Typ[3]	Max	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode								
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down						
		CCLK = 48 MHz, T_{amb} = 25°C	[4] [5]	-	2.1	4	-	mA
		CCLK = 48 MHz, T_{amb} = 55°C	[4] [5]	-	2.2	4.2	-	mA

Table 17. Static characteristics: Power consumption in active mode [1]*...continued*

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[2]	Typ[3]	Max	Unit
		CCLK = 48 MHz, T_{amb} = 85°C	[4] [5]	-	2.6	4.7	-	mA
		CCLK = 48 MHz, T_{amb} = 105°C	[4] [5]	-	3.1	5.2	-	mA
		CCLK = 96 MHz, T_{amb} = 25°C	[4] [5]	-	3.4	6.5	-	mA
		CCLK = 96 MHz, T_{amb} = 55°C	[4] [5]	-	3.5	6.6	-	mA
		CCLK = 96 MHz, T_{amb} = 85°C	[4] [5]	-	3.9	6.9	-	mA
		CCLK = 96 MHz, T_{amb} = 105°C	[4] [5]	-	4.4	7.5	-	mA
I_{DD}	supply current	CoreMark code executed from flash						
		CCLK = 48 MHz; 5 system clock flash access time, T_{amb} = 25°C	[4] [5] [6]	-	2.4	4.3	-	mA
		CCLK = 48 MHz; 5 system clock flash access time, T_{amb} = 55°C	[4] [5] [6]	-	2.5	4.5	-	mA
		CCLK = 48 MHz; 5 system clock flash access time, T_{amb} = 85°C	[4] [5] [6]	-	2.9	5	-	mA
		CCLK = 48 MHz; 5 system clock flash access time, T_{amb} = 105°C	[4] [5] [6]	-	3.3	5.5	-	mA
		CCLK = 96 MHz; 8 system clock flash access time, T_{amb} = 25°C	[4] [5] [6]	-	3.4	6.5	-	mA
		CCLK = 96 MHz; 8 system clock flash access time, T_{amb} = 55°C	[4] [5] [6]	-	3.5	6.6	-	mA
		CCLK = 96 MHz; 8 system clock flash access time, T_{amb} = 85°C	[4] [5] [6]	-	4.1	7	-	mA
		CCLK = 96 MHz; 8 system clock flash access time, T_{amb} = 105°C	[4] [5] [6]	-	4.8	7.6	-	mA

[1] For device revision 1B, power library in SDK sets the DCDC output based on the frequency selected. For frequencies 100 MHz or below, DCDC output is set between 1.0 V to 1.075 V. Frequencies between 101 MHz to 130 MHz, DCDC output is set between 1.025 V to 1.150 V, and for frequencies above 130 MHz, DCDC output is set between 1.050 V to 1.2 V. For device revision 0A, the default typical DCDC output is 1.1 V and for device revision 1B, the typical default DCDC output is 1.0 V.

[2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.VBAT_PMU = VBAT_DCDC = VDD = 3.0 V.

[3] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 C). Characterized through bench measurements using typical samples. VBAT_PMU = VBAT_DCDC = VDD = 1.8 V

[4] Clock source FRO. PLL disabled

[5] Compiler settings: IAR v.8.20.2., optimization level 0, optimized for time off.

[6] See the FLASHCFG register in the LPC55S6x User Manual for system clock flash access time settings. Power Library in SDK sets the flash wait states based on the frequency selected.

Table 18. Static characteristics: Power consumption in active mode [1]

T_{amb} = -40 °C to +105 °C, unless otherwise specified. VBAT_PMU = VBAT_DCDC = VDD = 3.0 V

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
ARM Cortex-M33 (CPU0) in active mode; ARM Cortex-M33 (CPU1) in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down					
		CCLK = 1 MHz, Tamb = 25 °C	[3][4]	-	0.8	-	mA
		CCLK = 16 MHz, Tamb = 25 °C	[4][5]	-	1.1	-	mA
I_{DD}	supply current	CoreMark code executed from flash					
		CCLK = 1 MHz, 1 system clock flash access time, Tamb = 25 °C	[3][4][6]	-	0.9	-	mA
		CCLK = 12 MHz, 2 system clock flash access time, Tamb = 25 °C	[4][5][6]	-	1.2	-	mA

[1] For device revision 1B, power library in SDK sets the DCDC output based on the frequency selected. For frequencies 100 MHz or below, DCDC output is set between 1.0 V to 1.075 V. Frequencies between 101 MHz to 130 MHz, DCDC output is set between 1.025 V to 1.150 V, and for frequencies above 130 MHz, DCDC output is set between 1.050 V to 1.2 V. For device revision 0A, the default typical DCDC output is 1.1 V and for device revision 1B, the typical default DCDC output is 1.0 V.
[2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[3] Clock source FRO. System Oscillator disabled. PLL disabled
[4] Compiler settings: IAR v.8.20.2., optimization level 0, optimized for time off.
[5] System Oscillator enabled. FRO disabled. PLL disabled.
[6] See the FLASHCFG register in the LPC55S6x/LPC55S2x User Manual for system clock flash access time settings. Power Library in SDK sets the flash wait states based on the frequency selected.

Table 19. Static characteristics: Power consumption in sleep mode

T_{amb} = -40 °C to +105 °C, unless otherwise specified. VBAT_PMU = VBAT_DCDC = VDD = 3.0 V

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M33 (CPU0) in sleep mode; ARM Cortex-M33 (CPU1) OFF (in reset, clock disabled)							
I_{DD}	supply current	CCLK = 12 MHz, PLL disabled	[1][2]	-	0.7	-	mA
		CCLK = 96 MHz, PLL disabled	[2]	-	2.7	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C). Characterized through bench measurements using typical samples.
[2] Clock source FRO. PLL disabled

Table 20. Static characteristics: Power consumption in deep-sleep, power-down, and deep power-down modes

T_{amb} = -40 °C to +105 °C; unless otherwise specified. IDD is total current from VBAT_DCDC, VBAT_PMU, VDDA, and VDD supply domains. VSUPPLY = VBAT_DCDC + VBAT_PMU + VDDA + VDD

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode; all SRAM on T_{amb} = 25 °C, *VSUPPLY* = 3.0 v	[2]	-	110	135	µA
		T_{amb} = 25 °C, *VSUPPLY* = 1.8 v	[2]	-	148	191	µA
		T_{amb} = 105 °C, *VSUPPLY* = 1.8 v	[2]	-	-	1850	µA
		Power-down mode.	[2]				

Table 20. Static characteristics: Power consumption in deep-sleep, power-down, and deep power-down modes*...continued*

T_{amb} = -40 °C to +105 °C; unless otherwise specified. IDD is total current from VBAT_DCDC, VBAT_PMU, VDDA, and VDD supply domains. VSUPPLY = VBAT_DCDC + VBAT_PMU + VDDA + VDD

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
		SRAM_X2 (4 KB) powered T_{amb} = 25 °C, *VSUPPLY* = 3.0 v		-	3.9	4.5	µA
		SRAM_X2 (4 KB) powered T_{amb} = 105 °C, *VSUPPLY* = 3.0 v		-	-	85	µA
		SRAM_X2 and SRAM_X3 (8 KB) powered T_{amb} = 25 °C, *VSUPPLY* = 3.0 v		-	4.0	-	µA
		320 KB full retention T_{amb} = 25 °C, *VSUPPLY* = 3.0 v		-	14	18	µA
		320 KB full retention T_{amb} = 105 °C, *VSUPPLY* = 3.0 v		-	-	480	µA
		SRAM_X2 (4 KB) powered T_{amb} = 25 °C, *VSUPPLY* = 3.0 v USART3 enabled as wake-up source		-	4.2	-	µA
		SRAM_X2 (4 KB) powered T_{amb} = 25 °C, *VSUPPLY* = 3.0 v OSTIMER enabled as wake-up source		-	4.1	-	µA
		Deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled, 4 KB SRAM powered) T_{amb} = 25 °C, *VSUPPLY*= 3.0 v	[2]	-	590	750	nA
		Deep power-down mode; RTC oscillator input grounded (RTC oscillator disabled, 4 KB SRAM powered) T_{amb} = 105 °C, *VSUPPLY*= 3.0 v	[2]	-	-	15	µA
		RTC oscillator running with external crystal (4 KB SRAM powered)		-	790	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).
[2] Characterized through bench measurements using typical samples.
[3] The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 21. Static characteristics: ADC Power consumption

T_{amb} = -40 °C to +105 °C, unless otherwise specified.0.985 V ≤ V_{REFP} ≤ V_{DDA} V; 1.8 V ≤ V_{DDA} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DDA}	analog supply current	ADC in low power mode (PWRSEL = 0) Idle mode (analog blocks pre-enabled, inc ADC Bias)	-	0.2	-	mA
		ADC in low power mode (PWRSEL = 0) Sampling/ SE Conversion mode (analog blocks ON) f_adc = 24 MHz	-	0.7	-	mA

Table 21. Static characteristics: ADC Power consumption*...continued*

T_{amb} = -40 °C to +105 °C, unless otherwise specified.0.985 V ≤ V_{REFP} ≤ V_{DDA} V; 1.8 V ≤ V_{DDA} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
		Temperature sensor (inc ADC Bias)	-	60	-	µA
I_{DDA}	Analog supply current	Deep Sleep Mode, ADC OFF	-	10	-	nA
		Power Mode, ADC OFF	-	6	-	nA
		Deep Power Down Mode, ADC OFF	-	5		nA
$I_{DD(VREFP)}$	VREFP supply current	ADC Idle mode(analog blocks pre_enabled)	-	5	-	nA

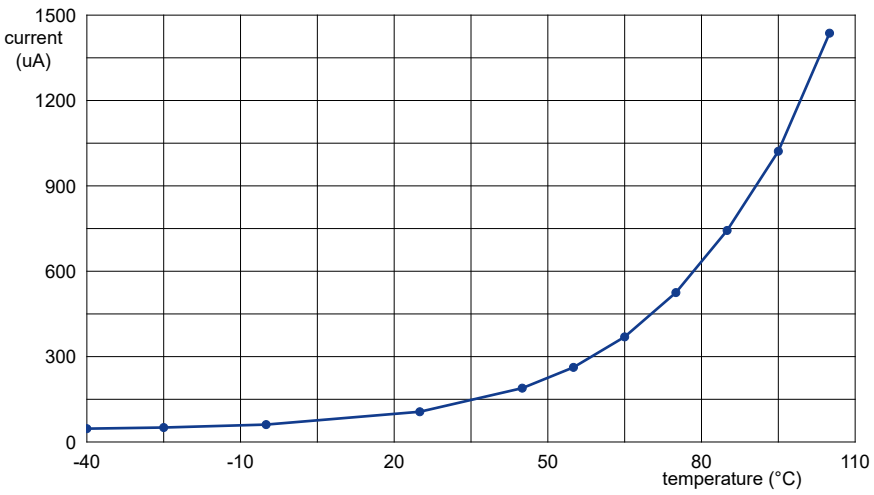
[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

Table 22. Static characteristics: USB Power consumption

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

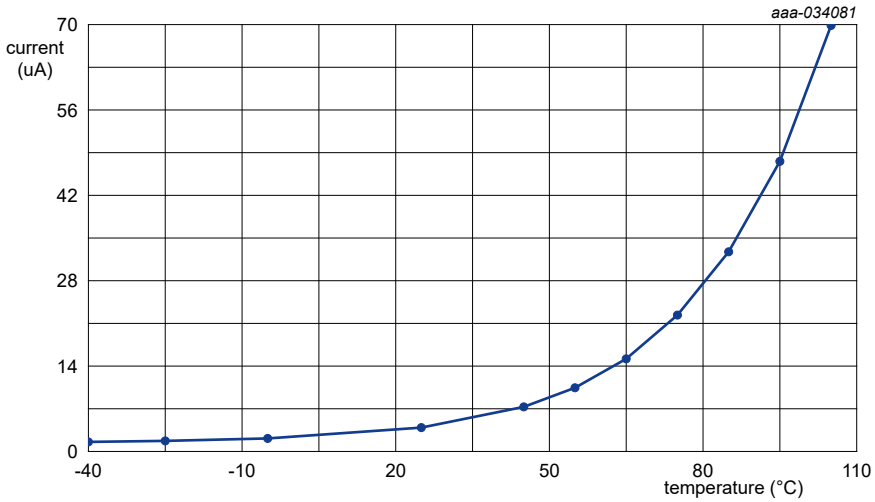
Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{DD(VBUS)}$	VBUS supply current for USB1	Power-down mode/Deep-power-down mode	-	6	-	µA
$I_{DD(USB1\_3V3)}$	USB1 analog 3.3 V supply	Active mode	-	1.2	-	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.



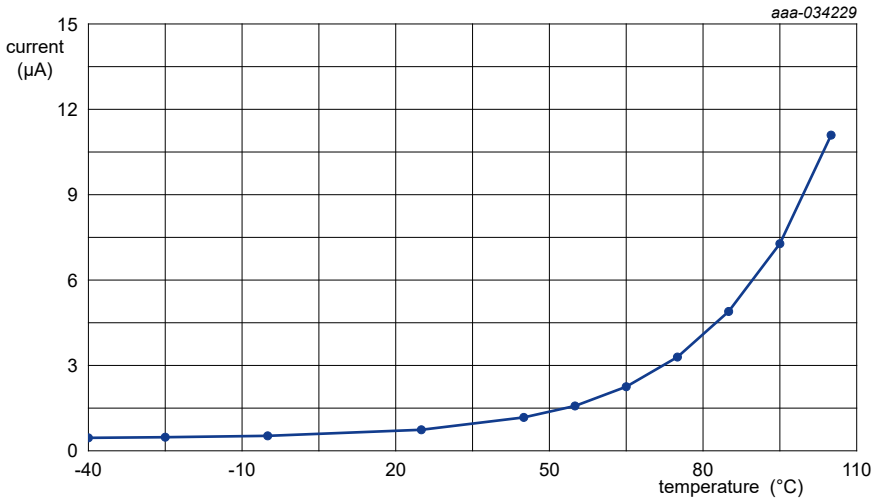
Conditions: all oscillators and analog blocks disabled. All SRAM blocks enabled.

Figure 10. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages VBAT_DCDC



Conditions: all oscillators and analog blocks disabled; all SRAM disabled except 4KB SRAM powered. Flash powered down.

Figure 11. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages VBAT_DCDC



RTC input grounded. 4KB SRAM powered.

Figure 12. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages VBAT_DCDC

10.3.1 Peripheral Power Consumption

Table 23 shows the typical peripheral power consumption measured on a typical sample at T_{amb} = 25 °C and VBAT_PMU = VBAT_DCDC = V_{DD} = 3.3 V. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using AHB clock control and PDRUNCFG registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, and 96 MHz.

Table 23. Typical peripheral power consumption

VBAT_PMU = VBAT_DCDC = V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} (uA)	
FRO (12 MHz)		41	-
FRO (1 MHz)		3.5	-
FRO (32 KHz)		0.3	-
System OSC		35	-
32.768 KHz OSC		3.7	-
Flash		79	-
BODVBAT		0.3	-
SRAM 0 (64 KB)	[1]	9.5	-
SRAM 1 (64 KB)	[1]	11.5	-
SRAM 2 (64 KB)	[1]	11.5	-
SRAM 3 (64 KB)	[1]	16	-
SRAM 4 (16 KB)	[1]	16	-
Comparator		59	-
Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz
		CPU: 12 MHz	**CPU: 96MHz**
FS USB0 Device		0.8	0.8
HS USB1 Device		1.0	1.3
RNG		17	2.8
INPUTMUX	[2]	0.4	0.5
IOCON	[2]	0.6	0.6
GPIO0	[2]	0.3	0.4
GPIO1	[2]	0.3	0.4
PINT		0.5	0.5
GINT		0.3	0.3
DMA0		1.7	1.7
DMA1		1.2	1.2
CRC		0.4	0.4
WWDT		0.2	0.2
RTC		0.2	0.2
MAILBOX		0.2	0.2
MRT		0.3	0.3
SCTimer/PWM		1.3	1.4
UTICK		0.2	0.2
OS Timer		0.2	0.2
Flexcomm Interface 0		0.8	0.8

Table 23. Typical peripheral power consumption...*continued*

VBAT_PMU = VBAT_DCDC = V_{DD} = 3.3 V; T = 25 °C

Peripheral		I_{DD} (uA)	
Flexcomm Interface 1		0.8	0.8
Flexcomm Interface 2		0.8	0.8
Flexcomm Interface 3		0.8	0.8
Flexcomm Interface 4		0.8	0.8
Flexcomm Interface 5		0.8	0.8
Flexcomm Interface 6		0.8	0.8
Flexcomm Interface 7		0.8	0.8
Timer0		0.3	0.3
Timer1		0.3	0.3
Timer2		0.3	0.3
Timer3		0.3	0.3
Timer4		0.3	0.3
SDIO		2.3	2.3
USB0 HOST		1.2	1.2
USB1 HOST		0.8	0.8
Power Quad		0.8	0.8
PLU		0.8	0.8
HS SPI		0.4	0.4
CASPER		0.6	0.6
PUF		2.3	2.3
AES_SHA		0.5	0.5

[1] Measured in power-down mode
[2] Turn off the peripheral when the configuration is done.

10.4 Pin characteristics

Table 24. Static characteristics: pin characteristics

T_{amb} = -40 °C to +105 °C, unless otherwise specified. 1.8 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard I/O pins , $\overline{\text{RESET}}$ pin							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	2	200	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	2	200	nA
V_I	input voltage	pin configured to provide a digital function;	[2]	0	-	3.6	V

Table 24. Static characteristics: pin characteristics...*continued*

T_{amb} = -40 °C to +105 °C, unless otherwise specified. 1.8 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		V_{DD} ≥ 1.8 V					
V_{IH}	HIGH-level input voltage			0.7 x V_{DD}	-	V_{DD}	V
V_{IL}	LOW-level input voltage			- 0.3	-	0.3 x V_{DD}	V
V_{hys}	hysteresis voltage			-	0.4	-	V
Output characteristics							
V_{OH}	HIGH-level output voltage	I_{OH} = -4 mA; 1.8 V ≤ V_{DD} < 2.7 V		V_{DD} - 0.5	-	-	V
		I_{OH} = -4 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} - 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.8 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 4 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
Weak input pull-up/pull-down characteristics							
R_{pd}	pull-down resistance	V_I = 0		40	50	62	kΩ
R_{pu}	pull-up resistance	V_I = V_{DD}		40	50	62	kΩ
Pin capacitance							
C_{io}	input/output capacitance	I^2C-bus pins	[3]	-	-	4.5	pF
		pins with digital functions only	[4]	-	-	2.5	pF
		Pins with digital and analog functions	[4]	-	-	3.0	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.
[2] With respect to ground.
[3] The value specified is a simulated value, excluding package/bondwire capacitance.
[4] The values specified are simulated and absolute values, including package/bondwire capacitance.

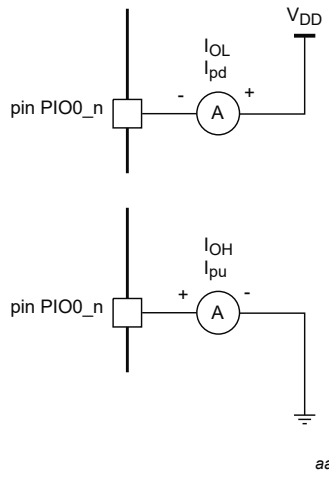


Figure 13. Pin input/output current measurement

11 Dynamic characteristics

11.1 Power-up ramp conditions

Table 25. Power-up ramp characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
tr	Rise time	T_{amb} = *-40 °C*	[1]	2.6	-	-	ms
		T_{amb} = *0 °C to +105°C*	[1]	0.5	-	-	ms

[1] Based on characterization, not tested in production.

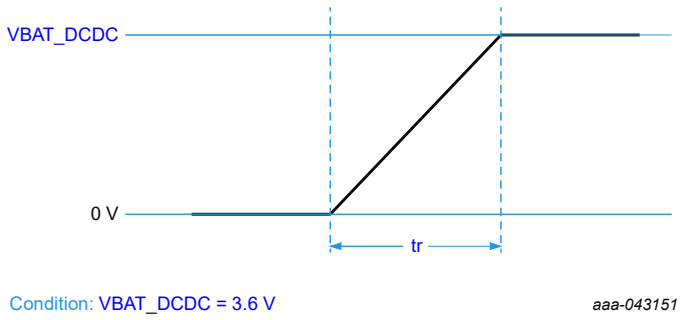


Figure 14. Power-up ramp

11.2 Flash memory

Table 26. Flash characteristics[1]

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [2]	Max	Unit
N_{endu}	endurance	Page erase/program, T_{amb} = *-40 °C to +85 °C*	[3]	100000	-	-	cycles
		Mass erase/program, T_{amb} = *-40 °C to +85 °C*		100000	-	-	cycles
		Page erase/program T_{amb} = *-40 °C to +105 °C,*		10000	-	-	cycles
		Mass erase/program T_{amb} = *-40 °C to +105 °C,*		10000	-	-	cycles
t_{ret}	retention time	< 1k erase/program cycles		25	100	-	years
		≥ 1k erase/program cycles		15	50	-	years
t_{er}	erase time	1 page or multiple pages		-	2.0	-	ms
t_{prog}	programming time			-	1.09	-	ms
Nupdates	number of page updates	1 page or multiple pages		-	-	50	million

[1] Flash operations (erase, blank check, program) and reading single word can only be performed for CPU frequencies of up to 100 MHz. Cannot be performed for frequencies above 100 MHz.
[2] Temperature = 25 C.
[3] Number of erase/program cycles.

11.3 I/O pins

Table 27. Dynamic characteristic: I/O pins[1]

T_{amb} = -40 °C to +105 °C; 1.8 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1	[2][3]	2.0	-	4.0	ns
t_f	fall time	pin configured as output; SLEW = 1	[2][3]	2.0	-	4.0	ns
t_r	rise time	pin configured as output; SLEW = 0	[2][3]	1.2	-	11.0	ns
t_f	fall time	pin configured as output; SLEW = 0	[2][3]	3.9	-	9.0	ns
I2C I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1	[2][3]	3.0	-	11.0	ns
t_f	fall time	pin configured as output; SLEW = 1	[2][3]	3.0	-	7.0	ns
t_r	rise time	pin configured as output; SLEW = 0	[2][3]	21.5	-	39.0	ns
t_f	fall time	pin configured as output; SLEW = 0	[2][3]	29.8	-	36.0	ns

[1] Based on characterized, not tested in production
[2] Rise and fall times measured between 90% and 10% of the full input signal level.
[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC55S6x user manual.

11.4 Wake-up process

Table 28. Dynamic characteristic: Typical wake-up times from low power modes

VBAT_PMU = VBAT_DCDC = V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
t_{wake}	wake-up time	from Sleep mode, 12 MHz, No PRIMASK backup and restore	[3][4]		4.0		µs
		from Sleep mode, 96 MHz, No PRIMASK backup and restore	[3][4]		500		ns
		from Deep-sleep mode with full SRAM retention:	[3]		64		µs
		from Power-down mode with CPU retention and 4 KB retained	[3]		346		µs
		from deep power-down mode; 4KB retained, RTC disabled; using $\overline{\text{RESET}}$ pin.	[5][6]		4.6		ms
		from deep power-down mode; 4KB retained, RTC disabled; using $\overline{\text{RESET}}$ pin.	[5][7]		17		ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.
[2] Compiler settings: IAR v8.40, High optimization
[3] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.
[4] FRO enabled, all peripherals off.
[5] RTC disabled. Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler. Wake-up time for non-secure mode.
[6] Applies to device revision 1B.
[7] Applies to device revision 0A.

11.5 FRO (12 MHz/96 MHz)

Table 29. Dynamic characteristic: FRO

T_{amb} = -40 °C to +105 °C; 1.8 V ≤ VBAT_DCDC ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-		11.76	12	12.24	MHz
$f_{osc(RC)}$	FRO clock frequency	-		94.08	96	97.92	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Table 30. Dynamic characteristic: FRO [1]

T_{amb} = 0 °C to +85 °C; 1.8 V ≤ VBAT_DCDC ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-		11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-		95.04	96	96.96	MHz

[1] The +/- 1% accuracy specification applies to devices with date code 2041 (yyww) and onwards.
[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 FRO (1 MHz)

Table 31. Dynamic characteristic: FRO

T_{amb} = -40 °C to +105 °C; 1.8 V ≤ VBAT_DCDC ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-		0.85	1	1.15	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.7 FRO (32 KHz)

Table 32. Dynamic characteristic: FRO

T_{amb} = -40 °C to +105 °C; 1.8 V ≤ VBAT_DCDC ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-		32.11	32.768	33.42	KHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.8 RTC oscillator

See Section 13.4 for connecting the RTC oscillator to an external clock source.

Table 33. Dynamic characteristic: RTC oscillator

T_{amb} = -40 °C to +105 °C; 1.8 ≤ VBAT_DCDC ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768		kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

11.9 I²C-bus

Table 34. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = -40 °C to +105 °C; 1.8 V ≤ VBAT_DCDC ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[3][4][5][6]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[7][3][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.
[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.
[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[4] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.
[5] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
[6] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[7] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.
[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

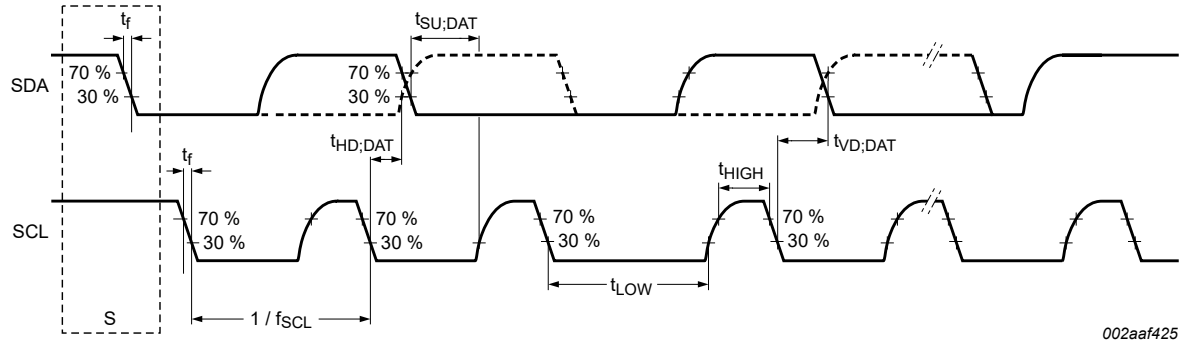


Figure 15. I^2C-bus pins clock timing

11.10 I^2S-bus interface

Table 35. Dynamic characteristics: I^2S-bus interface pins [1][4]

T_{amb} = -40 °C to 105 °C; VBAT_DCDC = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
				45%	-	55%	T_{cyc}
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
				45%	-	55%	T_{cyc}
Master; 1.8 V ≤ VDD < 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
				5	-	15	ns
		on pin I2Sx_WS					
				5	-	12	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
				4	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
				0	-	-	ns
Slave; 1.8 V ≤ VDD < 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
				9	-	26	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
				4	-	-	ns
		on pin I2Sx_WS					
				4	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
				0	-	-	ns

Table 35. Dynamic characteristics: I²S-bus interface pins [1][4] *...continued*

T_{amb} = -40 °C to 105 °C; VBAT_DCDC = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
		on pin I2Sx_WS					
				0	-	-	ns

1. Based on simulation; not tested in production.
2. Clock Divider register (DIV) = 0x0.
3. Typical ratings are not guaranteed.
4. The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM11126) to calculate clock and sample rates.
5. Based on simulation. Not tested in production.

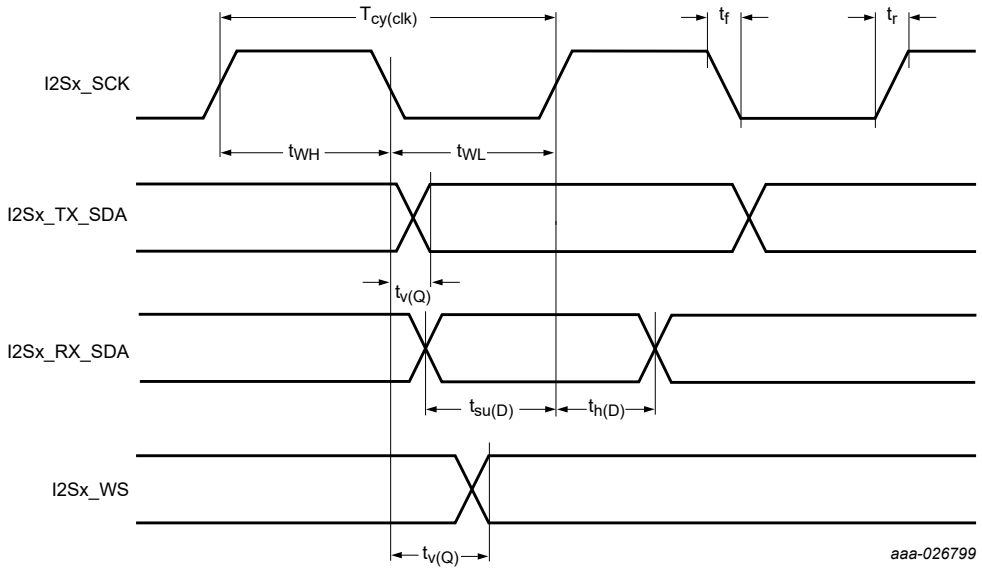


Figure 16. I²S-bus timing (master)

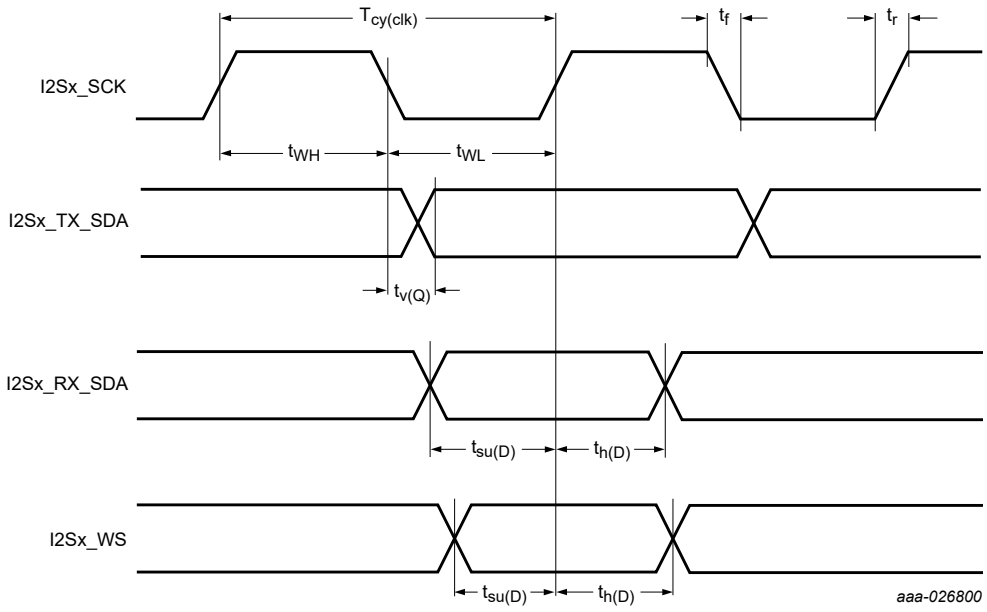


Figure 17. I^2S-bus timing (slave)

11.11 SPI interface (Flexcomm Interfaces 0 - 7)

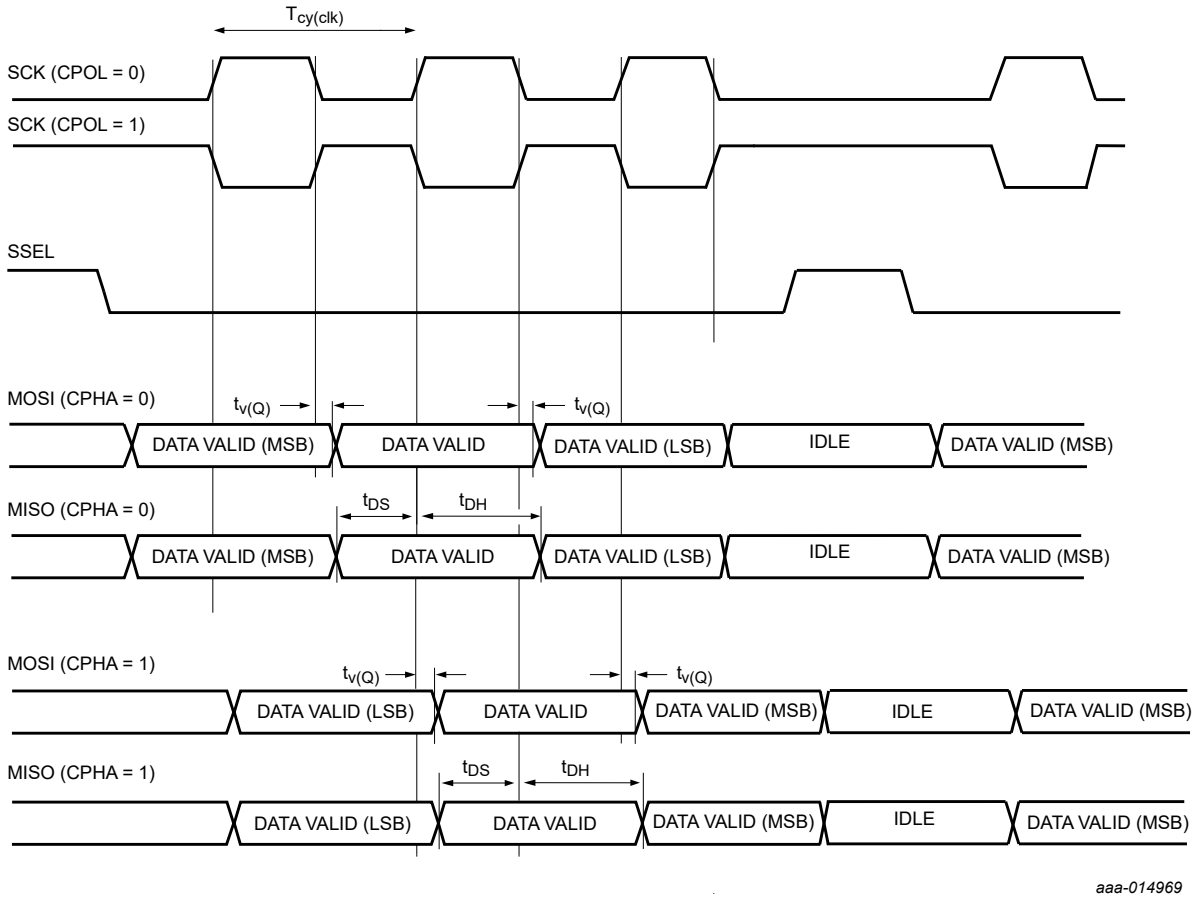
The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 32 Mbit/s. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI slave receive mode is 50 Mbit/s and for slave transmit mode is 16 Mbit/s.

Table 36. SPI dynamic characteristics[1]

T_{amb} = -40 °C to 105 °C; V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast mode for all pins;. Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master							
t_{DS}	data set-up time			5	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			5	-	13	ns
SPI slave							
t_{DS}	data set-up time			5	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			8	-	21	ns

[1] Based on simulated values. Not tested in production



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC55S6x User manual*.

Figure 18. SPI master timing

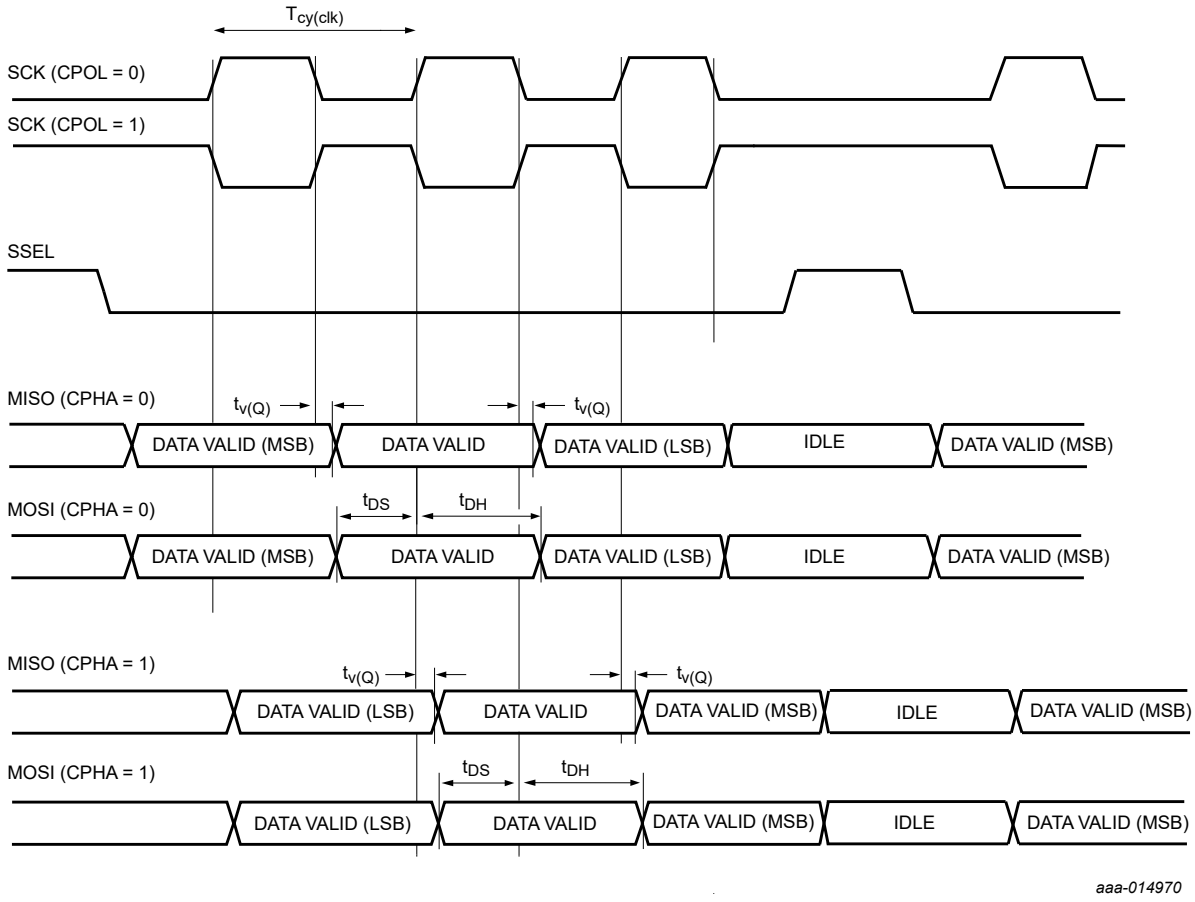


Figure 19. SPI slave timing

11.12 High-Speed SPI interface (Flexcomm Interface 8)

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode (transmit/receive) is 50 Mbit/s. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI slave receive mode is 50 Mbit/s and for SPI slave transmit mode is 25 Mbit/s.

Table 37. SPI dynamic characteristics[1]

T_{amb} = -40 °C to 105 °C; V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast mode for all pins;. Parameters sampled at the 50% level of the rising or falling edge.

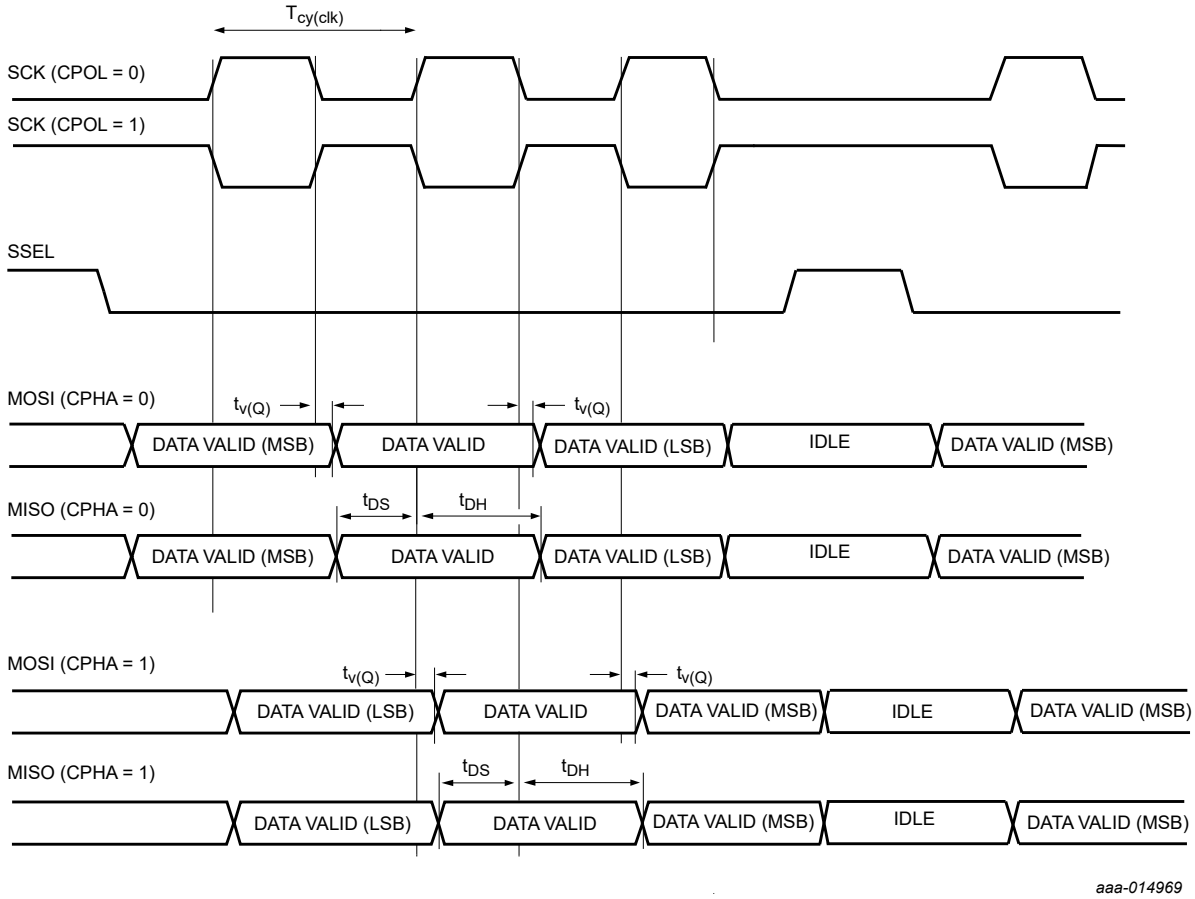
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master							
t_{DS}	data set-up time			4	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			3	-	8	ns
SPI slave							
t_{DS}	data set-up time			4	-	-	ns
t_{DH}	data hold time			0	-	-	ns

Table 37. SPI dynamic characteristics[1] *...continued*

T_{amb} = -40 °C to 105 °C; V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast mode for all pins;. Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{v(Q)}$	data output valid time			6	-	15	ns

[1] Based on simulated values. Not tested in production.



$T_{cy(clk)}$ = CCLK/DIVVAL with CCLK = system clock frequency. DIVVAL is the SPI clock divider. See the *LPC55S6x User manual*.

Figure 20. SPI master timing

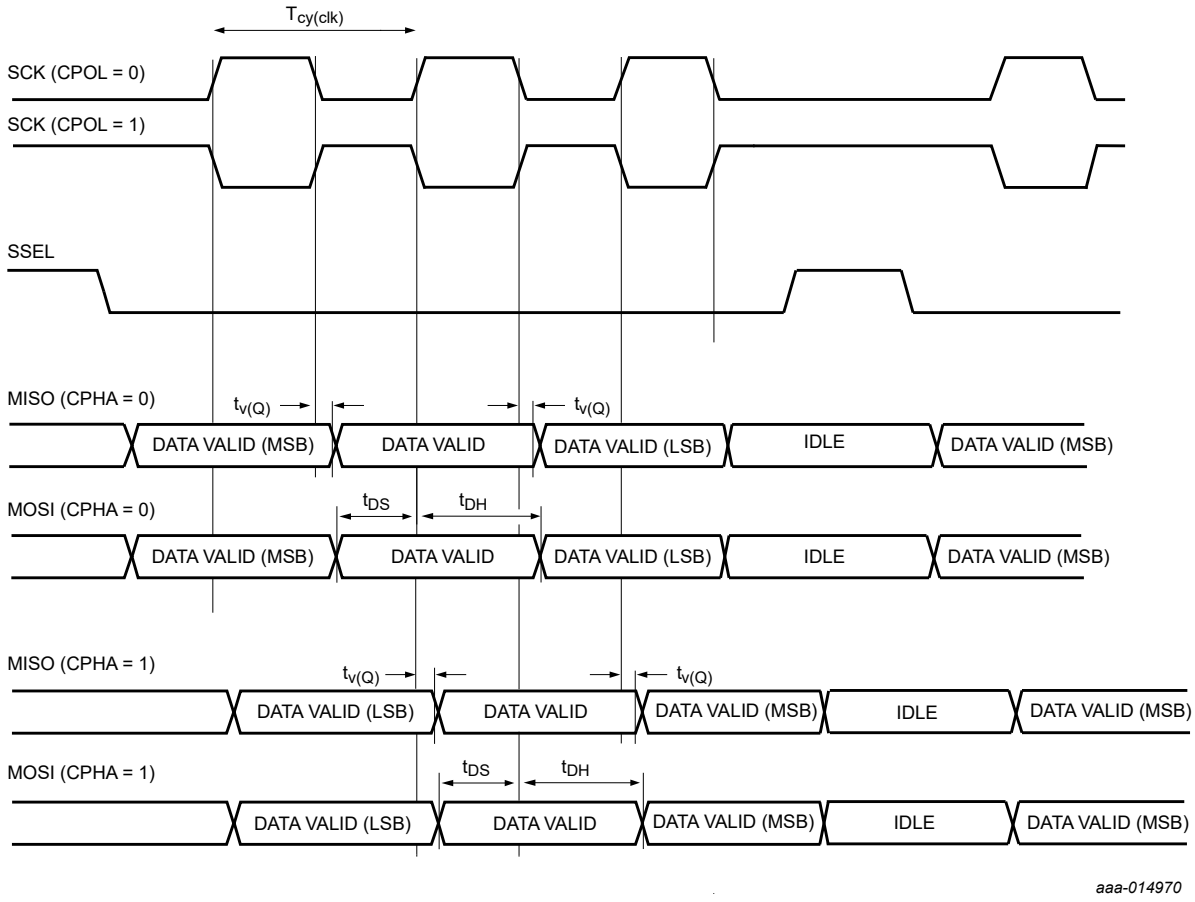


Figure 21. SPI slave timing

11.13 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master and slave synchronous mode is 25 Mbit/s. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master and slave asynchronous mode is 10 Mbit/s.

Table 38. USART dynamic characteristics[1]

T_{amb} = -40 °C to 105 °C; V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast-mode for all pins; Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode)						
$t_{su(D)}$	data input set-up time		6	-	-	ns
$t_{h(D)}$	data input hold time		0	-	-	ns
$t_{v(Q)}$	data output valid time		5	-	11	ns
USART slave (in synchronous mode)						
$t_{su(D)}$	data input set-up time		6	-	-	ns
$t_{h(D)}$	data input hold time		0	-	-	ns

Table 38. USART dynamic characteristics[1] *...continued*

T_{amb} = -40 °C to 105 °C; V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = fast-mode for all pins; Parameters sampled at the 50% level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(Q)}$	data output valid time		9	-	25	ns

[1] Based on simulated values. Not tested in production.

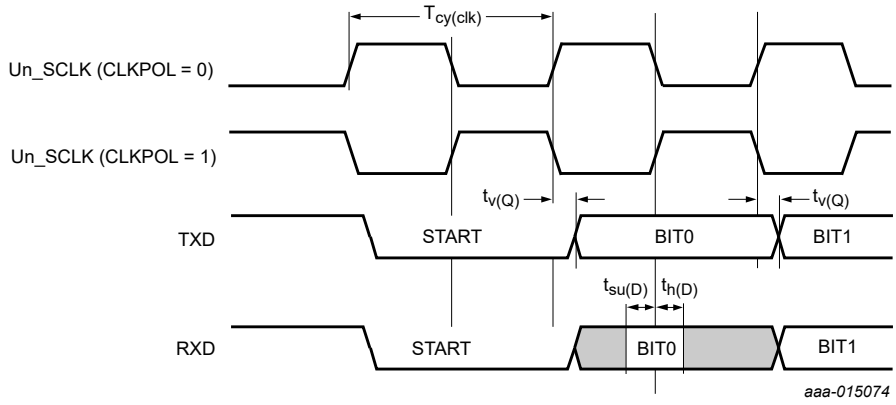


Figure 22. USART timing

11.14 SD/MMC and SDIO

Table 39. Dynamic characteristics: SD/MMC and SDIO

T_{amb} = -40 °C to +105 °C, V_{DD} = 1.8 V to 3.6 V; C_L = 10 pF. SAMPLE_DELAY = 0, DRV_DELAY = 0 in the SDDELAY register, SDIOCLKCTRL = 0x84, sampled at 90 % and 10 % of the signal level, SLEW = 1 ns for SD_CLK pin, SLEW = 1 ns for SD_DATn and SD_CMD pins. Simulated values in high-speed mode. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	-	50	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs				
			15	-	-	ns
		on pins SD_CMD as inputs				
			15	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs				
			0	-	-	ns
		on pins SD_CMD as inputs				
			0	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs				
			3	-	7	ns
		on pins SD_CMD as outputs				
			3	-	7	ns

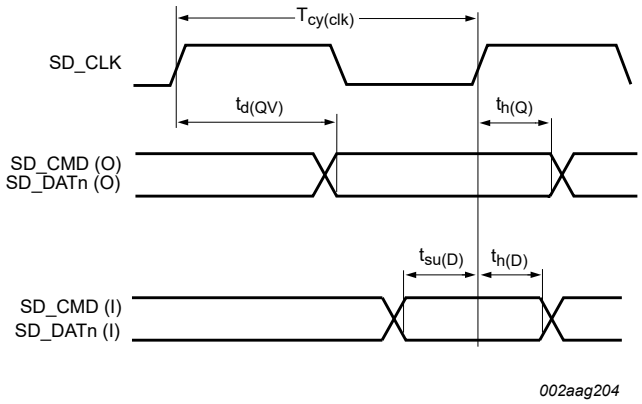


Figure 23. SD/MMC and SDIO timing

Definitions:

- Delay_O=cclk_in to cclk_out delay (including PAD).
- Delay_I=Input PAD delay + routing delay to input register.

Table 40. Minimum and Maximum values of parameters

Parameters	Minimum	Maximum
Delay_O	-	8nS
Delay_I	-	6nS

12 Analog characteristics

12.1 BODVBAT

Brown-out detector to monitor the voltage of VBAT. If the voltage falls below one of the selected voltages, the BOD asserts an interrupt to the NVIC or issues a reset. Single low threshold detection level (programmable trip low level) is used for either BOD interrupt or BOD reset. Hysteresis control on the BOD is programmable. Please refer to UM11126 for further details.

Table 41. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production. Please refer to UM11126 for further details.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage (TRIGLVL)		-	1.75	-	V
			-	1.80	-	V
			-	1.90	-	V
			-	2.00	-	V
			-	2.10	-	V
			-	2.20	-	V
			-	2.30	-	V
			-	2.40	-	V
			-	2.50	-	V

Table 41. BOD static characteristics...*continued*

T_{amb} = 25 °C; based on characterization; not tested in production. Please refer to UM11126 for further details.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
			-	2.60	-	V
			-	2.70	-	V
			-	2.80	-	V
			-	2.90	-	V
			-	3.00	-	V
			-	3.10	-	V
			-	3.20	-	V
			-	3.30	-	V

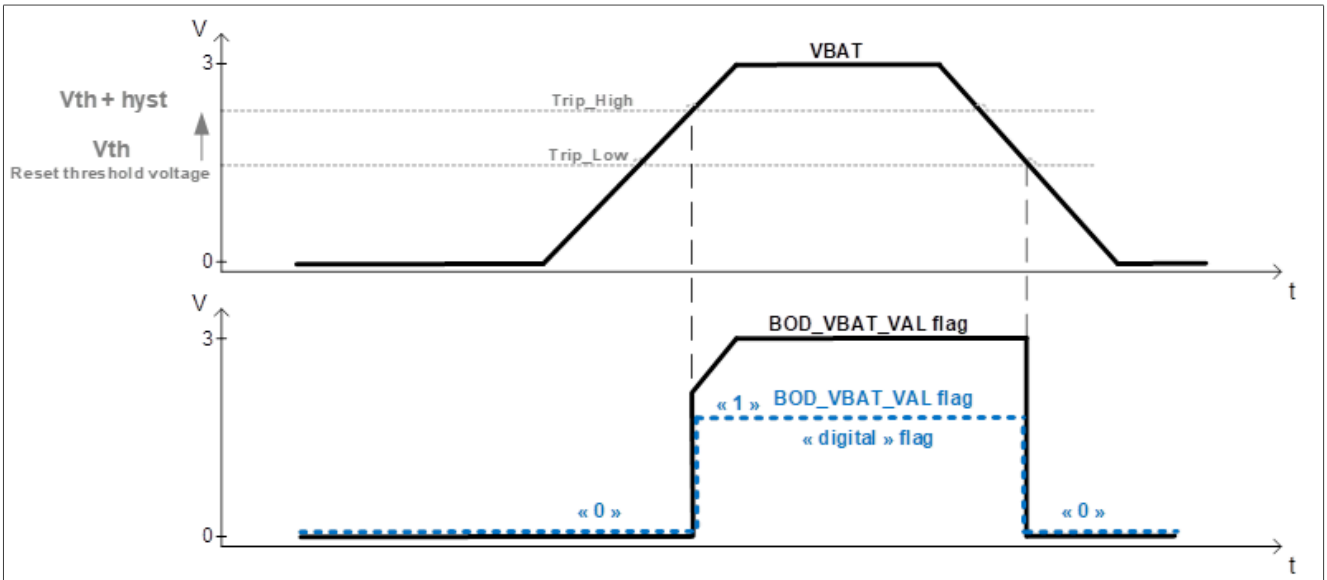


Figure 24. BOD

12.2 16-bit ADC characteristics

Table 42. 16-bit ADC static characteristics

T_{amb} = -40 °C to +105 °C; V_{DDA} = 1.8 V to 3.6 V; ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions		Min[1]	Typ[1]	Max[1]	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
CADIN	input capacitance			-	4	5	pF
$f_{clk(ADC)}$	ADC clock frequency		[2]		-	24	MHz
f_s	sampling frequency			-	-	1.0	Msamples/s

Table 42. 16-bit ADC static characteristics*...continued*

T_{amb} = -40 °C to +105 °C; V_{DDA} = 1.8 V to 3.6 V; ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions		Min[1]	Typ[1]	Max[1]	Unit
E_D	differential linearity error	16-bit differential mode, CTYPE = 2	[3][1][4][5][6]	-0.99	-	2.6	LSB
		16-bit single ended mode, CTYPE = 1	[3][1][4][5][6]	-1		+9.5	LSB
$E_{L(adj)}$	integral non-linearity	16-bit differential mode, CTYPE = 2	[3][1][4][5][7]	-16	-	+16	LSB
		16-bit single ended mode, CTYPE = 1	[3][1][4][5][7]	-12	-	+12	LSB
E_O	offset error	uncalibrated	[3][8]	-	2.3	-	mV
$V_{err(FS)}$	full-scale error voltage	uncalibrated	[3][9]	-	24	-	LSB
ENOB	[L:] Effective number of bits	16-bit differential mode, CTYPE = 2	[10]	-	12.6	-	bits
		16-bit single ended mode, CTYPE = 1	[10]	-	12.0	-	bits
THD	[L:] Total Harmonic Distortion	16-bit differential mode, CTYPE = 2	[10]	-	-85	-	dB
		16-bit single endedmode, CTYPE = 1	[10]	-	-85	-	dB
SFDR	[L:] Spurious Free Dynamic Range	16-bit differential mode, CTYPE = 2	[10]	-	86	-	dB
		16-bit single ended mode, CTYPE = 1	[10]	-	82	-	dB
tADCSTUP	Analog startup time	Wait time after setting ADC_CTRL[ADCEN] [10]	[11]	-	5	-	us

[1] These are typical values and are not guaranteed. Based on characterization. Not tested in production. If VREFP is less than VDDA, then voltage inputs greater than VREFP and less than VDDA are allowed but result in a full scale conversion result.
[2] To use temperature sensor, the maximum fclk(ADC) frequency is 6 MHz.
[3] Linear data collected using a linear histogram technique.
[4] $f_{clk(ADC)}$ = 24 MHz, STS = 3, Power select = 1, Average setting = 1, f_s = 1 Msample/s
[5] Differential linear results assume offset 0.2% from VREFL and 0.2% from VREFH
[6] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width.
[7] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors.
[8] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. For best performance, force the offset calibration to -16. Set this prior to performing the gain calibration
[9] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve.
[10] Input data is 1kHz sine wave, ADC conversion clock 24 MHz, Power Select = 3, Average setting = 4.
[11] Value of ADC_CFG[PUDLY] * 4 * ADCclk must be > tADCSTUP.

12.2.1 ADC input resistance (Please refer to the ADC Inputs Selection & ADC programming table in the UM)

Table 43. ADC input resistance

T_{amb} = -40 °C to +105 °C

			Min	Typ	Max	Unit
R_I	input resistance					

Table 43. ADC input resistance*...continued*

T_{amb} = -40 °C to +105 °C

			Min	Typ	Max	Unit
		Fast Input Channels				
		PIO0_16/PIO0_23	-	1	2	kΩ
		PIO0_11/PIO0_10	-	1	2	kΩ
		PIO0_12/PIO0_15	-	1	2	kΩ
		PIO1_0/PIO0_31	-	1	2	kΩ
		Standard Input Channels				
		PIO1_9/PIO1_8	-	1.4	3.6	kΩ

12.3 Temperature sensor

The ADC has a dedicated input channel for an on-chip temperate sensor that is mapped on channel 26.

Table 44. Temperature sensor static and dynamic characteristics

VBAT_PMU = VBAT_DCDC = VDD = 3.0 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = -40 °C to +105 °C	[1]	-	-	4	°C
$t_{s(pu)}$	power-up settling time		[2]	-	5	-	µs

[1] Absolute temperature accuracy. Based on characterization, not tested in production.
[2] Typical values are derived from nominal simulation

12.4 Comparator

Table 45. Comparator characteristics

T_{amb} = -40 °C to +105 °C unless noted otherwise; VBAT_PMU = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Static characteristics							
I_{DD}	supply current	Low Power Mode		-	2.5	-	µA
		Fast Mode		-	5	-	µA
V_{IC}	common-mode input voltage	Propagation delay; Vcm_min = 0.1 V to VBAT_PMU-0.1 V		0	-	VBAT_PMU	V
V_{offset}	offset voltage	Common mode input voltage < VBAT_PMU - 0.2 V		0	-	10	mV
V_{offset}	offset voltage	Common mode input voltage (Range: VBAT_PMU - 0.2 V:VBAT_PMU - 0.1 V)		0	-	20	mV
Dynamic characteristics							
$t_{startup}$	start-up time	nominal process; VBAT_PMU = 3.3 V; T_{amb} = 25 °C, Max overdrive with reference at mid-supply		-	3.3	-	µs

Table 45. Comparator characteristics...*continued*

T_{amb} = -40 °C to +105 °C unless noted otherwise; VBAT_PMU = 1.8 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{delay}	propagation delay time Low Power Mode negative input = VBAT_PMU/2	V_overdrive = 10 mV		-	1150	6000	ns
		V_overdrive = 50 mV		-	3100	-	ns
		V_overdrive = max [2]		-	900	3000	ns
	propagation delay time Low Power Mode negative input = VBAT_PMU - 0.1 V	V_overdrive = 10 mV		-	6000	-	ns
		V_overdrive = 50 mV		-	6000	-	ns
		V_overdrive = max [2]		-	4400	-	ns
	propagation delay time Low Power Mode negative input = 0.1 V	V_overdrive = 10 mV		-	2400	-	ns
		V_overdrive = 50 mV		-	2300	-	ns
		V_overdrive = max		-	50	2000	ns
	propagation delay time High Speed Mode negative input = VBAT_PMU/2	V_overdrive = 10 mV		-	800	2000	ns
		V_overdrive = 50 mV		-	520	-	ns
		V_overdrive = max [2]		-	210	300	ns
	propagation delay time High Speed Mode negative input = VBAT_PMU - 0.1 V	V_overdrive = 10 mV		-	1600	-	ns
		V_overdrive = 50 mV		-	1150	-	ns
		V_overdrive = max [2]		-	790	-	ns
	propagation delay time High Speed Mode negative input = 0.1 V	V_overdrive = 10 mV		-	1400	-	ns
		V_overdrive = 50 mV		-	405	-	ns
		V_overdrive = max [2]		-	40	100	ns
V_{hys} [3]	hysteresis voltage (VHYST_P - VHSYT_N)	Common Mode Input Voltages in [200 mV: Vbat - 200mV] range (See Vin_N in Figure 25)		-	100	200	mV
R_{lad}	ladder resistance	Resistive ladder, Divider ratio programmed with 5-bit control word. Entry point is either PIO1_19 or internal VBAT_PMU		-	1.27	-	MΩ

[1] Characterized on typical samples, not tested in production; T_{amb} = 25 °C
[2] Max is the difference between VBAT_PMU and negative voltage level.
[3] On device revision 0A, the hysteresis on the comparator cannot be enabled

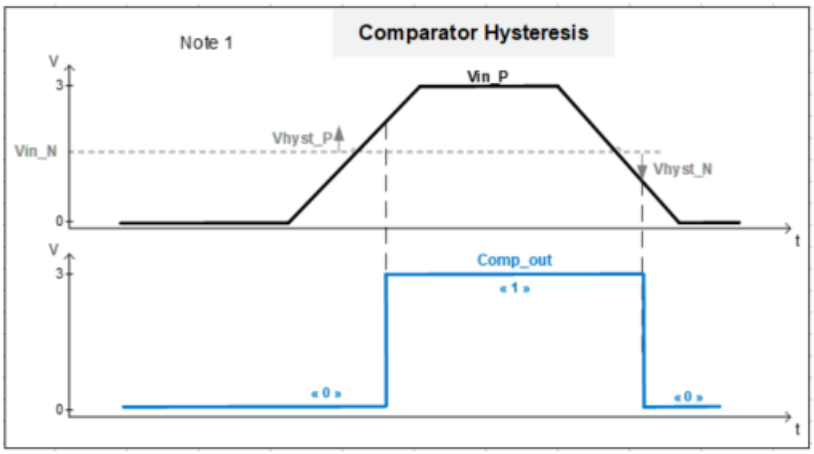


Figure 25. Comparator Hysteresis

13 Application information

13.1 Start-up behavior

Figure 26 shows the start-up timing after reset. The FRO oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

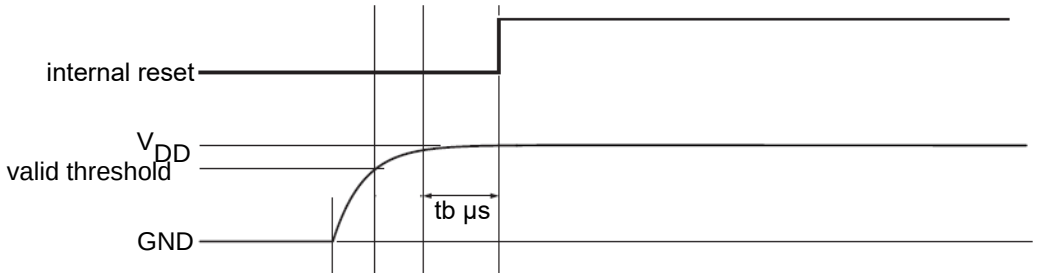


Figure 26. Start-up timing

Table 46. Typical start-up timing parameters

Symbol	Parameter	Conditions
t_b	Internal reset de-asserted	540 µs typical, 1 ms worst case

13.2 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 24 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 24, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 24 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

13.3 Crystal oscillator

The crystal oscillator has embedded capacitor bank where it can be used as an integrated load capacitor for the crystal oscillators. The capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) between 6 to 10pF (IEC equivalent). Simple APIs to configure the Capacitor Banks based on the crystal Capacitive Load (CL) and measured PCB parasitic capacitances on XIN and XOUT pins. In the crystal oscillator circuit, only the crystal (XTAL) needs to be connected with the option to connect capacitances CX1 and CX2 on XTAL32M_P and XTAL32M_N pins. Depending upon the computation of the required Capacitance Load, there is no need to add some capacitance on PCB if computation is less than 20 pF (10 pF equivalent IEC), and if computation is greater than 20 pF (10 pF equivalent IEC), then additional capacitance is on PCB required. See Figure 27 and refer to the "Cap Bank API" chapter in the user manual. In bypass mode, an external clock (maximum frequency of up to 25 MHz) can also be connected to XTAL32M_P if XTAL32M_N is left open. External [0 – VH] square signal can be applied on the XTAL32M_P pin from 0 V to 850 mV.

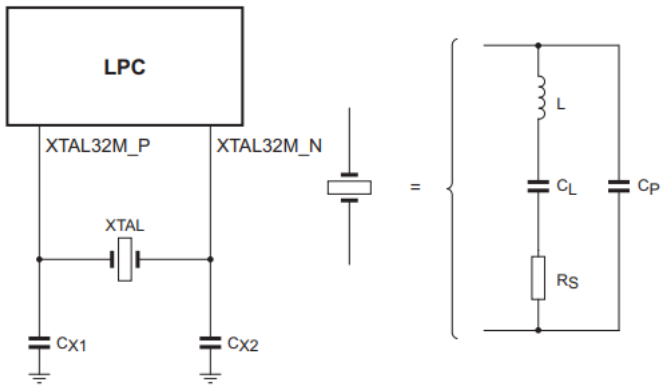


Figure 27. Crystal oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal.

13.3.1 Crystal Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.4 RTC oscillator

The crystal oscillator has embedded capacitor bank where it can be used as an integrated load capacitor for the crystal oscillators. The capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) between 6 to 10pF (IEC equivalent).

Simple APIs to configure the Capacitor Banks based on the crystal Capacitive Load (CL) and measured PCB parasitic capacitances on XIN and XOUT pins.

In the crystal oscillator circuit, only the crystal (XTAL) needs to be connected with the option to connect capacitances CX1 and CX2 on XTAL32K_P and XTAL32K_N pins. Depending upon the computation of the required Capacitance Load, there is no need to add some capacitance on PCB if computation is less than 20 pF (10 pF equivalent IEC), and if computation is greater than 20 pF (10 pF equivalent IEC), then additional capacitance is on PCB required. See Figure 23 and refer to the "Cap Bank API" chapter in the user manual.

In bypass mode, an external clock (maximum frequency of up to 100 kHz) can also be connected to XTAL32K_P if XTAL32K_N is left open. External [0 – VH] square signal can be applied on the XTAL32K_P pin with 1.1 V +/-10%

A external signal below 1.0 V or above 1.2 V cannot be applied

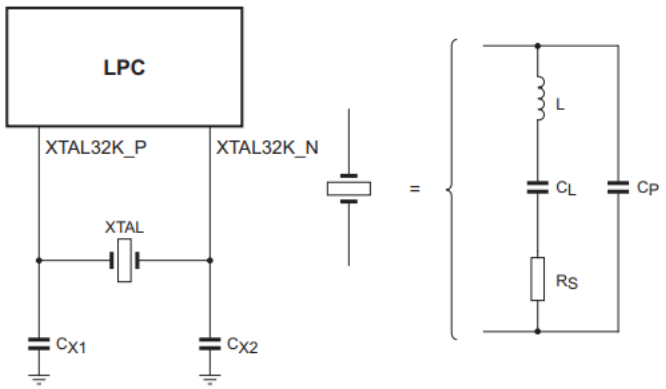


Figure 28. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal.

13.4.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.5 Suggested USB Full-speed interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 29"USB interface on a self-powered device where USB_VBUS = 5 V") or bus-powered device (see Figure 30).

The USB_VBUS pin is 5 V tolerant only when VDD is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when

VDD = 0 V.

If VDD is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For such USB applications, the internal pull-down on the GPIO/VBUS pad must be enabled on pins P0_22 or P1_11 when attaching/de-attaching in the USB application. Enable the internal pull-downs with user software. For USB ISP mode, the internal resistor pull-down is not enabled on the P0_22 pin where the VBUS pin can be floating. USB enumeration may still occur when VBUS is not connected.

For systems where VDD can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 VDD to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions:

VBUSmax = 5.25 V

VDD = 3.6 V

The voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

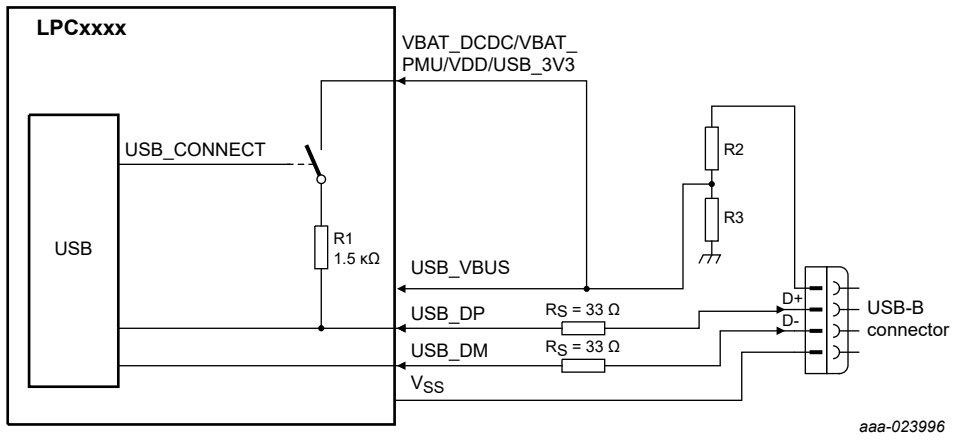


Figure 29. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kW) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.

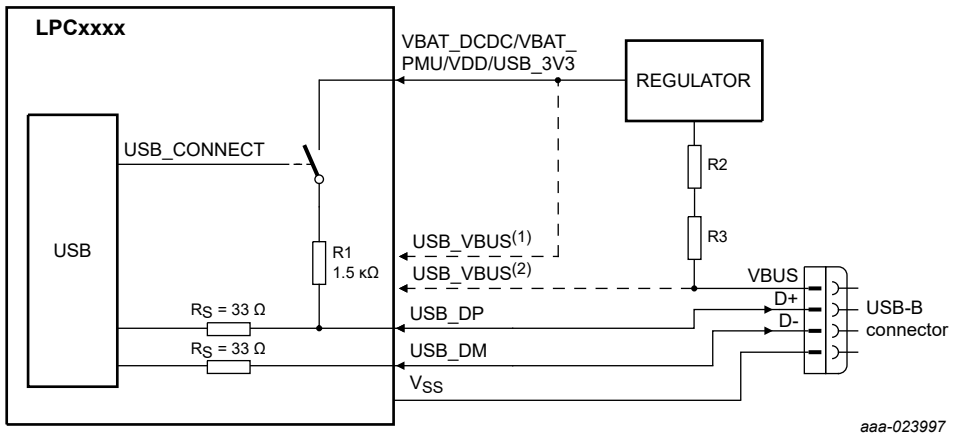


Figure 30. USB interface on a bus-powered device

Two options exist for connecting VBUS to the USB_VBUS pin:

- Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.
- Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply VDD. Since the USB_VBUS pin is only 5 V tolerant when VDD is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at Tamb = 45 °C and 8 years at Tamb = 55 °C assuming that USB_VBUS = 5 V is applied continuously while VDD = 0 V.

13.6 USB1 High-speed VBUS threshold levels

The USB1 has the following characteristics for VBUS (see Table 47). The USB1_VBUS can tolerate an input voltage of 5.5 V.

Table 47. USB1 High-speed VBUS threshold levels

Function	Min	Typ	Max	Unit
Votg_sess_valid	0.8	-	4.0	V
VBUS_valid	4.192	-	5.5	V
Vadp_probe	0.6	-	0.8	V
Vadp_sense	0.20	-	0.55	V

14 Package outline

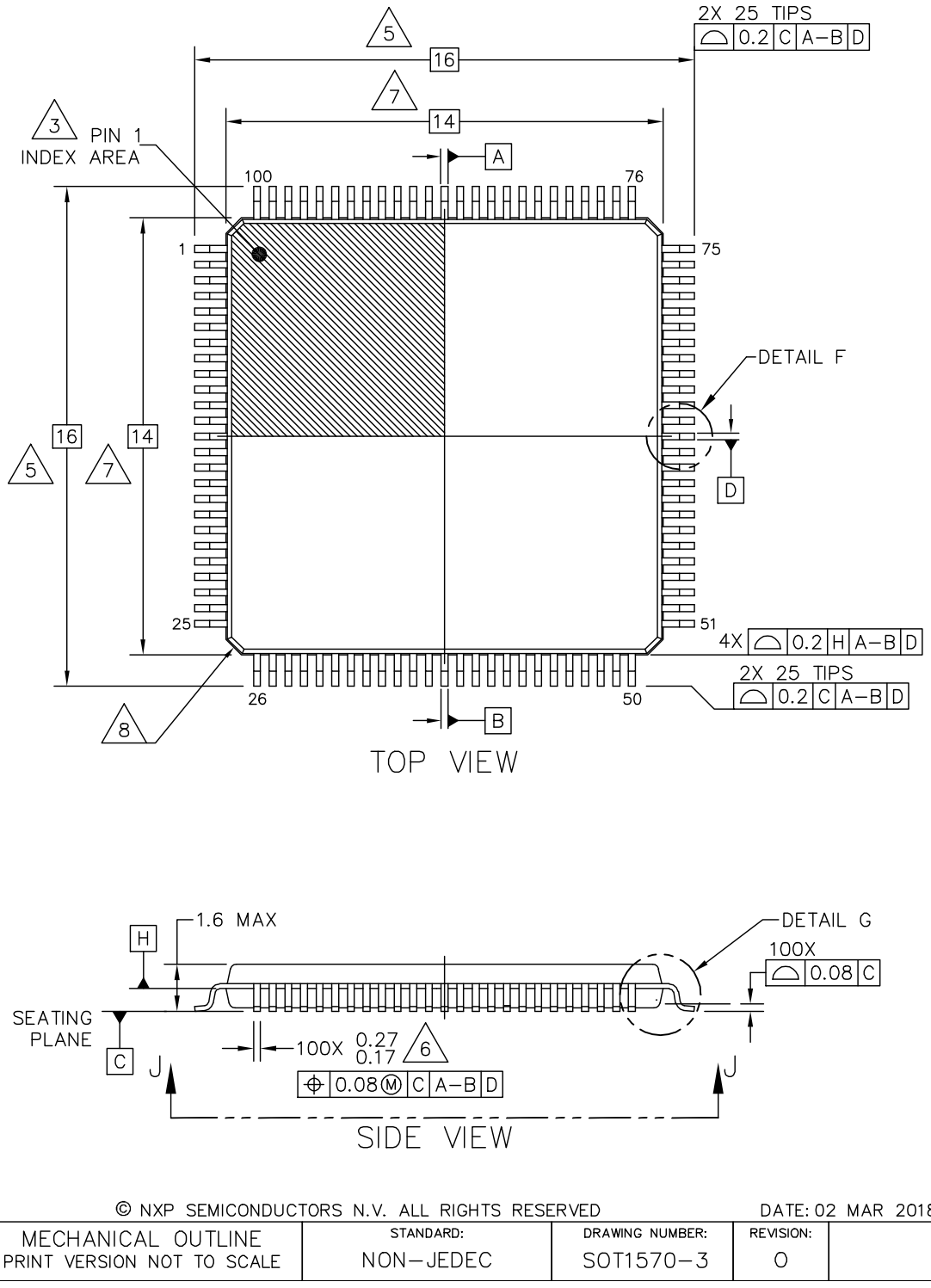


Figure 31. HLQFP100 Package outline 1

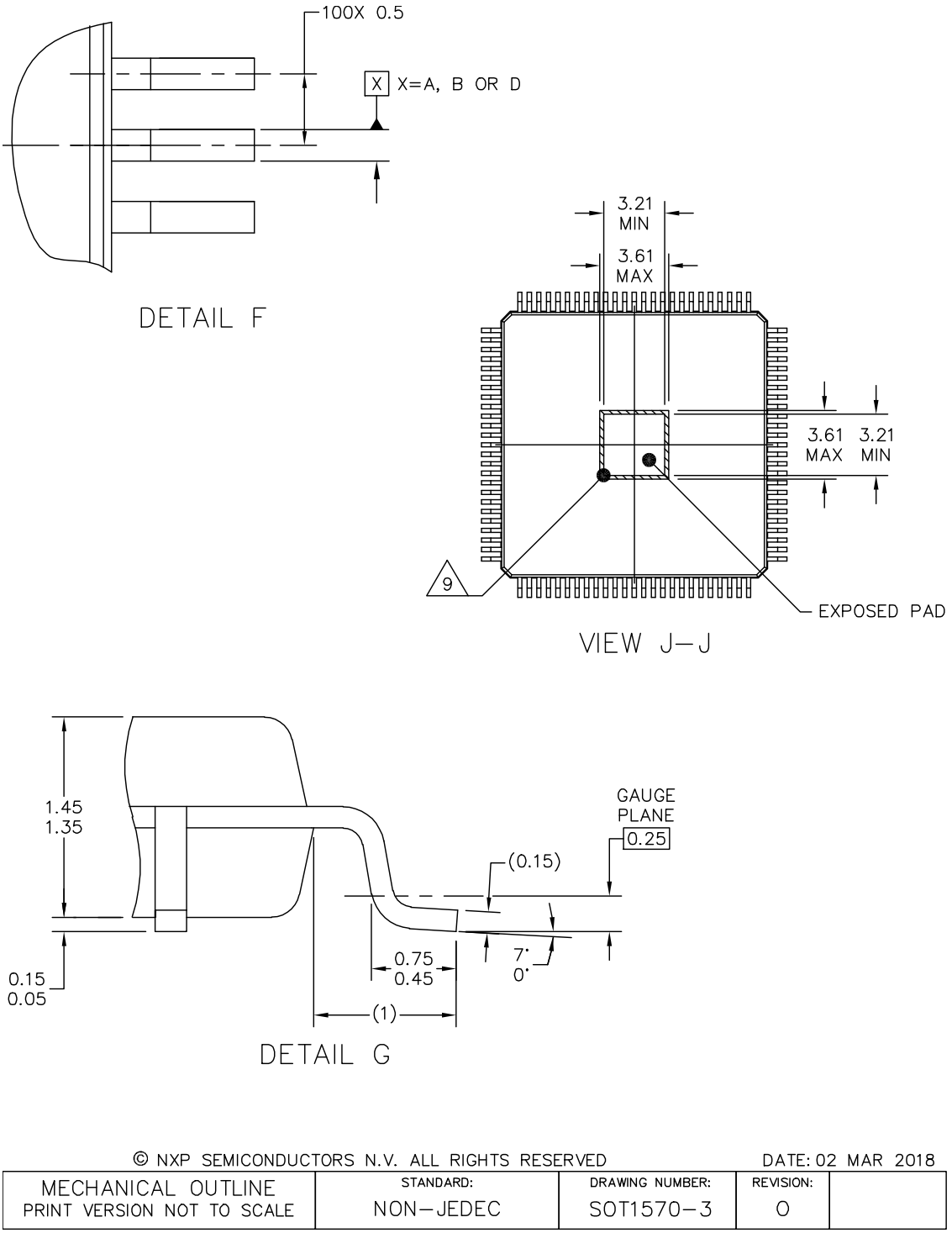
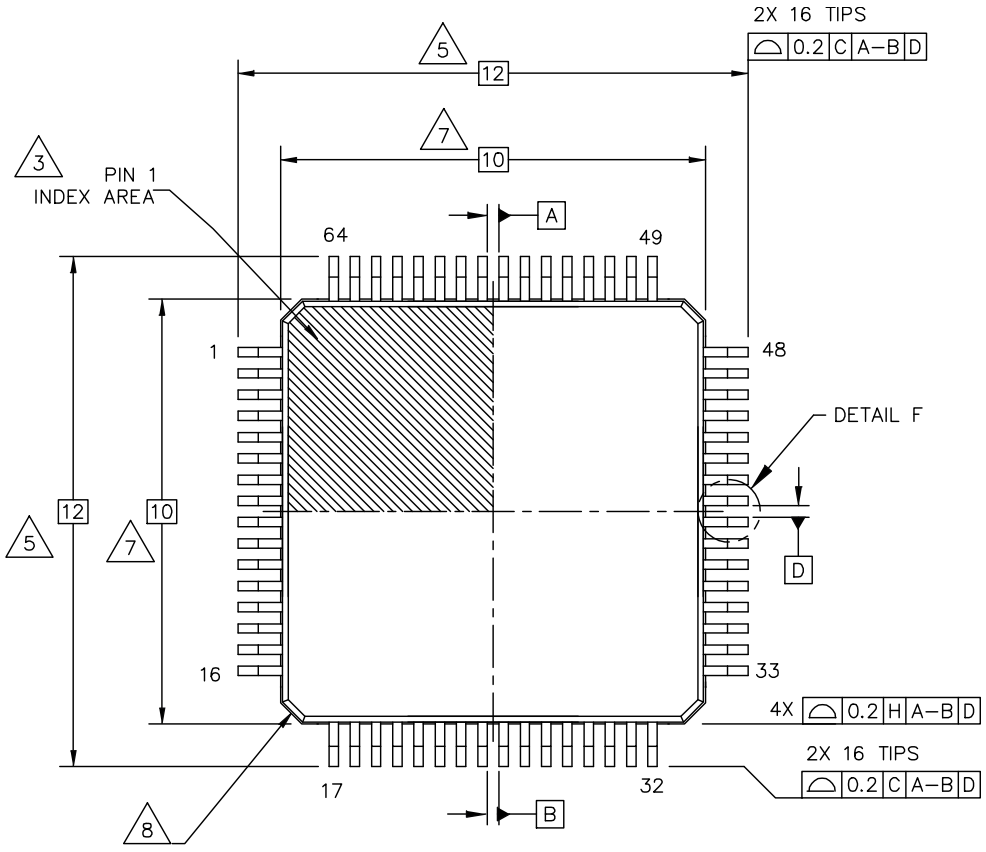
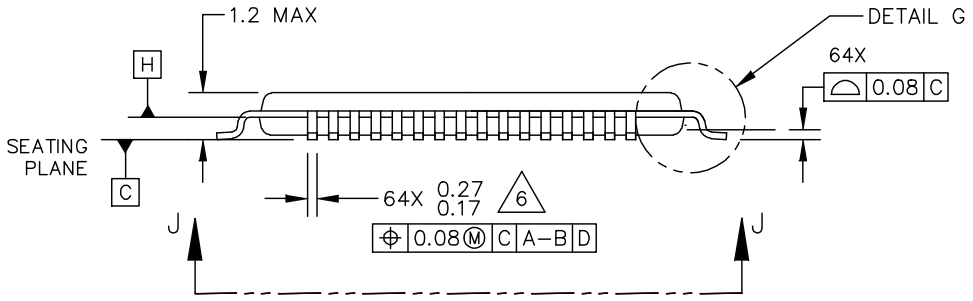


Figure 32. HLQFP100 Package outline 2





DATE: 18 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01376D	REVISION: O	

Figure 33. HTQFP64 Package outline 1

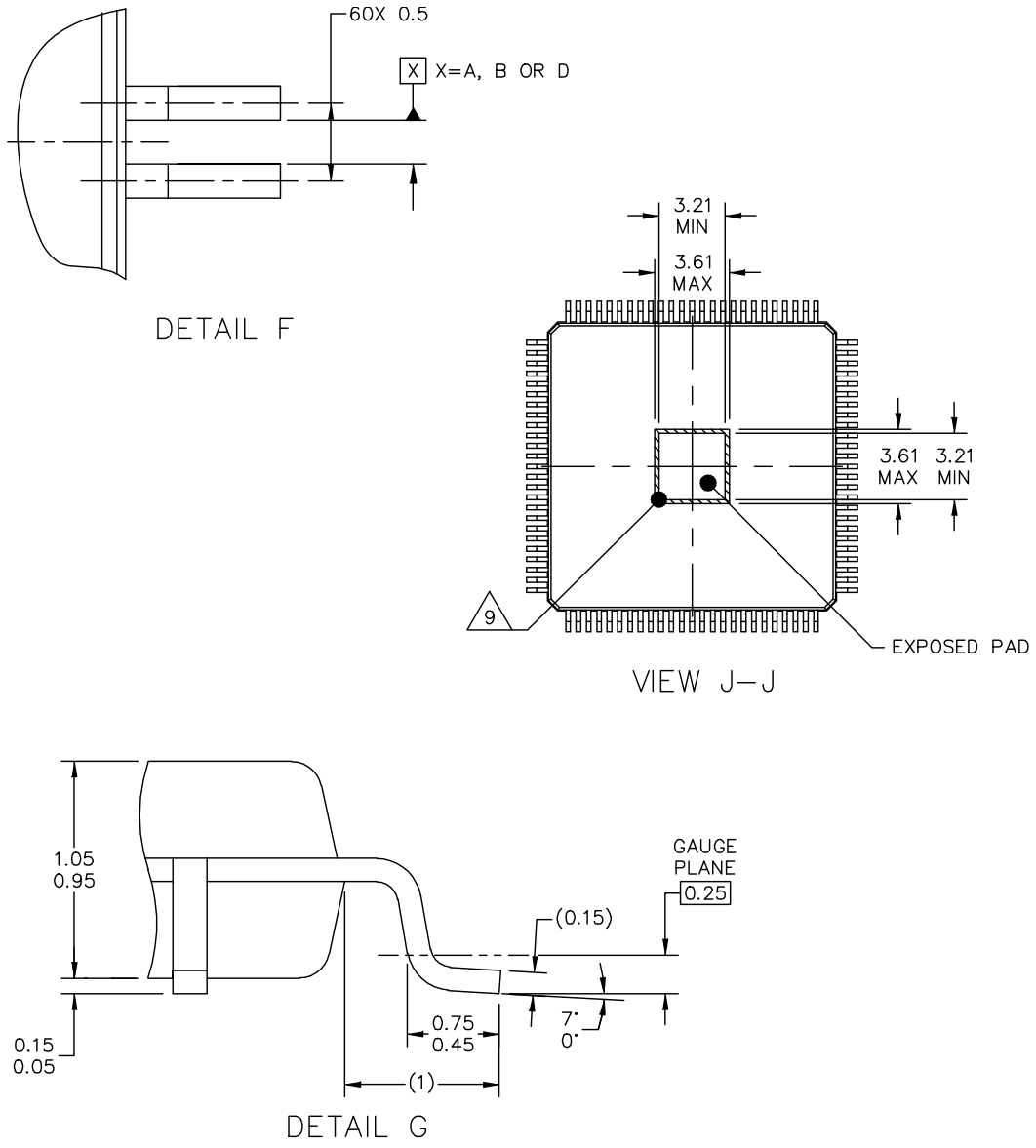


Figure 34. HTQFP64 Package outline 2

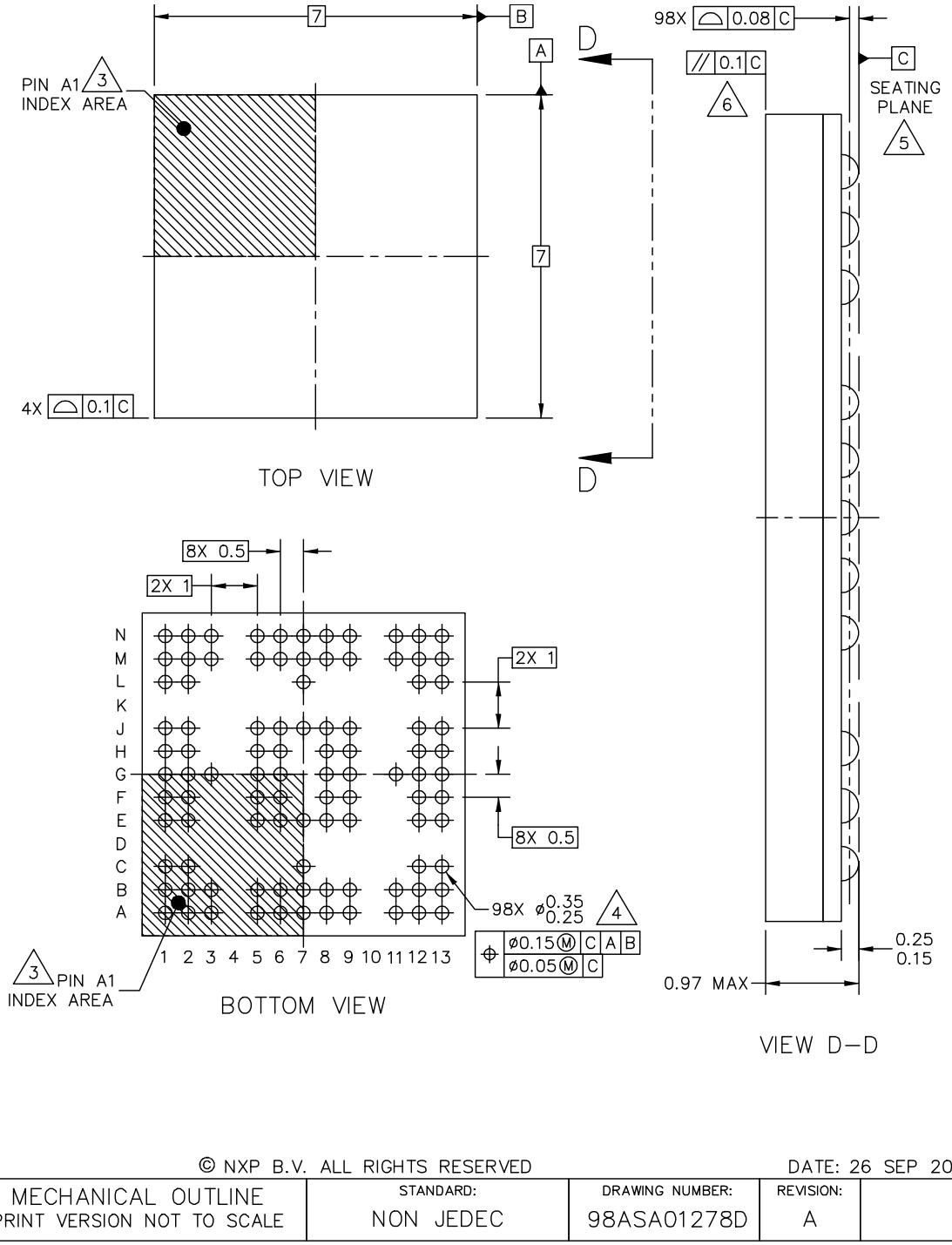


Figure 35. VFBGA98 Package outline

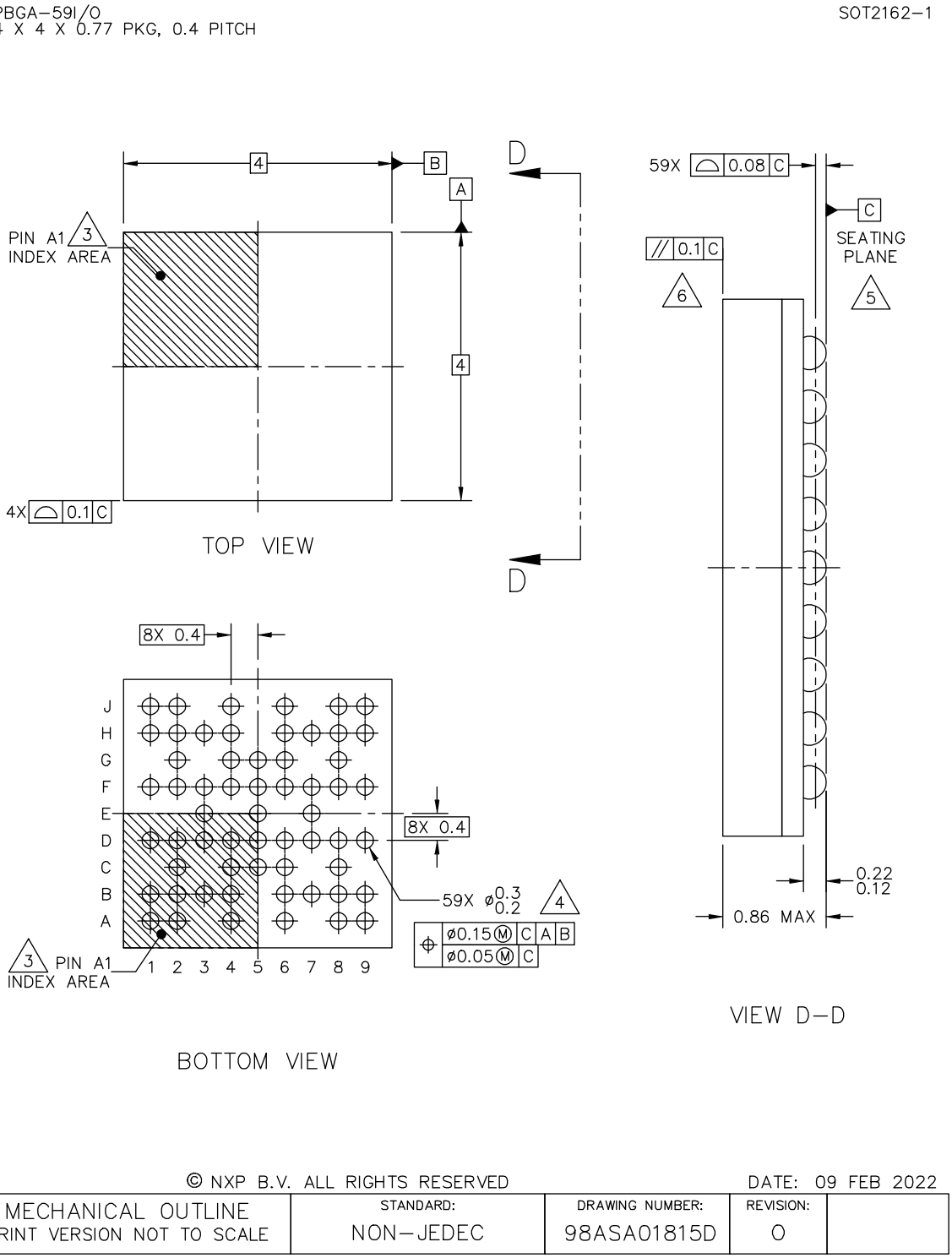
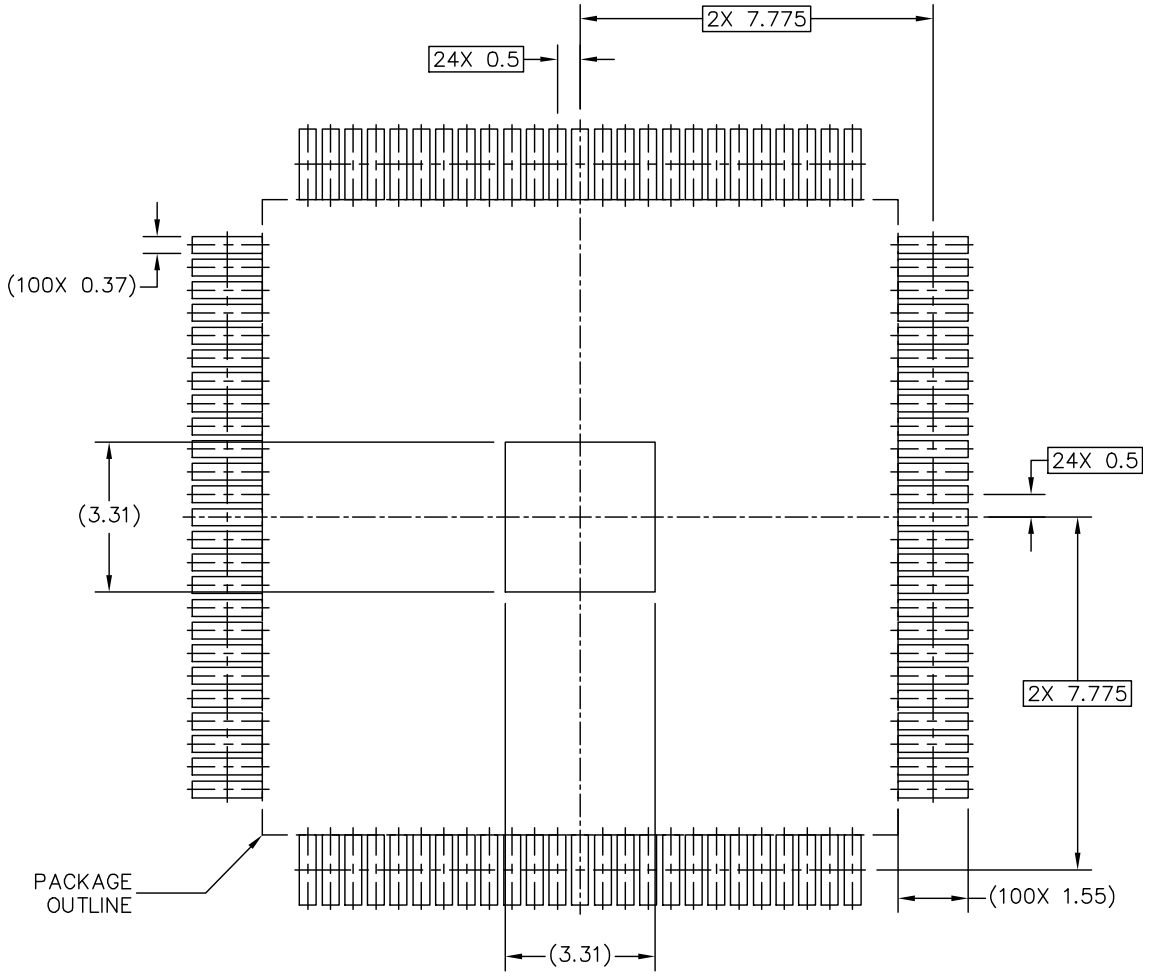


Figure 36. VFBGA59 Package outline

15 Soldering



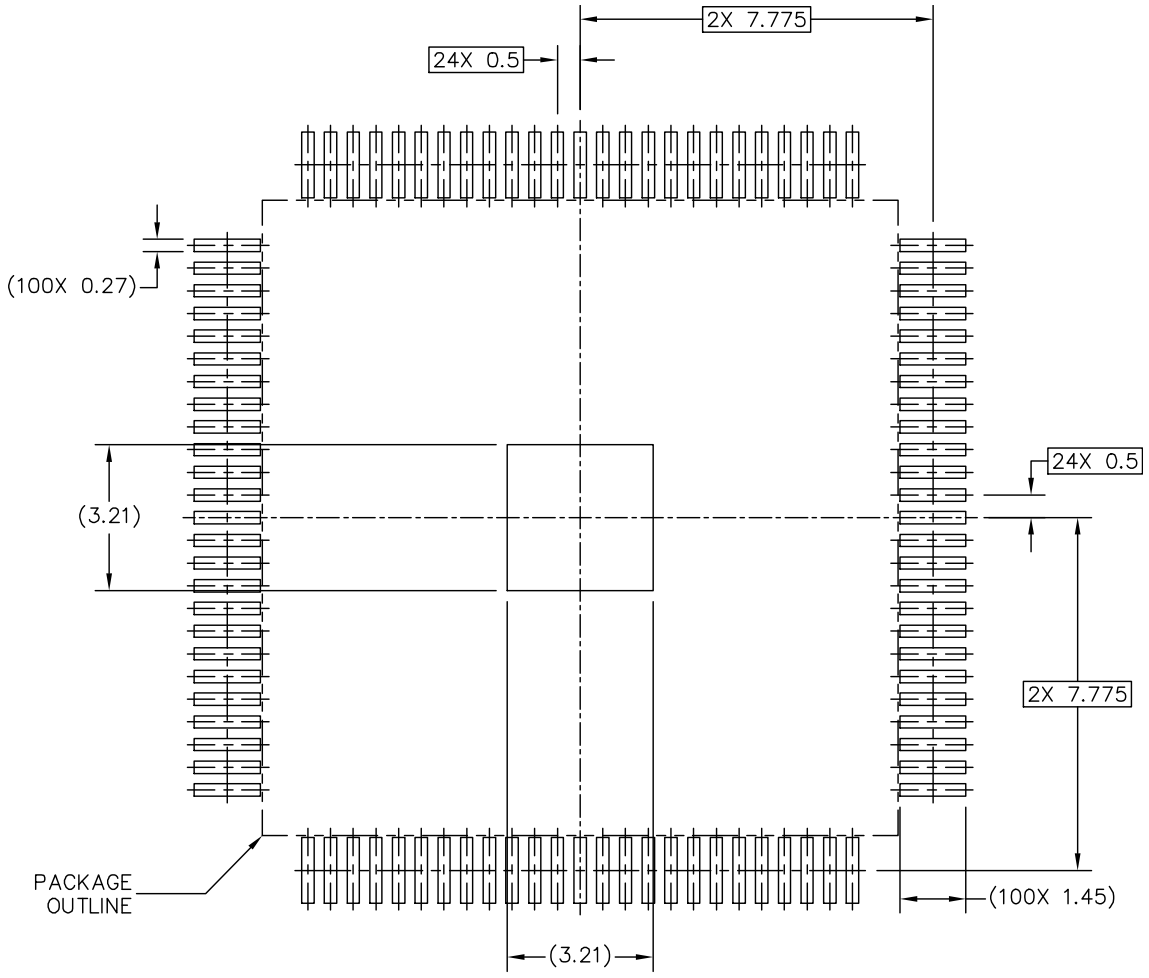
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

 DATE: 02 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: SOT1570–3	REVISION: O	

Figure 37. HLQFP100 Soldering footprint part 1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 02 MAR 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: SOT1570–3	REVISION: 0	

Figure 38. HLQFP100 Soldering footprint part 2

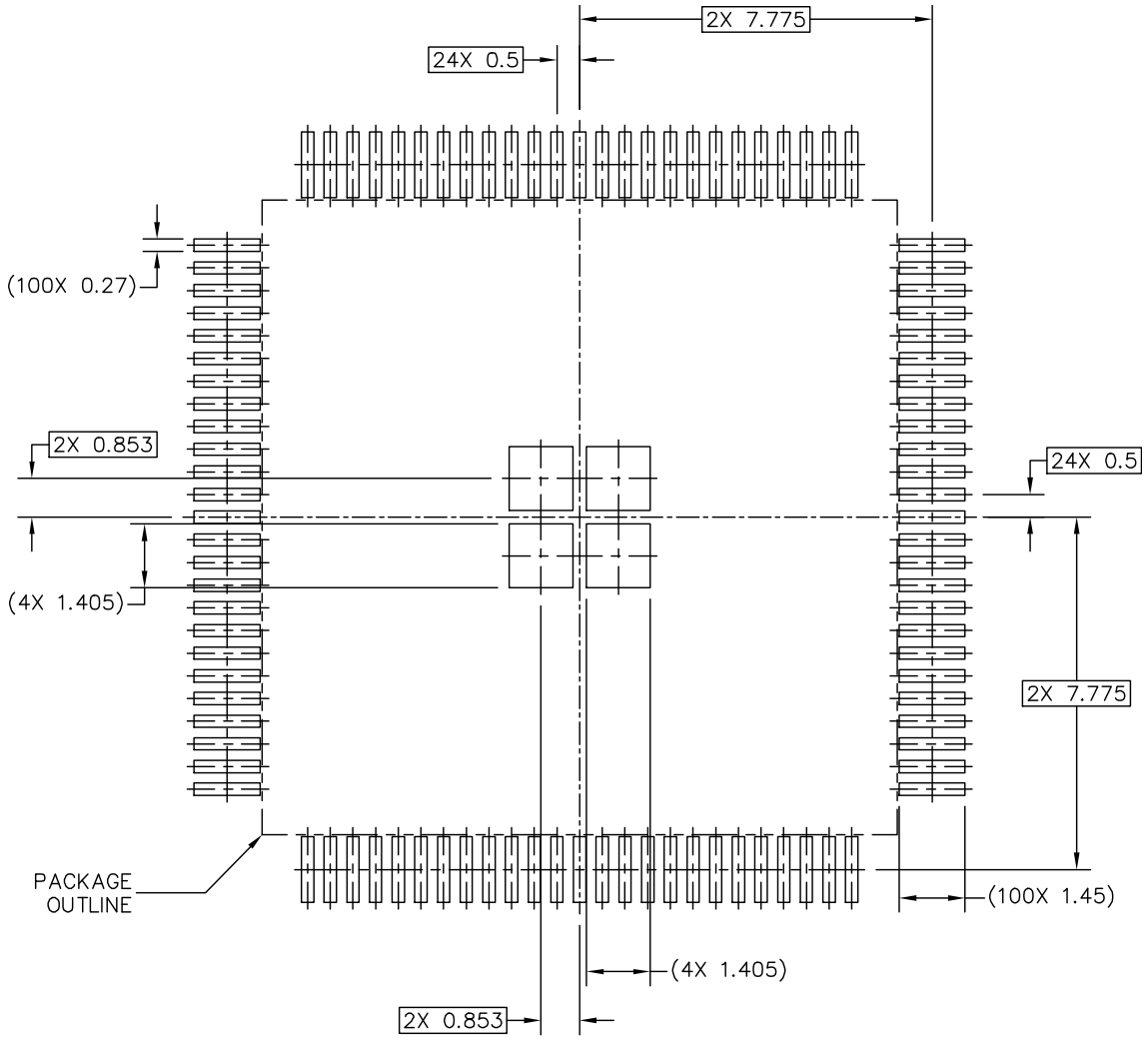


Figure 39. HLQFP100 Soldering footprint part 3

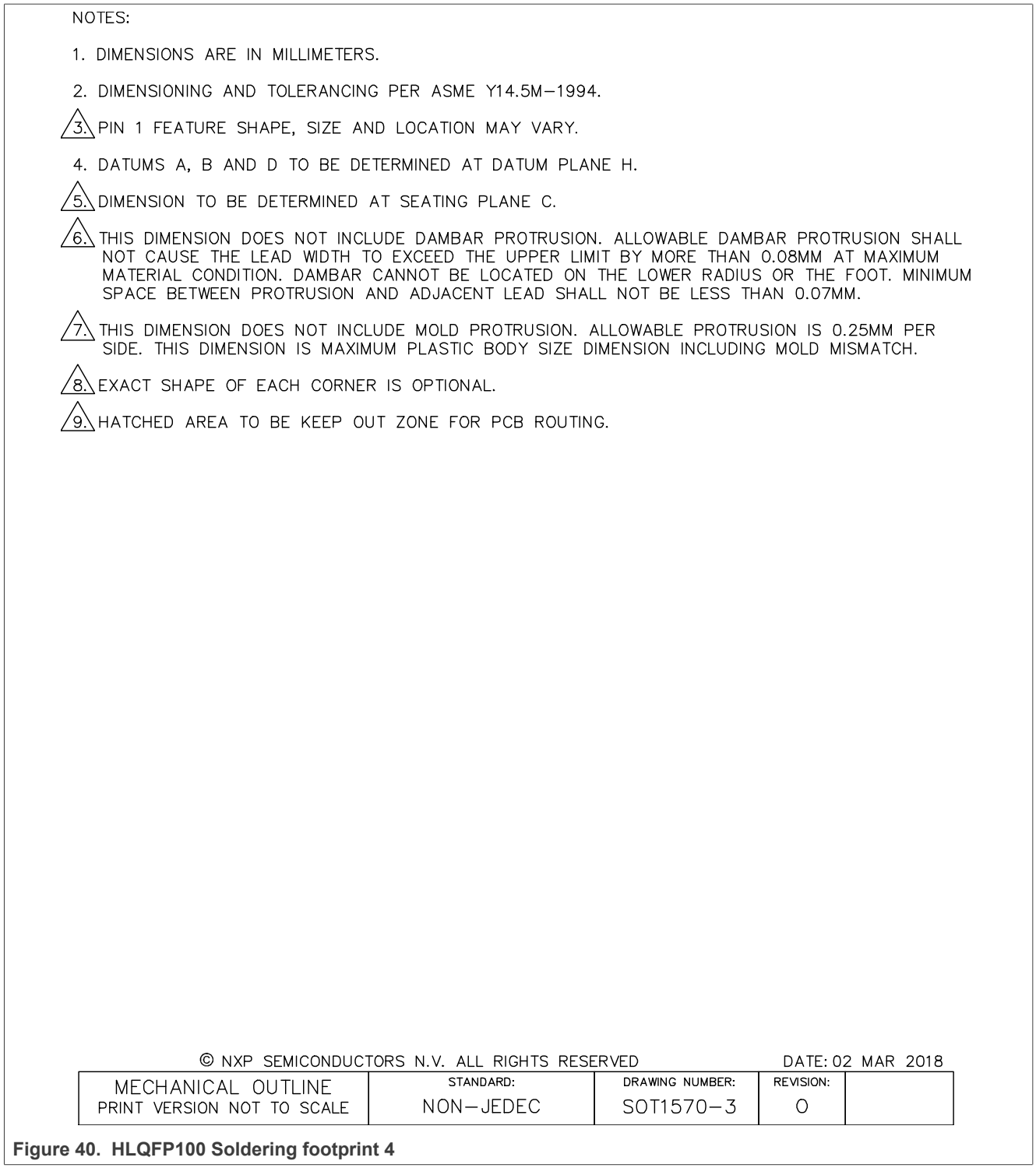
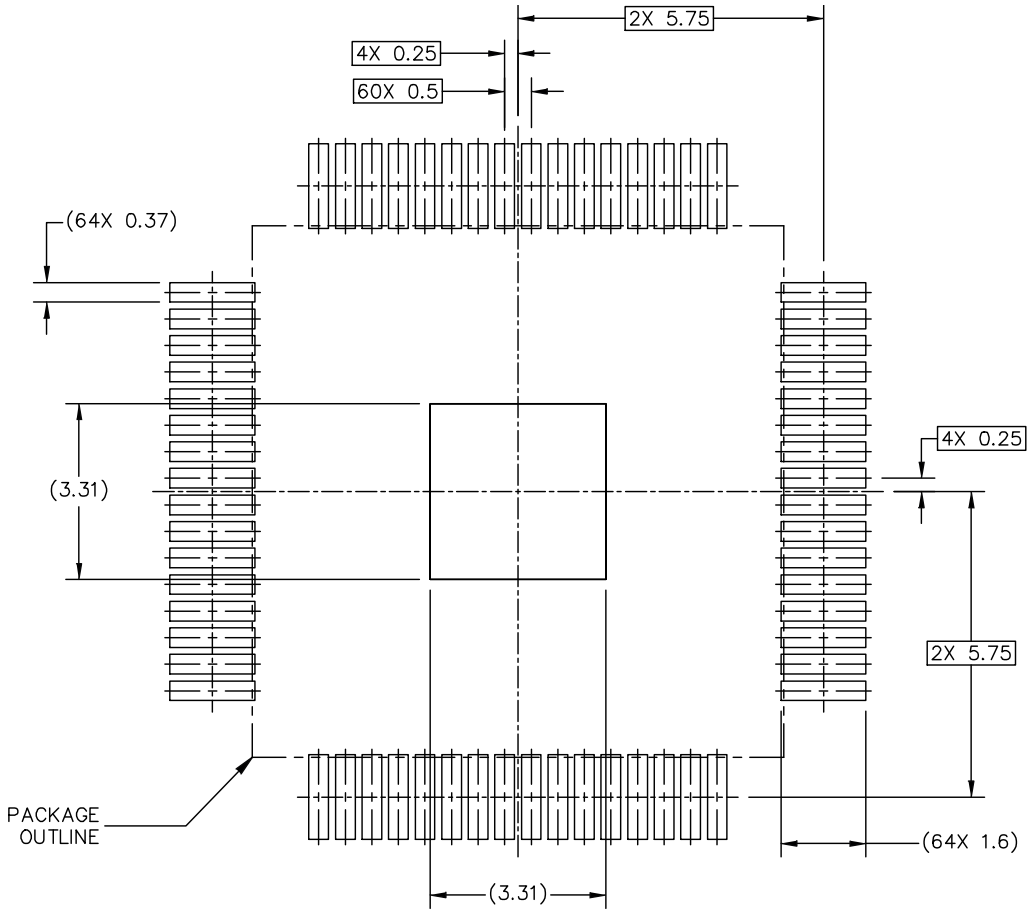


Figure 40. HLQFP100 Soldering footprint 4



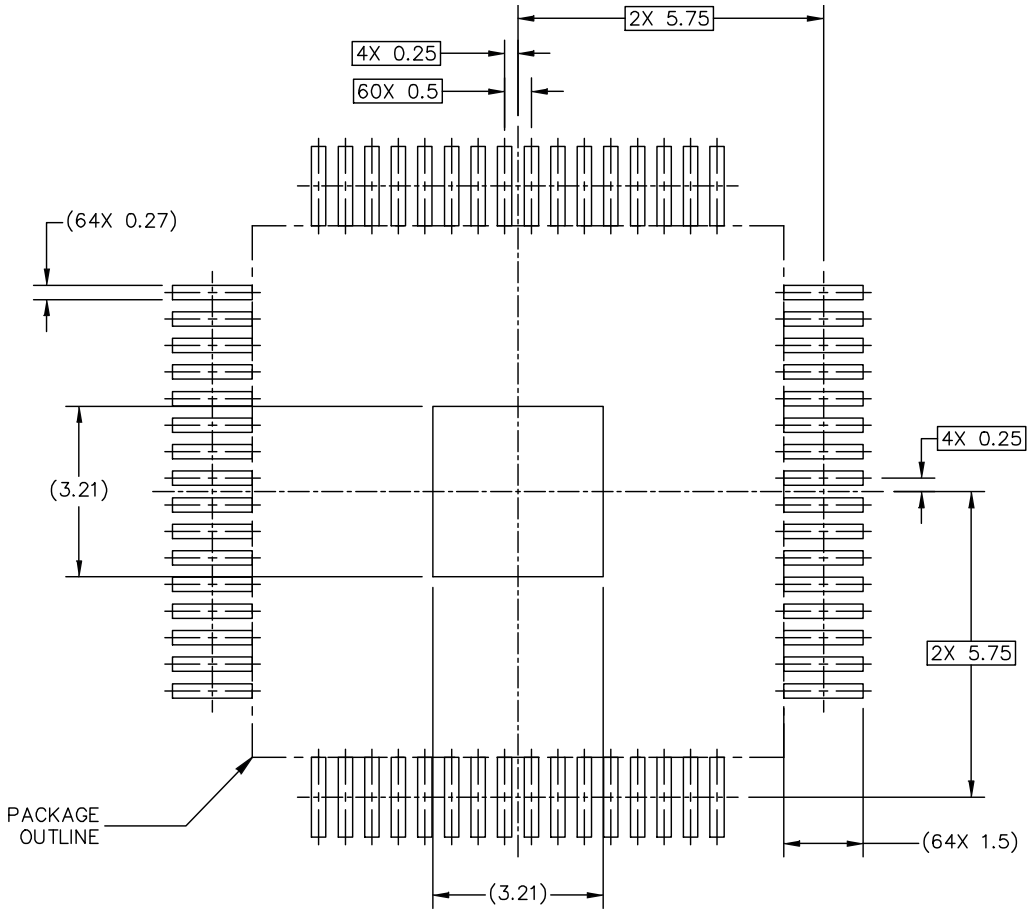
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 18 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01376D	REVISION: O	

Figure 41. HTQFP64 Soldering footprint part 1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 18 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01376D	REVISION: O	

Figure 42. HTQFP64 Soldering footprint part 2

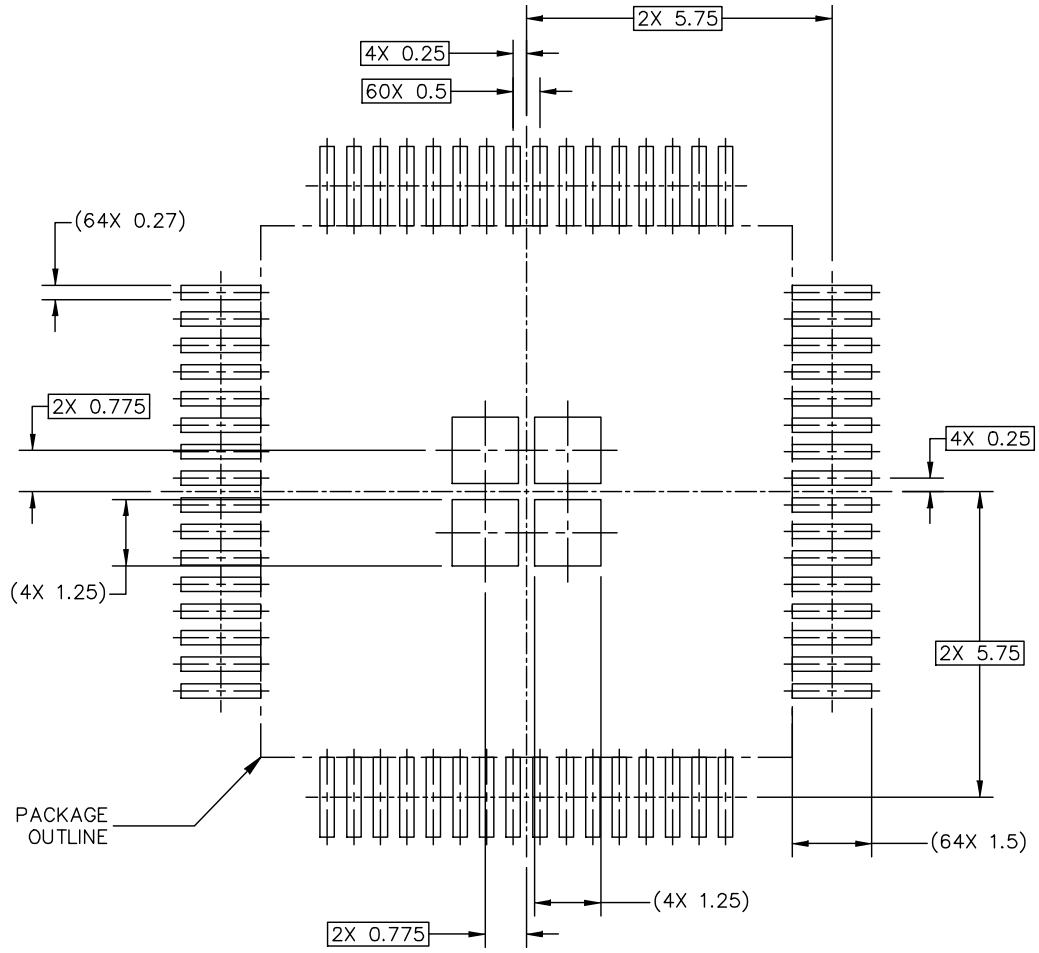


Figure 43. HTQFP64 Soldering footprint part 3

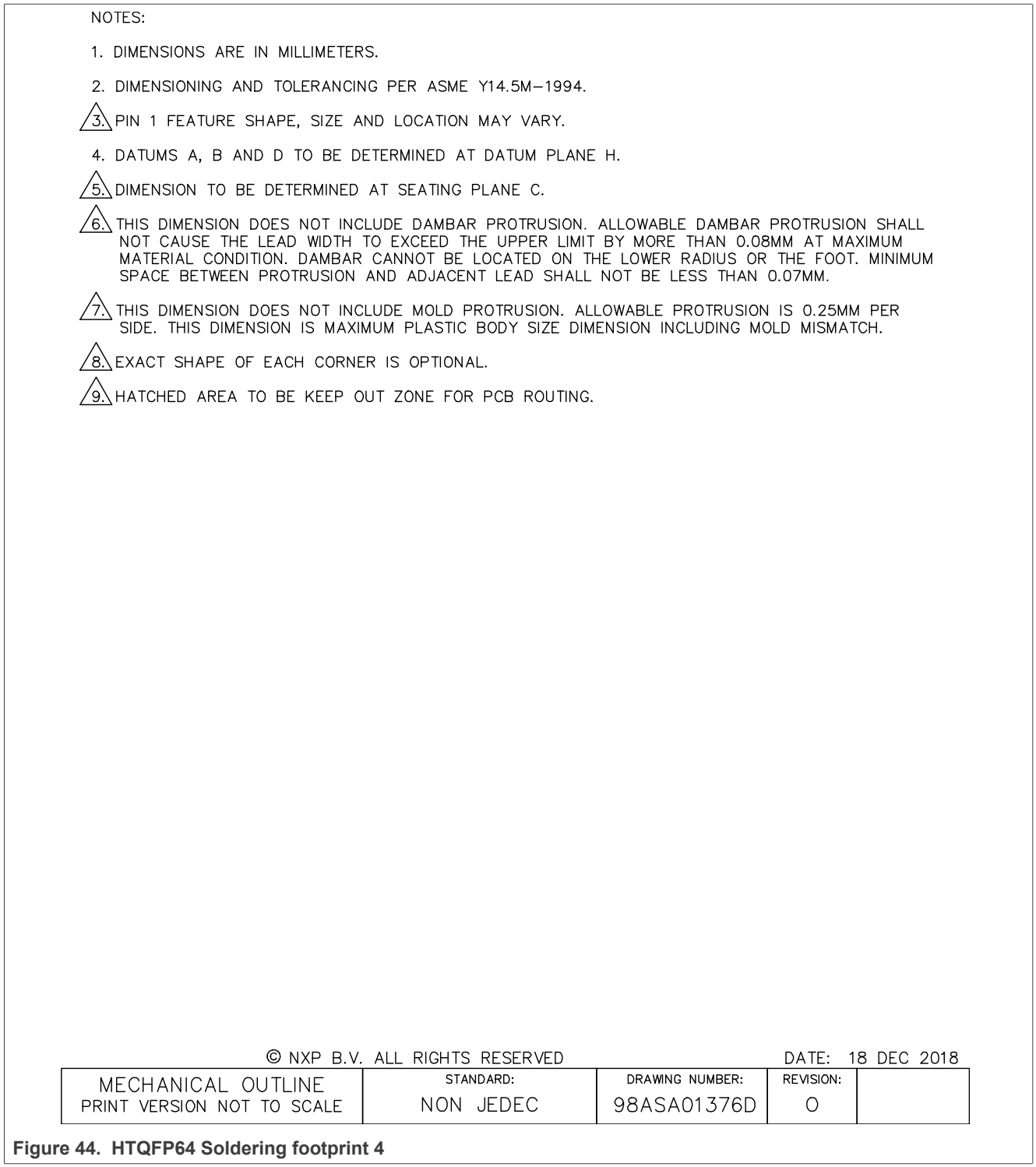
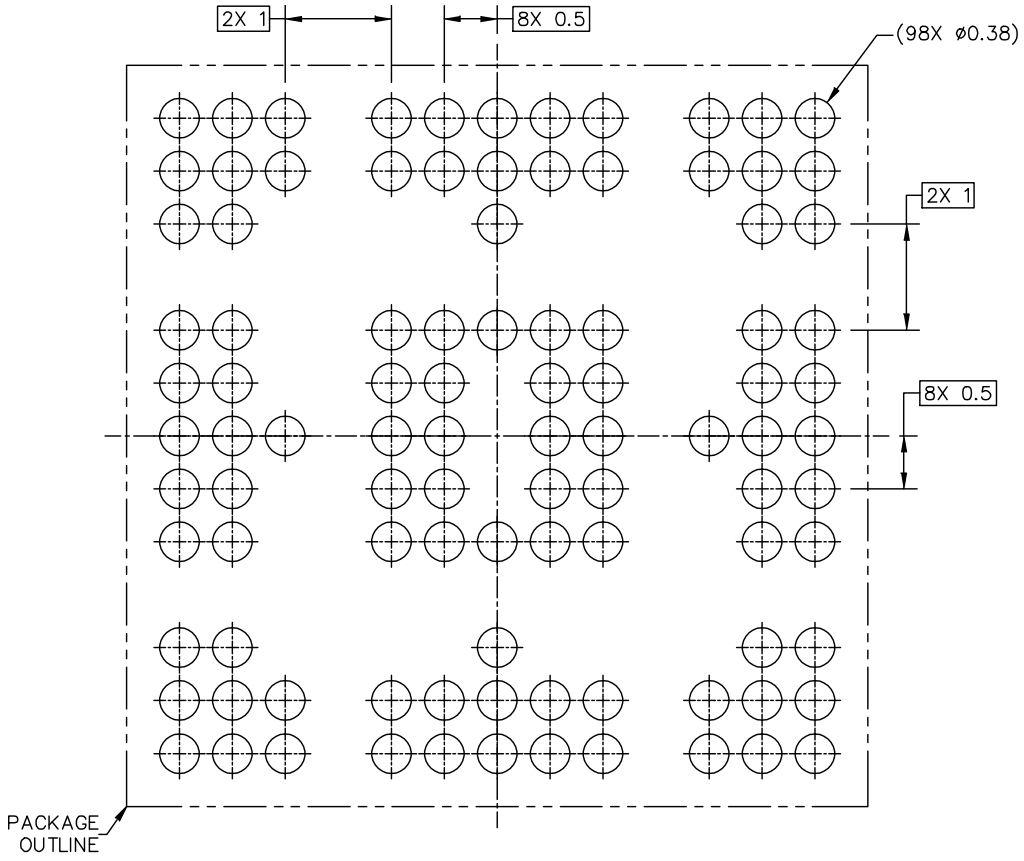


Figure 44. HTQFP64 Soldering footprint 4



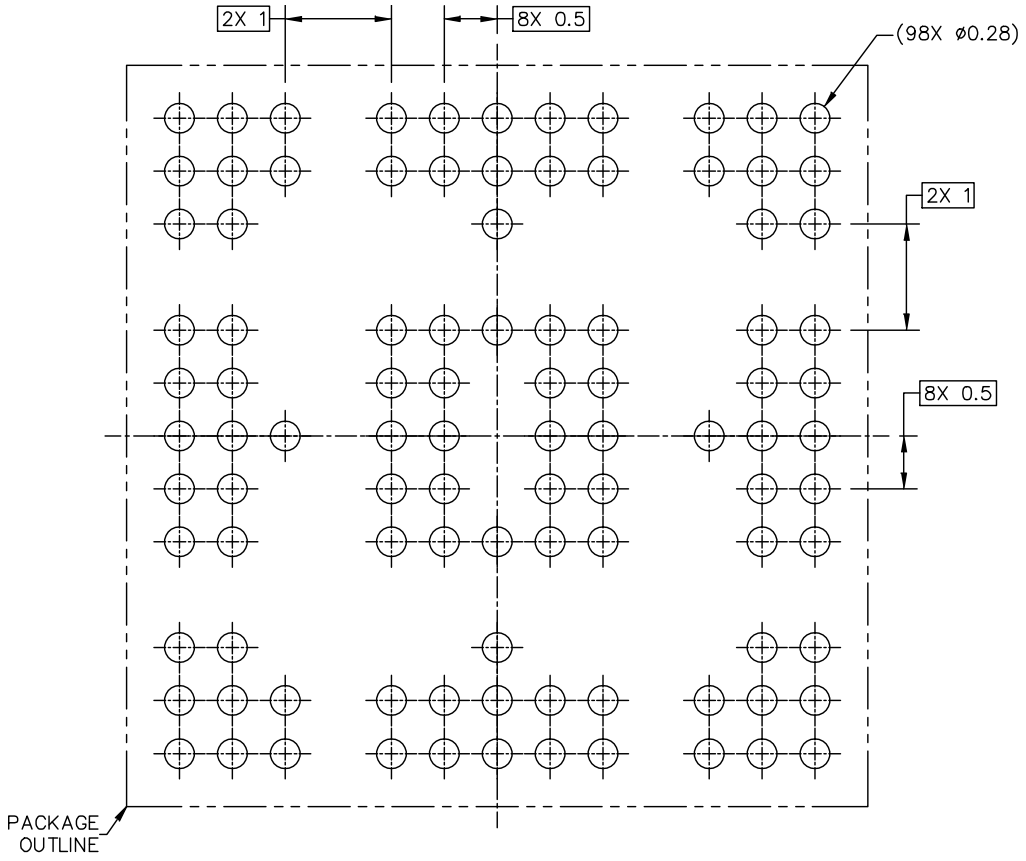
PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 26 SEP 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01278D	REVISION: A	

Figure 45. VFBGA98 Soldering footprint part 1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 26 SEP 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01278D	REVISION: A	

Figure 46. VFBGA98 Soldering footprint part 2

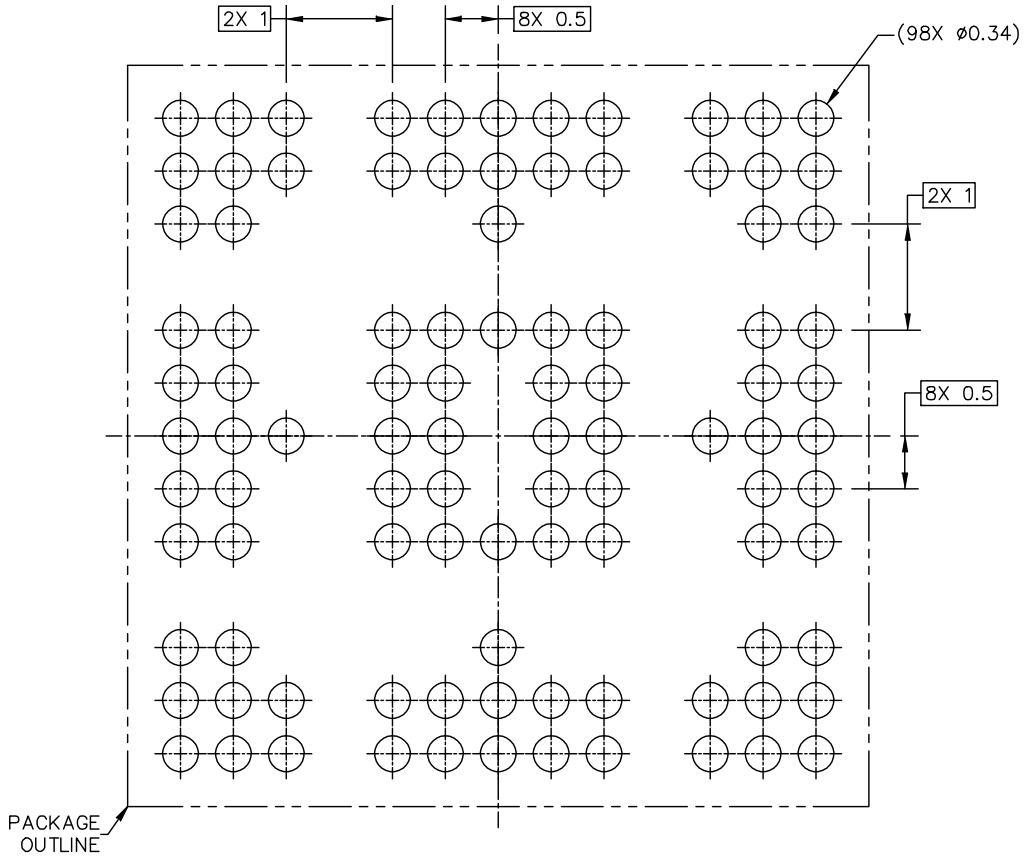


Figure 47. VFBGA98 Soldering footprint part 3

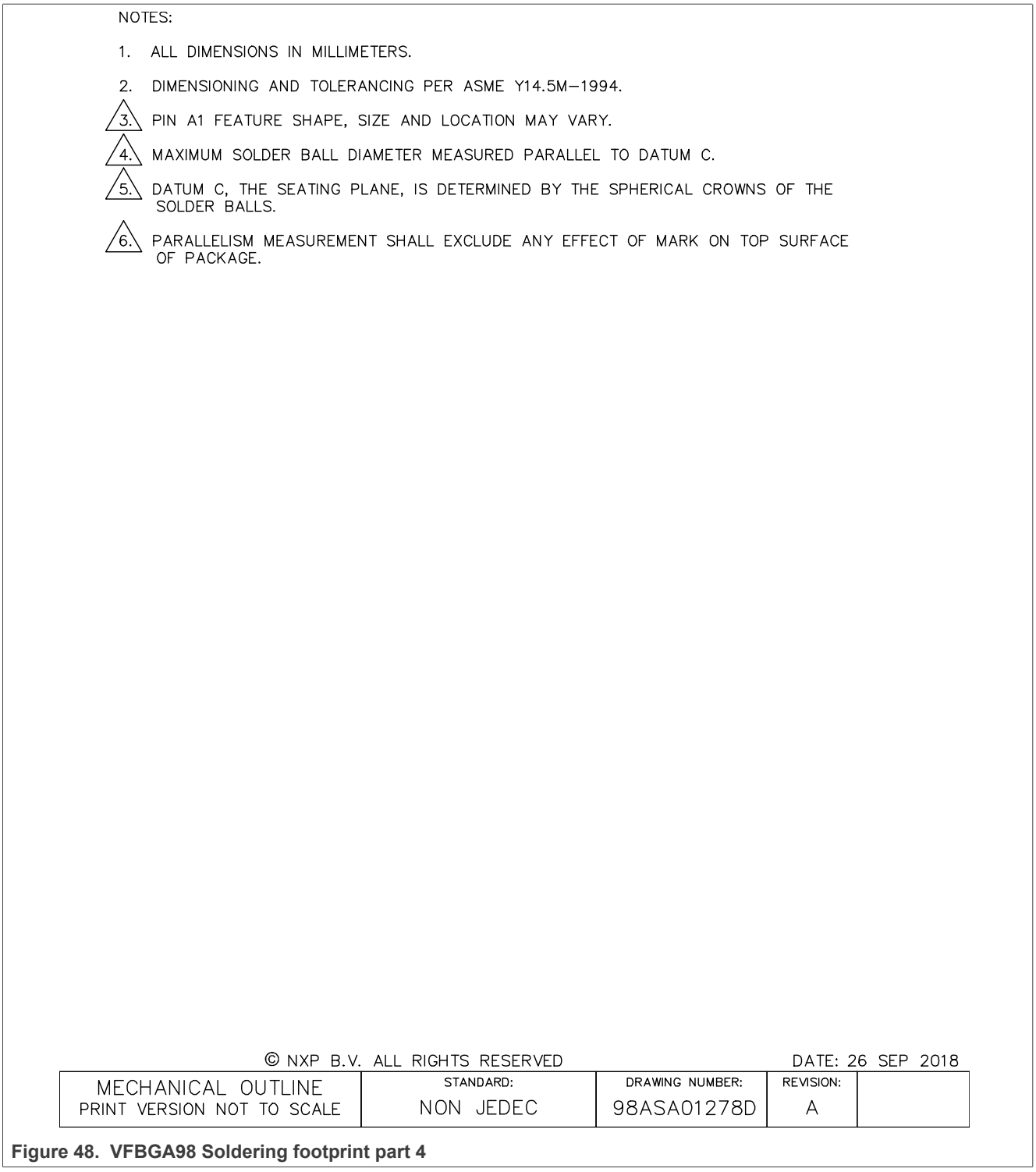


Figure 48. VFBGA98 Soldering footprint part 4

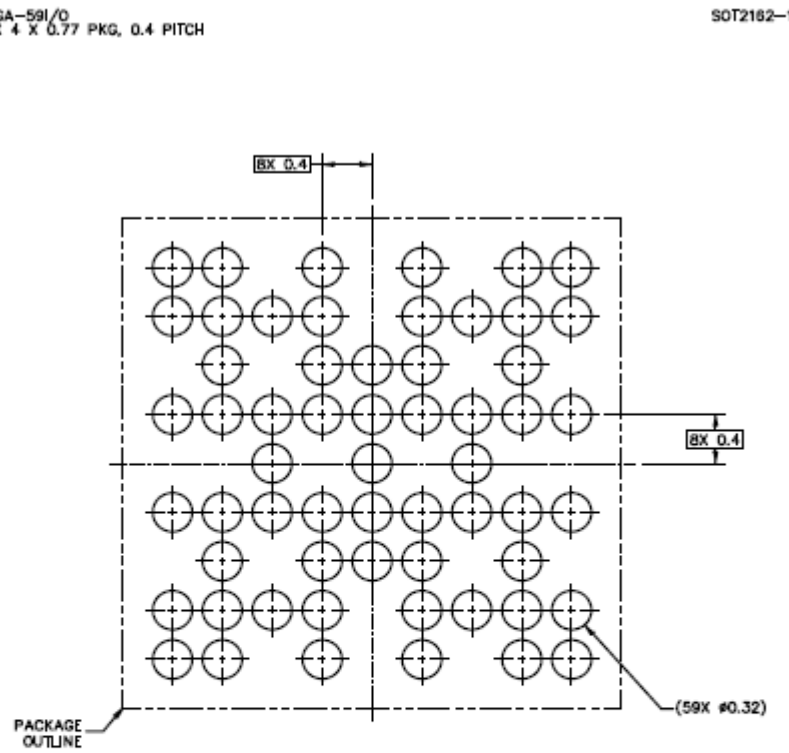


Figure 49. VFBGA59 Soldering footprint part 1

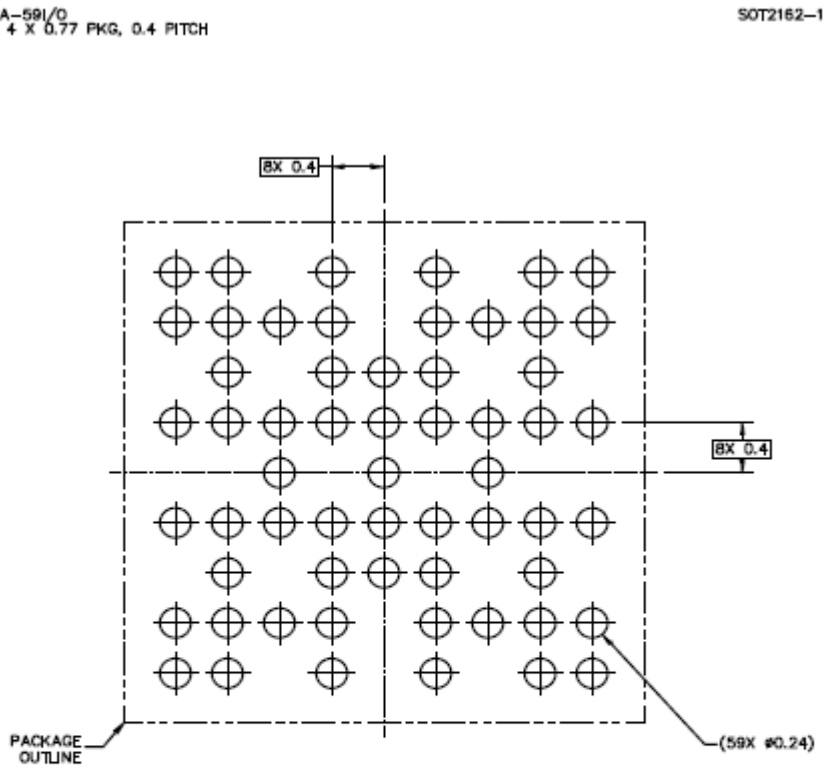


Figure 50. VFBGA59 Soldering footprint part 2

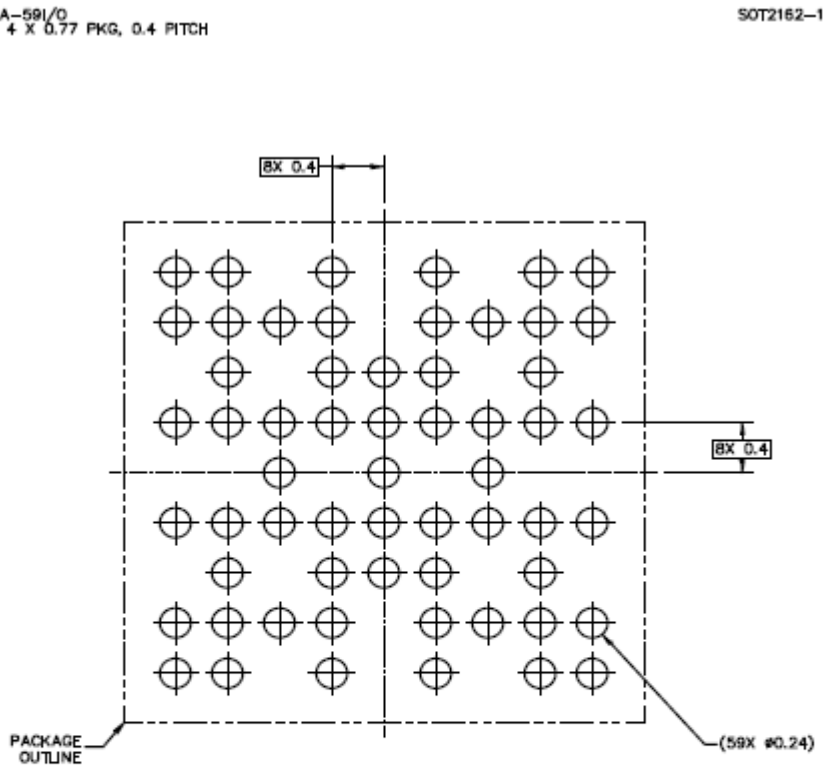


Figure 51. VFBGA59 Soldering footprint part 3

Figure 52. VFBGA59 Soldering footprint part 4

16 Abbreviations

Table 48. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator

Table 48. Abbreviations...*continued*

Acronym	Description
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17 Revision history

Table 49. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC55S6x v2.5	20240829	Product data sheet		v2.4
	• Shortened the descriptive title of the document. • Added VFBGA59 package details in Section 4. • Added VFBGA59 package details in Table 1 and Table 2. • Added pin description for 59 pin VFBGA in Table 3. • Added VFBGA59 in Table 11. • Added VFBGA59 package in Table 12. • Added VFBGA59 package outline and soldering information in Section 14 and Section 15. • Updated the 'First line' under HLQFP100 package marking in Section 4. • Added SDIO delay_i and delay_o parameters in Section 11.14.			
LPC55S6x v2.4	20221208	Product data sheet	202212017I	v2.3
	• Updated crystal oscillator frequency from 1 MHz to 12 MHz and clock frequencies from 24 MHz to 25 MHz in Section 7.22.1. • In Section 13.3 updated maximum frequency up to 25 MHz. • Updated endpoints to 12 physical (6 logical) in Section 7.26.2.1. • Updated recommended termination of unused pins for XTAL32M_P in Table 4. • In Table 4, updated pin USBn_3V3 to read "when not using USB, pin can be connected to ground as well". • USART3 and OSTIMER data added in Table 20. • Added Section 13.1. • Added Figure 2. • Added Table 17. • Updated minimum, maximum, and unit value of common to master and slave in Table 35. • In footnote 7 of Table 42 added "For best performance, force the offset calibration to -16. Set this prior to performing the gain calibration". • Added Section 13.5. • In Table 3, added "Maximum frequency on PLU clock input is 25 MHz" for PLU_CLKIN: PIO0_21 and PI01_25. • In Table 3 updated "Table note 3". In this table note, removed "Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value)". • In Table 3 updated "Table note 5", and "Table note 6". • Added GPIO logic state in Section 7.23.2 and in Section 7.23.3.			

Table 49. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	• In Section 7.23.3, added IOCON registers and peripheral registers details. • In Section 7.26.3.2, updated maximum supported bit rate for SPI master mode (transmit/ receive) to 32 Mbit/s and for SPI slave transmit mode to 16 Mbits/s. • In Section 7.26.3.4, updated maximum bit rate to 10 Mbit/s for asynchronous mode and 25 Mbit/s for synchronous mode. • Added text "External power supply" in Figure 6. • Updated maximum supported bit rate for master and slave synchronous mode in Section 11.11. • Updated maximum supported bit rate for master and slave synchronous mode in Section 11.13. • Updated $T_{jmax\ (Device)}$ and $T_{jmax\ (Silicon\ Process)}$ details in Table 13. • Added new parameter Nupdates in Table 26. • In Section 4, replaced "third line" with "Fifth line: zzzyywwxR". • Operating frequency of crystal oscillator updated to 16 MHz instead of 12 MHz in Section 2 and Section 7.22.1. • Added Table 18.		
LPC55S6x v2.3	20210709	Product data sheet	202108001I	v2.2
	Added new Section 11.1.			
LPC55S6x v2.2	20210510	Product data sheet	-	v2.1
	Updated DICE information in Section 1, Section 2, Section 7.11, and added Section 7.31.7.			
LPC55S6x v2.1	20201209	Product data sheet	-	v2.0
	SPI and HSPI max bit rates were updated in Section 11.11, and Section 11.12.			
LPC55S6x v2.0	20201123	Product data sheet	-	v1.9
	Updated various sections and added Section 13.6. The FRO spec was improved to +/- 1% for temp range 0 C to 85 C.			
LPC55S6x v1.9	20200210	Product data sheet	-	v1.8
	Updated Section 2 for Clock Generation regarding embedded capacitor bank for the crystal oscillator.			
LPC55S6x v1.8	20200122	Product data sheet	-	v1.7
	Updated Table 20 .			
LPC55S6x v1.7	20191122	Product data sheet	-	v1.6
	Updated HTQFP64 pin numbering for FB and VSS_DCDC pins See Table 3 Updated Table 26.			
LPC55S6x v1.6	20191016	Product data sheet	-	v1.5
	Updated Table 28 Updated Table 14 Updated Section 4			
LPC55S6x v1.5	20190930	Product data sheet	-	v1.4
	Updated Table 45 Updated Table 42 Updated Table 44			
LPC55S6x v1.4	20190722	Product data sheet	-	v1.3

Table 49. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
	Added device revision 1B Updated Table 42			
LPC55S6x v1.3	20190717	Product data sheet	-	v1.2
	Updated Table 42 Updated Table 23 Updated Figure 10			
LPC55S6x v1.2	20190702	Product data sheet	-	v1.1
	Updated Table 42 Updated Table 15. Updated Table 41 Updated Table 24 Updated Table 20 and Table 16 Updated Table 12 Updated Table 13 Updated Table 14 Updated Table 23 Updated Table 45 Updated Table 43			
LPC55S6x v1.1	20190402	Product data sheet	-	v1.0
Modifications:	• Updated Table 42 • Updated Table 44 • Updated Table 28 • Updated Table 27. • Updated Table 24 • Updated Table 20. • Updated Table 36, Table 37, and Table 38			
LPC55S6x v1.0	20190225	Product data sheet	-	-

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

LPC55S69-EVK LPC55S69JEV59E LPC55S66JEV59E LPC55S69JEV59Y LPC55S66JEV59Y