**KTVR5100FRDMEVM** evaluation board Rev. 1.0 — 3 August 2016

User guide





KITVR5100FRDMEVM evaluation board

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### 3 Overview of the VR5100 PMIC development environment

NXP offers a combination of boards that support the evaluation and programming of the VR5100 PMIC.

The KITVR5100FRDMEVM boards serves as an evaluation platform that allows designers to lab test and demo designs that incorporate the VR5100 PMIC. The evaluation board contains a preconfigured MC34VR5100 device and provides numerous jumpers and test points that allow designers to tailor the evaluation to their needs. The kit comes with a FRDM-KL25Z already mounted and loaded with compatible microcode. The FRDM-KL25Z's primary function is to control communication between the evaluation board and a PC.

The KITVR5100FRDMPGM board is designed to allow one-time programming of the VR5100's configuration fuses. The board contains a socket that houses a single VR5100 device during the OTP (One Time Programming) process. This kit also comes with a mounted FRDM-KL25Z loaded with compatible microcode. The KL25Z controls communication between the evaluation board and a PC.

Alternatively, the designer may disconnect the KITVR5100FRDMPGM socket board from its dedicated KL25Z board and mount the socket board to the top of the KL25Z on the KITVR5100FRDMEVM board. This configuration is referred to as 'Combo' mode. Microcode on the KL25Z connected to the KITVR5100FRDMEVM board recognizes whether the evaluation board is in standalone mode or whether a socket board is mounted in Combo mode. In Combo mode the designer can exercise the functionality of the evaluation board with respect to the device in the socket and use the OTP feature to program the device fuses.

The user interface for all three of the above configurations is a software GUI that can be downloaded and installed on a PC from NXP's website. The GUI provides direct access to the target VR5100 PMIC (either the device on the evaluation board or the device in the programming board socket). It allows the designer to load values for switches and regulators, read registers, clear interrupts and so forth. The GUI also provides a script editor that supports creating and executing a series of GUI commands. When the GUI is connected to a socket board, it serves as the interface for OTP programming of the VR5100 PMIC's onboard configuration fuses.

When the GUI is activated on a PC connected to a KL25Z in one of the three configurations, it senses which configuration is connected and provides the corresponding functionality.

KITVR5100FRDMEVM evaluation board

### 4 Getting started

#### 4.1 Kit contents/packing list

The KITVR5100FRDMEVM contents includes:

- Assembled and tested KITVR5100FRDMEVM evaluation board
- Firmware loaded FRDM-KL25Z board (mounted to the evaluation board)
- USB to Mini-USB cable
- Quick start guide

#### 4.2 Jump start

NXP's analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic ICs and system-in-package devices that use proven high-volume SMARTMOS technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state of the art systems.

- 1. Go to <u>www.nxp.com/KITVR5100FRDMEVM</u>.
- 2. Review your Tools Summary Page.
- 3. Locate and click:

# Jump Start Your Design

4. Download the documents, software and other information.

Once the files are downloaded, review the user guide in the bundle. The user guide includes setup instructions, BOM and schematics. Jump start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

#### 4.3 Required equipment

This kit requires the following items:

- 4.2 V power supply wall adaptor or lab power supply with 3.0 V to 5.0 V at 3.0 A capability
- Two power supply cables with banana connectors
- KITVR5100GUI installed on a Windows PC
- Optional voltmeters to measure regulator outputs
- Optional oscilloscope

#### 4.4 System requirements

The kit requires the following to function properly with the software:

• USB enabled computer running Windows XP, Vista, 7, 8, or 10 (32-bit or 64-bit)

KITVR5100FRDMEVM evaluation board

### 5 Getting to know the hardware

#### 5.1 Board overview

The KITVR5100FRDMEVM evaluation board (EVB) is an easy-to-use circuit board, allowing the user to exercise all the functions of the VR5100 power management IC.

An FRDM-KL25Z is mounted to the EVB as an integral component. The FRDM-KL25Z serves as an interface between the KITVR5100GUI and the VR5100 PMIC. The FRDM-KL25Z drives circuitry on the KITVR5100FRDMEVM, as well as provides an analog-todigital convertor (ADC) to allow real-time monitoring of the VR5100 regulator voltages, and display their values in the GUI.

#### 5.2 Board features

The board features are as follows:

- VR5100 Power Management IC
- Input supply using a wall adaptor or lab power supply through banana jacks
- Integrated FRDM-KL25Z as a communication link between the EVB and a PC
- Two 1.0 Amp E-loads with configurable current

#### 5.3 Device features

This evaluation board features the following NXP product:

#### Table 1. Device features <sup>[1]</sup>

Device	Description	Features
VR5100	Power management integrated circuit (PMIC) for i.MX series and i.MX 6 SL/SX	<ul> <li>Three adjustable high efficiency buck regulators: 1.75 A, 1.5 A, 1.25 A, 1.0 A</li> <li>5.0 V, 600 mA boost regulator with PFM or auto mode</li> <li>Six adjustable general purpose linear regulators</li> <li>Input voltage range: 2.8 V to 4.5 V OTP (One Time Programmable) memory for device configuration</li> </ul>

[1] Minimum start-up voltage is 3.1 V

KITVR5100FRDMEVM evaluation board

#### 5.4 Board description

Figure 1 describes the main elements on the KITVR5100FRDMEVM.



#### Table 2. Board description

Num ber	Name	Description
1	Coin cell battery	Backup power supply for VR5100 PMIC
2	Banana connector	Connection to power supply positive terminal
3	Banana connector	Connection to power supply negative terminal
4	FRDM-KL25Z	KL25Z board mounted via Arduino <sup>™</sup> connectors. Controls communication with PC
5	USB KL25Z	USB port for connection to PC
6	KITVR5100FRDMEVM	VR5100 PMIC evaluation board
7	MC34VR5100A1EP	VR5100 PMIC (Power Management IC)

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KITVR5100FRDMEVM evaluation board

### 5.5 Device description

The VR5100 device populated on KITVR5100FRDMEVM features the A1 OTP. See Figure 4.

#### Table 3. Startup configuration <sup>[1]</sup>

Register name	Address	Data	Value
OTP PU CONFIG 1	0xE0	0x01	PWRON = level sensitive   DVS clock speed = 12.5 mV/µs   sequencer clock = 2.0 ms
OTP PGOOD ENABLE	0xE8	0x00	Power good = disabled
OTP I2C ADDR	0xFF	0x08	I <sup>2</sup> C device address = 0x08
OTP SW1 VOLTS	0xA0	0x08	SW1 V <sub>OUT</sub> = 0.900 Volts
OTP SW1 SEQUENCE	0xA1	0x02	SW1 power up sequence = 4.0 ms
OTP SW1 CONFIG	0xA2	0x05	SW1 switching frequency = 2.0 MHz
OTP SW2 VOLTS	0xAC	0x06	SW2 V <sub>OUT</sub> = 3.200 Volts
OTP SW2 SEQUENCE	0xAD	0x01	SW2 power up sequence = 2.0 ms
OTP SW2 CONFIG	0xAE	0x01	SW2 switching frequency = 2.0 MHz
OTP SW3 VOLTS	0xB0	0x09	SW3 V <sub>OUT</sub> = 1.350 Volts
OTP SW3 SEQUENCE	0xB1	0x01	SW3 power up sequence = 2.0 ms
OTP SW3 CONFIG	0xB2	0x01	SW3 switching frequency = 2.0 MHz
OTP SWBST VOLTS	0xBC	0x00	SWBST V <sub>OUT</sub> = 5.000 Volts
OTP SWBST SEQUENCE	0xBD	0x00	SWBST power up sequence = OFF
OTP VSNVS VOLTS	0xC0	0x06	VSNVS V <sub>OUT</sub> = 3.000 Volts
OTP LDO1 VOLTS	0xC8	0x00	LDO1 V <sub>OUT</sub> = 1.800 Volts
OTP LDO1 SEQUENCE	0xC9	0x00	LDO1 power up sequence = OFF
OTP LDO2 VOLTS	0xCC	0x0F	LDO2 V <sub>OUT</sub> = 1.550 Volts
OTP LDO2 SEQUENCE	0xCD	0x01	LDO2 power up sequence = 2.0 ms
OTP VSD VOLTS	0xD0	0x03	VSD V <sub>OUT</sub> = 3.300 Volts
OTP VSD SEQUENCE	0xD1	0x01	VSD power up sequence = 2.0 ms
OTP V33 VOLTS	0xD4	0x03	V33 V <sub>OUT</sub> = 3.300 Volts
OTP V33 SEQUENCE	0xD5	0x01	V33 power up sequence = 2.0 ms
OTP LDO3 VOLTS	0xD8	0x0F	LDO3 V <sub>OUT</sub> = 3.300 Volts
OTP LDO3 SEQUENCE	0xD9	0x01	LDO3 power up sequence = 2.0 ms
OTP LDO4 VOLTS	0xDC	0x07	LDO4 V <sub>OUT</sub> = 2.500 Volts
OTP LDO4 SEQUENCE	0xDD	0x09	LDO4 power up sequence = 18.0 ms

[1] This table specifies the default output voltage of the LDOs and SWx after start-up and/ or when the LDOs and SWx are enabled. VREFDDR\_SEQ is internally fixed to be same as SW3\_SEQ. VCC\_SD voltage depends on the state of the SD\_VSEL pin.

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# **KTVR5100FRDMEVMUG**

KITVR5100FRDMEVM evaluation board

SEQ CLK	D	VS CL	к			PW	RON	CFG	PGC	OD		I2C ADDRESS			LINE	AR SUPPL	Y	VOUT	г		SEC	2
2.0 👻 ms	s 12	2.50	-	mV/u	s					1		0x08 👻			LDO1		1	1.800	•	۷	OFF	•
SWITC	HING	SUPPL	Y	VOU	т		SE	5	FS\	N		CONFIG	i		LDO2		1	1.550	•	۷	1	•
<b>SW1</b>				0.900	•	۷	2	•	2.0	•	MHz				LDO3			3.300	•	۷	1	•
<b>SW2</b>				1.800	•	۷	1	•	2.0	•	MHz	Range High:			LDO4		2	2.500	•	۷	9	•
<b>SW3</b>				1.350	•	V	1	•	2.0	•	MHz				VSD			3.300	•	۷	1	•
SWBST				5.000	•	V	OFF	•							V33			3.300	•	۷	1	•
									-						VSNVS			3.000	•	۷		
SW1		Q	5	Vout: ( SEQ D	0.90 elay	)0V r: 4.	Oms	DVS	Ramp	: 72	2.0us											
SW2	1	Vout SEQ	: 1.8 Dela	00V y: 2.0r	ns	DV	S Ran	p: 14	44.0u:	,												
	1	Vout SEQ	: 1.3 Dela	50V y: 2.0r	ns	DV	S Ram	p: 10	08.0u													
SWBST	=	OF	F																			
LDO1	=	OF	F																			
LDO2	1	Vout SEQ	: 1.5 Dela	50V y: 2.0r	ns																	
	9	Vout SEQ	: 3.3 Dela	00V y: 2.0r	ns																	
LDO4													9 <mark>v</mark>	ut: 2.5 Q Dela	00V y: 18.0ms							
VSD	ø	Vout SEQ	: 3.3 Dela	00V y: 2.0r	ns																	
	1	Vout SEQ	: 3.3 Dela	00V y: 2.0r	ns																	
	2.0	4.	0	6.0		8	.0	10	.0	12.	.0	1 <b>4.0 16.0</b> TIME (ms)	18.0	20.0	22.0	24.0	26.0	21	B.O		30.0	
Figure 2. VR	R510	0 GU	JI O	тр с	on	fig	urati	on	pane	el s	how	ing onboard	I VR510	0 star	tup co	nfigurati	ion da	ata				

KITVR5100FRDMEVM evaluation board

#### 5.6 LED display

The board contains the following LED:



#### Figure 3. LED locations

#### Table 4. LED locations

LED ID	Description
D1	LED Green, V33 regulator output from VR5100 PMIC. Displays when the board is connected to a PC through the FRDM-KL25Z's USB port.

KITVR5100FRDMEVM evaluation board

#### 5.7 Jumper and switch definitions

Figure 4 shows the location of jumpers and switches on the KITVR5100FRDMEVM evaluation board.



<u>Table 5</u> describes the function and settings for each jumper and switch. Default jumper settings are shown in bold text.

Table 5. Jumper and	d switch definitions
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Jumper/Switch	Description	Setting	Connection/Result
SW1	Reset	Open	Connects EN pin to GND when pressed. Resets the PMIC device.
J1	ELOAD B Drive	Open	ELOAD B has no drive (use for troubleshooting ELOAD only).
		[1-2]	ELOAD B drive is connected. ELOAD functions properly.
J8	VDDOTP Select	[1-2]	Connects VDDOTP pin to VDIG. PMIC in TBB mode. <sup>[1]</sup>
		[2-3]	Connects VDDOTP pin to GND. PMIC in Normal Operation (RUN mode).

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# **KTVR5100FRDMEVMUG**

#### KITVR5100FRDMEVM evaluation board

Jumper/Switch	Description	Setting	Connection/Result
J9	ELOAD A Drive	Open	ELOAD A has no drive. (Use for troubleshooting ELOAD only)
		[1-2]	ELOAD A drive is connected. ELOAD functions properly.
J10	VIN Pin	Open	No connection to VIN pin. PMIC VIN is isolated
		[1-2]	VIN pin is connected to VIN bus. PMIC VIN is powered from banana plug J5.
J11	SWBST Out	Open	SWBST output is not connected to Active Metering electronics.
		[1-2]	SWBST output can be measured with Active Metering electronics.
J12	EN Select	Open	EN pin is controlled by the state of SW1. PMIC in Normal Operation.
		[1-2]	Connects EN pin to GND. PMIC held in Reset.
J13	VDBG Enable	Open	On board 3.3V LDO (U1) is disabled. VDBG = 0 V
		[1-2]	On board 3.3V LDO (U1) is enabled. VDBG = 3.3 V.
J14	STANDBY Select	[1-2]	Connects STBY pin to GND. STANDBY is LOW (Not Enabled) <sup>[2]</sup>
		[2-3]	STBY pin is pulled up to V_PU. STANDBY is HIGH (Enabled).
J15	SD Select	[1-2]	Connects SD pin to GND. SD_VSEL is LOW (VSD = 3.3 V) . <sup>[3]</sup>
		[2-3]	SD pin is pulled up to V_PU. SD_VSEL is HIGH (VSD = 1.8 V)
J16	V_PU Select	[1-2]	V_PU is connected to VSNVS.
		[2-3]	V_PU is connected to VCCI2C.
J17	VCCI2C Select	[1-2]	VCCI2C is connected to SW2 Vout.
		[2-3]	VCCI2C is connected to VDBG (3.3V LDO).
J18	Coin Cell	Open	Coin Cell is isolated.

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Jumper/Switch	Description	Setting	Connection/Result
		[1-2]	Coin Cell is connected to LICELL pin.
J19	VLDOIN1 Select	Open	VLDOIN1 disconnected from VIN bus. LDO1 has no input source.
		[1-2]	VLDOIN1 connected to VIN bus. LDO1 is supplied from VIN.
J20	MUX_IN Select	Open	Active Metering analog mux devices are unpowered. Active Metering OFF.
		[1-2]	Active Metering analog mux devices powered from VDBG. Active Metering ON.
J21	VLDOIN34 Select	Open	VLDOIN34 disconnected from VIN bus. LDO3 and LDO4 have no input source.
		[1-2]	VLDOIN34 connected to VIN bus. LDO3 and LDO4 are supplied from VIN.
J22	VLDOIN2 Select	Open	VLDOIN2 disconnected from VIN bus. LDO2 has no input source.
		[1-2]	VLDOIN2 connected to VIN bus. LDO2 is supplied from VIN.

TBB Mode or "Try-Before-Burn" Mode is a special development mode that allows potential OTP configuration data to be previewed and tested before committing to permanently burning the OTP fuses. With this setting, STANDBY can be enabled/disabled within the GUI. With this setting, SD\_SEL can be set high/low within the GUI. [1]

[2] [3]

#### 5.8 Test point definitions

The following test points provide access to various signals to and from the board.

#### **NXP Semiconductors**

# **KTVR5100FRDMEVMUG**

#### KITVR5100FRDMEVM evaluation board



#### Figure 5. Test point locations

#### Table 6. Test point definitions

Test point name	Signal name	Description
TP1	PMIC_SCL	VR5100 PMIC I <sup>2</sup> C clock signal via Arduino J3 (to KL25Z PTE1)
TP2	PMIC_SDA	VR5100 PMIC I <sup>2</sup> C data line via Arduino J3 (to KL25Z PTE0)
TP3	MUX_SDA	Multiplex I <sup>2</sup> C data line via Arduino J2 (to KL25Z PTC9)
TP4	MUX_SCL	Multiplex I <sup>2</sup> C clock signal via Arduino J2 (to KL25Z PTC8)
TP5	NA	Ground loop
TP6	ELOAD_B	Si4156DY MOSFET (Q51) electronic load signal
TP7	SWBSTOUT	Output from SWBST boost regulator
TP8	VDIG	VR5100 PMIC VDIG (internal core supply) pin signal
TP9	nLDAC	MCP4728 DAC LDAC pin signal
TP10	RDY/BSY	MCP4728 DAC RDY/BSY pin signal
TP11	ELOAD_DAC_B	MCP4728 DAC VOUTB pin signal. When jumper J1 is set, positive input to MCP6V07 operational amplifier (U50A)
TP12	ELOAD_DAC_A	MCP4728 DAC VOUTA pin signal. When jumper J9 is set, positive input to MCP6V07 operational amplifier (U54A)
TP13	GND	Ground
TP14	PMIC_EN	VR5100 PMIC EN pin signal

#### KITVR5100FRDMEVM evaluation board

Test point name	Signal name	Description
TP15	NA	Ground loop
TP16	VIN_pin	VR5100 PMIC VIN pin signal
TP17	PMIC_INTB	VR5100 PMIC INTB pin signal
TP18	VSD	ADG715 (U55) SPST switch VSD pin signal
TP19	VCCI2C	VR5100 PMIC VCCI2C pin signal
TP20	VBG	VR5100 PMIC VBG pin signal
TP21	VCC	VR5100 PMIC VBG pin signal
TP22	VSNVS	ADG715 (U55) SPST switch VSNVS pin signal
TP23	SD_VSEL	VR5100 PMIC SD_VSEL pin signal
TP24	PMIC_Standby	VR5100 PMIC STBY pin signal
TP25	RESETBMCU	VR5100 PMIC PORB pin signal
TP26	SW1OUT	ADG715 (U56) SPST switch SW1OUT pin signal
TP27	GND	Ground loop
TP28	V33	ADG715 (U55) SPST switch V33 pin signal
TP29	SW3OUT	ADG715 (U56) SPST switch SW3OUT pin signal
TP30	ELOAD_B	Si4156DY MOSFET (Q50) electronic load signal
TP31	REFOUT	ADG715 (U55) SPST switch REFOUT pin signal
TP32	GND	Ground loop
TP33	VLDO2	ADG715 (U56) SPST switch VLDO2 pin signal
TP34	VLDO1	ADG715 (U56) SPST switch VLDO2 pin signal
TP35	GND	Ground
TP36	SW2OUT	ADG715 (U56) SPST switch SW2OUT pin signal
TP37	VLDO3	ADG715 (U56) SPST switch VLDO3 pin signal
TP38	VLDO4	ADG715 (U56) SPST switch VLDO4 pin signal
TP39	GND	Ground

#### 5.9 Banana connectors

The board has the following power supply banana connectors.

KTVR5100FRDMEVMUG

KITVR5100FRDMEVM evaluation board



#### Figure 6. Screw terminal locations

#### Table 7. Banana connectors

Banana connector name	Description
J4	Board ground
J5	2.8 V to 4.5 V supply input. Use only when SW1 is in position 2 (VIN path). <sup>[1]</sup>

[1] Minimum startup voltage is 3.1 V

#### 5.10 Coin cell battery

The KITVR5100FRDMEVM contains an on-board coin cell battery that supports the coin cell features of the VR5100 PMIC. The function of the coin cell is to retain data in the OTP registers when power is recycled during a TBB (Try Before Buy) session. The battery also becomes the power source for the device when the VSNVS pin on the VR5100 PMIC is connected directly to the VIN pin. See the VR5100 data sheet for additional information on the VR5100 PMIC's coin cell features.

The VR5100 PMIC contains on-chip circuitry to initiate recharging of the coin cell battery. This capability can be activated through the **Miscellaneous** panel of the VR5100 GUI.

To replace the coin cell battery, carefully lift the spring clip holding the coin cell in place. Slide out the old coin cell and slide in the new.

KITVR5100FRDMEVM evaluation board



Figure 7. Coin cell battery

#### Table 8. Coin cell battery

LED ID	Description
BAT1	MS621 surface mount rechargeable backup battery. 3.0 V 5.5 mA lithium coin cell.

KITVR5100FRDMEVM evaluation board

### 6 FRDM-KL25Z Freedom SPI dongle

The NXP Freedom development platform is a set of software and hardware tools supporting evaluation and development. It is ideal for rapid prototyping of microcontrollerbased applications. The NXP Freedom KL25Z hardware, FRDM-KL25Z, is a simple, yet sophisticated design featuring a Kinetis L series microcontroller, the industry's first microcontroller built on the ARM<sup>®</sup> Cortex<sup>™</sup>-M0+ core.



#### 6.1 Connecting the FRDM-KL25Z to the board

The FRDM-KL25Z evaluation board was chosen specifically to work with the KITVR5100FRDMEVM kit because of its low cost and features. The FRDM-KL25Z board makes use of the USB, built in LEDs and I/O ports available with NXP's Kinetis KL2x family of microcontrollers.

The KITVR5100FRDMEVM connects to the FRDM-KL25Z using the four dual row Arduino<sup>™</sup> R3 connectors on the bottom of the board. <u>Table 9</u> shows the signal connections between the FRDM-KL25Z and the KITVR5100FRDMEVM board.

KTVR5100FRDMEVMUG

#### KITVR5100FRDMEVM evaluation board

KITVR5100	FRDMEVM	FRDM-	KL25Z	Pin hardwa	ire name	
Header	Pin	Header	Pin	KITVR5100 FRDMEVM	FRDM-KL25Z	Description
J2	1	J1	1	Open	PTC7	Open
J2	2	J1	2	PMIC_INTB	PTA1	Interrupt signal from VR5100 PMIC
J2	3	J1	3	Open	PTC0	Open
J2	4	J1	4	N/C	PTA2	No connection
J2	5	J1	5	Open	PTC3	Open
J2	6	J1	6	RDY/BSY	PTD4	MCP4728 DAC RDY/ BSY pin signal
J2	7	J1	7	Open	PTC4	Open
J2	8	J1	8	nLDAC	PTA12	MCP4728 DAC LDAC pin signal
J2	9	J1	9	Open	PTC5	Open
J2	10	J1	10	N/C	PTA4	No connection
J2	11	J1	11	Open	PTC6	Open
J2	12	J1	12	N/C	PTA5	No connection
J2	13	J1	13	Open	PTC10	Open
J2	14	J1	14	MUX_SCL	PTC8	Multiplex I <sup>2</sup> C clock
J2	15	J1	15	Open	PTC11	Open
J2	16	J1	16	MUX_SDA	PTC9	Multiplex I <sup>2</sup> C data line
J3	1	J2	1	Open	PTC12	Open
J3	2	J2	2	PMIC_EN	PTA13	Power ON/OFF input to VR5100 PMIC
J3	3	J2	3	Open	PTC13	Open
J3	4	J2	4	PMIC_STANDBY	PTD5	VR5100 PMIC STBY pin signal
J3	5	J2	5	Open	PTC16	Open
J3	6	J2	6	SD_VSEL	PTD0	VR5100 PMIC SD regulator voltage selection
J3	7	J2	7	Open	PTC17	Open
J3	8	J2	8	MUX_RESETB	PTD2	NA
J3	9	J2	9	Open	PTA16	Open
J3	10	J2	10	RESETBMCU	PTD3	VR5100 PMIC PORB pin signal
J3	11	J2	11	Open	PTA17	Open
J3	12	J2	12	N/C	PTD1	No connection
J3	13	J2	13	Open	PTE31	Open
J3	14	J2	14	GND	GND	Ground
J3	15	J2	15	Open	N/C	Open
J3	16	J2	16	N/C	VREFH	No connection
J3	17	J2	17	Open	PTD6	Open
J3	18	J2	18	PMIC_SDA	PTE0	VR5100 PMIC I <sup>2</sup> C data line
J3	19	J2	19	Open	PTD7	Open
J3	20	J2	20	PMIC_SCL	PTE1	VR5100 PMIC I <sup>2</sup> C clock line
J6	1	J10	1	Open	PTE20	Open

#### Table 9. KITVR5100FRDMEVM to FRDM-KL25Z connections

#### KITVR5100FRDMEVM evaluation board

KITVR5100	FRDMEVM	FRDM-I	KL25Z	Pin hardwa	re name	
Header	Pin	Header	Pin	KITVR5100 FRDMEVM	FRDM-KL25Z	Description
J6	2	J10	2	N/C	PTB0	Not connected
J6	3	J10	3	Open	PTE21	Open
J6	4	J10	4	N/C	PTB1	No connection
J6	5	J10	5	Open	PTE22	Open
J6	6	J10	6	VOUT_SNS	PTB2	NA
J6	7	J10	7	Open	PTE23	Open
J6	8	J10	8	ADC_1	PTB3	NA
J6	9	J10	9	Open	PTE29	Open
J6	10	J10	10	ADC_0	PTC2	No connection
J6	11	J10	11	Open	PTE30	Open
J6	12	J10	12	N/C	PTC1	No connection
J7	1	J9	1	Open	PTB8	Open
J7	2	J9	2	N/C	SDA_PTD5	No connection
J7	3	J9	3	Open	PTB9	Open
J7	4	J9	4	3V3_FRDM	P3V3	NA
J7	5	J9	5	Open	PTB10	Open
J7	6	J9	6	N/C	RESET/PTA20	No connection
J7	7	J9	7	Open	PTB11	Open
J7	8	J9	8	N/C	P3V3	No connection
J7	9	J9	9	Open	PTE2	Open
J7	10	J9	10	N/C	P5V_USB	No connection
J7	11	J9	11	Open	PTE3	Open
J7	12	J9	12	GND	GND	Ground
J7	13	J9	13	Open	PTE4	Open
J7	14	J9	14	GND	GND	Ground
J7	15	J9	15	Open	PTE5	Open
J7	16	J9	16	NC	P5-9V_VIN	No connection

KITVR5100FRDMEVM evaluation board

### 7 Installing the software and setting up the hardware

#### 7.1 Installing VR5100GUI on your computer

- 1. Download VR5100GUI.zip from http://www.nxp.com/KITVR5100FRDMEVM.
- 2. Extract all the files to C:/NXP/VR5100GUI or any other desired folder on your PC.
- 3. Run setup.exe and click **Install** in the dialog box.

Application Install - Security Warning	×
Publisher cannot be verified. Are you sure you want to install this application?	<b>§</b>
Name: VR5100_HID_GUI From (Hover over the string below to see the full domain): C:\Users\B37063\Documents\Data\VR5100_HID_GUI\VR5100_HID_GUI\Publish Publisher: Unknown Publisher	
Install	Don't Install
While applications can be useful, they can potentially harm your computer. If you source, do not install this software. <u>More Information</u>	do not trust the

4. The GUI installation is complete and Installation Confirmation window appears. Do not click on anything until the board is plugged in.

NP VR5100 GUI (Version 1.1)		
LISB Connection	Switching Supplies Linear Supplies Miscellane	eous Interrupts OTP Configuration Script Editor Functional Registers OTP Registers
Vendor ID: 0x15A2 Target:	SW1 FUNCTIONAL	SW2 FUNCTIONAL Vin
Part ID: 0x00A1 Device:	Vout: < ▶ 0.700 V	Vout: < > 1.500 V O
Click to Enable Target: Scan For Devices	Vstby: < > 0.700 V	Vstbv:
FRDM+VR5100 Found	Voff: < ▶ 0.700 V	
Scan for I2C Address?	Mode: < > OFFIOFF	Mode:
	Normal: OFF Standby: OFF	Normal: OFF Standby: OFF PHASE: 0* ON: OFF
	OMODE Enabled:	OMODE Enabled:
	DVS: ∢ ► 12.50 mV/µs	DVS: ∢ → 12.50 mV/µs
	Phase: < > 0 °	Phase:
	Fsw: < 1.0 MHz	Fsw: < + 1.0 MHz
	Pseg: < ▶ 40 %	Pseg: ∢ ▶ 38 % V0UT: 1.500V
	Current Limit = 2.0x	Current Limit = 2.0x DVS: 12.50mV/µs PHASE:0° OM: 0FF
		FSW: 1.0MHz IL: 2.0x
	SW3 FUNCTIONAL	SWBST FUNCTIONAL
	Vout: < ▶ 0.900 V	Vout:
	Vstby: < ▶ 0.900 V	NMode: < > OFF SW3
	Voff: ∢ ► 0.900 V	SMode: ( ) OFF VOUT: 0.900V
	Mode:   OFF OFF	MODE: OFF [OFF DVS: 12.50mV/ps DNASE. 00.005
	Normal: OFF Standby: OFF	FSW: 1.0MHz IL: 2.0x
	OMODE Enabled:	
Save Log Clear Log I2C Address: 0x08 -	DVS: < 12.50 mV/jus	
Direct 120 Communication	Phase: < > 0 °	
- 12C Byte Read Page - 12C Byte Write	Fsw: < 🕨 1.0 MHz	LX
Register: 0x00 @ P0 Register: 0x00	Pseg: < ▶ 40 %	SWBST
Data: 0x00 O P1 Data: 0x00	Current Limit = 2.0x	PD
		VOUT: 5.000V
Byte Read Byte Write		AMODE: OFF
Build: (Not Published) Quit	L	

KITVR5100FRDMEVM evaluation board

# 7.2 Configuring the hardware and using the GUI for control and monitoring

- 1. Apply input voltage to the board: use a 4.2 V supply connected to J5 (+) and J4 (-).
- 2. Plug the mini-USB side of the mini-USB to USB cable into the KL25Z USB port on the FRDM-KL25Z board and the other end to an available USB port on the PC.



- 3. Windows automatically installs the necessary drivers. Wait for this to complete.
- 4. Launch the VR5100 GUI.
- 5. In the VR5100 GUI window, click **Scan For Devices** button in the top-left portion. A confirmation message that a valid device is available is logged.

KITVR5100FRDMEVM evaluation board

USB Connect	tion			
Vendor ID:	0x15A2	Target:	VR.	5100 EVK
Part ID:	0x00A1	Device:	MC3	4VR5100
Target Enab	led:		Scan Fo	r Devices
FRDM+VR51	100 Four	nd Areas?		
VR5100 EV	VK Enabl	Led		
Save Log	Cle	ear Log	I2C Address:	0x08 👻

- 6. Enable the communication by clicking the **Target Enabled:** check box. The window turns from grey to color. The green LED on the FRDM-KL25Z also turns on.
- 7. The GUI installation and hardware setup is now complete.

# 7.3 Configuring the KITVR5100FRDMEVM and the KITVR5100FRDMPGM in Combo mode

The KITVR5100FRDMEVM and the KITVR5100FRDMPGM can be connected to function as a unit in Combo mode. In Combo mode, the functionality of both the evaluation board and the programming board can be utilized through the VR5100 GUI.

To configure the boards in Combo mode:

- Disconnect any power being supplied to the KITVR5100FRDMEVM board connectors. Also disconnect any USB cables connecting either of the FRDM-KL25Z boards to a PC.
- Carefully detach the KITVR5100FRDMPGM programming board from the Arduino<sup>™</sup> connectors on the FRDM-KL25Z board.

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KITVR5100FRDMEVM evaluation board

- 3. Pull the Arduino connectors off the programming board's FRDM-KL25Z board and attach them to the top of the evaluation board's FRDM-KL25Z.
- 4. Mount the KITVR5100FRDMPGM programming board to the evaluation board's FRDM-KL25Z. Note that the evaluation board FRDM-KL25Z must be used because it contains the microcode to recognize and support Combo mode. Make sure that the programming board is firmly attached to the FRDM-KL25.
- 5. Connect the power supply to the KITVR5100FRDMEVM evaluation board. Then connect a USB cable from the USB KL25Z port on the FRDM-KL25Z to a USB port on the PC with the GUI installed. Green LEDS should light up on both the evaluation board and on the programming board.
- 6. Activate the GUI and click in the **Target Enabled** check box in the upper left corner of the panel. The log section displays the message **VR5100 COMBO Enabled**.



#### Figure 9. VR5100 GUI log with Combo mode target enabled

If the log section displays the message **VR5100EVK Enabled**, the programming board is not firmly connected to the FRDM-KL25Z. This may be the case even when the green LEDs are lit on both boards.

#### 7.4 Using on-board ELOADs

Two on-board electronic loads (ELOADs) provide adjustable load currents from 0 to 1000 mA in 50 mA steps. The ELOADs are useful for testing supply performance or evaluating a particular PMIC supply rail at a specified load current.

To use the ELOADS, connect a suitable jumper wire (short length with proper gauge) between ELOAD A or ELOAD B and the desired supply VOUT.

Note that up to 2000 mA of load current can be achieved by using ELOAD A and ELOAD B connected in parallel. Each ELOAD's current must be set separately in the VR5100 GUI **Miscellaneous** panel. Be aware that continuous operation under full load current heats up the EVB.

Set each ELOAD back to 0 mA when finished.

KTVR5100FRDMEVMUG

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KITVR5100FRDMEVM evaluation board

Below is an example of a script that demonstrates the use of the ELOAD to test the LDO1 current limit of 150 mA. The KITVR5100FRDMEVM jump start package also contains this script.

#### 7.5 Measuring switching supply efficiency

Switching supply conversion efficiency is an important system performance parameter effecting the overall runtime of battery powered equipment. Efficiency is calculated as follows:

$$Efficiency = \eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

The diagram below illustrates how to make an efficiency measurement for the SW1 supply.

#### KITVR5100FRDMEVM evaluation board



The V<sub>OUT</sub> test points for most of the VR5100 PMIC supplies are placed for user convenience near the edges of the VR5100 EVB. The voltages measured at these test points, for light-load conditions, are extremely accurate. When making efficiency calculations for full-load currents, the Vout measurement should be taken at the switching supply feedback node. This is the 'regulation point' for the supply.

Under full-load conditions, there can be a significant voltage drop between the supply regulation point, and the output test point terminal. Each switching supply has a zero-ohm resistor in the feedback loop, and is a good place to measure the  $V_{OUT}$  voltage for the supply.

The figure below shows where to measure the  $V_{\text{OUT}}$  for each switching supply when calculating their efficiencies.

KITVR5100FRDMEVM evaluation board



KITVR5100FRDMEVM evaluation board

#### 7.6 Understanding and using the GUI

#### 7.6.1 GUI structure for VR5100

Figure 12 shows the different components of the GUI.

To enable the volt meters on the board, click **Read Meters** button located in the bottom left of the window. The output of the meters is displayed in the right side of the window. Clicking the **Enable Live Meters** button enables continuous polling of the meters.



#### 7.6.2 GUI panels

When the GUI is launched, it looks for a VR5100 target board connected via the USB cable. If connected, the USB Connection panel displays the Vendor ID: 0x15A2, and Part ID: 0x00A1.

The Main Log window displays messages **FRDM+VR5100 Found**, and **Scan for I2C Address**.

KITVR5100FRDMEVM evaluation board



Pressing the **Scan For Devices** button attempts to read from each of the eight permissible I2C device addresses, and displays the results in the Main Log window. If multiple PMIC devices are detected, the GUI can be configured to communicate with a particular device by selecting the corresponding device address in the I2C Address list.

Note: The GUI can communicate with only one PMIC device at a time.

KITVR5100FRDMEVM evaluation board



Figure 14. GUI connected to target board

#### 7.6.2.1 Switching Supplies panel

The Switching Supplies panel allows users to adjust the functional parameters of each supply.

KITVR5100FRDMEVM evaluation board



To change supply parameters, click and adjust the desired control. An **UPDATE** button appears whenever a change is made, and pressing the **UPDATE** button writes the change to the PMIC.

**Note:** Multiple changes can be made at a time, and all changes are written when the **UPDATE** button is pressed.

When the **Read Meters** button is pressed, or if the **Enable Live Meters** checkbox is selected, real-time output voltage measurements are displayed to the right of each supply block diagram.

#### 7.6.2.2 Linear Supplies panel

The Linear Supplies panel allows users to adjust the functional parameters of each supply. To change supply parameters, click and adjust the desired control.

KITVR5100FRDMEVM evaluation board



#### Figure 16. Linear Supplies panel

An **UPDATE** button appears whenever a change is made, and pressing the **UPDATE** button writes the change to the PMIC. Note that multiple changes can be made at a time, and all changes are written when the **UPDATE** button is pressed.

When the **Read Meters** button is pressed, or if the **Enable Live Meters** checkbox is selected, real-time output voltage measurements are displayed to the right of each supply block diagram.

#### 7.6.2.3 Miscellaneous panel

The Miscellaneous panel contains an assortment of general purpose commands.

KTVR5100FRDMEVMUG

KITVR5100FRDMEVM evaluation board

Switching Supplies Linear Supplies	Miscellaneous	Interrupts OTP Configuration	Script Editor Fu	nctional Registers	OTP Registers		
DEVICE INFORMAT	TON				HARI	DWARE CON	TROL
Device ID: 0x30					Toggle PWRON	1.0	
Full Layer Revision: 0x01					ssert PWPONI OW		
Metal Layer 0x01					ssert SD. Select Pin		
FAB: 0x00							
FIN: 0x00					ELOAD_A		ELOAD_B
POWER CONTRO	)L	-		IS	ET: 0 -	mA ISET	:0 <b>-</b> mA
LDO Short Circuit Protection Each					_		_
Standby Active Low							
Statudy Acuve Low:							
Auto-Destart After Deset Enables							
Auto Restairt Arter Reset Eridole.	102.05.05						
Standby Delay:	γ 122.06 μs						
PWRON Debounce:	r 0.0 ms						
COIN CELL CHARG	ER						
Charger Enable:	<b></b>						
Charge Voltage:	2.500 V						
FREE RAM							
MEMA: W 0x00	R 0x00						
MEMC: W 0x00	R 0x00						
MEMD: W 0x00	<b>R</b> 0x00						
Figure 17. Miscellaneou	us panel						

#### 7.6.2.4 Interrupts panel

The Interrupts panel displays the state of all the VR5100 interrupts.

#### KITVR5100FRDMEVM evaluation board



Pressing the **Read Interrupts** button reads and displays Status, Mask, and Sense registers for INT0, INT1, INT3, and INT4. Selecting the Poll Interrupts checkbox enables periodic update of this information.

The state of the VR5100 INTB pin is displayed, and updated asynchronously. Interrupts that are unmasked, causes the INTB pin go LOW while the interrupt condition exists. The VR5100 target hardware detects when the INTB pin goes LOW, and sends a message to the GUI to indicate that an interrupt has occurred. The INTB label on the panel flashes until the interrupt condition is cleared.

Figure 19 shows an example of a SW1 overcurrent fault condition.

KTVR5100FRDMEVMUG

KITVR5100FRDMEVM evaluation board



MASK - Controls the assertion of the INTB pin. When Unchecked, INTB will be asserted by interrupt. SENSE - Is the real-time state of the interrupt. READ ONLY

SW1 Overcurrent Fault

Main Log Display

#### Figure 19. SW1 overcurrent fault condition

Figure 20 shows an example of an LDO1 overcurrent fault condition.

NTB State:	LOW	INTB		
	INTERRUPT 0		INTERRUPT 1	
STATUS	MASK	SENSE	STATUS MASK SENSE	*** INTB ASSERTED LOW ***
Power On		•	SW1 Over-current	<ul> <li>LDO1 FAULT</li> </ul>
Low Voltage			SW2 Over-current	
110°C Therma	al 🔽 le		SW3 Over-current 🔽	
120°C Therma	al 🔽 le		🔲 Clear Ali 🔽 Ali	
125°C Therma	al 🔽 le			
130°C Therma	al 🔽 le			
Clear All	🔽 All			
	INTERRUPT 3		INTERRUPT 4	
STATUS	MASK	SENSE	STATUS MASK SENSE	
SWBST Over-	current 🔽		✓ LDO1 Over-current	
OTP AutoBlow	Done 🔽		LDO2 Over-current	
OTP ECC Erro	r 🔍		VSD Over-current	
🔲 Clear All	V Al		V33 Over-current	
			LDO3 Over-current	
			🖸 LDO4 Over-current 🔄	
			🗖 Clear Ali 📃 Ali	
TATUS - Report ASK - Controls t ENSE - Is the re	ts the latched state the assertion of t ral-time state of t	ate of the interrup he INTB pin. Wh the interrupt. REA	ot. Uncheck to CLEAR interrupt. en Unchecked, INTB will be asserted by interrupt. D ONLY	L
	I	DO1 Over	current Fault	Main Log Display
igure 20. L	DO1 overc	urrent fault	condition	
	0		All information provided in this document is subject to le	anal disclaimers @ NXP R V 2

KITVR5100FRDMEVM evaluation board

#### 7.6.2.5 OTP Configuration panel

The OTP Configuration panel allows access and editing of the VR5100 startup parameters.



#### Figure 21. OTP Configuration panel

Initially, the panel display is greyed out. To populate the panel, press **Edit Configuration**, and select a data source to read from.

#### KITVR5100FRDMEVM evaluation board

Switching Supplies Linear Supplies Miscellaneous Int	terrupts OTP Configuration Script Editor Functional Registers OTP	Registers
SEQ CLK DVS CLK PWRON CFG	PGOOD I2C ADDRESS LINEAR SUPPLY	VOUT SEQ Return to Run Mode
0.5 🗣 ms 12.50 🗣 mV/us 🕅	□ 0x08   LDO1	1.800 V OFF V
SWITCHING SUPPLY VOUT SEQ	FSW CONFIG	0.800 V OFF V Input Data
SW1 0.700 V OFF V	1.0 V MHz DO3	1.800
SW2 1.500 V OFF V	1.0 V MHz Range High:	1.800
SW3 0.900 V OFF V	1.0 VSD	2.850 V OFF V
SWBST 5.000 V OFF V	V33	2.850 V OFF V Update From Target
	VSNVS	1.000 V Output Data
		Save CEG Ele
SWI - OFF		
SW2 = OFF		Save HEX File
		Generate Report
SW3 = OFF		<u>Compare Data</u>
SWBST = OFF		Compare to CFG
		Compare HEX File
LDO1 = OFF		
LDO3 = OFF		
LDO4 = OFF		Restart PMIC
V33 = OPF		
0.5 1.0 1.5 2.0 2.5	3,0 3,5 4,0 4,5 5,0 5,5 6,0 6,5	7.0 7.5 <b>TBB</b>
	TIME (ms)	

#### Figure 22. OTP Configuration Panel (TBB Mode on evaluation board)

The **Load CFG File** button opens the Configuration File Open dialog, and populates the panel with the parameters contained in this file.

The **Load HEX File** button opens the Hex File Open dialog, and populates the panel with the parameters contained in this file. Hex file format is an OTP data storage format used by most distributor programming services.

KITVR5100FRDMEVM evaluation board

Switching Supplies Linear Su	upplies Miscellaneous	Interrupts OTP Configuration Script	Editor Functional Registers OT	P Registers	
SEQ CLK DVS CLK	PWRON CF	G PGOOD I2C ADDRESS	LINEAR SUPPLY	VOUT SEQ	Return to Run Mode
0.5 🕶 ms 12.50	▼ mV/us	0x08 🗸	LDO1	1.800 ¥ V OFF ¥	
SWITCHING SUPPLY	VOUT SEQ	FSW CONFIG	LDO2	0.800 V OFF V	<u>Input Data</u>
<b>SW1</b>	0.700 V OFF	✓ 1.0 ✓ MHz	LDO3	1.800 ¥ V OFF ¥	Load CFG File
SW2	1.500 V OFF	✓ 1.0 ✓ MHz Range High:	E LD04	1.800 ¥ V OFF ¥	Load HEX File
SW3	0.900 - V OFF		VSD	2.850 ¥ V OFF ¥	[underson Transfer
SWBST	5.000 V OFF	•	V33	2.850 ¥ V OFF ¥	Update From Target
			VSNVS	1.000 V	<u>Output Data</u>
SW1 = OFF					Save CFG File
SW2 = OFF					Save HEX File
					Generate Report
5W3 = UN					Compare Data
SWBST = OFF					Compare to CFG
LDO1 = OFF					Compare HEX File
					PROGRAM
LDO3 = OFF					
LDO4 = OFF					Restart PMIC
VSD = OFF	=				
V33 = 00					
0.5 1.0	1.5 2.0	2.5 3.0 3.5 4.0 4.5	5.0 5.5 6.0 6.	5 7.0 7.5	IBB
		TIME (ms)			

Figure 23. OTP Configuration panel (TBB Mode on socket or combo board)

If the target connected is a VR5100 socket board, or a VR5100 evaluation board with the VR5100 socket board mounted atop (COMBO), the GUI displays the **PROGRAM** button, and device programming is permitted.

KITVR5100FRDMEVM evaluation board

Switching Supplies Linear Supplies Miscellaneous Interrupts	OTP Configuration Script Editor Functional Registers OT	P Registers
SEQ CLK DVS CLK PWRON CFG PGOOD	I2C ADDRESS LINEAR SUPPLY	VOUT SEQ Return to Run Mode
2.0 🕶 ms 12.50 🖝 mV/us 📃	0x08 - LDO1	1.800 V OFF V
SWITCHING SUPPLY VOUT SEQ FSW	CONFIG IV LDO2	1.550 V 1 V IIV
■ 🕼 SW1 0.900 🗸 V 2 👻 2.0 👻	MHz DO3	3.300  v V 1  v Load CFG File
■ 🕼 SW2 1.800 🗸 V 1 🚽 2.0 🚽	MHz Range High:	2.500 ▼ V 9 ▼
■ 👽 SW3 1.350 👻 V 1 👻 2.0 👻	MHz VSD	3.300 ▼ V 1 ▼
SWBST 5.000 V OFF V	V33	3.300 ▼ V 1 ▼ Update From Target
	VSNVS	3.000 V Output Data
SW1 2 Vout: 0.900V DVS Ramp: 7 SEQ Delay: 4.0ms	2.0us	Save CFG File
SW2 1 Vout: 1.800V DVS Ramp: 144.0us SEO Delay: 2.0ms		Save HEX File
SW3 1 Vout: 1.350V DVS Ramp: 108.0us		Generate Report
SEQ Delay: 2.0ms		<u>Compare Data</u>
SWBST = OFF		Compare to CFG
LDO1 = OFF		Compare HEX File
LDO2 1 Yout: 1.550V SEQ Delay: 2.0ms		
LDO3 1 Vout: 3.300V SEQ Delay: 2.0ms		
LD04	9 Vout: 2.500V SEQ Delay: 18.0ms	Restart PMIC
VSD 1 Vout: 3.300V SEQ Delay: 2.0ms		
VAN 1 Vout: 3.300V SEQ Delay: 2.0ms		
2.0 4.0 6.0 8.0 10.0 12	.0 14.0 15.0 18.0 20.0 22.0 24.0 26 TIME (ms)	.0 28.0 30.0 <b>TBB</b>

Figure 24. OTP Configuration panel (OTP data loaded from target EVB)

The **Update From Target** button loads the OTP configuration data from the target evaluation board.

KITVR5100FRDMEVM evaluation board

#### 7.6.2.6 Script Editor panel

The script editor allows the user to write and execute scripts that exercise various functions on the VR5100 PMIC, including setting voltages on the regulators, assigning values to free RAM, reading and writing I<sup>2</sup>C addresses, and clearing interrupts. Script commands can be written directly in an editor window. Alternatively, the user can activate a scratch pad window and build the scripts by selecting commands from drop-down menus and entering the appropriate values. When the target is a KITVR5100FRDMPGM board or a KITVR5100FRDMEVM board mounted to a socket board (Combo mode), the Script Editor can also be used to initiate the programming of a device in the socket. See the *KITVR5100FRDMPGM programming socket board* user guide for details on OTP programming.

The scripts are executed within the **Files:** section of the panel and the results are displayed in the **Script Log** section.

Completed scripts can be saved as text files for later use.

The KITVR5100FRDMPGM board jump start package contains a number of example scripts. Go the tool summary page at <u>http://www.nxp.com/KITVR5100FRDPGM</u> to view and download the example scripts.



Figure 25 shows the main elements in the Script Editor panel.

1. The Files: section allows scripts to be loaded, edited and executed.

#### KITVR5100FRDMEVM evaluation board

- 2. The Script Log displays the results of an executed script.
- 3. Load Script loads a previously saved script into the Files: section.
- 4. **Insert Line Separator** inserts a dashed line after the last line of text in the **Files**: section. The separator is cosmetic and has no effect on the executed script.
- 5. Save Script saves the contents of the Files: section into a .txt file.
- Commands opens the Scripting Commands Scratch Pad window. The window opens loaded with the script currently in the Files: section. See <u>Section 7.6.2.6.1</u> <u>"Scripting Command Scratchpad"</u> for details on using the Scripting Commands Scratch Pad to build scripts.
- 7. Clear Script clears the contents of the Files: section.
- 8. **Run Script** executes the script currently in the **Files:** section. The results display in the **Script Log** section.
- 9. Save Script Log saves the contents of the Script Log section into a .txt file.
- 10.Clear Script Log clears the contents of the Script Log.

#### 7.6.2.6.1 Scripting Command Scratchpad

The **Scripting Command Scratchpad** is a pop-up window that allows users to build a script by selecting commands and command parameters from drop-down menus. As commands are selected they appear in the script panel at the left of the window. Clicking **Done** loads the script into the **Files:** section of the **Script Editor** panel. The script is executed by click **Run Script** in the **Script Editor** panel.

The Scripting Command Scratchpad is activated by clicking the Command button in the Script Editor panel.

<u>Figure 26</u> shows the types of commands available through the **Scripting Command Scratchpad** window.



1. The SWITCHING SUPPLIES section contains commands that set buck regulator and boost regulator parameters.

#### KITVR5100FRDMEVM evaluation board

- 2. The LINEAR SUPPLIES section contains commands that set LDO regulator parameters.
- 3. The LOG COMMAND section contains commands that output the value of the selected supplies.
- 4. The I2C COMMANDS section contains commands related to connected I<sup>2</sup>C devices.
- 5. The OTHER COMMANDS section contains miscellaneous commands that set delays, insert pauses, dump registers and so forth.
- 6. The INTERRUPTS section contains commands that clear interrupts.
- 7. The FREE RAM section contains commands that assign values to the embedded memory register banks.
- 8. The TEST COMMAND section contains commands that perform tests on the target device (for example, is VSENSE greater than some value) when the script is executed.
- The PROGRAMMERS COMMANDS section contains commands that initiate the OTP programming of an unprogrammed device. This section is not visible unless the target is a KITVR5100FRDMPM socket board or a KITVR5100FRDMEVM with a mounted socket board (Combo mode).
- 7.6.2.6.1.1 Switching supply commands

SWIT	CHING SUPPLI	<u>ES</u>
SUPPLY:	SW1	•
VOUT:	•	
VSTBY:	•	
VOFF:	•	
MODE:		•
OMODE:	ON OFF	=
ILIMIT:	1.5x 2.0:	x

#### Figure 27. Switching supplies

Name	Description
SW1, SW2, SW3, or SWBST	Select supply from the list
VOUT	Select voltage from the list
VSTBY	Select voltage from the list
VOFF	Select voltage from the list

#### KITVR5100FRDMEVM evaluation board

Name	Description
MODE	Select mode from the list
OMODE	ON or OFF
ILIMIT	1.5x or 2.0x

#### Examples:

SW1:VOUT:1.000 SW2:VSTBY:1.600 SW3:VOFF:1.050 SWBST:MODE\_NORM:AUTO SW1:OMODE:ON SW2:MODE:PWM | PWM SW3:ILIMIT:2.0x

7.6.2.6.1.2 Linear supply commands

LIN	LINEAR SUPPLIES	
SUPPLY:	LDO 1	-
VOUT:		•
ENABLE:	ON	OFF
STDBY:	ON	OFF
LWPWR	ON	OFF
OMODE:	ON	OFF

#### Figure 28. Linear supplies

Name	Description
LDO1, LDO2, VSD, V33, LDO3, LDO4, REFOUT	Select supply from the list
VOUT	Select voltage from the list
ENABLE	ON or OFF
STDBY	ON or OFF
LWPWR	ON or OFF
OMODE	ON or OFF

#### Examples:

LDO1:ENABLE:ON

LDO2:VOUT:1.300

KITVR5100FRDMEVM evaluation board

VSD:STBY:ON
V33:LOWPWR:ON
LDO3:OMODE:ON
LDO4:VOUT:3.000
REFOUT:ENABLE:ON

7.6.2.6.1.3 Log commands

	LOG COMMAND		
SOURCE:	•		
PARAMETER:		•	

Figure 29. Log commands

Name	Description
SOURCE	Select source from the list
PARAMETER	Select parameter from the list

#### Examples:

LOG:SW1:VSENSE

LOG:LDO1:ENABLE

LOG:INT:SW3\_FAULT

7.6.2.6.1.4 I2C commands

I2C COMMANDS	
WRITE_I2C: <addr>:<data></data></addr>	READ_I2C: <addr></addr>
PING_I2C1:<0xAddr>	PING_I2C2:<0xAddr>
SCAN_DEVICES:	

#### Figure 30. I2C commands

Name	Description
WRITE_I2C	Enter address and data
READ_I2C	Enter address
PING_I2C1	Enter 0xAddress
PING_I2C2	Enter 0xAddress
SCAN_DEVICES	

#### Examples:

WRITE\_I2C:20:05

KITVR5100FRDMEVM evaluation board

READ\_I2C:1C I2C1\_PING:0x08

I2C2 PING:0xC0

SCAN\_DEVICES:

7.6.2.6.1.5 Other commands



#### Figure 31. Other commands

Name	Description
DELAY	Enter delay time in milliseconds
PAUSE	Click on control
// Separator Bar	Click on control
GET_TARGET	Click on control
TIMESTAMP	Click on control
DUMP_SWREGS	Enter switching supply
DUMP_LINREGS	Enter linear supply
DUMP_OTPREGS	Enter OTP supply register
PWRON	HIGH, LOW, or TOGGLE
SD_VSEL	HIGH or LOW
STANDBY	ON or OFF
EXTRACT_OTP	EVB or Socket

#### Examples:

DELAY:100 PAUSE:

KITVR5100FRDMEVM evaluation board

GET\_TARGET: TIMESTAMP: DUMP\_SWREGS:SW2 DUMP\_LINREGS:LDO1 DUMP\_OTPREGS:SYS DUMP\_OTPREGS:SWBST PWRON:HIGH SD\_VSEL:LOW STANDBY:ON EXTRACT\_OTP:EVB





Figure 32. Interrupts commands

Name	Description
REGISTER	Select register from the list
INTO, INT1, INT3, INT4	Select interrupt event from the list
ACTION	SET or CLR

#### Examples:

INT0:STATUS\_110C:CLR INT0:STATUS\_ALL:CLR INT1:STATUS\_SW1A\_FAULT:CLR INT1:MASK\_SW2\_FAULT:SET INT1:MASK\_ALL:CLR INT3:STATUS\_SWBST\_FAULT:CLR INT4:MASK\_LD02\_FAULT:CLR

#### KITVR5100FRDMEVM evaluation board

#### 7.6.2.6.1.7 Free RAM commands



#### Figure 33. Free RAM commands

Name	Description
MEMA	Enter hex data
MEMB	Enter hex data
MEMC	Enter hex data
MEMD	Enter hex data

Examples:	
MEMA:2C	
MEMB:04	

MEMC:55

MEMD:3F

7.6.2.6.1.8 Test commands



#### Figure 34. Test commands

Name	Description
TEST SOURCE	Select item
PARAMETER	Select item
TEST	Select item

KITVR5100FRDMEVM evaluation board



Name	Description
VPGM SUPPLY	Toggles VPGM supply on and off
VPGM SET	Sets the value of VPGM
PROGRAM	Initiates OTP programming
COMPARE OTP TO CFG	Compares the values in the OTP registers with the values in the CFG file used to program the device.
COMPARE OTP TO HEX	Compares the values in the OTP registers with the values in the HEX file used to program the device.

#### 7.6.2.7 Functional Registers panel

The Functional Registers panel provides bit-level access to each register.

#### KITVR5100FRDMEVM evaluation board

ADDRESS       SWI VOUT       VOUT       VOUT       VOUT       1.100 Volts         0x20       0	Switching Sup	plies Lir	near S	upplie	s N	/iscel	laneou	us In	iterrup	ots OTP	Configurati	ion Script Editor Funct	tional Registers	OTP Registers		
0x20       07       06       05       04       03       02       01       00       0x10         PAGE 0       X       X       X       083       082       081       080       082       081       080         ADDRESS       V       X       X       X       01       03       02       01       00       0x08         PAGE 0       X       X       X       084       083       082       081       080       0x08         PAGE 0       X       X       X       084       083       082       081       080       0x08         PAGE 0       X       X       X       084       083       082       081       080       0x08         PAGE 0       X       X       084       083       082       081       080       0X08       NMODE = 01SABLED         PAGE 0       X       X       084       083       082       081       080       0X08       NMODE = APS         PAGE 0       X       X       084       083       082       081       080       0VS = 12.50 mV/as         PAGE 0       X       X       093       02       01	ADDRESS				SV	V1 V	OUT					VOUT = 1.100 Volts				MISC
PAGE 0       X       X       X       DB3       DB2       DB1       DB0         ADDRESS       SW1       VSTBY       VSTBY <th< th=""><th>0x20</th><th>D7</th><th>D</th><th>5 D</th><th>5</th><th>D4 ▼</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>0x10</th><th></th><th></th><th></th><th></th><th>RAM</th></th<>	0x20	D7	D	5 D	5	D4 ▼	D3	D2	D1	D0	0x10					RAM
ADDRESS       USTBY       VSTBY = 0.900 Volts         0x21       0       0       0       0       0x08         PAGE 0       X       X       0B4       0B3       0B2       0B1       0B0         ADDRESS       USTBY = 0.900 Volts       0x08       VSTBY = 0.900 Volts         ADDRESS       USTBY = 0.900 Volts       0x08       VSTBY = 0.900 Volts         0x22       0       0       0       0       0x08         PAGE 0       X       X       0B4       0B3       0B2       0B1       0B0         0x23       07       06       05       04       03       02       01       00         0x23       07       06       05       04       03       02       01       00         PAGE 0       X       X       0M3       02       01       00       0x08       NMODE = DISABLED         NMODES       USTBY = 0.000       0x08       MODE = APS       SMODE = APS       SMODE = APS         PAGE 0       X       0M       X       0B3       02       01       00         0x24       07       06       05       04       03       02       0X	PAGE 0	X	×	: >	< I	DB4	DB3	DB2	DB1	DBO						IWS
0x21 $D^7$ $D6$ $D5$ $D4$ $D3$ $D2$ $D1$ $D0$ $0x08$ PAGE 0       X       X       X $DB3$ $DB2$ $DB1$ $DB0$ ADDRESS       V       V       I       I $D2$ $D1$ $D0$ $0x08$ PAGE 0       X       X       X $DB3$ $D2$ $D1$ $D0$ $0x08$ PAGE 0       X       X $DB3$ $D2$ $D1$ $D0$ $0x08$ PAGE 0       X       X $DB3$ $DB2$ $DB1$ $D0$ $0x08$ ADDRESS       V       X $X$ $DB3$ $D2$ $D1$ $D0$ $0x23$ I       D0 $V$ I $D3$ $D2$ $D1$ $D0$ $PAGE 0$ X       X $DB3$ $DB2$ $DB1$ $D00$ $0X08$ $MODE = DISABLED$ $MODRESS$ SW1 $V$ $D3$ $D2$ $D1$ $D0$ $0X04$ $PHASE = 0^{\circ}$ $0x24$ IV       I       ID       <	ADDRESS				SW	/1 VS	STBY					VSTBY = 0.900 Volts				[] []
PAGE 0 $X$ $X$ $X$ $X$ $Z$ $DB1$ $DB2$ $DB1$ $DB0$ $UB1$ $UB1$ $DB1$ <th>0x21</th> <th>D7</th> <th>De</th> <th>5 D</th> <th>5  </th> <th>D4</th> <th>D3</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>0x08</th> <th></th> <th></th> <th></th> <th></th> <th>W2 S</th>	0x21	D7	De	5 D	5	D4	D3	D2	D1	D0	0x08					W2 S
ADDRESS       SW1 VOFF       VOFF = 0.900 Volts         0x22       D7       D6       D5       D4       D3       D2       D1       D0       0x08         PAGE 0       X       X       DB4       DB3       DB2       DB1       DB0       OMODE = DISABLED         ADDRESS       SW1       VOFF       OMODE       DISABLED       NMODE = APS       SMODE = APS         PAGE 0       X       X       OM       X       DB3       DB2       DB1       DB0         ADDRESS       SW1       CONFIGURATION       DVS       12.50 mV/µs       PHASE = 0 °       SMODE = 0'S         PAGE 0       X       DVS       PH1       PH0       FS1       FS0       X       ILM       PKE = 100%         ADDRESS       SW1 POWER SEGMENTS       PSEG = 100%       PSEG = 100%       PSEG = 100%	PAGE 0	X	×	: >	< I	DB4	DB3	DB2	DB1	DBO						ŴЗ
0x22 $D7$ $D6$ $D5$ $D4$ $D3$ $D2$ $D1$ $D0$ $0x08$ PAGE 0       X       X       X $DB4$ $DB3$ $DB2$ $DB1$ $DB0$ $DB1$ <t< th=""><th>ADDRESS</th><th></th><th></th><th></th><th>sv</th><th>V1 V</th><th>OFF</th><th></th><th></th><th></th><th></th><th>VOFF = 0.900 Volts</th><th></th><th></th><th></th><th>SMB</th></t<>	ADDRESS				sv	V1 V	OFF					VOFF = 0.900 Volts				SMB
PAGE 0 $X$ $X$ $X$ $X$ $X$ $DB3$ $DB2$ $DB1$ $DB0$ $DD0$ ADDRESS $$	0x22	D7	De	5 D	5	D4	D3	D2	D1	D0	0x08					ST LINI
ADDRESSSW1 MODEOMODE = DISABLED NMODE = APS SMODE = APS SMODE = APSDAGE 0XXDMXDB3DB2DB1DB0DVS $1 \times 10^{10}$ ADDRESSSW1CVNFIGURATIONVD1D2D1D0D0DVS $1 \times 10^{10}$ DVS = $12.50 \text{ mV/}\mus$ PAGE 0XDVSPH1PH0FS1FS0XILIMDVS $2 \times 10^{10}$ DVS = $12.50 \text{ mV/}\mus$ ADDRESSSW1CVVSPH1PH0FS1FS0XILIMPSEG = $100\%$	PAGE 0	X	×	: >	< I	DB4	DB3	DB2	DB1	DBO						Ę
D7D6D5D4D3D2D1D0 $0x08$ NMODE = APS SMODE = APSPAGE 0XXOMXDB3DB2DB1DB0DVPHASE = 0 °ADDRESS $\sum$ $\sum$ D4D3D2D1D0 $0x04$ PHASE = 0 °PAGE 0XDVSPH1PH0FS1FS0XILIMADDRESS $\sum$ DVSFS1FS0XILIM	ADDRESS	S SW1 MODE										OMODE = DISABLED				
OX23 $X$ $X$ $DB3$ $DB2$ $DB1$ $DB0$ SMODE = APSPAGE 0 $X$ $X$ $DB3$ $DB2$ $DB1$ $DB0$ $DVS = 12.50 \text{ mV/} \mu s$ ADDRESS $SW1$ $CONFIGURATION$ $DVS = 12.50 \text{ mV/} \mu s$ OX24 $D7$ $D6$ $D5$ $D4$ $D3$ $D2$ $D1$ $D0$ $OX24$ $D7$ $D6$ $D5$ $D4$ $D3$ $D2$ $D1$ $D0$ $SWS = 12.50 \text{ mV/} \mu s$ PAGE 0 $X$ $DVS$ $PHASE = 0^{\circ}$ $FSW = 2.0 \text{ MHz}$ $ILIMIT = 2.0x$ ADDRESS $SW1$ $POWER$ $SEGMENTS$ $PSEG = 100\%$	0,22	D7	De	D	5 1	D4	D3	D2	D1	DO	009	NMODE = APS				
PAGE 0XXOMXDB3DB2DB1DB0ADDRESSSW1 CONFIGURATION $V$	UX23										0x08	SMODE = APS				
ADDRESS       SW1 CONFIGURATION       DVS = 12.50 mV/µs         D7       D6       D5       D4       D3       D2       D1       D0         0x24       Image: Convertige of the second secon	PAGE 0	X	X	0	м	X	DB3	DB2	DB1	DBO						
D7D6D5D4D3D2D1D0PHASE = 0OX24 $\frown$ $\frown$ $\frown$ $\checkmark$ $\frown$ $\frown$ $\frown$ $\frown$ $\frown$ $\frown$ PAGE 0 $X$ DVSPH1PH0FS1FS0 $X$ ILIMPSEG = 100%ADDRESSSW1 POWER SEGMENTSPSEG = 100%	ADDRESS			SW1	l CO	NFIG	SURA'	TION				DVS = 12.50 mV/µs				
PAGE 0     X     DVS     PH1     PH0     FS1     FS0     X     ILIMIT       ADDRESS     SW1 POWER SEGMENTS     PSEG = 100%	0x24	D7	De	5 D	5	D4	D3	D2	D1	DO	0x04	FSW = 2.0 MHz				
ADDRESS SW1 POWER SEGMENTS PSEG = 100%	PAGE 0	×	DV	'S PI	H1	рно	FS1	FSO	x	ILIM		ILIMIT = 2.0x				
	ADDRESS	S SW1 POWER SEGMENTS										PSEG = 100%	-			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	0x81	D7	De	5 D	5	D4	D3	D2	D1	D0	0x07					
PAGE 2 X X X X X DB2 DB1 DB0	PAGE 2	x	×	: >	<	x	x	DB2	DB1	DBO						

#### Figure 36. Functional Registers panel

Clicking on a checkbox immediately sets or clears the corresponding register bit. Key bit-fields in each register are decoded to assist in displaying the actual state of each parameter.

Registers are grouped within each tab by function.

#### 7.6.2.8 OTP Registers panel

The OTP Registers panel provides bit-level access to each register.

KTVR5100FRDMEVMUG

KITVR5100FRDMEVM evaluation board

Swi	tching Suppli	ies Lin	ear Su	pplies	Misc	ellane	ous	Interru	ipts OTF	Configurati	on Script Editor Function	nal Registers	OTP Registers		
4	DDRESS			SV	V1 01	rp vo	UT				VOUT = 0.900 Volts	]		Edit Configuration	SYSTE
	0xA0	D7	D6	D5	D4	D3 √	D2	D1	D0	0x08					≚  ⊻
	DACE 1	×	X	X	DB4	DB3	DB2	DB1	DBO						1
	DDDESS			SW/1	OTP	SEOL					SEOUENCE = 2	]			SW2
ľ	DDRESS	D7	D6	D5	D4	D3	D2	D1	D0						SWS
	0xA1							1		0x02					S I
	PAGE 1	X	X	X	X	X	DB2	DB1	DBO						WBST
4	DDRESS		SW	/1 OT	P CO	NFIG	JRAT	ION			FSW = 2.0 MHz				EN
	0xA2	D7	D6	D5	D4	D3	D2 √	D1	D0	0x05					
	PAGE 1	×	Х	Х	Х	Х	Х	F51	F50						ß
			_	_	_	_	_	_				1			ы
															FI
														<b>D</b> ////	
														RUN	

Figure 37. OTP Registers panel

Bits can only be changed after the Edit Configuration has been pressed.

Clicking on a checkbox immediately sets or clears the corresponding register bit. Key bit-fields in each register are decoded to assist in displaying the actual state of each parameter.

Registers are grouped within each tab by function.

While in Edit Configuration (TBB mode), the OTP data import, export, and compare buttons are visible. The buttons function the same as those on the OTP Configuration panel.

KITVR5100FRDMEVM evaluation board

S	vitching Suppl	ies Lin	ear Su	pplies	Misc	ellane	ous	Interru	ipts OTP	Configurati	on Script Editor Function	nal Registers	OTP Registers		
	ADDRESS			SV	V1 O1		DUT				VOUT = 0.900 Volts	]		Return to Run Mode	SYSTE
	0xA0	D7	D6	D5	D4	D3	D2	D1	D0	0x08				<u>Input Data</u>	<u>ू</u>
	PAGE 1	×	Х	Х	DB4	DB3	DB2	DB1	DBO					Load CFG File	1
	ADDRESS			SW1	ОТР	SEQU	JENC				SEQUENCE = 2	]		Load HEX File	SW2
	0×41	D7	D6	D5	D4	D3	D2	D1	D0	0202				Update From Target	SW3
	UXAI	×	X	X	X	X	DB2	DB1	DBO	0x02				<u>Output Data</u>	ws.
	PAGE 1											]		Save CFG File	BST
	ADDRESS	07	SW	/1 OT	TP CO	NFIG	URAT	ION	D0		FSW = 2.0 MHz			Save HEX File	EI
	0xA2						<b>V</b>		<b>V</b>	0x05				Generate Report	턻
	PAGE 1	Х	Х	Х	×	Х	×	F51	F50					Compare Data	ß
		_	_	_	_	_	_	_				1		Compare to CFG	lΩ.
														Compare HEX File	۲I
														Restart PMIC	
														TBB	
-															-

Figure 38. OTP Registers panel (TBB mode on evaluation board)

If the target connected is a VR5100 Socket board, or a VR5100 EVB with the VR5100 Socket board mounted atop (COMBO), the GUI displays the **PROGRAM** button, and device programming is permitted.

KITVR5100FRDMEVM evaluation board

Sw	tching Suppl	lies Lin	near Su	pplies	Miso	ellane	ous	Interru	ipts OTP	Configurati	ion Script Editor Function	nal Registers	OTP Registers		1
	ADDRESS			SV	N1 0		UT				VOUT = 1.150 Volts	]		Return to Run Mode	SYSTE
	0xA0	D7	D6	D5	D4	D3	D2	D1	D0	0x12				<u>Input Data</u>	୍ଲ କୁ
	PAGE 1	×	Х	Х	DB4	DB3	DB2	DB1	DBO					Load CFG File	-
ľ	ADDRESS			SW1	ОТР	SEQL	JENC	:			SEQUENCE = 1	1		Load HEX File	SW2
	0xA1	D7	D6	D5	D4	D3	D2	D1	D0	0x01				Update From Target	SM3
		X	X	X	X	X	DB2	DB1	DBO	0,01				<u>Output Data</u>	WS
	PAGE 1										ESW = 2.0 MHz	] 1		Save CFG File	BST
	ADDRESS	D7	D6	V1 O1 D5	D4	D3	DRAT D2	D1	D0		F5W = 2.0 MH2			Save HEX File	LIN1
	0xA2					1	$\checkmark$			0x0D				Generate Report	E
	PAGE 1	×	×	Х	Х	Х	Х	F51	F50					Compare Data	
														Compare to CFG	ű
														PROGRAM	
														Restart PMIC	
														TRR	
_															<u> </u>

Figure 39. OTP Registers panel (TBB mode on socket or combo board)

#### 7.6.2.9 Try-Before-Buy mode using the "Configuration" tab

The KITVR5100FRDMEVM comes with a VR5100 device whose OTP memory is preprogrammed. The VR5100 allows the user to override the OTP memory using the **Try-Before-Buy** mode.

To use this mode, go to the **OTP Configuration** tab and click **Edit Configuration** button in the top-right of the window. Use the drop down option to change the voltage, sequence and configuration of the regulators. Click the **Update** button after all the desired options are selected.

To restart the VR5100 using the selected configuration, click **Restart PMIC** button. Alternatively, you can toggle the PWRON button to initiate the startup. The startup sequence can be monitored on an oscilloscope and will match this selection in the **Configuration** tab. To measure voltages, use either a stand-alone meter or the on-board meters available in the GUI.

Use the **Save Configuration** and **Load Configuration** buttons to save the configuration for later use.

KTVR5100FRDMEVMU
User guide

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#### KITVR5100FRDMEVM evaluation board



### 8 Schematics, board layout and bill of materials

KITVR5100FRDMEVM board schematics, board layout and bill of materials are available in the download tab of the KITVR5100FRDMEVM Tool summary page at the following URL: <u>http://www.nxp.com/KITVR5100FRDMEVM</u>

#### 9 References

Following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com support pages	Description	URL
	Tool summary page	http://www.nxp.com/ KITVR5100FRDMEVM
KITVR5100FRDMEVM	Schematic, BOM, board layout	https://www.nxp.com/ KITVR5100FRDMEVM (Download section)
KITVR5100FRDPGM	Tool summary page	http://www.nxp.com/ KITVR5100FRDPGM
VR5100	Product summary page	http://www.nxp.com/VR5100
FRDM-KL25Z	Freedom Development Platform	http://www.nxp.com/FRDM-KL25Z

### **10** Contact information

Visit <u>http://www.nxp.com/support</u> for a list of phone numbers within your region. Visit <u>http://www.nxp.com/warranty</u> to submit a request for tool warranty.

KITVR5100FRDMEVM evaluation board

## **11 Revision history**

Revision	Date	Description of changes
1.0	8/2016	Initial release

#### KITVR5100FRDMEVM evaluation board

### 12 Legal information

#### **12.1 Definitions**

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#### **NXP Semiconductors**

# **KTVR5100FRDMEVMUG**

KITVR5100FRDMEVM evaluation board

### Tables

Tab. 1.	Device features Minimum start-up voltage is
	3.1 V5
Tab. 2.	Board description6
Tab. 3.	Startup configuration This table specifies
	the default output voltage of the LDOs and
	SWx after start-up and/ or when the LDOs
	and SWx are enabled. VREFDDR SEQ is
	internally fixed to be same as SW3_SEQ.

	VCC_SD voltage depends on the state of the	
	SD_VSEL pin.	7
Tab. 4.	LED locations	9
Tab. 5.	Jumper and switch definitions	. 10
Tab. 6.	Test point definitions	. 13
Tab. 7.	Banana connectors	. 15
Tab. 8.	Coin cell battery	. 16
Tab. 9.	KITVR5100FRDMEVM to FRDM-KL25Z	
	connections	. 18

KITVR5100FRDMEVM evaluation board

## Figures

Fig. 1.	Board description	6
Fig. 2.	VR5100 GUI OTP Configuration panel	
	showing onboard VR5100 startup	
	configuration data	8
Fig. 3.	LED locations	9
Fig. 4.	Jumper and switch locations	10
Fig. 5.	Test point locations	13
Fig. 6.	Screw terminal locations	15
Fig. 7.	Coin cell battery	16
Fig. 8.	FRDM-KL25Z	17
Fig. 9.	VR5100 GUI log with Combo mode target	
	enabled	23
Fig. 10.	Efficiency measurement for SW1 supply	25
Fig. 11.	VOUT measurement locations	26
Fig. 12.	VR5100 GUI main window	27
Fig. 13.	GUI startup	28
Fig. 14.	GUI connected to target board	29
Fig. 15.	Switching Supplies panel	30
Fig. 16.	Linear Supplies panel	.31
Fig. 17.	Miscellaneous panel	32
Fig. 18.	Interrupts panel	33
Fig. 19.	SW1 overcurrent fault condition	34
Fig. 20.	LDO1 overcurrent fault condition	.34
Fig. 21.	OTP Configuration panel	35

Fig. 22.	OTP Configuration Panel (TBB Mode on	
	evaluation board)	36
Fig. 23.	OTP Configuration panel (TBB Mode on	
	socket or combo board)	37
Fig. 24.	OTP Configuration panel (OTP data loaded	
	from target EVB)	38
Fig. 25.	Script Editor panel	39
Fig. 26.	Scripting Command Scratchpad command	
	types	40
Fig. 27.	Switching supplies	41
Fig. 28.	Linear supplies	42
Fig. 29.	Log commands	43
Fig. 30.	I2C commands	43
Fig. 31.	Other commands	44
Fig. 32.	Interrupts commands	45
Fig. 33.	Free RAM commands	46
Fig. 34.	Test commands	46
Fig. 35.	Programmer Commands	47
Fig. 36.	Functional Registers panel	48
Fig. 37.	OTP Registers panel	49
Fig. 38.	OTP Registers panel (TBB mode on	
	evaluation board)	50
Fig. 39.	OTP Registers panel (TBB mode on socket	
-	or combo board)	51
Fig. 40.	Try-Before-Buy window	52

KITVR5100FRDMEVM evaluation board

### Contents

1 2 3	KITVR5100FRDMEVM Important notice Overview of the VR5100 PMIC development environment	1 2
4	Getting started	4
4.1	Kit contents/packing list	4
4.2	Jump start	4
4.3	Required equipment	4
4.4	System requirements	4
5	Getting to know the hardware	5
5.1	Board overview	5
5.2	Board features	5
5.3	Device features	5
5.4	Board description	6
5.5	Device description	7
5.6	LED display	9
5.7	Jumper and switch definitions	. 10
5.8	Test point definitions	12
5.9	Banana connectors	14
5.10	Coin cell battery	15
6	FRDM-KL25Z Freedom SPI dongle	17
6.1	Connecting the FRDM-KL25Z to the board	17
7	Installing the software and setting up the	
	hardware	. 20
7.1	Installing VR5100GUI on your computer	. 20
7.2	Configuring the hardware and using the GUI	
	for control and monitoring	21
7.3	Configuring the KITVR5100FRDMEVM and	
	the KITVR5100FRDMPGM in Combo mode	22
7.4	Using on-board ELOADs	. 23
7.5	Measuring switching supply efficiency	24
7.6	Understanding and using the GUI	. 27
7.6.1	GUI structure for VR5100	27
7.6.2	GUI panels	27
7.6.2.1	Switching Supplies panel	29
7.6.2.2	Linear Supplies panel	30
7.6.2.3	Miscellaneous panel	. 31
7.6.2.4	Interrupts panel	32
7.6.2.5	OTP Configuration panel	. 35
7.6.2.6	Script Editor panel	. 39
7.6.2.6.	1 Scripting Command Scratchpad	.40
7.6.2.7	Functional Registers panel	.47
7.6.2.8	OTP Registers panel	. 48
7.6.2.9	Try-Before-Buy mode using the	
~	"Configuration" tab	.51
8	Schematics, board layout and bill of	
•	materials	52
9	Reterences	. 52
10	Contact information	. 52
11	Revision nistory	. 53
12	Legal information	. 54

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