HEF4013B-Q100

Dual D-type flip-flop

Rev. 4 — 23 November 2021 | Product data sheet

1. General description

The HEF4013B-Q100 is a dual D-type flip-flop with set and reset; positive-edge trigger. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Complies with JEDEC standard JESD 13-B

3. Applications

- Counters and dividers
- Registers
- Toggle flip-flops

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4013BT-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4013BTT-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

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5. Functional diagram

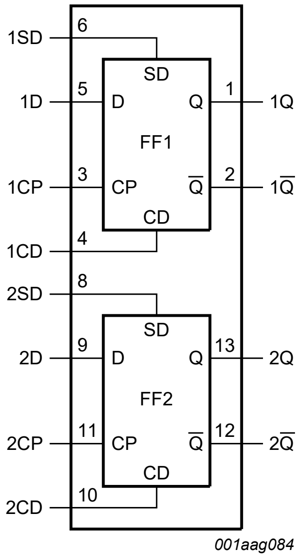


Fig. 1. Functional diagram

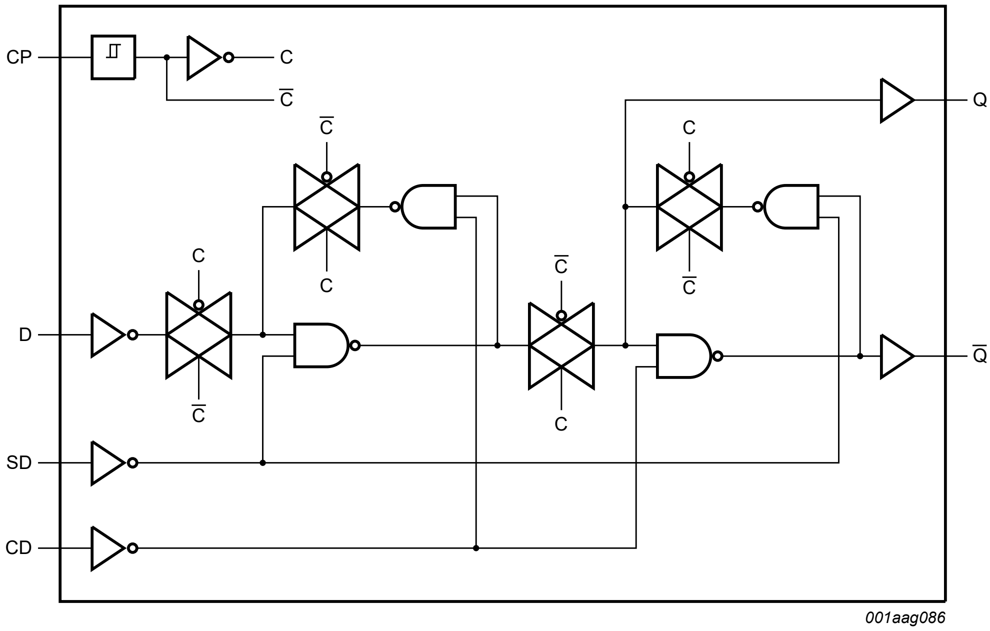


Fig. 2. Logic diagram (one flip-flop)

6. Pinning information

6.1. Pinning

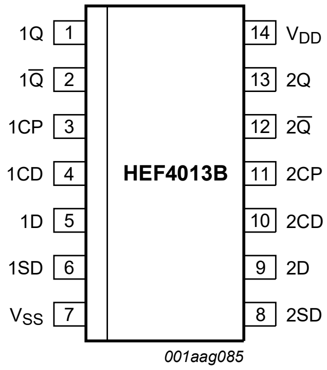


Fig. 3. Pin configuration for SOT108-1 (SO14) and SOT402-1 (TSSOP14)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q	1, 13	true output
$1\overline{Q}$, $2\overline{Q}$	2, 12	complement output
1CP, 2CP	3, 11	clock input (LOW to HIGH edge-triggered)
1CD, 2CD	4, 10	asynchronous clear-direct input (active HIGH)
1D, 2D	5, 9	data input
1SD, 2SD	6, 8	asynchronous set-direct input (active HIGH)
V_{SS}	7	ground (0 V)
V_{DD}	14	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.

Control			Input	Output	
nSD	**nCD**	**nCP**	**nD**	**nQ**	**$n\overline{Q}$**
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	μs/V
		V_{DD} = 10 V	-	0.5	μs/V
		V_{DD} = 15 V	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\| < 1$ μA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\| < 1$ μA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\| < 1$ μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\| < 1$ μA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I_{DD}	supply current	all valid input combinations; $\|I_O\|$ = 0 A	5 V	-	1.0	-	1.0	-	30	-	30	μA
			10 V	-	2.0	-	2.0	-	60	-	60	μA
			15 V	-	4.0	-	4.0	-	120	-	120	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

T_{amb} = 25 °C, unless otherwise specified. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nCP to nQ, $n\overline{Q}$; see Fig. 4	5 V	[1]	83 + 0.55 × C_L	-	110	220	ns
			10 V		34 + 0.23 × C_L	-	45	90	ns
			15 V		22 + 0.16 × C_L	-	30	60	ns
		nSD to $n\overline{Q}$	5 V	[1]	73 + 0.55 × C_L	-	100	200	ns
			10 V		29 + 0.23 × C_L	-	40	80	ns
			15 V		22 + 0.16 × C_L	-	30	60	ns
		nCD to nQ	5 V	[1]	73 + 0.55 × C_L	-	100	200	ns
			10 V		29 + 0.23 × C_L	-	40	80	ns
			15 V		22 + 0.16 × C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	nCP to nQ, $n\overline{Q}$; see Fig. 4	5 V	[1]	68 + 0.55 × C_L	-	95	190	ns
			10 V		29 + 0.23 × C_L	-	40	80	ns
			15 V		22 + 0.16 × C_L	-	30	60	ns
		nSD to nQ	5 V	[1]	48 + 0.55 × C_L	-	75	150	ns
			10 V		24 + 0.23 × C_L	-	35	70	ns
			15 V		17 + 0.16 × C_L	-	25	50	ns
		nCD to $n\overline{Q}$	5 V	[1]	33 + 0.55 × C_L	-	60	120	ns
			10 V		19 + 0.23 × C_L	-	30	60	ns
			15 V		12 + 0.16 × C_L	-	20	40	ns
t_t	transition time	see Fig. 4	5 V	[1]	10 + 1.00 × C_L	-	60	120	ns
			10 V		9 + 0.42 × C_L	-	30	60	ns
			15 V		6 + 0.28 × C_L	-	20	40	ns
t_{su}	set-up time	nD to nCP; see Fig. 4	5 V			40	20	-	ns
			10 V			25	10	-	ns
			15 V			15	5	-	ns
t_h	hold time	nD to nCP; see Fig. 4	5 V			20	0	-	ns
			10 V			20	0	-	ns
			15 V			15	0	-	ns
t_W	pulse width	nCP input LOW; see Fig. 4	5 V			60	30	-	ns
			10 V			30	15	-	ns
			15 V			20	10	-	ns
		nSD input HIGH; see Fig. 5	5 V			50	25	-	ns
			10 V			24	12	-	ns
			15 V			20	10	-	ns
		nCD input HIGH; see Fig. 5	5 V			50	25	-	ns
			10 V			24	12	-	ns
			15 V			20	10	-	ns

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{rec}	recovery time	nSD input; see Fig. 5	5 V		+15	-5	-	ns
			10 V		15	0	-	ns
			15 V		15	0	-	ns
		nCD input; see Fig. 5	5 V		40	25	-	ns
			10 V		25	10	-	ns
			15 V		25	10	-	ns
$f_{clk(max)}$	maximum clock frequency	see Fig. 4	5 V		7	14	-	MHz
			10 V		14	28	-	MHz
			15 V		20	40	-	MHz

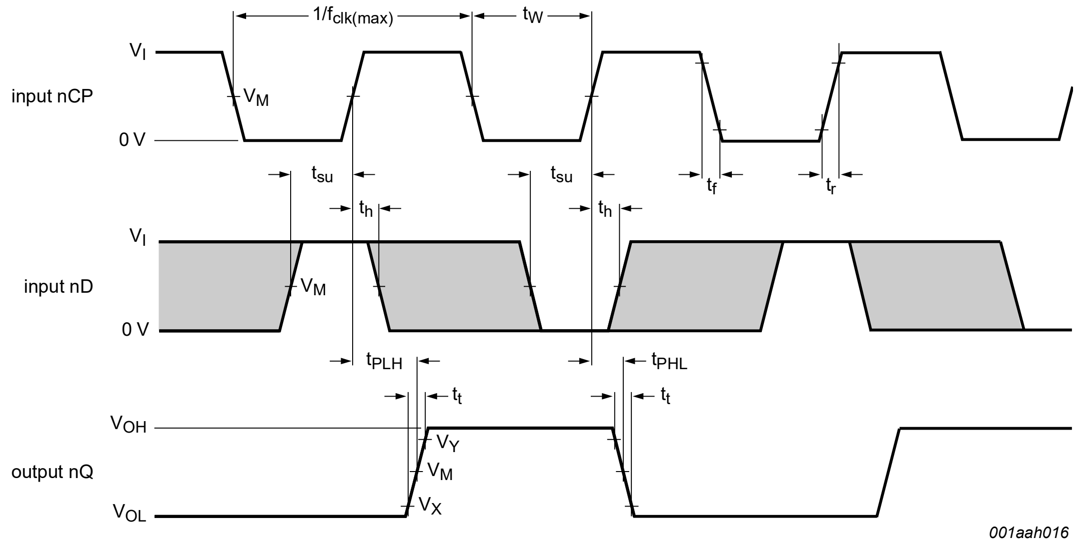
[1] Typical values of the propagation delays and output transition times can be calculated with the extrapolation formulas (C_L in pF).

Table 8. Dynamic power dissipation

V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

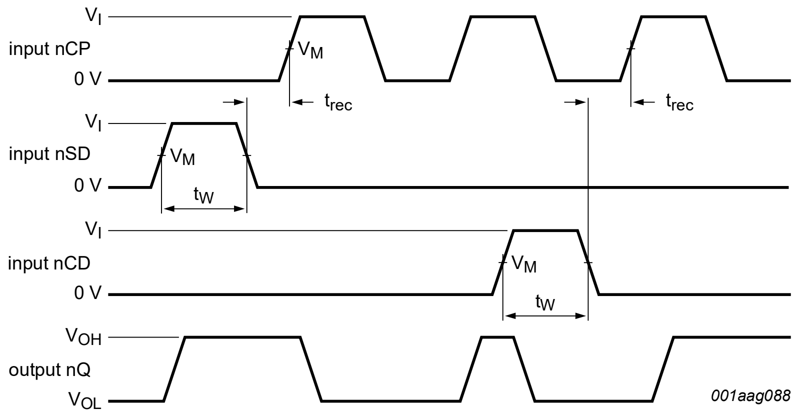
Symbol	Parameter	V_{DD}	Typical formula	Where
P_D	dynamic power dissipation	5 V	$P_D = 850 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ μW	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 3600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ μW	
		15 V	$P_D = 9000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ μW	

11.1. Waveforms and test circuit



Set-up and hold times are shown as positive values but may be specified as negative values.
The shaded areas indicate when the input is permitted to change for predictable output performance.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
Measurement points are given in Table 9.

Fig. 4. Set-up time, hold time, minimum clock pulse width, propagation delays and transition times



Recovery times are shown as positive values but may be specified as negative values.

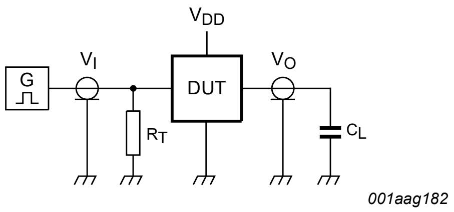
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Measurement points are given in Table 9.

Fig. 5. nSD, nCD recovery time and pulse width

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	**V_M**	**V_M**	**V_X**	**V_Y**
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



Test and measurement data is given in Table 10;

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	**V_I**	**t_r, t_f**	**C_L**
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Application information

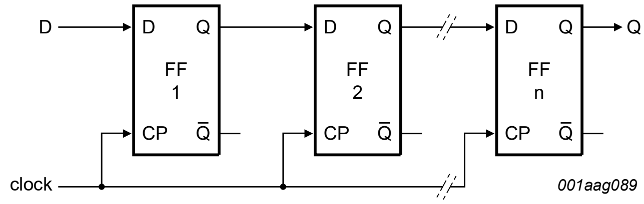


Fig. 7. N-stage shift register

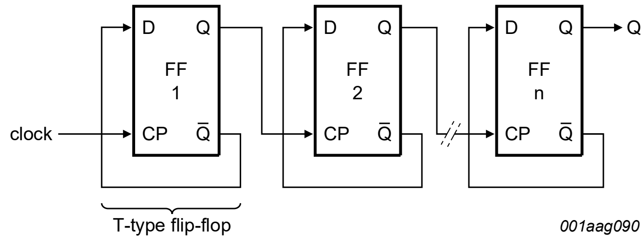


Fig. 8. Binary ripple up-counter; divide-by-2^n

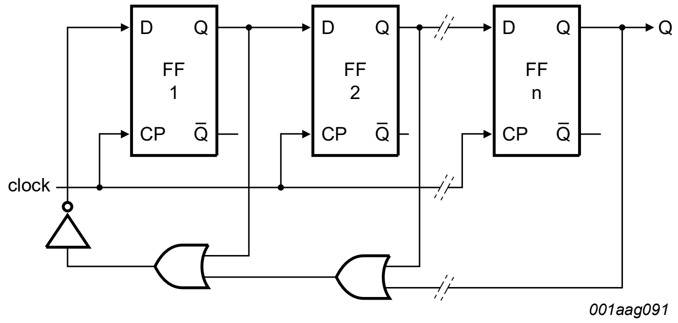
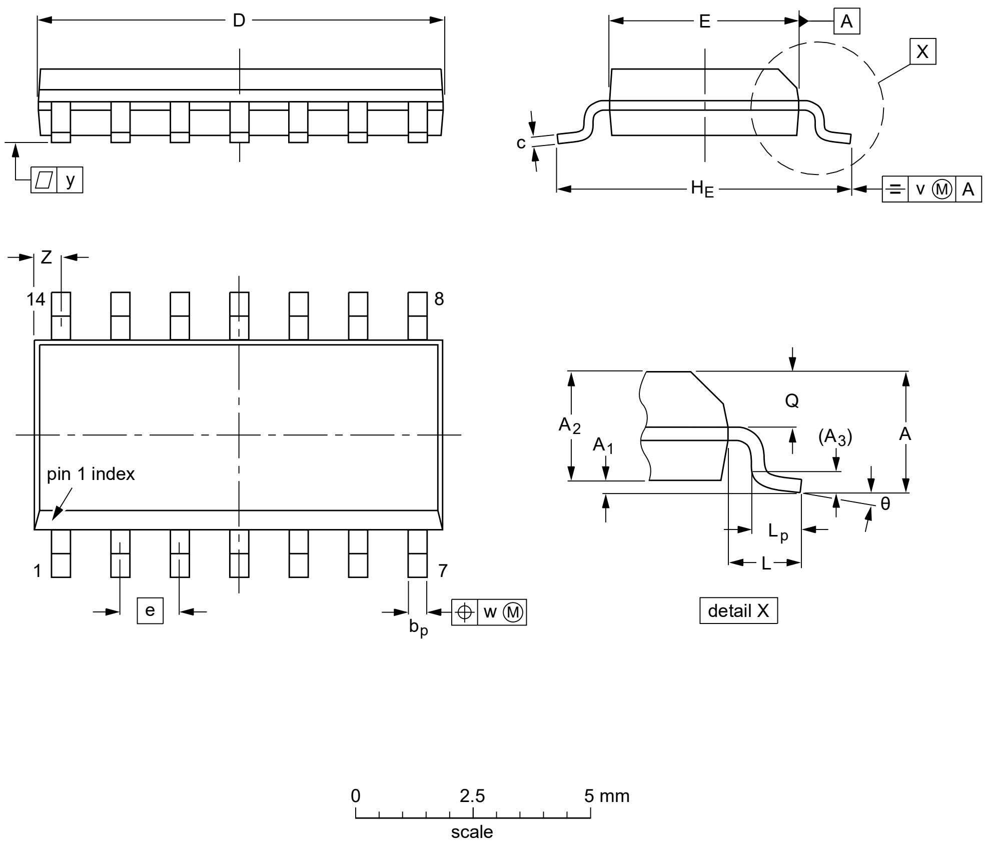


Fig. 9. Modified ring counter; divide-by-(n + 1)

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

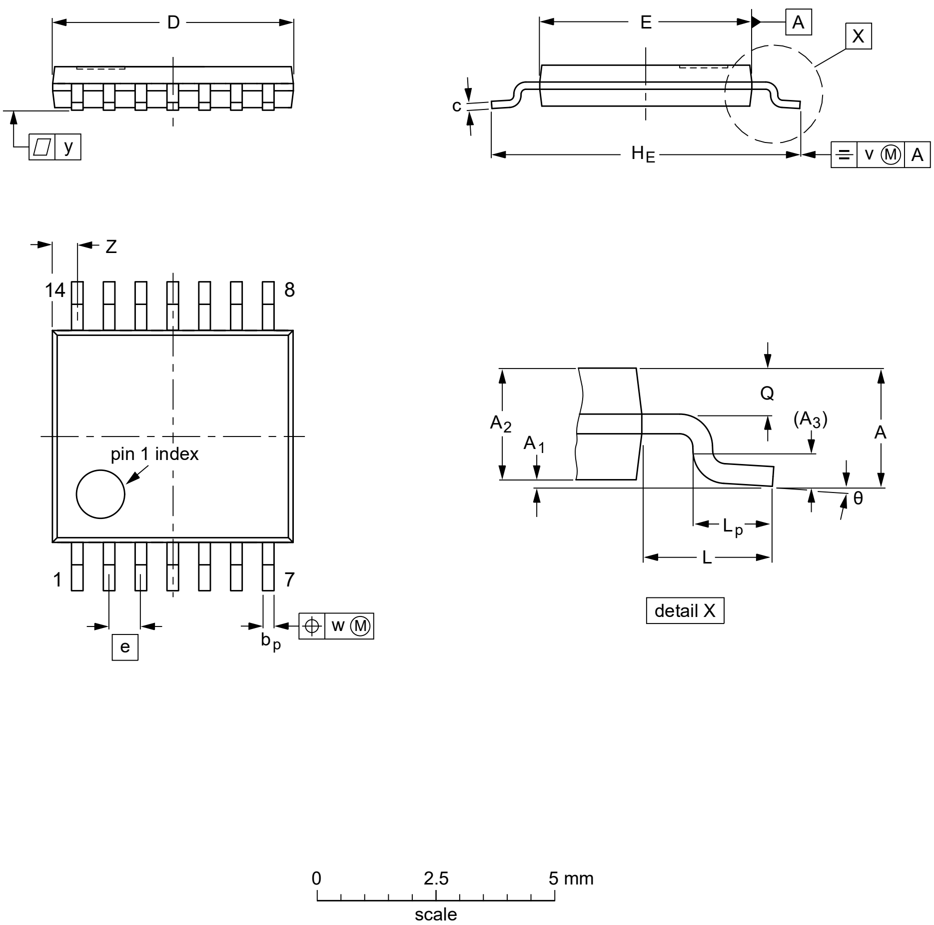
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 11. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4013B_Q100 v.4	20211123	Product data sheet	-	HEF4013B_Q100 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated.			
HEF4013B_Q100 v.3	20151215	Product data sheet	-	HEF4013B_Q100 v.2
Modifications:	• Type number HEF4013BP-Q100 (SOT27-1) removed.			
HEF4013B_Q100 v.2	20130220	Product data sheet	-	HEF4013B_Q100 v.1
Modifications:	• HEF4013BP-Q100 (DIP14) added.			
HEF4013B_Q100 v.1	20120807	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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