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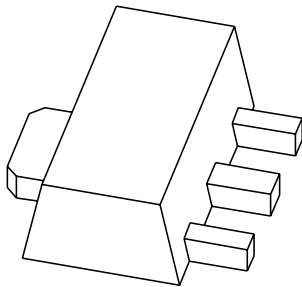
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If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

DATA SHEET



BST60; BST61; BST62 PNP Darlington transistors

Product data sheet
Supersedes data of 2001 Feb 20

2004 Dec 09

PNP Darlington transistors

BST60; BST61; BST62

FEATURES

- High current (max. 0.5 A)
- Low voltage (max. 80 V)
- Integrated diode and resistor.

APPLICATIONS

- Industrial switching applications such as:
 - Print hammer
 - Solenoid
 - Relay and lamp driving.

DESCRIPTION

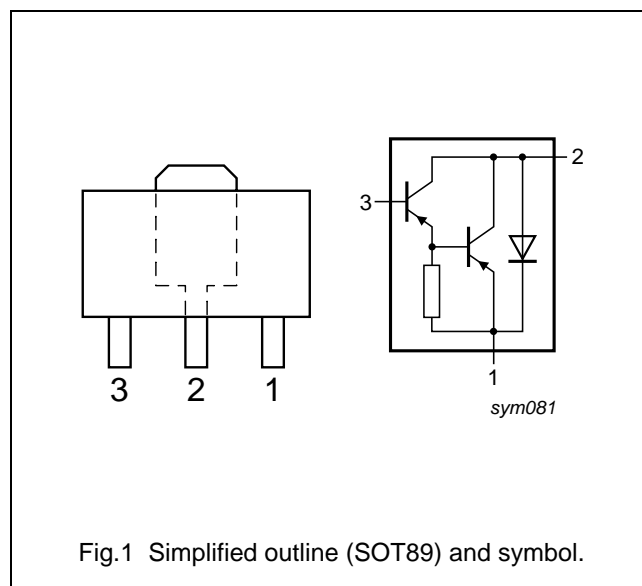
PNP Darlington transistor in a SOT89 plastic package.
NPN complements: BST50, BST51 and BST52.

MARKING

TYPE NUMBER	MARKING CODE
BST60	BS1
BST61	BS2
BST62	BS3

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BST60	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89
BST61			
BST62			

PNP Darlington transistors

BST60; BST61; BST62

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter			
	BST60		–	–60	V
	BST61		–	–80	V
	BST62		–	–90	V
V _{CES}	collector-emitter voltage	V _{BE} = 0 V			
	BST60		–	–45	V
	BST61		–	–60	V
	BST62		–	–80	V
V _{EBO}	emitter-base voltage	open collector	–	–5	V
I _C	collector current (DC)		–	–1	A
I _{CM}	peak collector current		–	–2	A
I _B	base current (DC)		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	1.3	W
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	ambient temperature		–65	+150	°C

Note

- Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm².
For other mounting conditions, see “*Thermal considerations for SOT89 in the General Part of associated Handbook*”.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	note 1	96	K/W
R _{th(j-s)}	thermal resistance from junction to soldering point		16	K/W

Note

- Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm².
For other mounting conditions, see “*Thermal considerations for SOT89 in the General Part of associated Handbook*”.

PNP Darlington transistors

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CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

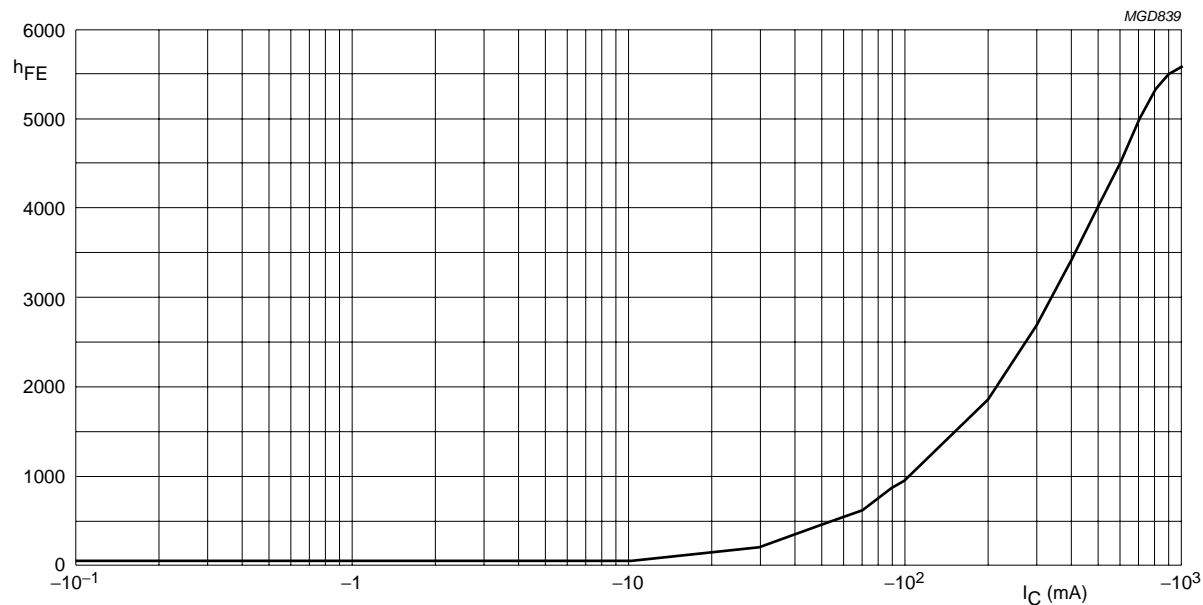
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CES}	collector-emitter cut-off current					
	BST60	$V_{BE} = 0\text{ V}; V_{CE} = -45\text{ V}$	–	–	–50	nA
	BST61	$V_{BE} = 0\text{ V}; V_{CE} = -60\text{ V}$	–	–	–50	nA
	BST62	$V_{BE} = 0\text{ V}; V_{CE} = -80\text{ V}$	–	–	–50	nA
I_{EBO}	emitter-base cut-off current	$I_C = 0\text{ A}; V_{EB} = -4\text{ V}$	–	–	–50	nA
h_{FE}	DC current gain	$V_{CE} = -10\text{ V}$; note 1; see Fig.2				
		$I_C = -150\text{ mA}$	1000	–	–	
		$I_C = -500\text{ mA}$	2000	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}$	–	–	–1.3	V
		$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}; T_j = 150\text{ }^{\circ}\text{C}$	–	–	–1.3	V
V_{BEsat}	base-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -0.5\text{ mA}$	–	–	–1.9	V
f_T	transition frequency	$I_C = -500\text{ mA}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	–	200	–	MHz
Switching times (between 10% and 90% levels); (see Fig.3)						
t_{on}	turn-on time	$I_{Con} = -500\text{ mA}; I_{Bon} = -0.5\text{ mA}; I_{Boff} = 0.5\text{ mA}$	–	500	–	ns
t_{off}	turn-off time		–	700	–	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

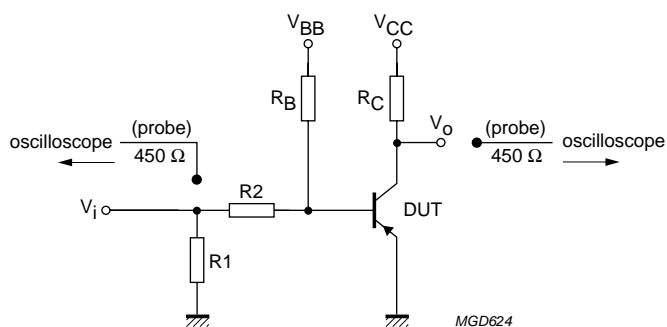
PNP Darlington transistors

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$V_{CE} = -10$ V.

Fig.2 DC current gain; typical values.



$V_i = -10$ V; $T = 200$ μ s; $t_p = 6$ μ s; $t_r = t_f \leq 3$ ns.
 $R_1 = 56$ Ω ; $R_2 = 10$ k Ω ; $R_B = 10$ k Ω ; $R_C = 18$ Ω .
 $V_{BB} = 1.8$ V; $V_{CC} = -10.7$ V.
 Oscilloscope: input impedance $Z_i = 50$ Ω .

Fig.3 Test circuit for switching times.

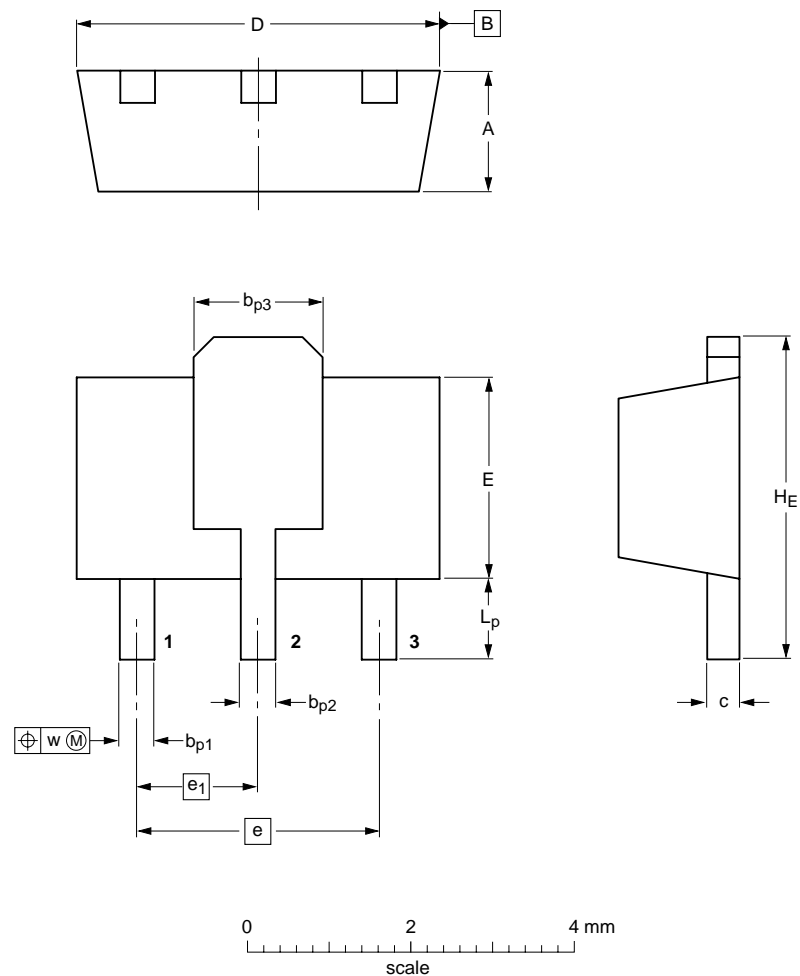
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PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	bp1	bp2	bp3	c	D	E	e	e1	HE	Lp	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			04-08-03 06-03-16

PNP Darlington transistors

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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