

Power Amplifier Module for LTE and 5G

The AFSC5G37E38 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

3600–3800 MHz

- Typical LTE Performance: $P_{out} = 6.3 \text{ W Avg.}$, $V_{DD} = 29 \text{ Vdc}$, $1 \times 20 \text{ MHz LTE}$, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF. (1)

| Carrier Center Frequency | Gain (dB) | ACPR (dBc) | PAE (%) |
|--------------------------|-----------|------------|---------|
| 3610 MHz | 28.2 | -27.5 | 41.5 |
| 3700 MHz | 28.3 | -27.3 | 41.8 |
| 3790 MHz | 28.4 | -26.9 | 41.0 |

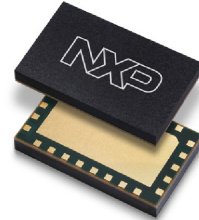
1. All data measured with device soldered in NXP reference circuit.

Features

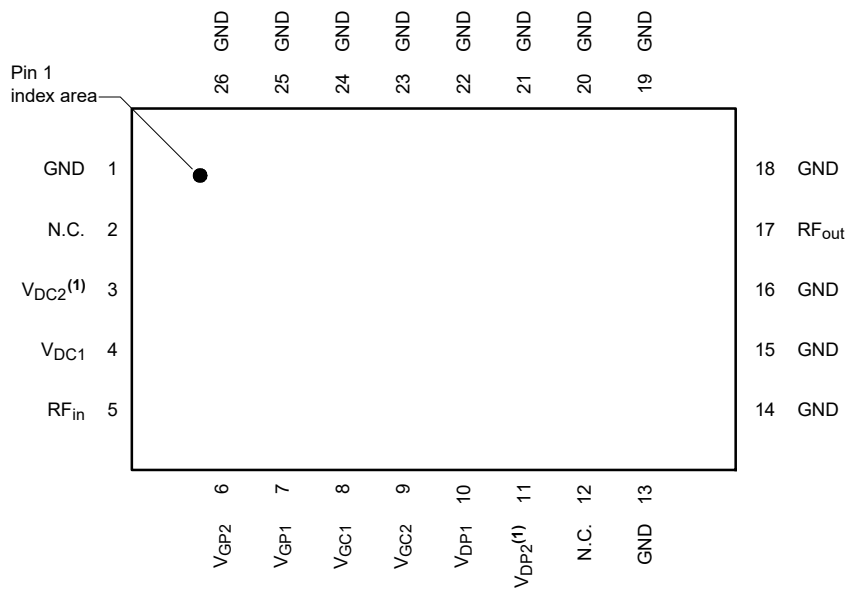
- Frequency: 3600–3800 MHz
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems

AFSC5G37E38

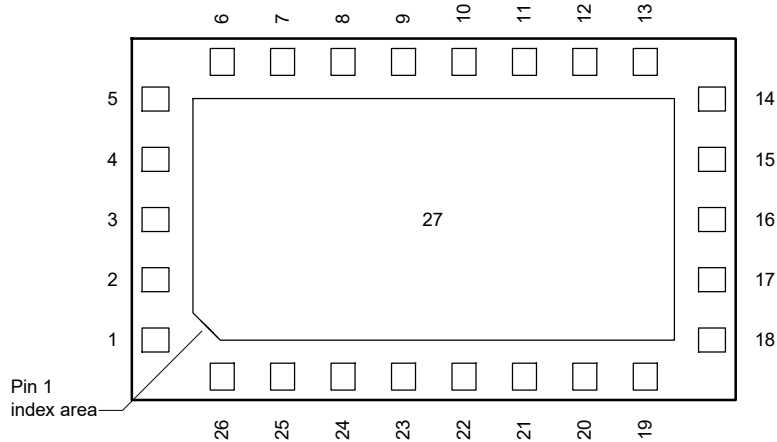
**3600–3800 MHz, 28 dB, 6.3 W Avg.
AIRFAST POWER AMPLIFIER
MODULE**



10 mm × 6 mm Module



(Top View)



(Bottom View)

Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin Connections

1. V_{DC2} and V_{DP2} are DC coupled internal to the package and must be powered by a single DC power supply.

Table 1. Functional Pin Description

| Pin Number | Pin Function | Pin Description |
|---|-------------------|-------------------------------|
| 1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27 | GND | Ground |
| 2, 12 | N.C. | No Connection |
| 3 | V _{DC2} | Carrier Drain Supply, Stage 2 |
| 4 | V _{DC1} | Carrier Drain Supply, Stage 1 |
| 5 | RF _{in} | RF Input |
| 6 | V _{GP2} | Peaking Gate Supply, Stage 2 |
| 7 | V _{GP1} | Peaking Gate Supply, Stage 1 |
| 8 | V _{GC1} | Carrier Gate Supply, Stage 1 |
| 9 | V _{GC2} | Carrier Gate Supply, Stage 2 |
| 10 | V _{DP1} | Peaking Drain Supply, Stage 1 |
| 11 | V _{DP2} | Peaking Drain Supply, Stage 2 |
| 17 | RF _{out} | RF Output |

Table 2. Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|-------------|------|
| Gate-Bias Voltage Range | V_G | -0.5 to +10 | Vdc |
| Operating Voltage Range | V_{DD} | 24 to 30 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Case Operating Temperature | T_C | 125 | °C |
| Peak Input Power (3700 MHz, Pulsed CW, 10 μ sec(on), 10% Duty Cycle) | P_{in} | 25 | dBm |

Table 3. Lifetime

| Characteristic | Symbol | Value | Unit |
|--|--------|-------|-------|
| Mean Time to Failure Case Temperature 125°C, 6.3 W Avg., 30 Vdc | MTTF | > 10 | Years |

Table 4. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|-------|
| Human Body Model (per JS-001-2017) | 1B |
| Charge Device Model (per JS-002-2014) | C3 |

Table 5. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Typ | Range | Unit |
|---|--------------|-----|-----------|------|
| Carrier Stage 1 — On Characteristics | | | | |
| Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10\text{ Vdc}$, $I_D = 1.6\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1.2 | ± 0.4 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 29\text{ Vdc}$, $I_{DQ1A} = 18\text{ mAdc}$) | $V_{GS(Q)}$ | 2.0 | ± 0.4 | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD} = 29\text{ Vdc}$, $I_{DQ1A} = 18\text{ mAdc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 5.3 | ± 1.4 | Vdc |
| Carrier Stage 2 — On Characteristics | | | | |
| Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10\text{ Vdc}$, $I_D = 13.6\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1.2 | ± 0.4 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 29\text{ Vdc}$, $I_{DQ2A} = 58\text{ mAdc}$) | $V_{GS(Q)}$ | 1.8 | ± 0.4 | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD} = 29\text{ Vdc}$, $I_{DQ2A} = 58\text{ mAdc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 3.0 | ± 1.2 | Vdc |
| Peaking Stage 1 — On Characteristics ⁽¹⁾ | | | | |
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1.2 | ± 0.4 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 29\text{ Vdc}$, $I_{DQ1A} = 15\ \mu\text{Adc}$) | $V_{GS(Q)}$ | 1.3 | ± 0.4 | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD} = 29\text{ Vdc}$, $I_{DQ1A} = 15\ \mu\text{Adc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 1.3 | ± 0.4 | Vdc |
| Peaking Stage 2 — On Characteristics ⁽¹⁾ | | | | |
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 27.2\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1.2 | ± 0.4 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 29\text{ Vdc}$, $I_{DQ2A} = 146\ \mu\text{Adc}$) | $V_{GS(Q)}$ | 1.3 | ± 0.4 | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD} = 29\text{ Vdc}$, $I_{DQ2A} = 146\ \mu\text{Adc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 1.3 | ± 0.4 | Vdc |

1. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------------------|------|------------|-----|-------|
| Functional Tests — 3600 MHz ⁽¹⁾ (In NXP Doherty Production ATE ⁽²⁾ Test Fixture, 50 ohm system) $V_{DD} = 29\text{ Vdc}$, $I_{DQ1A} = 18\text{ mA}$, $I_{DQ2A} = 58\text{ mA}$, $V_{GS1B} = (V_t - 0.31)\text{ Vdc}$, $V_{GS2B} = (V_t - 0.3)\text{ Vdc}$, $P_{out} = 6.3\text{ W Avg.}$, 1-tone CW, $f = 3600\text{ MHz}$. | | | | | |
| Gain | G | 25.7 | 27.4 | — | dB |
| Drain Efficiency | η_D | 38.3 | 45.3 | — | % |
| P_{out} @ 3 dB Compression Point | P3dB | 44.9 | 45.6 | — | dBm |
| Functional Tests — 3800 MHz ⁽¹⁾ (In NXP Doherty Production ATE ⁽²⁾ Test Fixture, 50 ohm system) $V_{DD} = 29\text{ Vdc}$, $I_{DQ1A} = 18\text{ mA}$, $I_{DQ2A} = 58\text{ mA}$, $V_{GS1B} = (V_t - 0.31)\text{ Vdc}$, $V_{GS2B} = (V_t - 0.3)\text{ Vdc}$, $P_{out} = 6.3\text{ W Avg.}$, 1-tone CW, $f = 3800\text{ MHz}$. | | | | | |
| Gain | G | 25.4 | 27.3 | — | dB |
| Drain Efficiency | η_D | 32.6 | 37.8 | — | % |
| P_{out} @ 3 dB Compression Point | P3dB | 44.8 | 45.3 | — | dBm |
| Wideband Ruggedness ⁽³⁾ (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) $I_{DQ1A} = 18\text{ mA}$, $I_{DQ2A} = 58\text{ mA}$, $V_{GSP1} = 1.35\text{ Vdc}$, $V_{GSP2} = 1.2\text{ Vdc}$, $f = 3700\text{ MHz}$, Additive White Gaussian Noise (AWGN) with 10 dB PAR | | | | | |
| ISBW of 400 MHz at 30 Vdc, 3 dB Input Overdrive from 6.3 W Avg. Modulated Output Power | No Device Degradation | | | | |
| Typical Performance ⁽³⁾ (In NXP Doherty Power Amplifier Module Reference Circuit, 50 ohm system) $V_{DD} = 29\text{ Vdc}$, $I_{DQ1A} = 18\text{ mA}$, $I_{DQ2A} = 58\text{ mA}$, $V_{GSP1} = 1.35\text{ Vdc}$, $V_{GSP2} = 1.2\text{ Vdc}$, $P_{out} = 6.3\text{ W Avg.}$, 3700 MHz | | | | | |
| VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point) | VBW _{res} | — | 210 | — | MHz |
| Quiescent Current Accuracy over Temperature ⁽⁴⁾ with 2.2 k Ω Gate Feed Resistors (–40 to 85°C) Stage 1 with 2.2 k Ω Gate Feed Resistors (–40 to 85°C) Stage 2 | ΔI_{QT} | — | 1.0 2.0 | — | % |
| 1-carrier 20 MHz LTE, 8 dB Input Signal PAR | | | | | |
| Gain | G | — | 28.3 | — | dB |
| Power Added Efficiency | PAE | — | 41.8 | — | % |
| Adjacent Channel Power Ratio | ACPR | — | –27.3 | — | dBc |
| Adjacent Channel Power Ratio | ALT1 | — | –42.0 | — | dBc |
| Adjacent Channel Power Ratio | ALT2 | — | –50.8 | — | dBc |
| Gain Flatness ⁽⁵⁾ | G_F | — | 0.3 | — | dB |
| Fast CW, 27 ms Sweep | | | | | |
| P_{out} @ 3 dB Compression Point | P3dB | — | 45.5 | — | dBm |
| AM/PM @ P3dB | Φ | — | –23 | — | ° |
| Gain Variation @ Avg. Power over Temperature (–40°C to +105°C) | ΔG | — | 0.036 | — | dB/°C |
| P3dB Variation over Temperature (–40°C to +105°C) | P3dB | — | 0.011 | — | dB/°C |

Table 7. Ordering Information

| Device | Tape and Reel Information | Package |
|---------------|---|---------------------|
| AFSC5G37E38T2 | T2 Suffix = 2,000 Units, 24 mm Tape Width, 13-inch Reel | 10 mm × 6 mm Module |

- Part input and output matched to 50 ohms.
- ATE is a socketed test environment.
- All data measured in fixture with device soldered in NXP reference circuit.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.
- Gain flatness = $\text{Max}(G(f_{Low} \text{ to } f_{High})) - \text{Min}(G(f_{Low} \text{ to } f_{High}))$

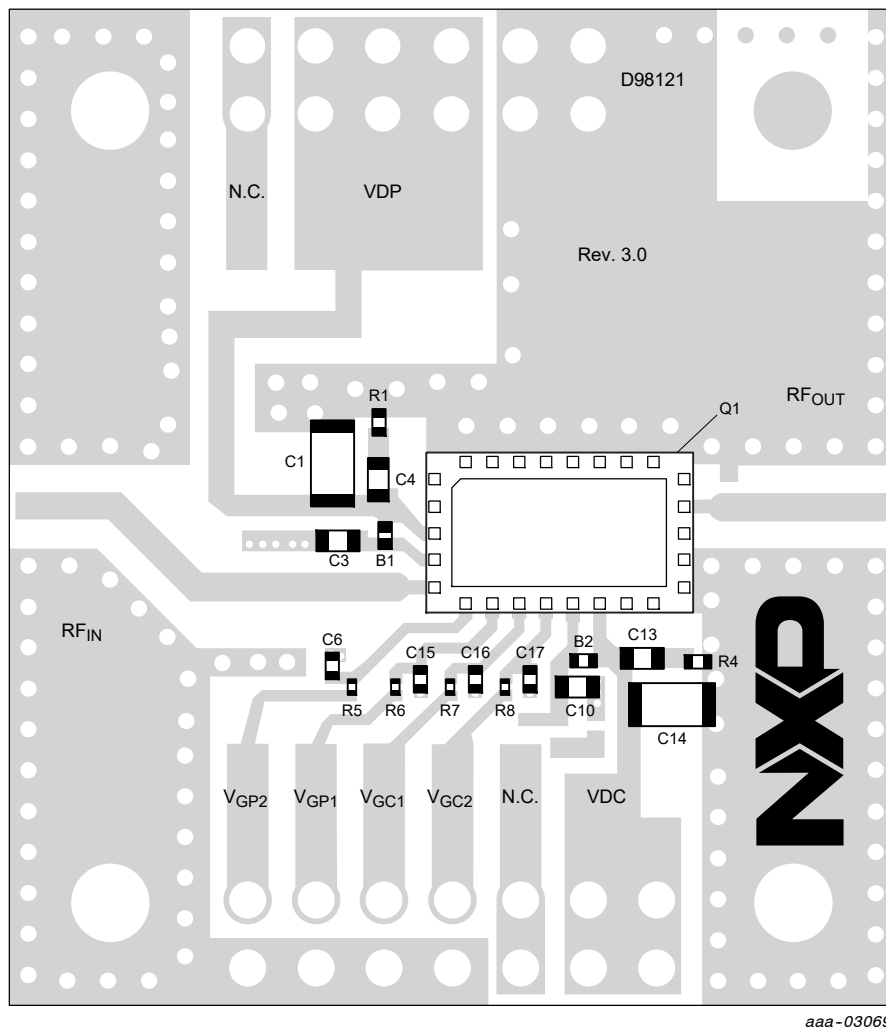


Figure 2. AFSC5G37E38 Reference Circuit Component Layout

Table 8. AFSC5G37E38 Reference Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|-------------------|---|-------------------|--------------|
| B1, B2 | 30 Ω Ferrite Bead | BLM15PD300SN1 | Murata |
| C1, C14 | 10 μ F Chip Capacitor | CL31A106KBHNNNE | Samsung |
| C3, C4, C10, C13 | 1 μ F Chip Capacitor | 06035D105KAT2A | AVX |
| C6, C15, C16, C17 | 0.1 μ F Chip Capacitor | GRM155R61H104KE14 | Murata |
| Q1 | Power Amplifier Module | AFSC5G37E38 | NXP |
| R1, R4 | 5.1 Ω , 1/10 W Chip Resistor | ERJ-2GEJ5R1X | Panasonic |
| R5, R6, R7, R8 | 2.2 k Ω , 1/20 W Chip Resistor | ERJ-1GNJ222C | Panasonic |
| PCB | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D98121 | MTL |

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.

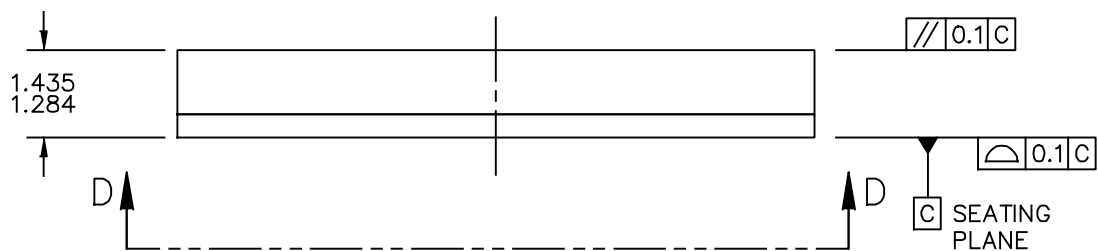
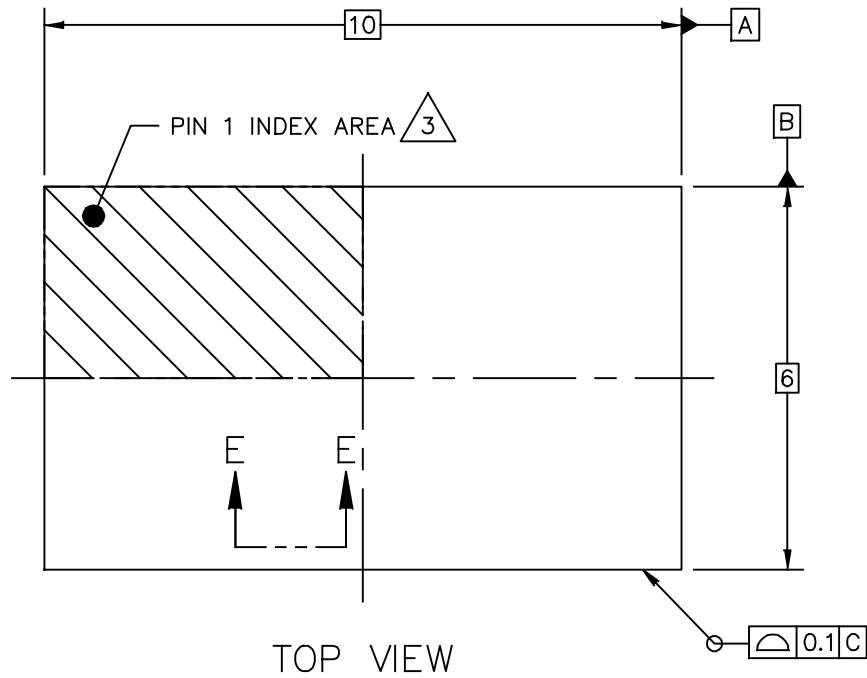


Figure 3. Product Marking

PACKAGE INFORMATION

H-PLGA-27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2

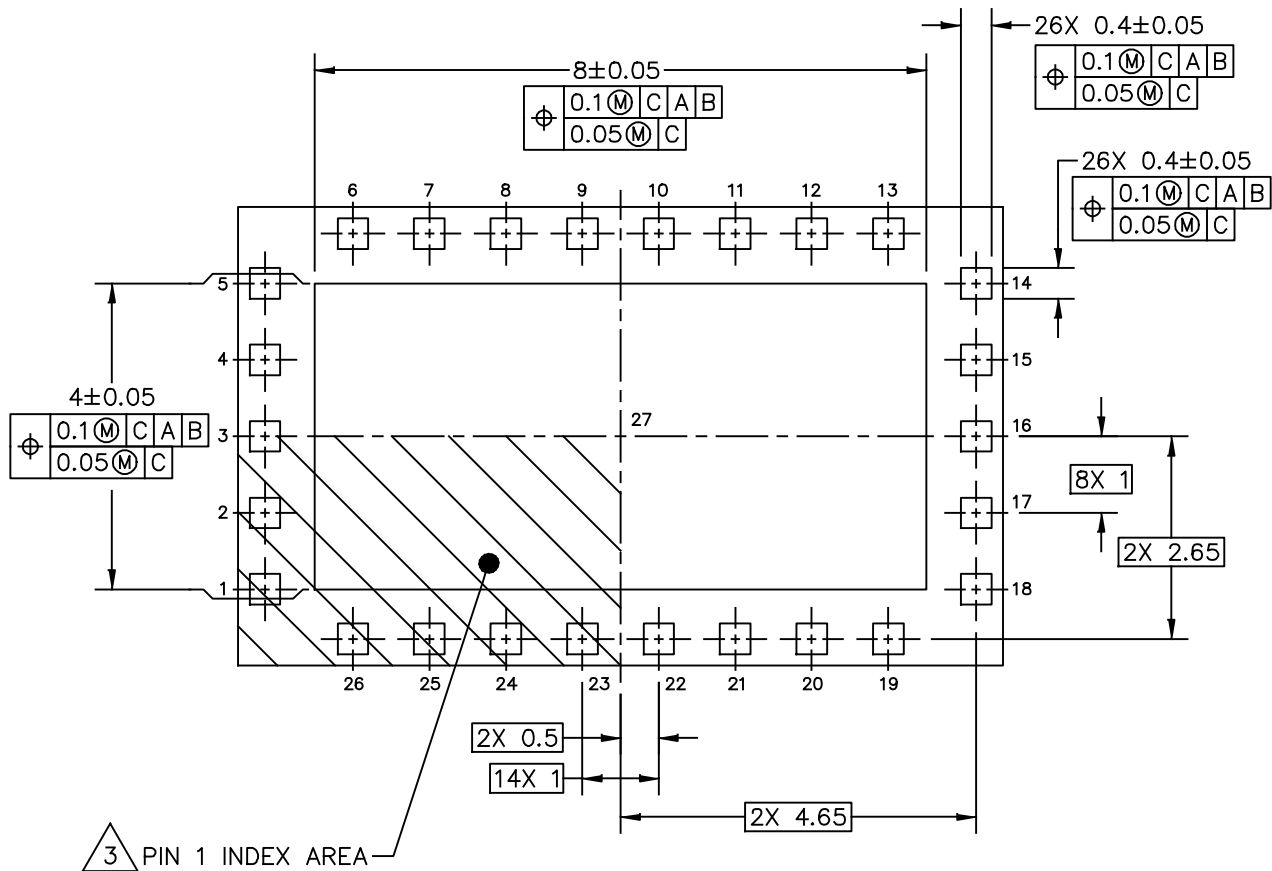


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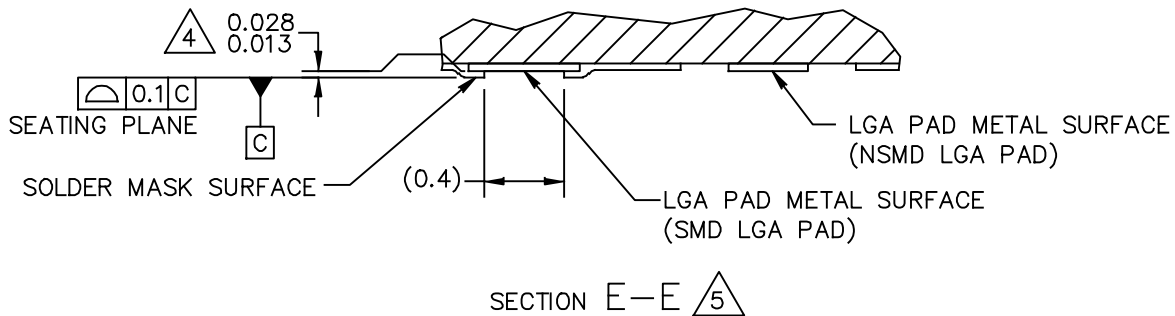
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AFSC5G37E38



VIEW D-D
 (BOTTOM VIEW)

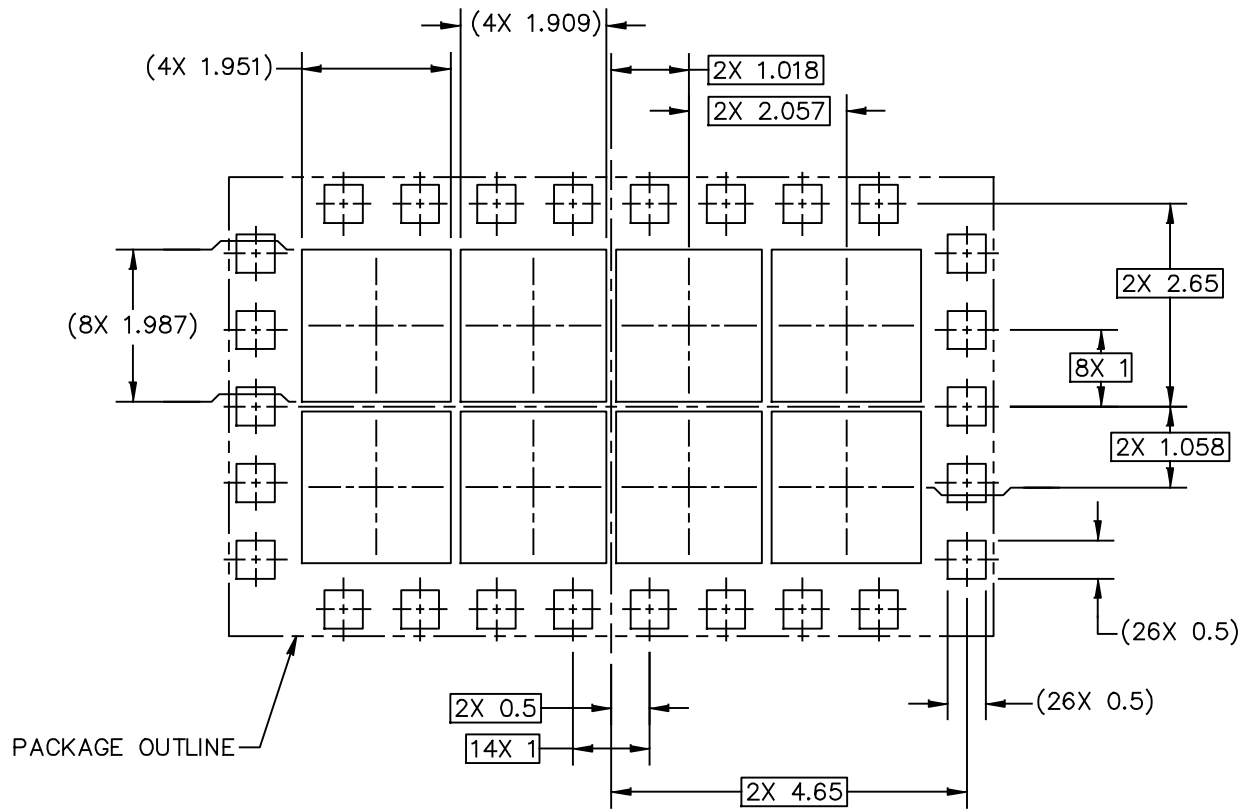


SECTION E-E 5

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PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

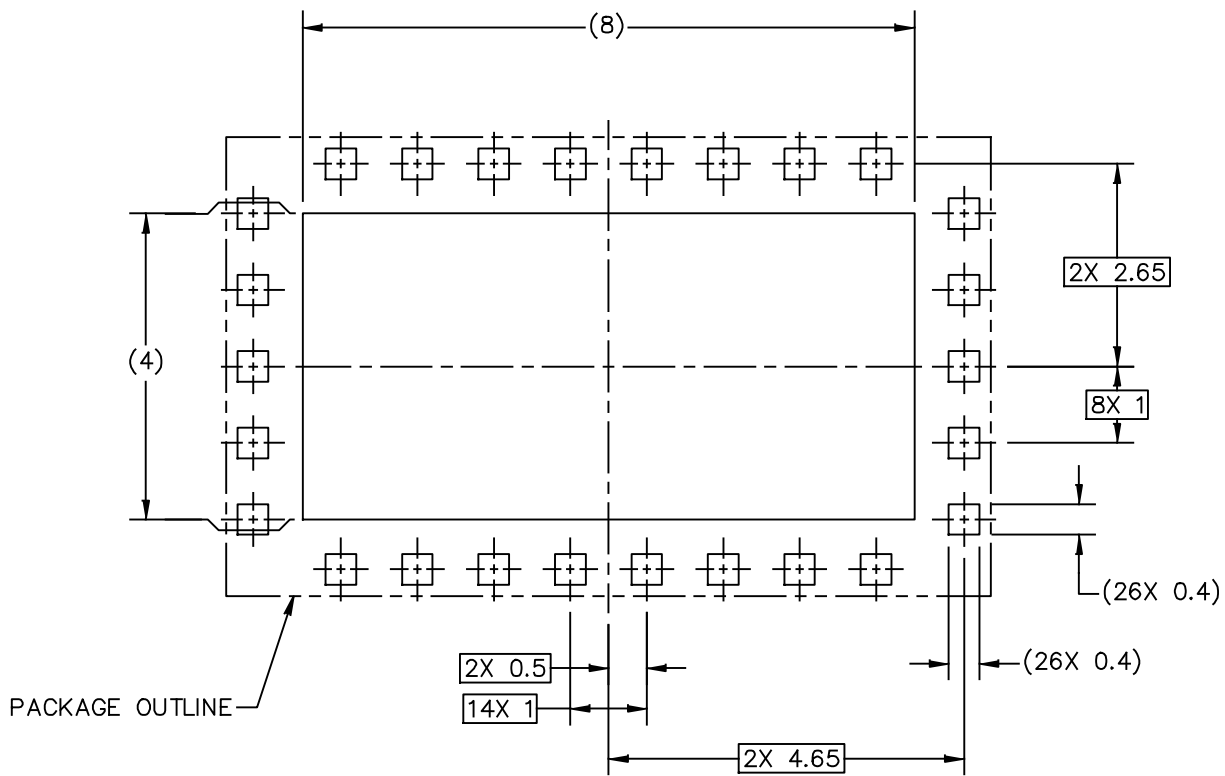
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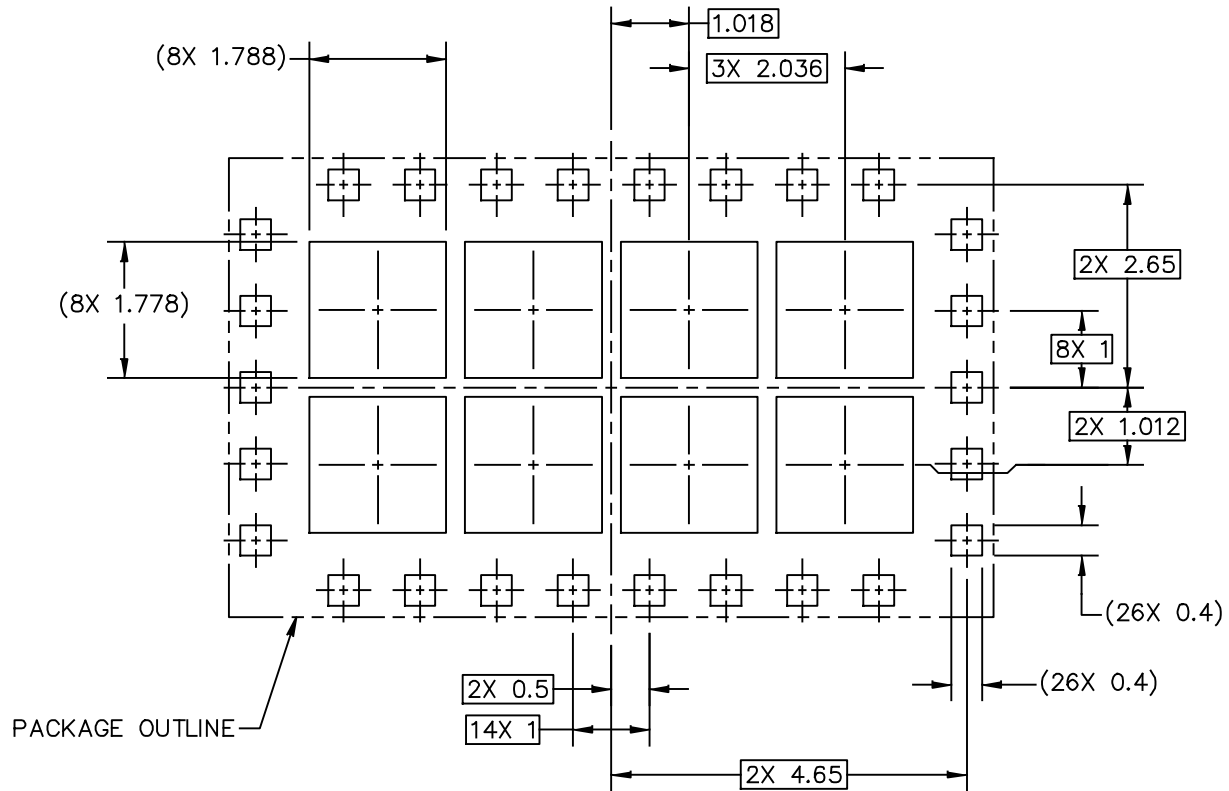
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RECOMMENDED STENCIL THICKNESS 0.125

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AFSC5G37E38

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON-SOLDERMASK DEFINED (NSMD).

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PRODUCT DOCUMENTATION AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Development Tools

- Printed Circuit Boards

FAILURE ANALYSIS

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|---------------------------------|
| 0 | Aug. 2020 | • Initial release of data sheet |

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