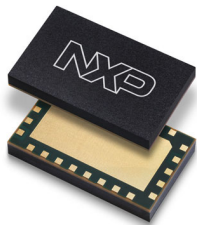


# AFSC5G35E38

## Airfast Power Amplifier Module

Rev. 2 — 14 June 2024

Product data sheet



## 1 General description

The AFSC5G35E38 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

## 2 Typical performance

**Table 1. 3400–3600 MHz — Typical LTE Performance**

$P_{out} = 7\text{ W Avg.}$ ,  $V_{DD} = 30\text{ Vdc}$ ,  $1 \times 20\text{ MHz LTE}$ ,  $\text{Input Signal PAR} = 8\text{ dB @ } 0.01\% \text{ Probability on CCDF. }^{(1)}$

| Carrier Center Frequency | Gain (dB) | ACPR (dBc) | PAE (%) |
|--------------------------|-----------|------------|---------|
| 3410 MHz                 | 30.4      | –30.0      | 43.0    |
| 3500 MHz                 | 30.8      | –28.0      | 42.0    |
| 3590 MHz                 | 31.1      | –29.0      | 41.0    |

1. All data measured with device soldered in NXP reference circuit.

## 3 Features and benefits

- Frequency: 3400–3700 MHz
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems



4 Pinning information

4.1 Pinning

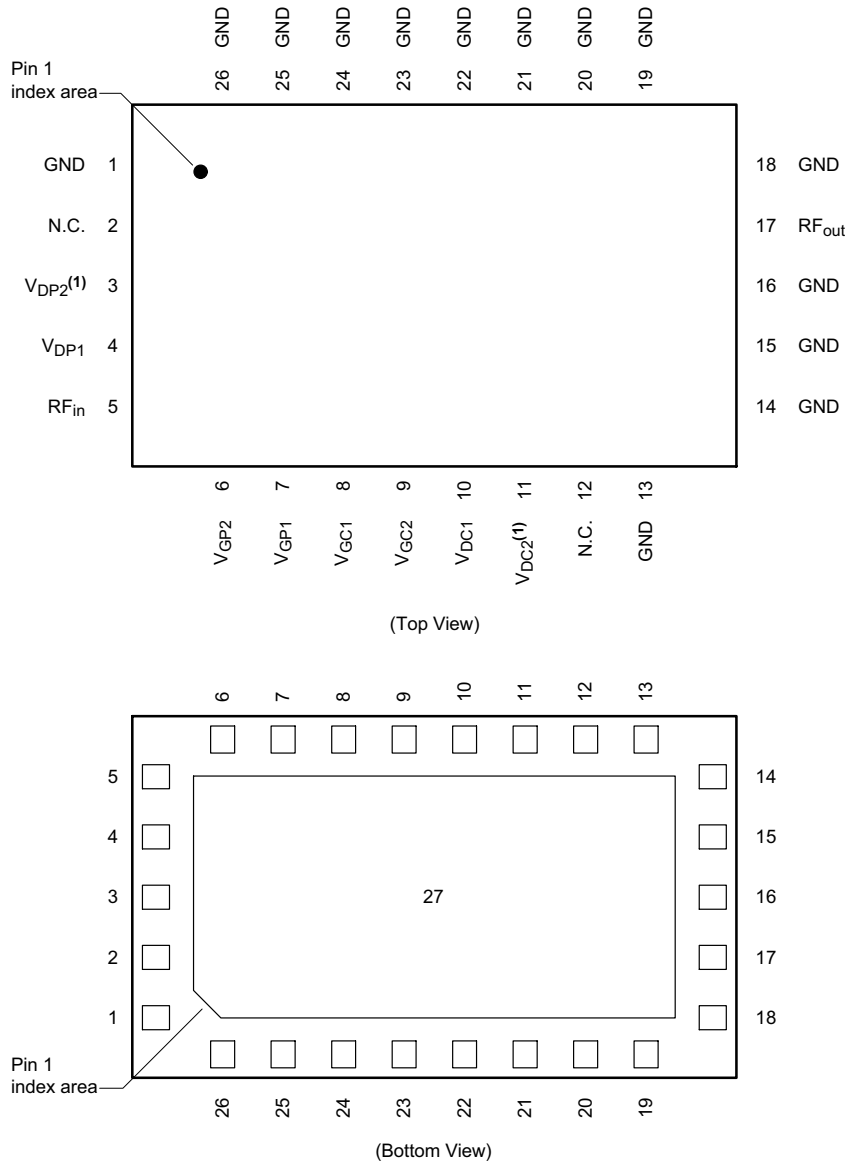


Figure 1. Pin Connections

1.  $V_{DP2}$  and  $V_{DC2}$  are DC coupled internal to the package and must be powered by a single DC power supply.

4.2 Functional pin description

Table 2. Functional Pin Description

| Pin Number  | Pin Function      | Pin Description               |
|---|-------------------|-------------------------------|
| 1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27 | GND               | Ground                        |
| 2, 12   | N.C.              | No Connection                 |
| 3   | V <sub>DP2</sub>  | Peaking Drain Supply, Stage 2 |
| 4   | V <sub>DP1</sub>  | Peaking Drain Supply, Stage 1 |
| 5   | RF <sub>in</sub>  | RF Input                      |
| 6   | V <sub>GP2</sub>  | Peaking Gate Supply, Stage 2  |
| 7   | V <sub>GP1</sub>  | Peaking Gate Supply, Stage 1  |
| 8   | V <sub>GC1</sub>  | Carrier Gate Supply, Stage 1  |
| 9   | V <sub>GC2</sub>  | Carrier Gate Supply, Stage 2  |
| 10  | V <sub>DC1</sub>  | Carrier Drain Supply, Stage 1 |
| 11  | V <sub>DC2</sub>  | Carrier Drain Supply, Stage 2 |
| 17  | RF <sub>out</sub> | RF Output                     |

5 Maximum ratings

Table 3. Maximum Ratings

| Rating   | Symbol           | Value       | Unit |
|--|------------------|-------------|------|
| Gate–Bias Voltage Range  | V <sub>G</sub>   | –0.5 to +10 | Vdc  |
| Operating Voltage Range  | V <sub>DD</sub>  | 24 to 31    | Vdc  |
| Storage Temperature Range  | T <sub>stg</sub> | –65 to +150 | °C   |
| Case Operating Temperature   | T <sub>C</sub>   | 125         | °C   |
| Peak Input Power<br>(3500 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle) | P <sub>in</sub>  | 25          | dBm  |

6 Lifetime

Table 4. Lifetime

| Characteristic   | Symbol | Value | Unit  |
|--|--------|-------|-------|
| Mean Time to Failure<br>Case Temperature 125°C, 7 W Avg., 31 Vdc | MTTF   | >10   | Years |

7 ESD protection characteristics

Table 5. ESD Protection Characteristics

| Test Methodology                      | Class |
|---------------------------------------|-------|
| Human Body Model (per JS–001–2017)    | 1A    |
| Charge Device Model (per JS–002–2014) | C2a   |

8 Moisture sensitivity level

Table 6. Moisture Sensitivity Level

| Test Methodology                     | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22–A113, IPC/JEDEC J–STD–020 | 3      | 260                      | °C   |

## 9 Electrical characteristics

### 9.1 DC characteristics

**Table 7. DC Characteristics**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Characteristic  | Symbol       | Typ | Range     | Unit |
|---|--------------|-----|-----------|------|
| <b>Carrier Stage 1 — On Characteristics</b>   |              |     |           |      |
| Gate Threshold Voltage <sup>(1)</sup><br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 1.2\text{ }\mu\text{Adc}$ )                            | $V_{GS(th)}$ | 1.2 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 30\text{ Vdc}$ , $I_{DQ1A} = 12\text{ mAdc}$ )  | $V_{GS(Q)}$  | 1.9 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage<br>( $V_{DD} = 30\text{ Vdc}$ , $I_{DQ1A} = 12\text{ mAdc}$ , Measured in Functional Test)           | $V_{GG(Q)}$  | 5.0 | $\pm 1.4$ | Vdc  |
| <b>Carrier Stage 2 — On Characteristics</b>   |              |     |           |      |
| Gate Threshold Voltage <sup>(1)</sup><br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 12.8\text{ }\mu\text{Adc}$ )                           | $V_{GS(th)}$ | 1.2 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 30\text{ Vdc}$ , $I_{DQ2A} = 47\text{ mAdc}$ )  | $V_{GS(Q)}$  | 1.8 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage<br>( $V_{DD} = 30\text{ Vdc}$ , $I_{DQ2A} = 47\text{ mAdc}$ , Measured in Functional Test)           | $V_{GG(Q)}$  | 2.8 | $\pm 1.2$ | Vdc  |
| <b>Peaking Stage 1 — On Characteristics <sup>(1)</sup></b>  |              |     |           |      |
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 1.6\text{ }\mu\text{Adc}$ )   | $V_{GS(th)}$ | 1.2 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 30\text{ Vdc}$ , $I_{DQ1A} = 1.7\text{ }\mu\text{Adc}$ )                                      | $V_{GS(Q)}$  | 1.2 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage<br>( $V_{DD} = 30\text{ Vdc}$ , $I_{DQ1A} = 1.7\text{ }\mu\text{Adc}$ , Measured in Functional Test) | $V_{GG(Q)}$  | 1.2 | $\pm 0.4$ | Vdc  |
| <b>Peaking Stage 2 — On Characteristics <sup>(1)</sup></b>  |              |     |           |      |
| Gate Threshold Voltage<br>( $V_{DS} = 10\text{ Vdc}$ , $I_D = 27.2\text{ }\mu\text{Adc}$ )  | $V_{GS(th)}$ | 1.2 | $\pm 0.4$ | Vdc  |
| Gate Quiescent Voltage<br>( $V_{DS} = 30\text{ Vdc}$ , $I_{DQ2A} = 1.3\text{ }\mu\text{Adc}$ )                                      | $V_{GS(Q)}$  | 1.2 | $\pm 0.4$ | Vdc  |
| Fixture Gate Quiescent Voltage<br>( $V_{DD} = 30\text{ Vdc}$ , $I_{DQ2A} = 1.3\text{ }\mu\text{Adc}$ , Measured in Functional Test) | $V_{GG(Q)}$  | 1.2 | $\pm 0.4$ | Vdc  |

1. Each side of device measured separately.

## 9.2 Functional tests

**Table 8. Functional Tests — 3400 MHz <sup>(1)</sup>**

(In NXP Doherty Production ATE <sup>(2)</sup> Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $V_{DD} = 30\text{ Vdc}$ ,  $I_{DQ1A} = 12\text{ mA}$ ,  $I_{DQ2A} = 47\text{ mA}$ ,  $V_{GS1B} = (V_t - 0.31)\text{ Vdc}$ ,  $V_{GS2B} = (V_t - 0.30)\text{ Vdc}$ ,  $P_{out} = 7\text{ W Avg.}$ , 1-tone CW,  $f = 3400\text{ MHz}$ .

| Characteristic   | Symbol   | Min  | Typ  | Max | Unit |
|--|----------|------|------|-----|------|
| Gain   | G        | 29.0 | 30.1 | —   | dB   |
| Drain Efficiency   | $\eta_D$ | 38.0 | 43.0 | —   | %    |
| $P_{out}$ @ 3 dB Compression Point<br>(Pulsed CW, 5% Duty Cycle) | P3dB     | 43.7 | 44.8 | —   | dBm  |

**Table 9. Functional Tests — 3600 MHz <sup>(1)</sup>**

(In NXP Doherty Production ATE <sup>(2)</sup> Test Fixture,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $V_{DD} = 30\text{ Vdc}$ ,  $I_{DQ1A} = 12\text{ mA}$ ,  $I_{DQ2A} = 47\text{ mA}$ ,  $V_{GS1B} = (V_t - 0.31)\text{ Vdc}$ ,  $V_{GS2B} = (V_t - 0.30)\text{ Vdc}$ ,  $P_{out} = 7\text{ W Avg.}$ , 1-tone CW,  $f = 3600\text{ MHz}$ .

| Characteristic   | Symbol   | Min  | Typ  | Max | Unit |
|--|----------|------|------|-----|------|
| Gain   | G        | 29.3 | 30.5 | —   | dB   |
| Drain Efficiency   | $\eta_D$ | 38.0 | 43.1 | —   | %    |
| $P_{out}$ @ 3 dB Compression Point<br>(Pulsed CW, 5% Duty Cycle) | P3dB     | 44.7 | 45.7 | —   | dBm  |

## 9.3 Wideband ruggedness

**Table 10. Wideband Ruggedness <sup>(3)</sup>**

(In NXP Doherty Power Amplifier Module Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $I_{DQ1A} = 12\text{ mA}$ ,  $I_{DQ2A} = 47\text{ mA}$ ,  $V_{GSP1} = 1.20\text{ Vdc}$ ,  $V_{GSP2} = 1.16\text{ Vdc}$ ,  $f = 3500\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR

| Characteristic  | Test Results          |
|---|-----------------------|
| ISBW of 400 MHz at 31 Vdc, 3 dB Input Overdrive from 7 W Avg.<br>Modulated Output Power | No Device Degradation |

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. All data measured in fixture with device soldered in NXP reference circuit.

## 9.4 Typical performance

**Table 11. Typical Performance <sup>(1)</sup>**

(In NXP Doherty Power Amplifier Module Reference Circuit,  $T_A = 25^\circ\text{C}$  unless otherwise noted, 50 ohm system)  $V_{DD} = 30\text{ Vdc}$ ,  $I_{DQ1A} = 12\text{ mA}$ ,  $I_{DQ2A} = 47\text{ mA}$ ,  $V_{GSP1} = 1.20\text{ Vdc}$ ,  $V_{GSP2} = 1.16\text{ Vdc}$ ,  $P_{out} = 7\text{ W Avg.}$ , 3500 MHz

| Characteristic   | Symbol             | Min    | Typ        | Max    | Unit  |
|--|--------------------|--------|------------|--------|-------|
| VBW Resonance Point, 2-tone, 1 MHz Tone Spacing<br>(IMD Third Order Intermodulation Inflection Point)  | VBW <sub>res</sub> | —      | 190        | —      | MHz   |
| Quiescent Current Accuracy over Temperature <sup>(2)</sup><br>with 2.2 k $\Omega$ Gate Feed Resistors (–40 to 85°C) Stage 1<br>with 2.2 k $\Omega$ Gate Feed Resistors (–40 to 85°C) Stage 2 | $\Delta I_{QT}$    | —<br>— | 1.0<br>2.0 | —<br>— | %     |
| <b>1-carrier 20 MHz LTE, 8 dB Input Signal PAR</b>   |                    |        |            |        |       |
| Gain   | G                  | —      | 30.8       | —      | dB    |
| Power Added Efficiency   | PAE                | —      | 42.0       | —      | %     |
| Adjacent Channel Power Ratio   | ACPR               | —      | –28.0      | —      | dBc   |
| Adjacent Channel Power Ratio   | ALT1               | —      | –42.0      | —      | dBc   |
| Adjacent Channel Power Ratio   | ALT2               | —      | –52.0      | —      | dBc   |
| Gain Flatness <sup>(3)</sup>   | G <sub>F</sub>     | —      | 0.7        | —      | dB    |
| <b>Fast CW, 27 ms Sweep</b>  |                    |        |            |        |       |
| P <sub>out</sub> @ 3 dB Compression Point  | P3dB               | —      | 46.0       | —      | dBm   |
| AM/PM @ P3dB   | $\Phi$             | —      | –20        | —      | °     |
| Gain Variation @ Avg. Power over Temperature<br>(–40°C to +105°C)  | $\Delta G$         | —      | 0.032      | —      | dB/°C |
| P3dB Variation over Temperature<br>(–40°C to +105°C)   | P3dB               | —      | 0.012      | —      | dB/°C |

## 10 Ordering information

**Table 12. Ordering Information**

| Device        | Tape and Reel Information                               | Package             |
|---------------|---|---------------------|
| AFSC5G35E38T2 | T2 Suffix = 2,000 Units, 24 mm Tape Width, 13–inch Reel | 10 mm × 6 mm Module |

- All data measured in fixture with device soldered in NXP reference circuit.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.
- Gain flatness =  $\text{Max}(G(f_{\text{Low}} \text{ to } f_{\text{High}})) - \text{Min}(G(f_{\text{Low}} \text{ to } f_{\text{High}}))$

11 Component layout and parts list

11.1 Component layout

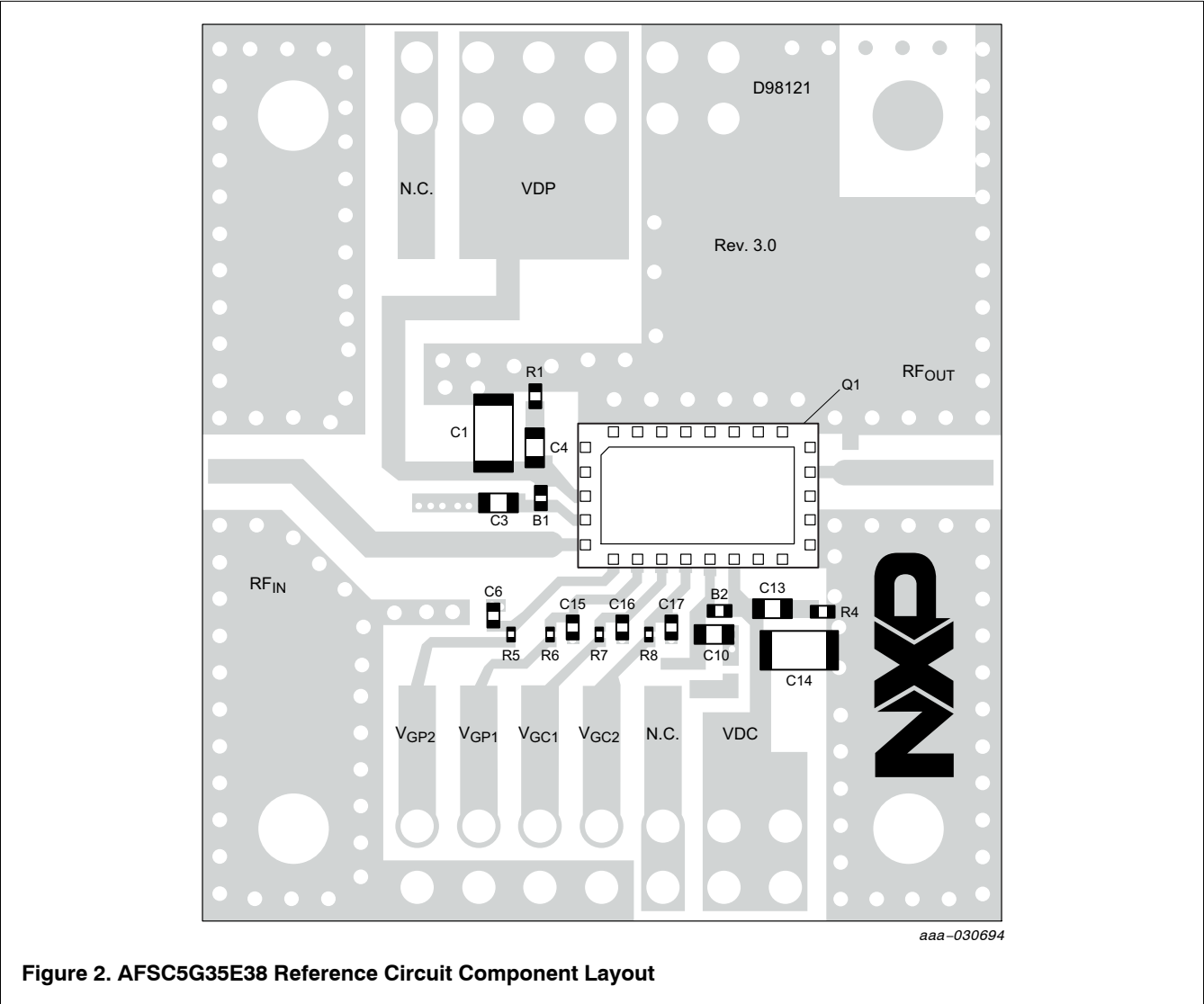


Figure 2. AFSC5G35E38 Reference Circuit Component Layout

11.2 Component designations and values

Table 13. AFSC5G35E38 Reference Circuit Component Designations and Values

| Part              | Description                                 | Part Number       | Manufacturer |
|-------------------|---|-------------------|--------------|
| B1, B2            | 30 $\Omega$ Ferrite Bead                    | BLM15PD300SN1     | Murata       |
| C1, C14           | 10 $\mu$ F Chip Capacitor                   | CL31A106KBHNNNE   | Samsung      |
| C3, C4, C10, C13  | 1 $\mu$ F Chip Capacitor                    | 06035D105KAT2A    | AVX          |
| C6, C15, C16, C17 | 0.1 $\mu$ F Chip Capacitor                  | GRM155R61H104KE14 | Murata       |
| Q1                | Power Amplifier Module                      | AFSC5G35E38       | NXP          |
| R1, R4            | 5.1 $\Omega$ , 1/10 W Chip Resistor         | ERJ-2GEJ5R1X      | Panasonic    |
| R5, R6, R7, R8    | 2.2 k $\Omega$ , 1/20 W Chip Resistor       | ERJ-1GNJ222C      | Panasonic    |
| PCB               | Rogers RO4350B, 0.020", $\epsilon_r = 3.66$ | D98121            | MTL          |

Note: Component numbers C2, C5, C7, C8, C9, C11, C12, R2 and R3 are intentionally omitted.



12 Product marking

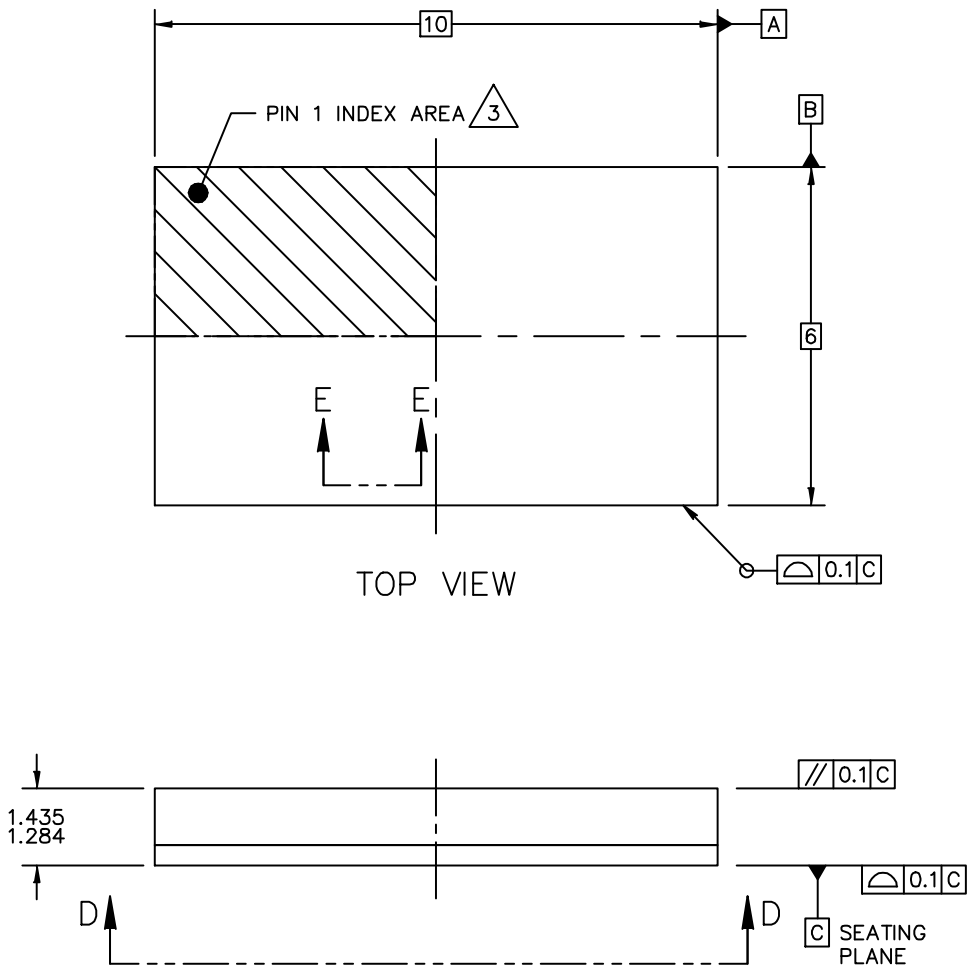


Figure 3. Product Marking

13 Package information

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

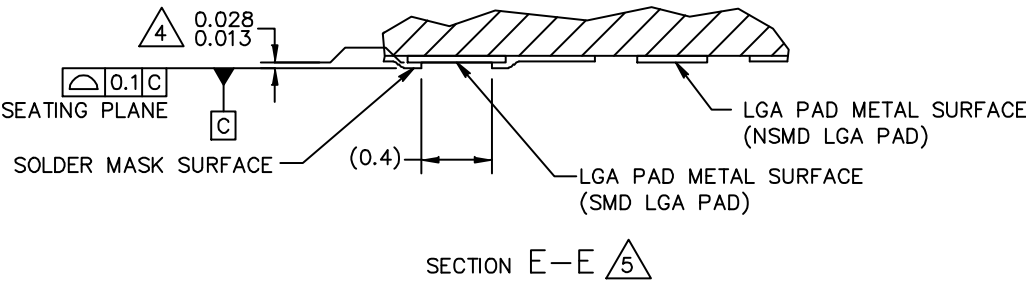
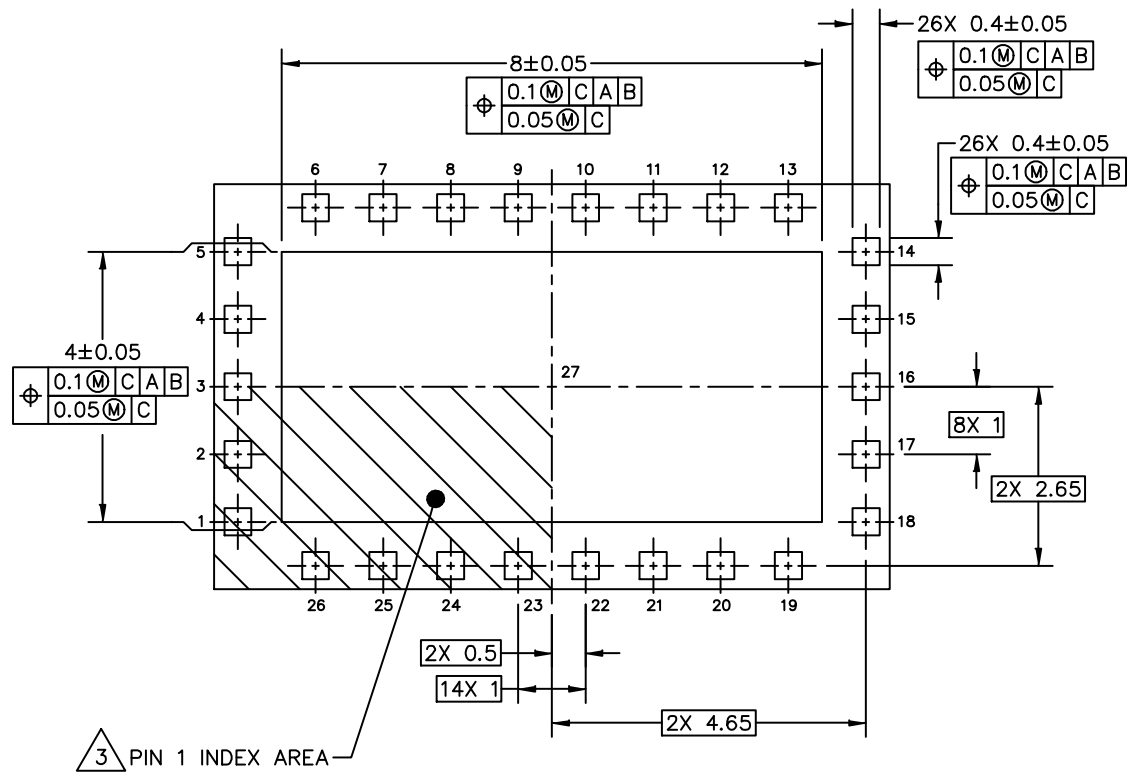
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10 X 6 X 1.365 PKG, 1 PITCH

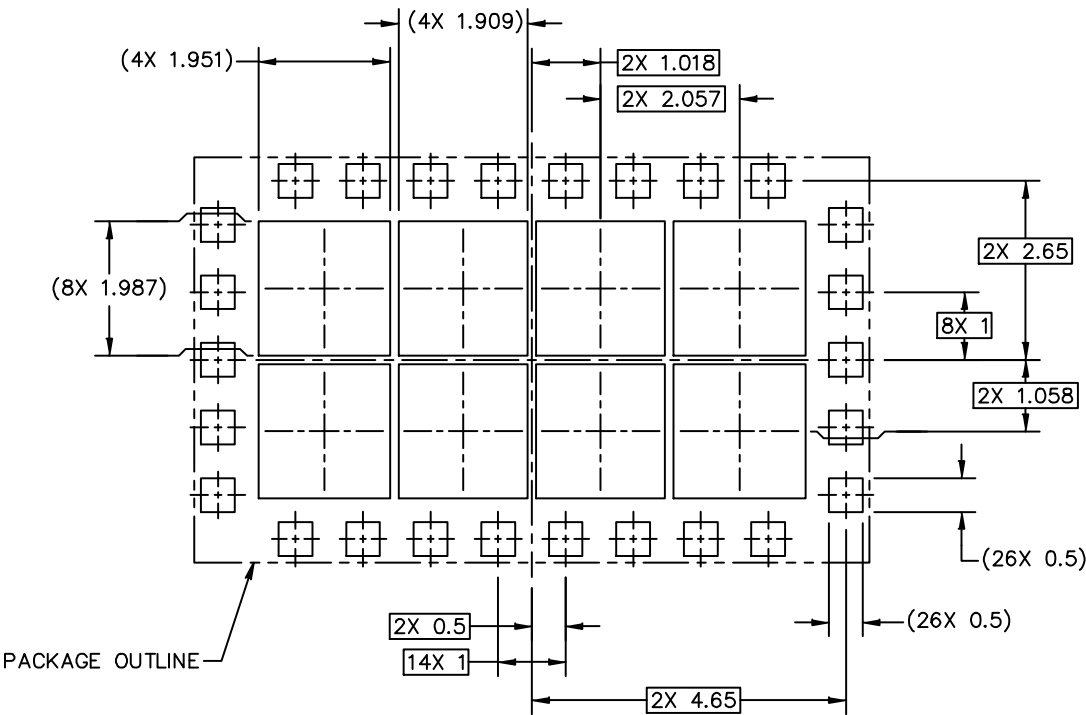
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H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

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PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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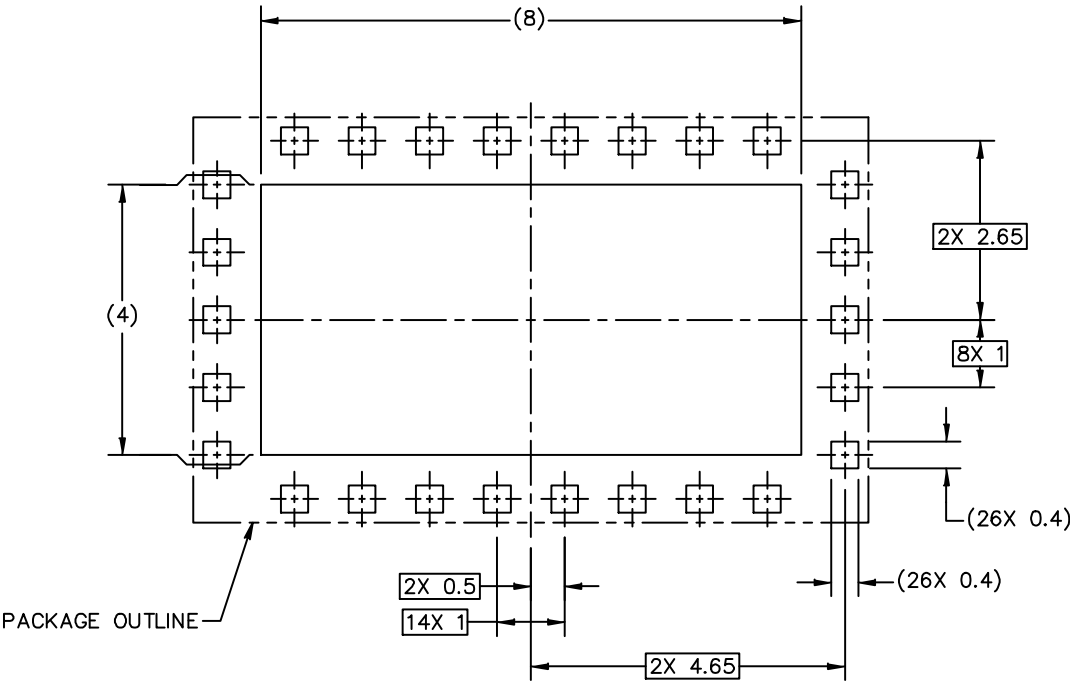
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|--|------------------------|--------------------------------|----------------|------------|

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



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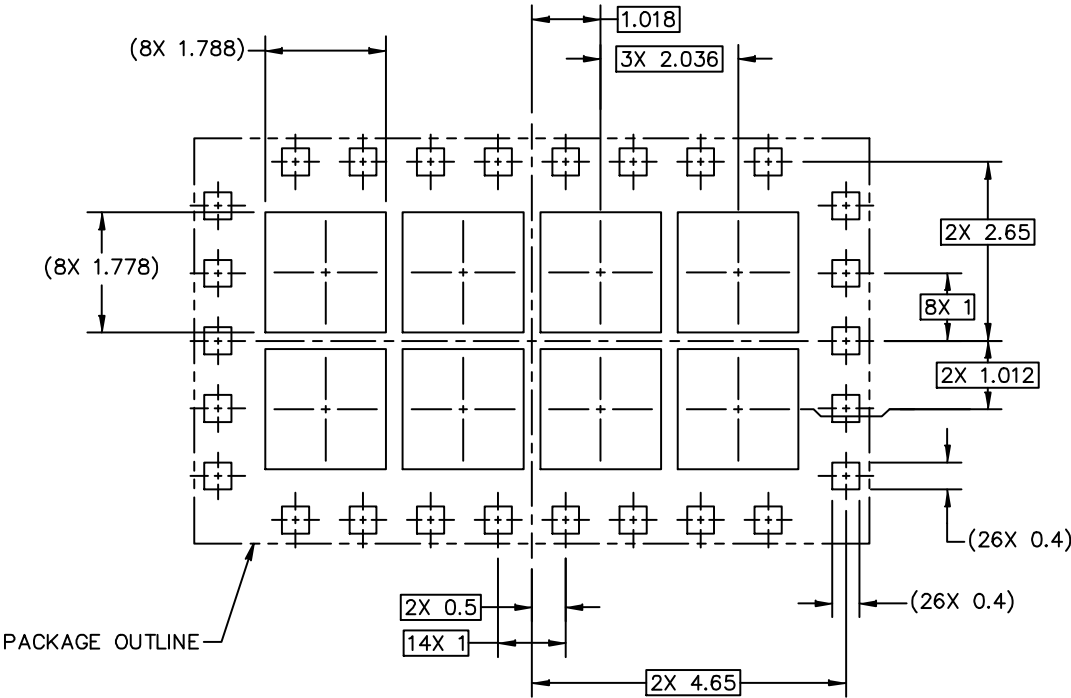
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H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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|--|------------------------|--------------------------------|----------------|------------|

H-PLGA-27 I/O  
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831-2

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON-SOLDERMASK DEFINED (NSMD).

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|  |                        |                                |                |            |
|--|------------------------|--------------------------------|----------------|------------|
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|--|------------------------|--------------------------------|----------------|------------|

## 14 Product documentation and tools

Refer to the following resources to aid your design process.

### Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

### Development Tools

- Printed Circuit Boards

## 15 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

## 16 Revision history

The following table summarizes revisions to this document.

**Table 14. Revision History**

| Document ID        | Release Date      | Description  |
|--------------------|-------------------|--|
| AFSC5G35E38 Rev. 2 | 14 June 2024      | <ul style="list-style-type: none"><li>• Tables 8 and 9, Functional Tests, 3400 MHz and 3600 MHz: updated output power test condition, p. 6</li></ul> |
| AFSC5G35E38 Rev. 1 | 30 September 2020 | <ul style="list-style-type: none"><li>• Update made to align data sheet to current standard</li></ul>  |
| AFSC5G35E38 Rev. 0 | 31 July 2020      | <ul style="list-style-type: none"><li>• Initial release of product data sheet</li></ul>  |



Legal information

Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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