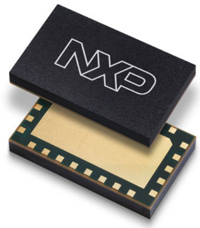
A3M35TL039

Airfast Power Amplifier Module

Rev. 4 — 14 June 2024 **Product data sheet**



1 General description

The A3M35TL039 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field−proven LDMOS power amplifiers are designed for TDD and FDD LTE systems.

2 Typical performance

Table 1. 3300–3700 MHz — Typical LTE Performance

P_{out} = 7 W Avg., V_{DD} = 26 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF. (1)

Carrier Center Frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3310 MHz	28.7	–25.1	39.0
3400 MHz	28.4	–28.0	41.2
3500 MHz	28.3	–29.7	41.3
3600 MHz	28.1	–31.0	40.4
3690 MHz	28.0	–29.6	38.7

1. All data measured with device soldered in NXP reference circuit.

3 Features and benefits

- Frequency: 3300–3700 MHz
- Advanced high performance in−package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity analog or digital linearization systems

4 Pinning information

4.1 Pinning

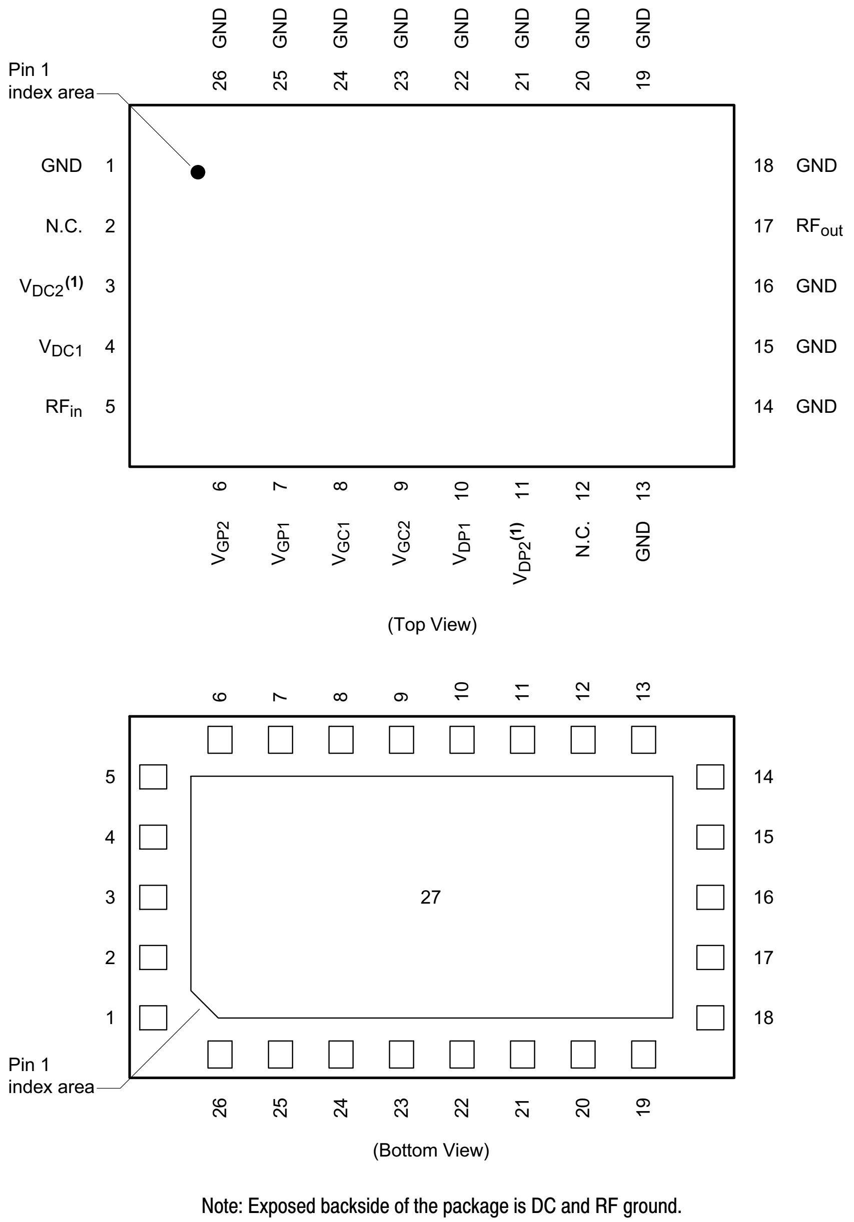


Figure 1. Pin Connections

1. V_{DC2} and V_{DP2} are DC coupled internal to the package and must be powered by a single DC power supply.

4.2 Functional pin description

Table 2. Functional Pin Description

Pin Number	Pin Function	Pin Description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	N.C.	No Connection
3	V_{DC2}	Carrier Drain Supply, Stage 2
4	V_{DC1}	Carrier Drain Supply, Stage 1
5	RF_{in}	RF Input
6	V_{GP2}	Peaking Gate Supply, Stage 2
7	V_{GP1}	Peaking Gate Supply, Stage 1
8	V_{GC1}	Carrier Gate Supply, Stage 1
9	V_{GC2}	Carrier Gate Supply, Stage 2
10	V_{DP1}	Peaking Drain Supply, Stage 1
11	V_{DP2}	Peaking Drain Supply, Stage 2
17	RF_{out}	RF Output

5 Maximum ratings

Table 3. Maximum Ratings

Rating	Symbol	Value	Unit
Gate–Bias Voltage Range	V_G	–0.5 to +10	Vdc
Operating Voltage Range	V_{DD}	24 to 30	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature	T_C	125	°C
Peak Input Power (3500 MHz, Pulsed CW, 10 μsec(on), 10% Duty Cycle)	P_{in}	25	dBm

6 Lifetime

Table 4. Lifetime

Characteristic	Symbol	Value	Unit
Mean Time to Failure Case Temperature 125°C, 7 W Avg., 30 Vdc	MTTF	>10	Years

7 ESD protection characteristics

Table 5. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS–001–2017)	1B
Charge Device Model (per JS–002–2014)	C2a

8 Moisture sensitivity level

Table 6. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

9 Electrical characteristics

9.1 DC characteristics

Table 7. DC Characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
Carrier Stage 1 — On Characteristics				
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 2 μAdc)	$V_{GS(th)}$	1.3	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_{DQ1A} = 23 mAdc)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_{DQ1A} = 23 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	5.9	±1.4	Vdc
Carrier Stage 2 — On Characteristics				
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 19 μAdc)	$V_{GS(th)}$	1.3	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_{DQ2A} = 72 mAdc)	$V_{GS(Q)}$	1.8	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_{DQ2A} = 72 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	3.0	±1.2	Vdc
Peaking Stage 1 — On Characteristics (1)				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 4 μAdc)	$V_{GS(th)}$	1.3	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_{DQ1A} = 85 μAdc)	$V_{GS(Q)}$	1.5	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_{DQ1A} = 85 μAdc, Measured in Functional Test)	$V_{GG(Q)}$	1.5	±0.4	Vdc
Peaking Stage 2 — On Characteristics (1)				
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 38 μAdc)	$V_{GS(th)}$	1.3	±0.4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_{DQ2A} = 550 μAdc)	$V_{GS(Q)}$	1.4	±0.4	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 26 Vdc, I_{DQ2A} = 550 μAdc, Measured in Functional Test)	$V_{GG(Q)}$	1.4	±0.4	Vdc

1. Each side of device measured separately.

9.2 Functional tests

Table 8. Functional Tests — 3400 MHz (1)

(In NXP Doherty Production ATE (2) Test Fixture, T_A = 25°C unless otherwise noted, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1A} = 23 mA, I_{DQ2A} = 72 mA, V_{GS1B} = (V_t – 0.2) Vdc, V_{GS2B} = (V_t – 0.25) Vdc, P_{out} = 7 W Avg., 1–tone CW, f = 3400 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	26.8	28.8	—	dB
Drain Efficiency	η_D	36.0	42.7	—	%
P_{out} @ 3 dB Compression Point (Pulsed CW, 5% Duty Cycle)	P3dB	46.0	47.0	—	dBm

Table 9. Functional Tests — 3600 MHz (1)

(In NXP Doherty Production ATE (2) Test Fixture, T_A = 25°C unless otherwise noted, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1A} = 23 mA, I_{DQ2A} = 72 mA, V_{GS1B} = (V_t – 0.2) Vdc, V_{GS2B} = (V_t – 0.25) Vdc, P_{out} = 7 W Avg., 1–tone CW, f = 3600 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	26.5	27.8	—	dB
Drain Efficiency	η_D	34.5	39.4	—	%
P_{out} @ 3 dB Compression Point (Pulsed CW, 5% Duty Cycle)	P3dB	45.4	46.2	—	dBm

9.3 Wideband ruggedness

Table 10. Wideband Ruggedness (3)

(In NXP Doherty Power Amplifier Module Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system) I_{DQ1A} = 23 mA, I_{DQ2A} = 72 mA, V_{GSP1} = 1.5 Vdc, V_{GSP2} = 1.35 Vdc, f = 3500 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR

Characteristic	Test Results
ISBW of 400 MHz at 30 Vdc, 3 dB Input Overdrive from 7 W Avg. Modulated Output Power	No Device Degradation

1. Part input and output matched to 50 ohms.
2. ATE is a socketed test environment.
3. All data measured in fixture with device soldered in NXP reference circuit.

9.4 Typical performance

Table 11. Typical Performance (1)

(In NXP Doherty Power Amplifier Module Reference Circuit, T_A = 25°C unless otherwise noted, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1A} = 23 mA, I_{DQ2A} = 72 mA, V_{GSP1} = 1.5 Vdc, V_{GSP2} = 1.35 Vdc, P_{out} = 7 W Avg., 3500 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
VBW Resonance Point, 2–tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	360	—	MHz
Quiescent Current Accuracy over Temperature (2) with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 1 with 2.2 kΩ Gate Feed Resistors (–40 to 85°C) Stage 2	ΔI_{QT}	 — —	 2.8 6.3	 — —	%
1–carrier 20 MHz LTE, 8 dB Input Signal PAR					
Gain	G	—	28.3	—	dB
Power Added Efficiency	PAE	—	41.3	—	%
Adjacent Channel Power Ratio	ACPR	—	–29.7	—	dBc
Adjacent Channel Power Ratio	ALT1	—	–40.1	—	dBc
Adjacent Channel Power Ratio	ALT2	—	–50.7	—	dBc
Gain Flatness (3)	G_F	—	0.5	—	dB
Fast CW, 27 ms Sweep					
P_{out} @ 3 dB Compression Point	P3dB	—	47.2	—	dBm
AM/PM @ P3dB	Φ	—	–28	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +105°C)	ΔG	—	0.037	—	dB/°C
P3dB Variation over Temperature (–40°C to +105°C)	P3dB	—	0.013	—	dB/°C

10 Ordering information

Table 12. Ordering Information

Device	Tape and Reel Information	Package
A3M35TL039T2	T2 Suffix = 2,000 Units, 24 mm Tape Width, 13–inch Reel	10 mm × 6 mm Module

1. All data measured in fixture with device soldered in NXP reference circuit.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
3. Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High}))

11 Component layout and parts list

11.1 Component layout

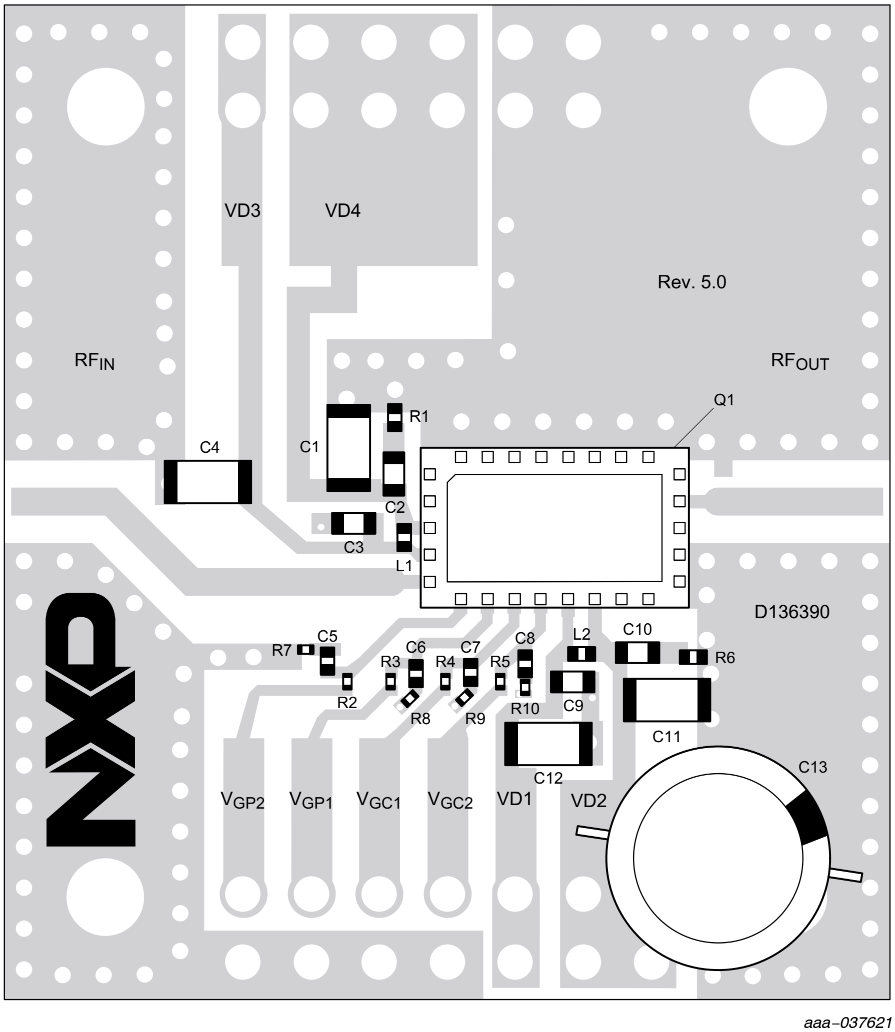


Figure 2. A3M35TL039 Reference Circuit Component Layout

11.2 Component designations and values

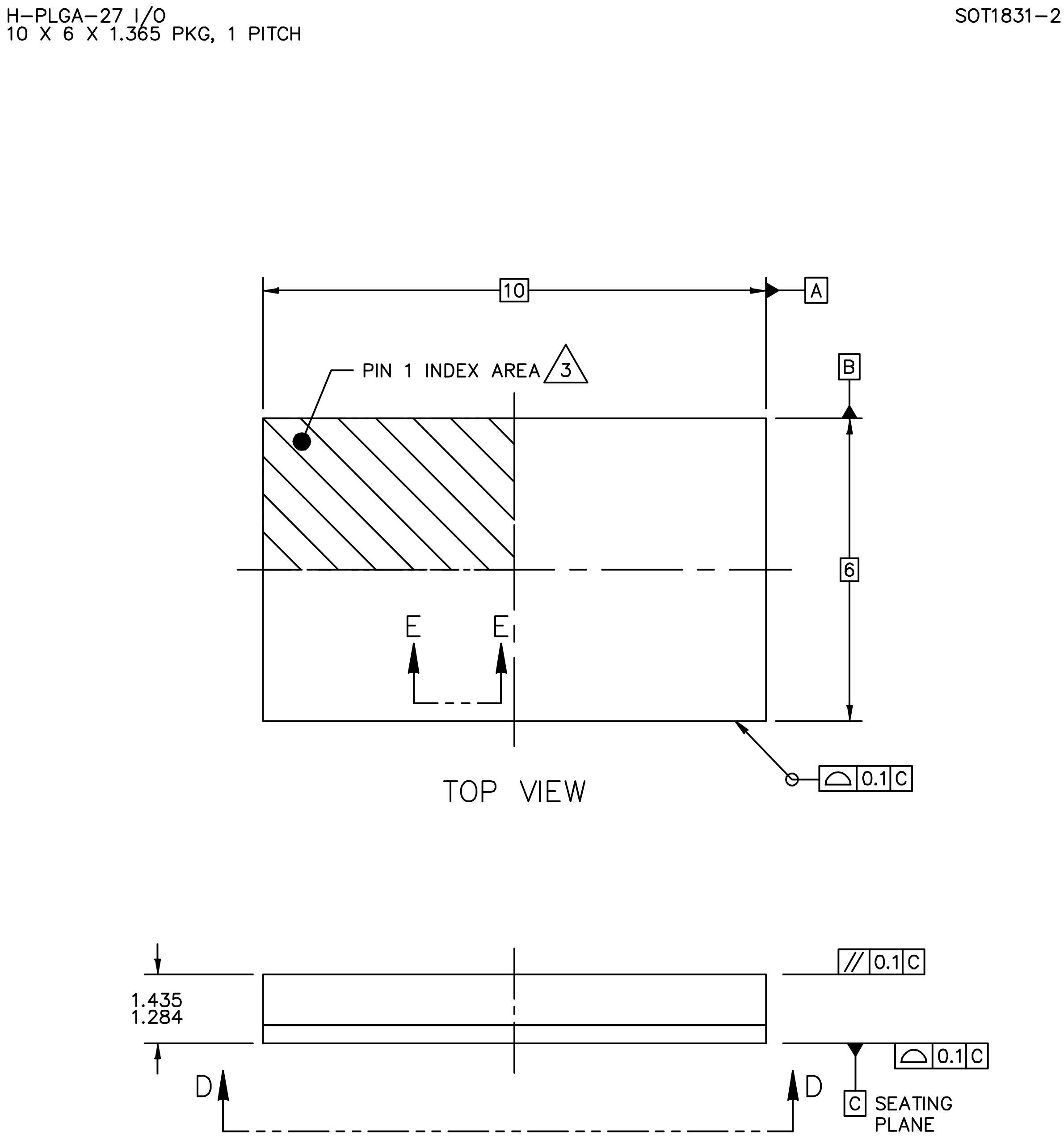
Table 13. A3M35TL039 Reference Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C11, C12	10 μF Chip Capacitor	GRM31CR61H106KA12	Murata
C2, C3, C9, C10	1 μF Chip Capacitor	GRM188R61H105KAAL	Murata
C5, C6, C7, C8	0.1 μF Chip Capacitor	GRM155R61H104KE19	Murata
C13	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26	Multicomp
L1, L2	30 Ω Ferrite Bead	BLM15PD300SN1	Murata
Q1	Power Amplifier Module	A3M35TL039	NXP
R1, R6	5.1 Ω, 1/10 W Chip Resistor	ERJ-2GEJ5R1X	Panasonic
R2, R3, R4, R5	2.2 kΩ, 1/20 W Chip Resistor	ERJ-1GNJ222C	Panasonic
R7, R8, R10	0 Ω, 1/20 W Chip Resistor	ERJ-1GN0R00C	Panasonic
R9	2.0 Ω, 1/20 W Chip Resistor	ERJ-1GNJ2R0C	Panasonic
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D136390	MTL

12 Product marking

Figure 3. Product Marking

13 Package information



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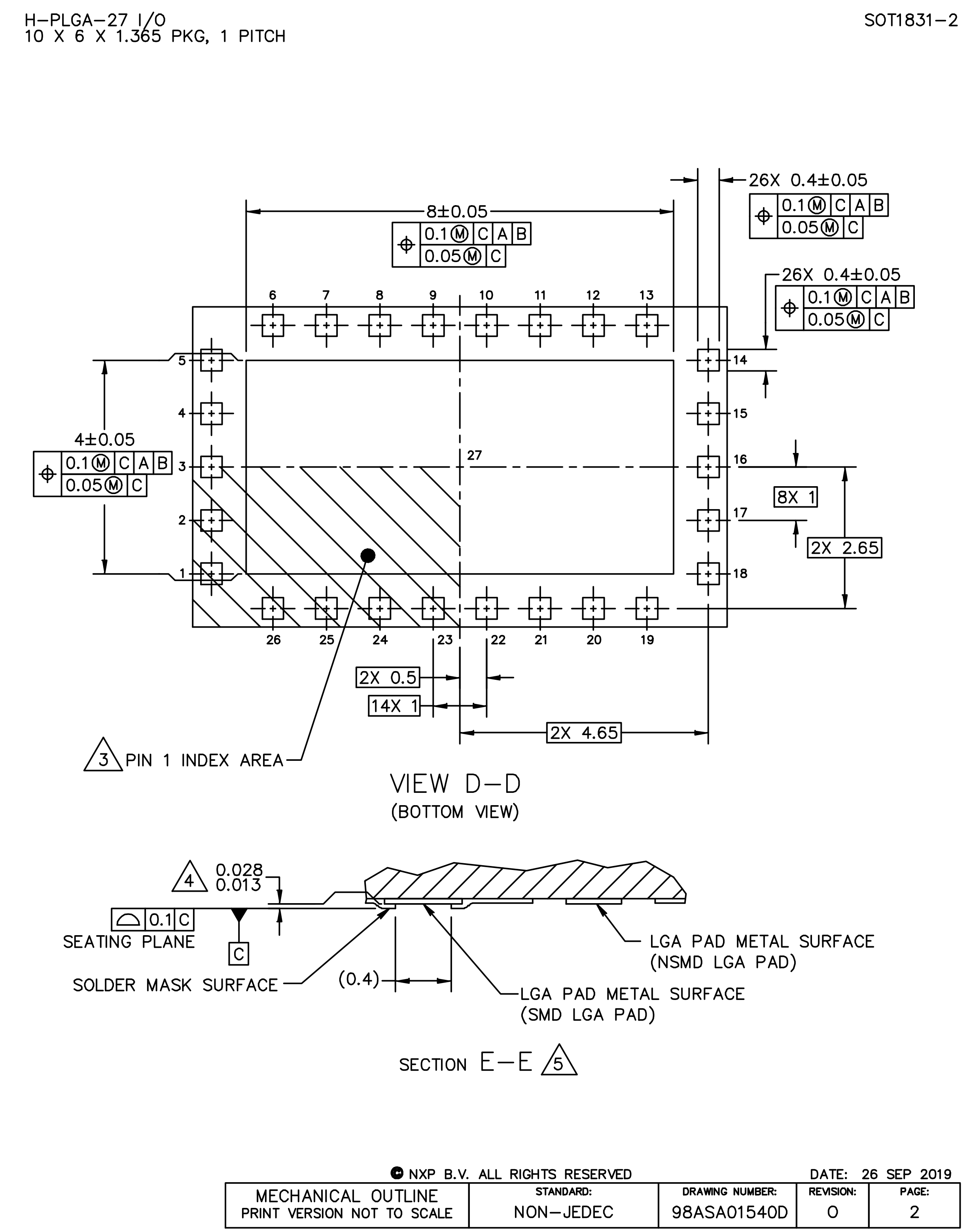
H-PLGA-27 I/O
10 X 6 X 1.365 PKG, 1 PITCH
SOT1831-2
26X 0.4±0.05
8±0.05
0.1 Ⓜ C A B
0.05 Ⓜ C
26X 0.4±0.05
4±0.05
8X 1
2X 2.65
2X 0.5
14X 1
2X 4.65
3 PIN 1 INDEX AREA
VIEW D-D
(BOTTOM VIEW)
4 0.028
0.013
0.1 C
SEATING PLANE
C
SOLDER MASK SURFACE
(0.4)
LGA PAD METAL SURFACE
(NSMD LGA PAD)
LGA PAD METAL SURFACE
(SMD LGA PAD)
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H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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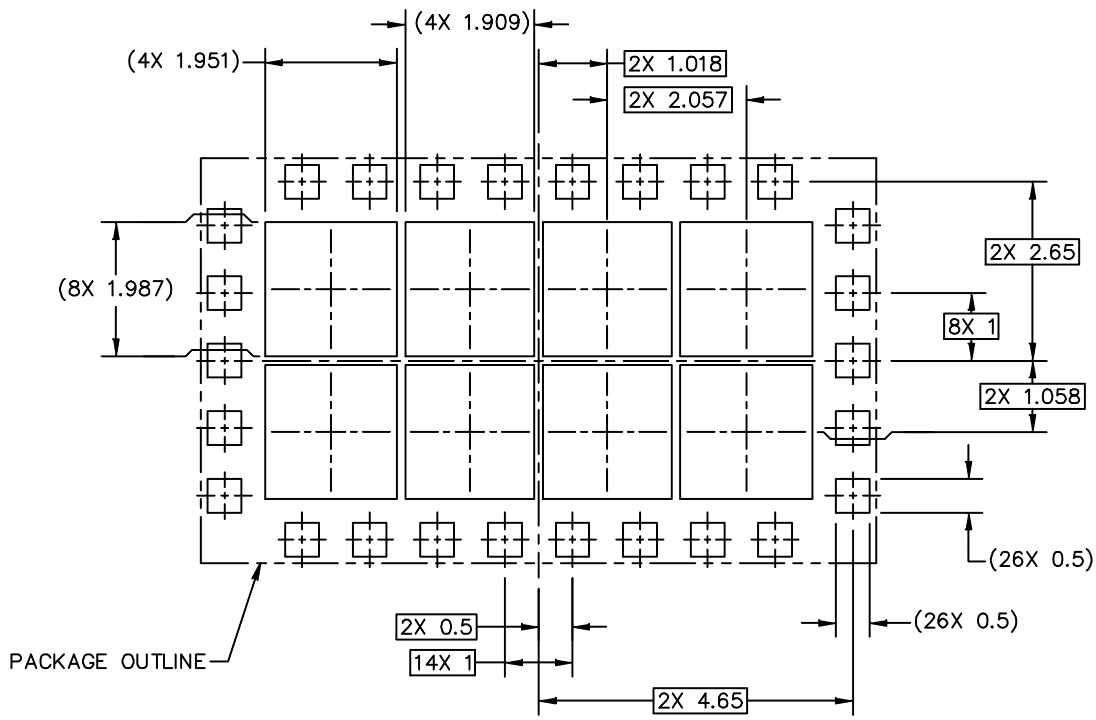

PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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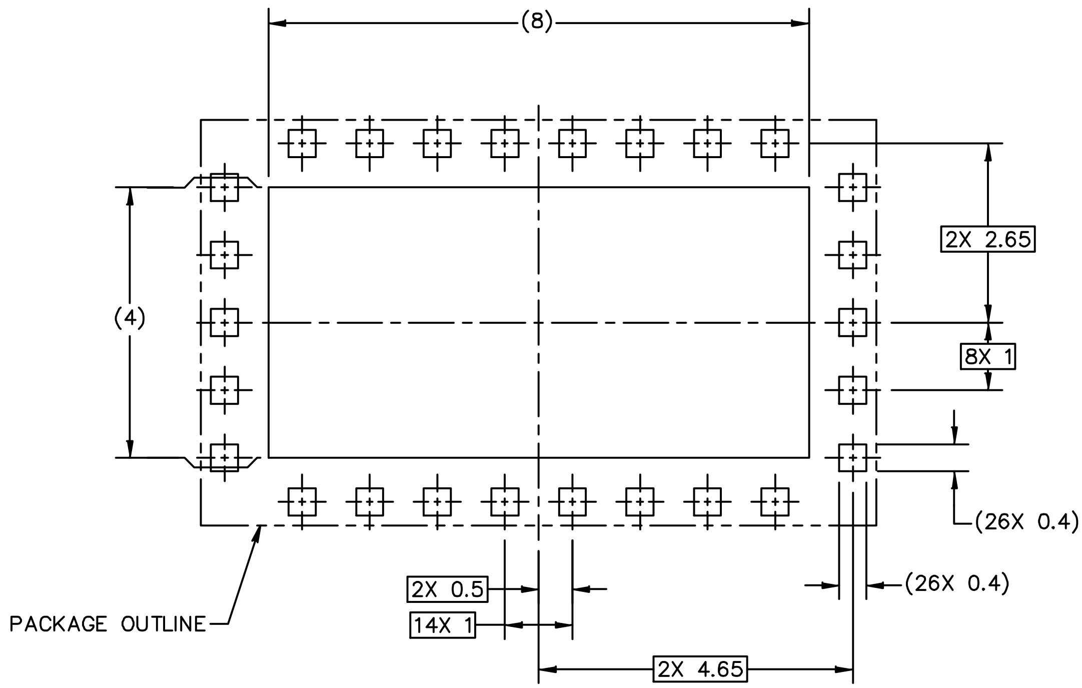

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H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

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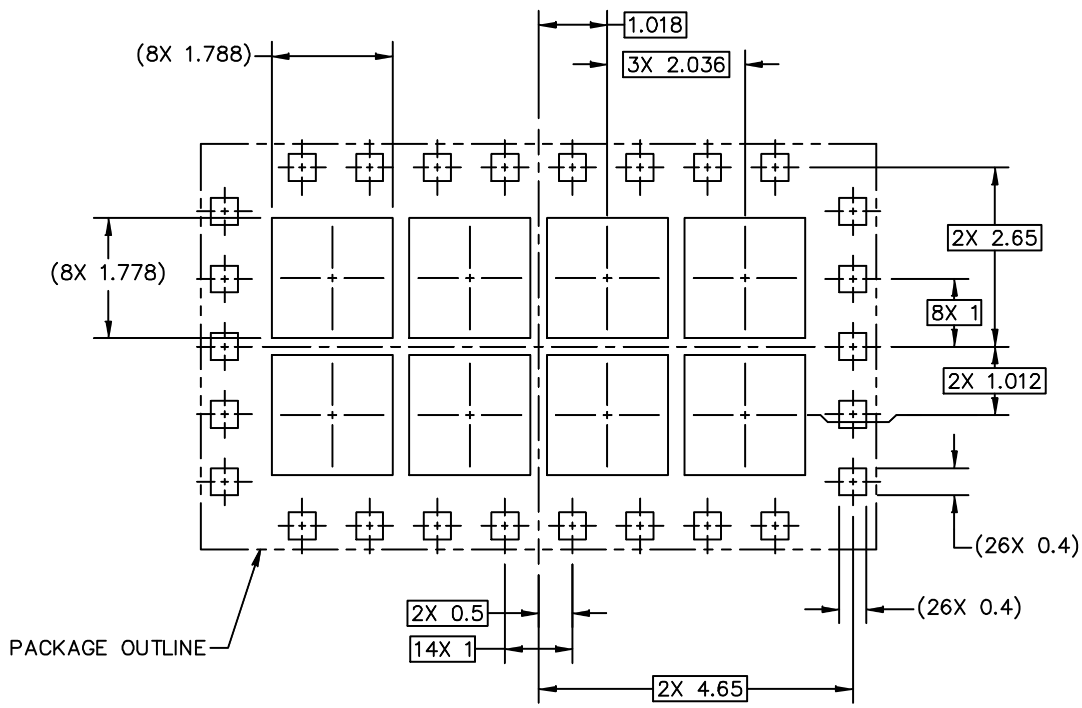

RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
	NON–JEDEC	98ASA01540D	0	6

14 Product documentation and tools

Refer to the following resources to aid your design process.

Application Notes

- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Development Tools

- Printed Circuit Boards

15 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

16 Revision history

The following table summarizes revisions to this document.

Table 14. Revision History

Document ID	Release Date	Description
A3M35TL039 Rev. 4	14 June 2024	• Tables 8 and 9, Functional Tests, 3400 MHz and 3600 MHz: updated output power test condition, p. 6
A3M35TL039 Rev. 3	28 February 2022	• Updated frequency band of operation for this device to 3300–3700 MHz and updated performance table to include corresponding measured data, p. 1 • Typical Performance 1–carrier 20 MHz LTE table: PAE and ACPR Typ values updated, p. 6
A3M35TL039 Rev. 2	14 December 2020	• Changed higher frequency operation of the part from 3600 MHz to 3650 MHz. Added 3640 MHz to performance table with corresponding measured data, p. 1 • Table 4, ESD Protection Characteristics: updated Human Body Model ESD from Class 1A to 1B to reflect actual Qual Report results, p. 4
A3M35TL039 Rev. 1	30 September 2020	• General updates made to align data sheet to current standard
A3M35TL039 Rev. 0	28 May 2020	• Initial release of product data sheet

Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term ‘short data sheet’ is explained in section “Definitions”.
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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