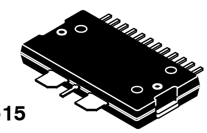
RF LDMOS Wideband Integrated Power Amplifiers

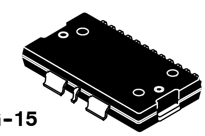
The A2I20H060N wideband integrated circuit is an asymmetrical Doherty designed with on-chip matching that makes it usable from 1800 to 2200 MHz. This multi-stage structure is rated for 26 to 32 V operation and covers all typical cellular base station modulation formats.

A2I20H060NR1
A2I20H060GNR1

1800–2200 MHz, 12 W AVG., 28 V AIRFAST RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS



TO-270WB-15 PLASTIC A2I20H060NR1



TO-270WBG-15 PLASTIC A2I20H060GNR1

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 145 mA, V_{GS1B} = 1.65 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 12 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1805 MHz	28.5	42.7	–37.4
1840 MHz	28.4	43.8	–37.8
1880 MHz	28.1	43.1	–34.7

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 145 mA, V_{GS1B} = 1.65 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 12 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2110 MHz	27.8	42.3	–36.0
2140 MHz	27.5	42.2	–38.3
2170 MHz	27.3	42.2	–37.7

Features

- Advanced High Performance In-Package Doherty
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Designed for Digital Predistortion Error Correction Systems

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

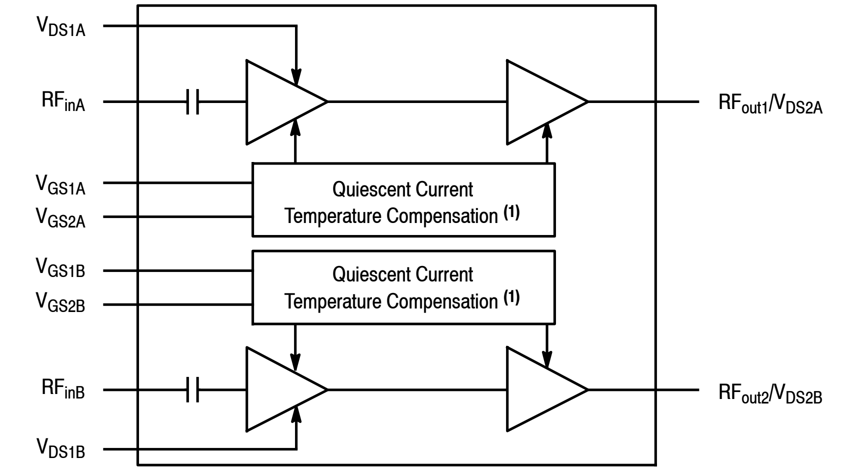
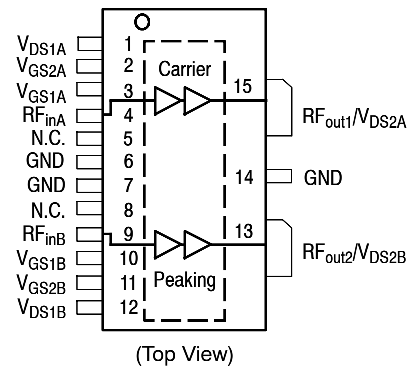


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (2,3)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (3,4)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 12 W Avg., W-CDMA, 1840 MHz Stage 1, 28 Vdc, I_{DQ1A} = 24 mA, V_{GS1B} = 1.65 Vdc Stage 2, 28 Vdc, I_{DQ2A} = 145 mA, V_{GS2B} = 1.3 Vdc	$R_{\theta JC}$	 5.2 1.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.
2. Continuous use at maximum temperature will affect MTTF.
3. MTTF calculator available at http://www.nxp.com/RF/calculators.
4. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 – Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 1 – On Characteristics					
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 3 μAdc)	$V_{GS(th)}$	0.8	1.3	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1A} = 24 mAdc)	$V_{GS(Q)}$	—	2.2	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1A} = 24 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	3.4	4.4	4.9	Vdc
Carrier Stage 2 – Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Carrier Stage 2 – On Characteristics					
Gate Threshold Voltage [1] (V_{DS} = 10 Vdc, I_D = 24 μAdc)	$V_{GS(th)}$	0.8	1.3	1.6	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 145 mAdc)	$V_{GS(Q)}$	—	1.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 145 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	2.7	3.7	4.2	Vdc
Drain-Source On-Voltage [1] (V_{GS} = 10 Vdc, I_D = 280 mAdc)	$V_{DS(on)}$	0.1	0.34	1.5	Vdc

1. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Peaking Stage 1 - Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 1 - On Characteristics [1]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 8 μAdc)	$V_{GS(th)}$	0.8	1.3	1.6	Vdc
Peaking Stage 2 - Off Characteristics [1]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Peaking Stage 2 - On Characteristics [1]					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 40 μAdc)	$V_{GS(th)}$	0.8	1.3	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 350 mAdc)	$V_{DS(on)}$	0.1	0.17	1.5	Vdc

1. Each side of device measured separately.

(continued)

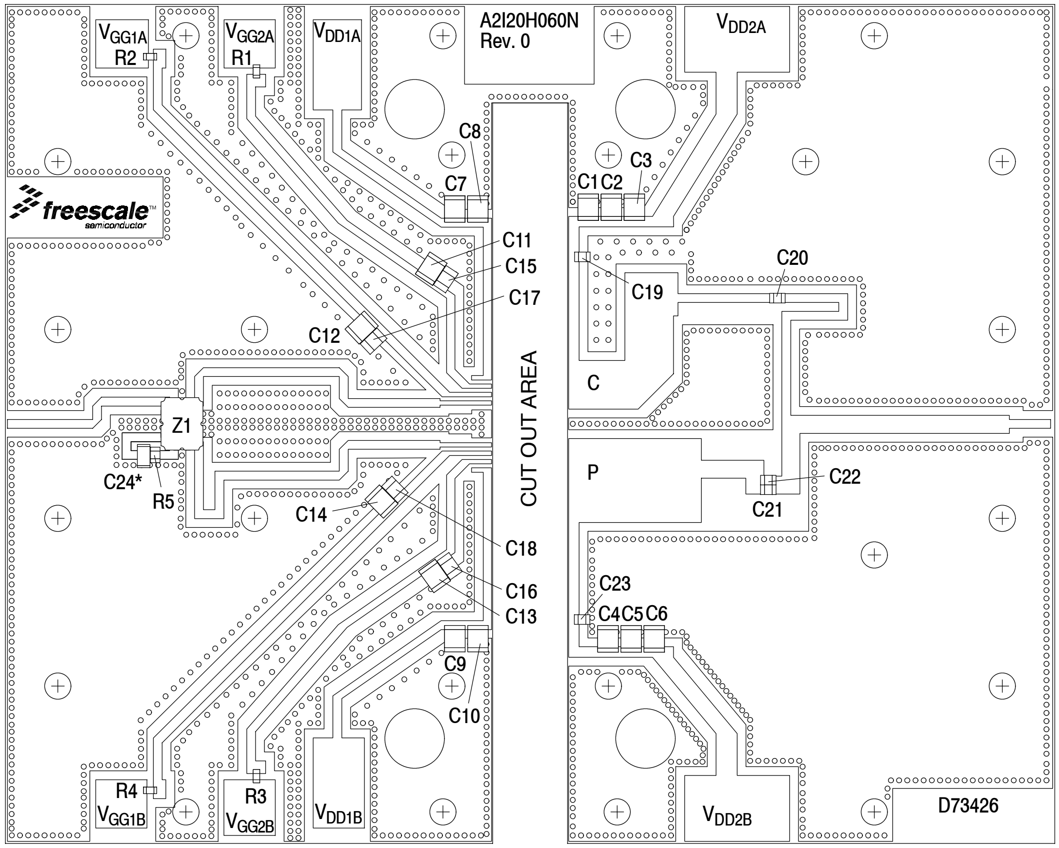
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 145 mA, V_{GS1B} = 1.65 Vdc, V_{GS2B} = 1.3 Vdc, P_{out} = 12 W Avg., f = 1842.5 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	27.5	28.9	30.9	dB
Power Added Efficiency	PAE	42.0	47.3	—	%
Adjacent Channel Power Ratio	ACPR	—	–34.5	–30.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	65	74	—	W
Load Mismatch (2) (In Freescale Doherty Production Test Fixture, 50 ohm system) I_{DQ1A} = 24 mA, I_{DQ2A} = 145 mA, V_{GS1B} = 1.65 Vdc, V_{GS2B} = 1.3 Vdc, f = 1840 MHz					
VSWR 10:1 at 32 Vdc, 80 W CW Output Power (3 dB Input Overdrive from 69 W CW Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 145 mA, V_{GS1B} = 1.65 Vdc, V_{GS2B} = 1.3 Vdc, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	63	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	74	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.)	Φ	—	–15	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	120	—	MHz
Quiescent Current Accuracy over Temperature (5)	ΔI_{QT}				%
with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1		—	1.0	—	
with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 2		—	2.0	—	
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 12 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.026	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	$\Delta P1dB$	—	0.011	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2I20H060NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-15
A2I20H060GNR1		TO-270WBG-15

1. Part internally input matched.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

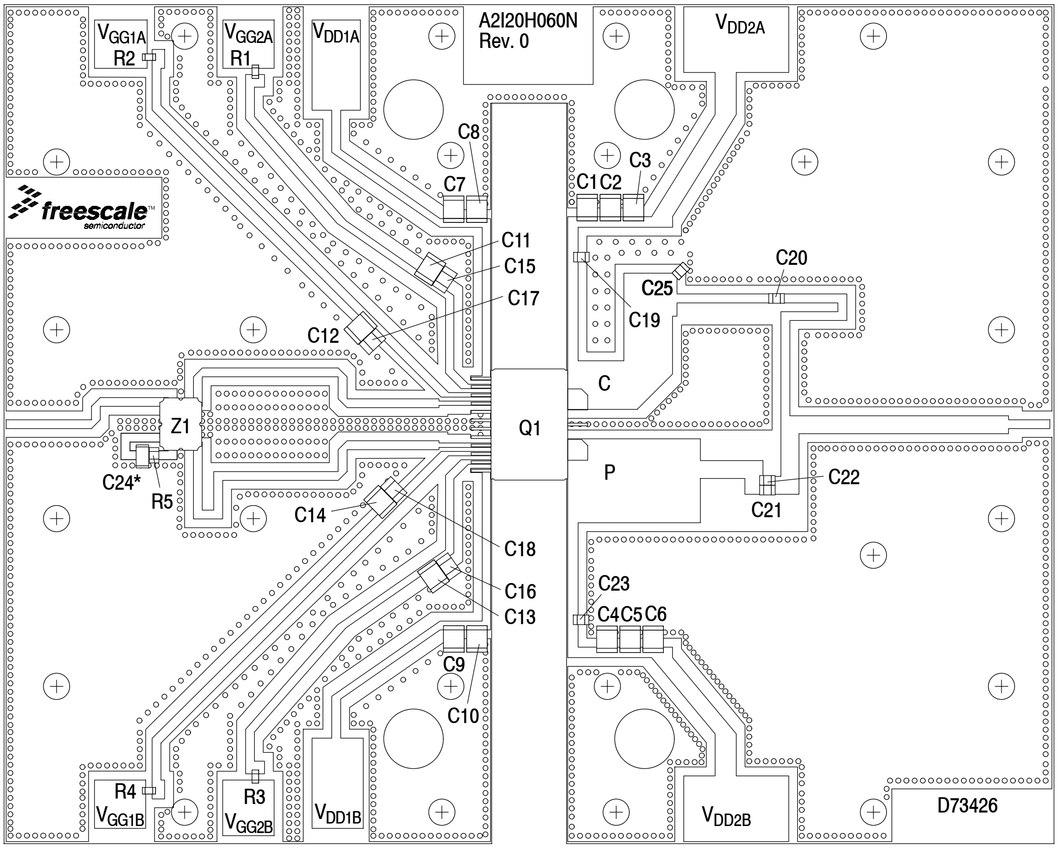


*C24 is mounted vertically.

Figure 3. A2I20H060NR1 Production Test Circuit Component Layout

Table 7. A2I20H060NR1 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitors	C3225X7S1H106K250AB	TDK
C15, C16, C17, C18	10 nF Chip Capacitors	08055C103KAT2A	AVX
C19, C20, C21, C22, C23	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C24	1.3 pF Chip Capacitor	ATC100B1R3BT500XT	ATC
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistors	WCR0805-2K2FI	Welwyn
R5	50 Ω, 8 W Chip Resistor	C8A50Z4A	Anaren
Z1	1700–2000 MHz Band, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	RF35, 0.020″, ε_r = 3.55	D73426	MTL



*C24 is mounted vertically.

Note: All data measured in fixture with device soldered to heatsink.

Figure 4. A2I20H060NR1 Characterization Test Circuit Component Layout

Table 8. A2I20H060NR1 Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	10 μF Chip Capacitors	C3225X7S1H106K250AB	TDK
C15, C16, C17, C18	10 nF Chip Capacitors	08055C103KAT2A	AVX
C19, C20, C21, C22, C23	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C24	1.3 pF Chip Capacitor	ATC100B1R3BT500XT	ATC
C25	0.3 pF Chip Capacitor	ATC600S0R3BT250XT	ATC
Q1	RF LDMOS Power Amplifier	A2I20H060NR1	Freescale
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistors	WCR0805-2K2FI	Welwyn
R5	50 Ω, 8 W Chip Resistor	C8A50Z4A	Anaren
Z1	1700–2000 MHz Band, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	RF35, 0.020″, ε_r = 3.55	D73426	MTL

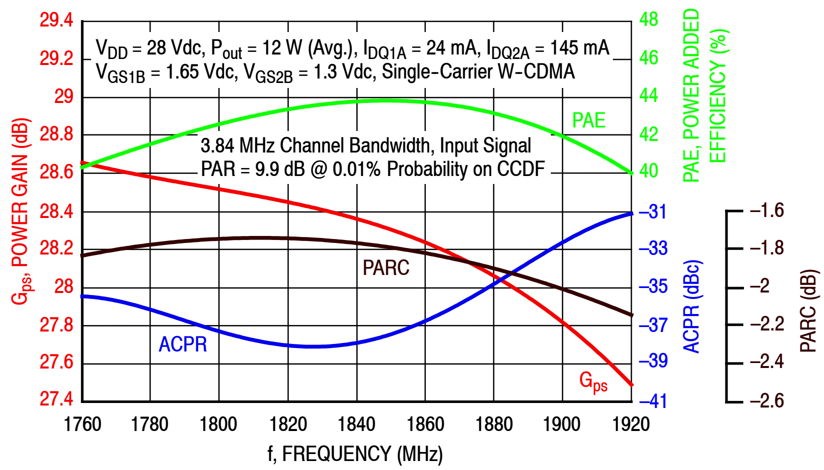


Figure 5. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 12 Watts Avg.

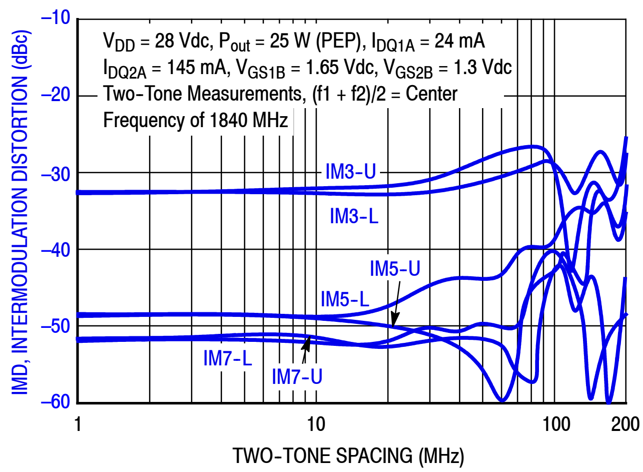


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

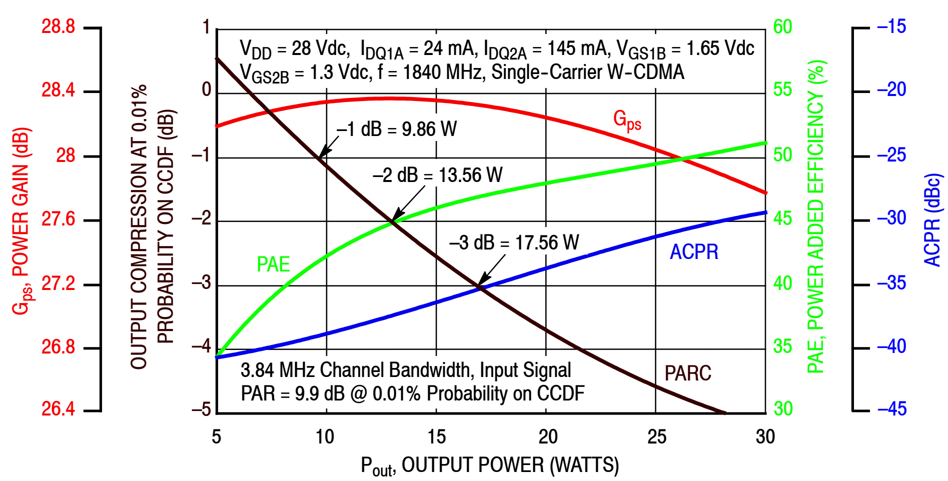


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

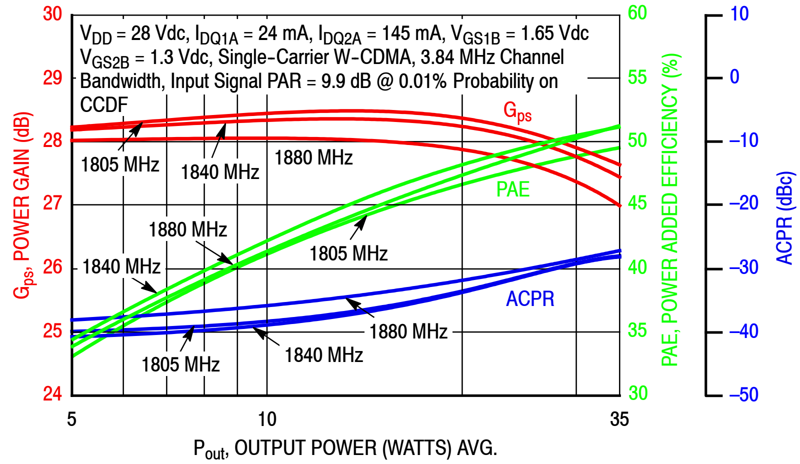


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

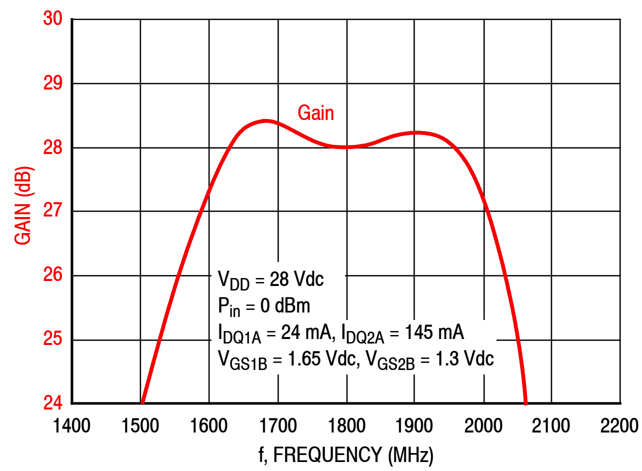


Figure 9. Broadband Frequency Response

Table 9. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 149 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	43.9 – j21.6	41.6 + j19.1	4.30 + j0.95	32.2	44.3	27	55.7	–7
1840	49.1 – j21.7	45.4 + j19.9	3.91 + j1.32	32.4	44.4	28	57.7	–7
1880	54.0 – j19.0	51.9 + j17.3	3.92 + j1.42	32.3	44.4	28	58.3	–8

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	43.9 – j21.6	43.8 + j18.4	4.55 + j0.70	30.0	45.0	32	57.1	–11
1840	49.1 – j21.7	47.9 + j18.3	4.31 + j1.06	30.2	45.1	32	58.6	–11
1880	54.0 – j19.0	53.9 + j14.6	4.31 + j1.12	30.0	45.1	32	58.4	–11

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 149 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	43.9 – j21.6	41.9 + j25.2	2.87 + j4.44	33.8	41.9	16	65.5	–12
1840	49.1 – j21.7	47.7 + j27.1	2.25 + j4.50	33.9	41.6	14	69.2	–13
1880	54.0 – j19.0	55.7 + j23.0	2.35 + j4.13	33.7	42.1	16	69.0	–13

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	43.9 – j21.6	42.7 + j23.9	2.62 + j4.15	32.0	42.7	19	66.4	–17
1840	49.1 – j21.7	48.7 + j24.0	2.47 + j4.20	31.9	42.8	19	70.0	–17
1880	54.0 – j19.0	56.7 + j20.7	2.17 + j4.13	31.7	42.5	18	69.3	–19

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

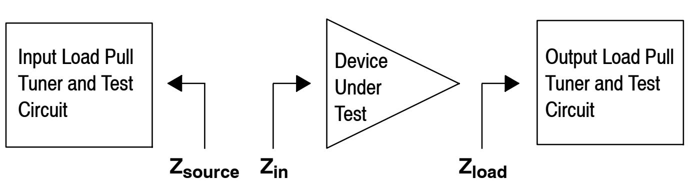


Table 11. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 43 mA, V_{GS2B} = 1.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	35.1 – j7.58	36.1 + j8.10	2.33 – j0.53	28.6	46.5	45	57.5	–16
1840	33.9 – j9.77	35.8 + j8.91	2.23 – j0.44	28.6	46.6	45	58.0	–17
1880	36.6 – j10.5	37.3 + j8.43	2.22 – j0.35	28.5	46.5	45	57.0	–15

			Max Output Power P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	35.1 – j7.58	38.7 + j9.21	2.56 – j0.71	26.5	47.2	52	58.2	–21
1840	33.9 – j9.77	38.7 + j9.51	2.44 – j0.60	26.4	47.2	52	58.4	–22
1880	36.6 – j10.5	40.5 + j8.27	2.43 – j0.48	26.4	47.1	51	57.6	–20

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

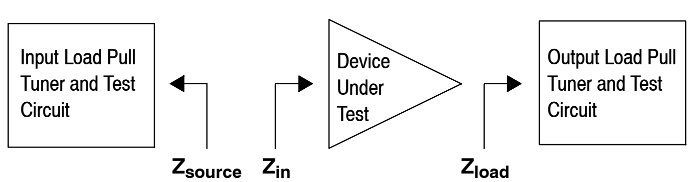
Table 12. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 43 mA, V_{GS2B} = 1.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	35.1 – j7.58	32.3 + j11.3	0.81 + j2.03	29.2	41.8	15	73.5	–56
1840	33.9 – j9.77	32.9 + j12.8	0.84 + j1.97	28.8	41.8	15	72.7	–62
1880	36.6 – j10.5	35.1 + j12.5	0.96 + j1.83	28.9	42.4	17	70.3	–67

			Max Drain Efficiency P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	35.1 – j7.58	34.1 + j11.5	0.83 + j1.85	27.4	42.7	19	72.9	–49
1840	33.9 – j9.77	34.8 + j12.0	1.07 + j1.56	27.5	43.8	24	71.8	–53
1880	36.6 – j10.5	37.7 + j10.8	1.45 + j1.41	27.4	44.9	31	69.5	–32

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1840 MHz

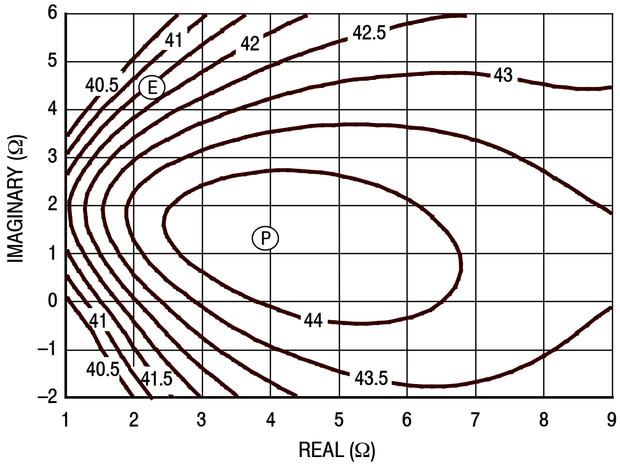


Figure 10. P1dB Load Pull Output Power Contours (dBm)

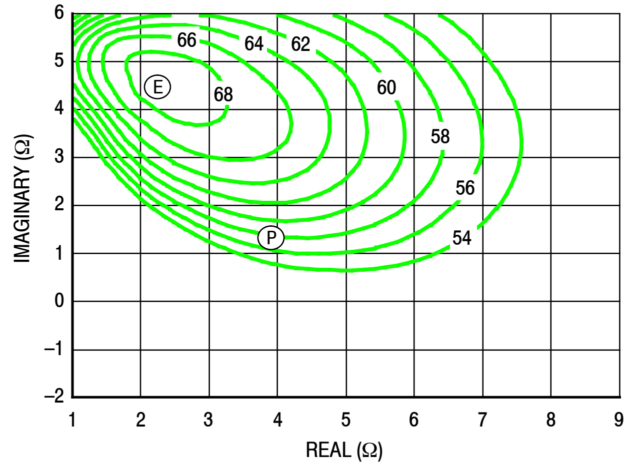


Figure 11. P1dB Load Pull Efficiency Contours (%)

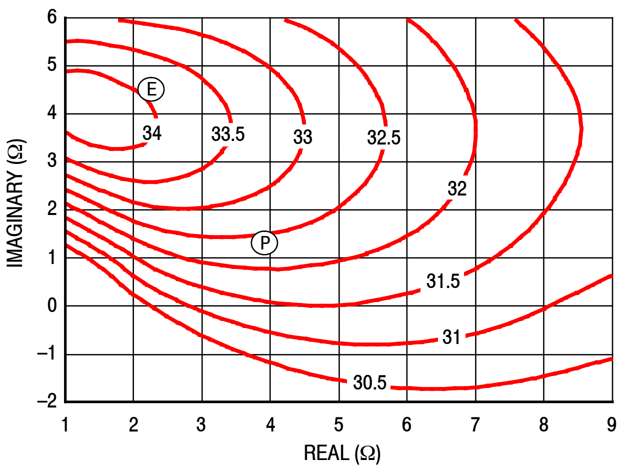


Figure 12. P1dB Load Pull Gain Contours (dB)

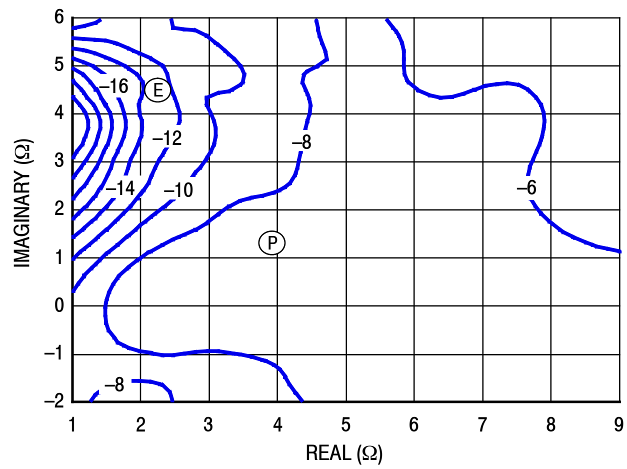


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1840 MHz

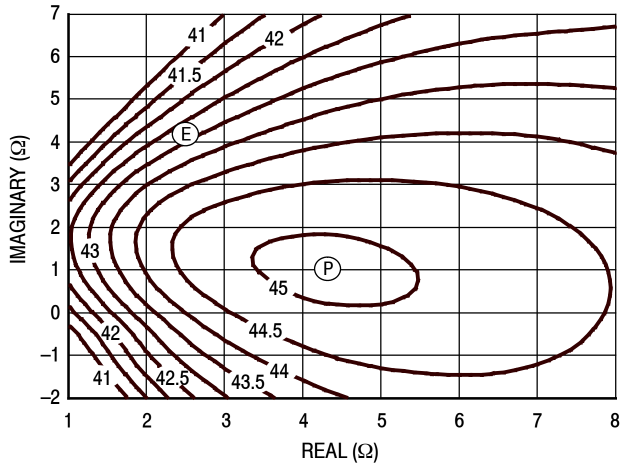


Figure 14. P3dB Load Pull Output Power Contours (dBm)

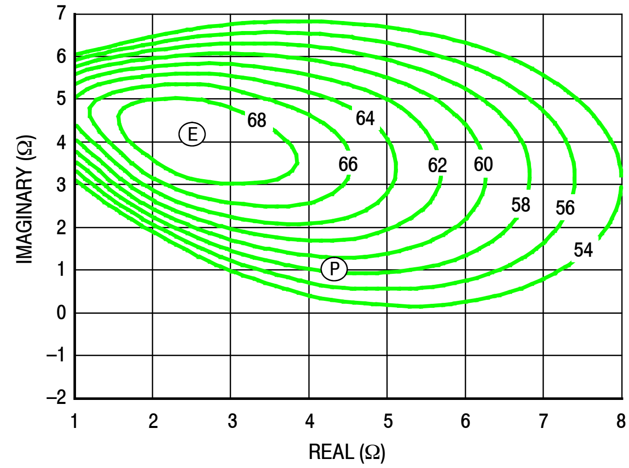


Figure 15. P3dB Load Pull Efficiency Contours (%)

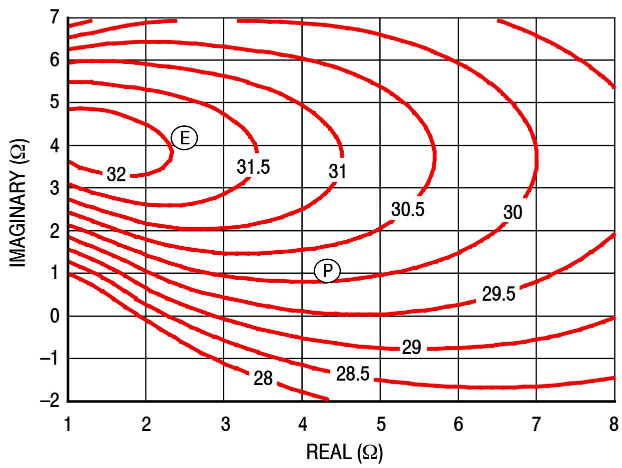


Figure 16. P3dB Load Pull Gain Contours (dB)

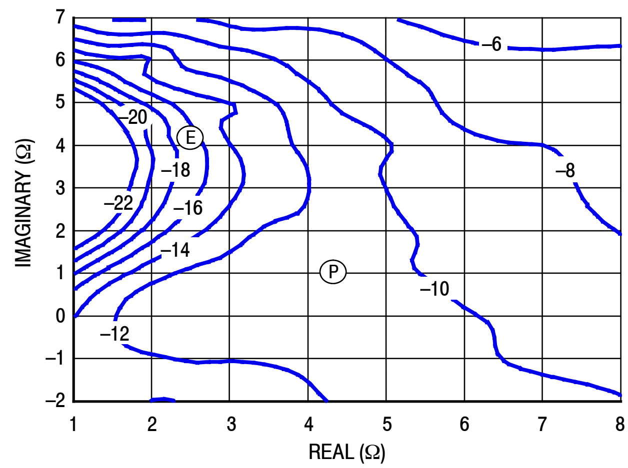


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

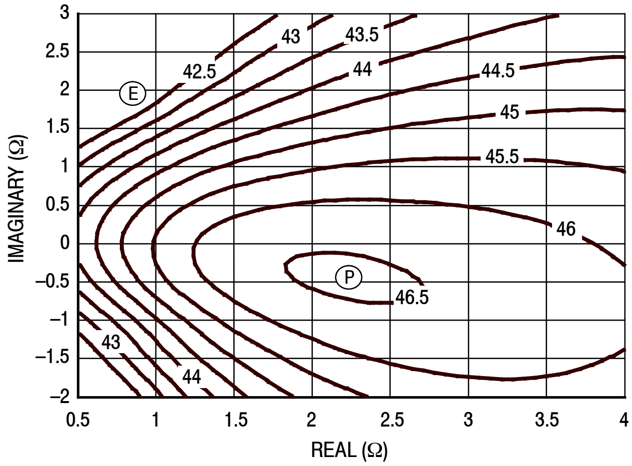


Figure 18. P1dB Load Pull Output Power Contours (dBm)

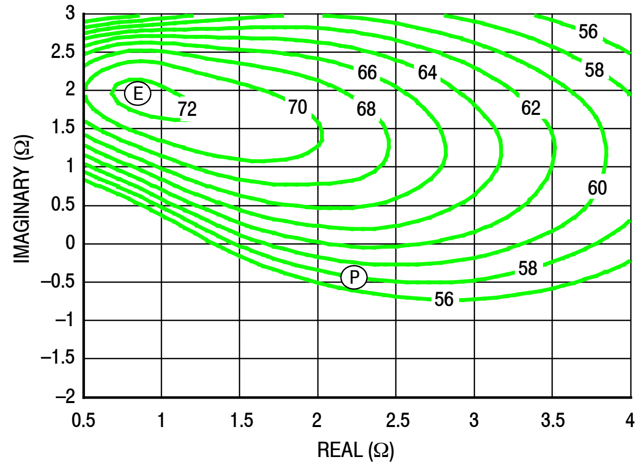


Figure 19. P1dB Load Pull Efficiency Contours (%)

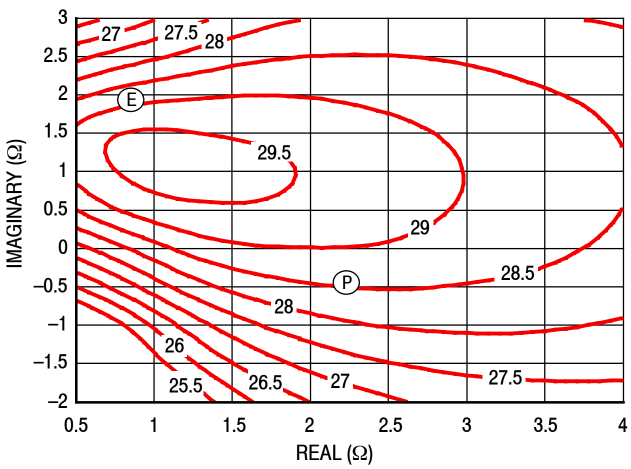


Figure 20. P1dB Load Pull Gain Contours (dB)

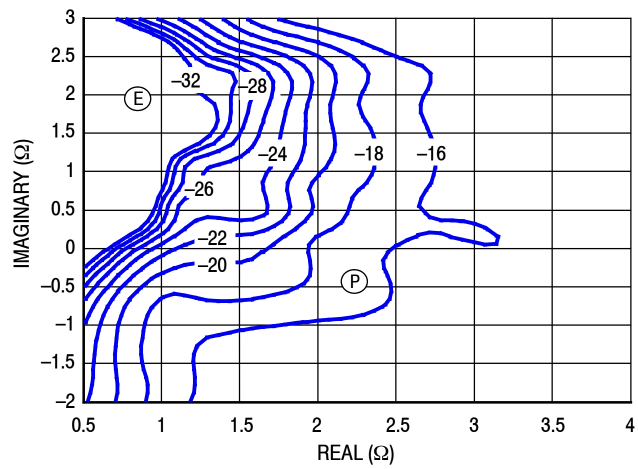


Figure 21. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1840 MHz

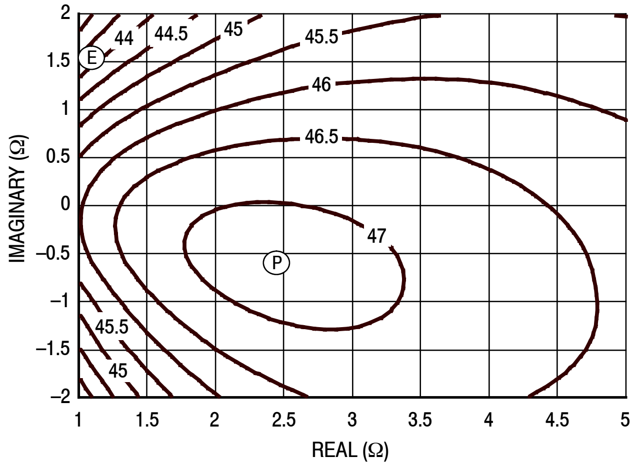


Figure 22. P3dB Load Pull Output Power Contours (dBm)

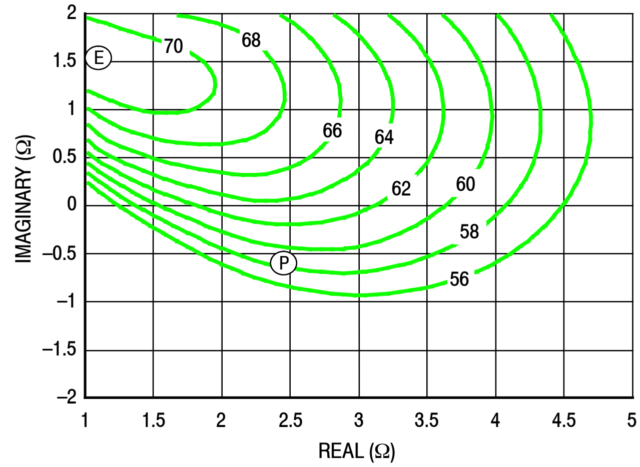


Figure 23. P3dB Load Pull Efficiency Contours (%)

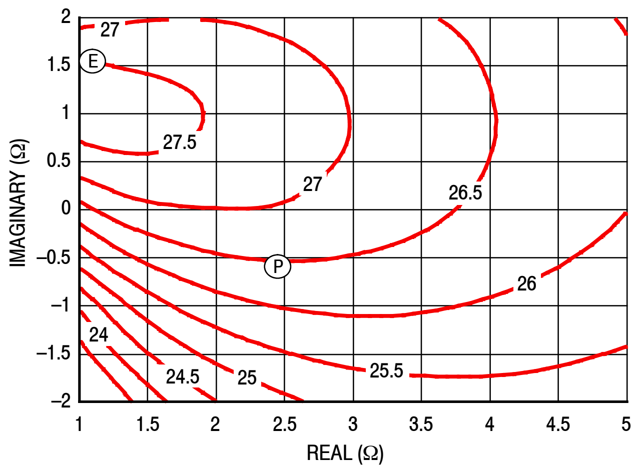


Figure 24. P3dB Load Pull Gain Contours (dB)

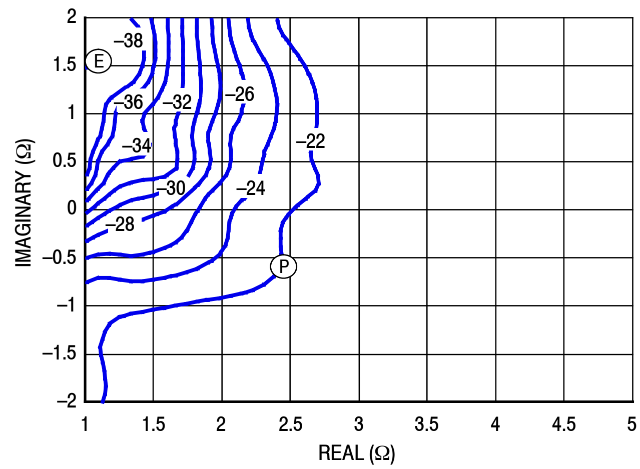
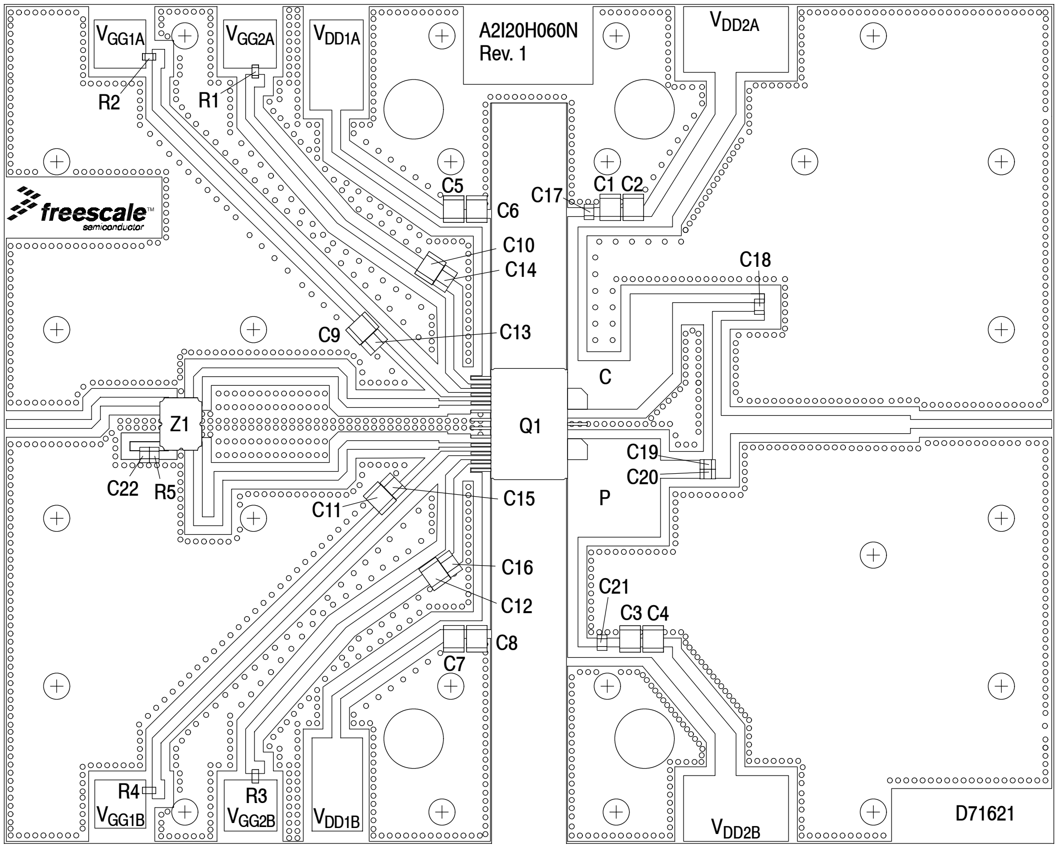


Figure 25. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power



Note: All data measured in fixture with device soldered to heatsink.

Figure 26. A2I20H060NR1 Test Circuit Component Layout — 2110–2170 MHz

Table 13. A2I20H060NR1 Test Circuit Component Designations and Values — 2110–2170 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12	10 μF Chip Capacitors	C3225X7S1H106K250AB	TDK
C13, C14, C15, C16	10 nF Chip Capacitors	08055C103KAT2A	AVX
C17, C18, C19, C20, C21	10 pF Chip Capacitors	ATC600S100JT250XT	ATC
C22	0.7 pF Chip Capacitor	ATC600S0R7BT250XT	ATC
Q1	RF LDMOS Power Amplifier	A2I20H060NR1	Freescale
R1, R2, R3, R4	2.2 kΩ, 1/8 W Chip Resistors	WCR0805-2K2FI	Welwyn
R5	50 Ω, 8 W Chip Resistor	C8A50Z4A	Anaren
Z1	2000–2300 MHz Band, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	RF35, 0.020″, ε_r = 3.55	D71621	MTL

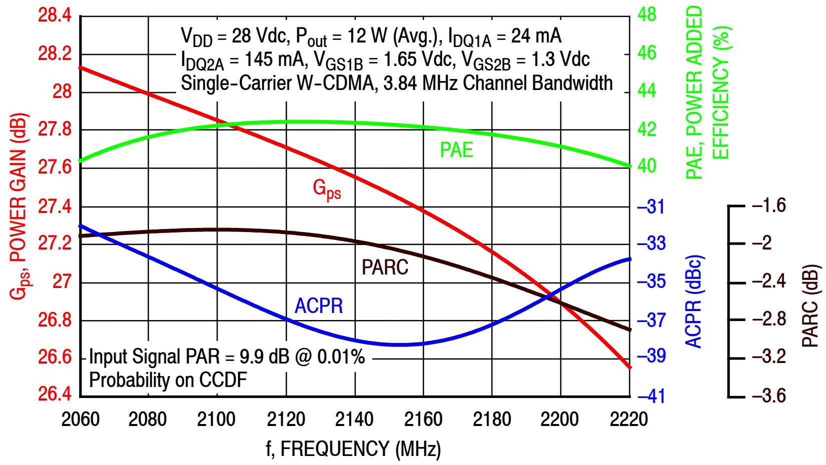


Figure 27. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 12 Watts Avg.

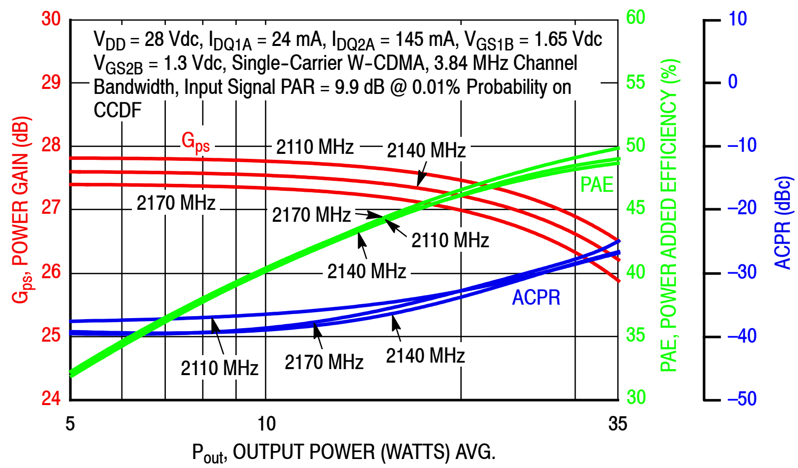


Figure 28. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

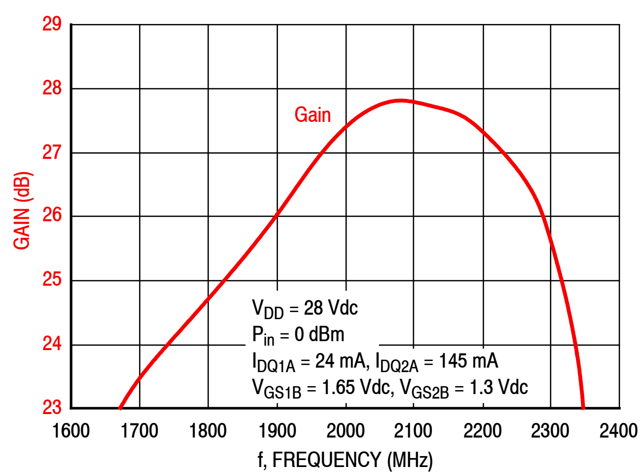


Figure 29. Broadband Frequency Response

Table 14. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 149 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	69.5 + j18.1	70.6 – j18.1	3.84 + j1.66	31.7	44.1	26	53.2	–8
2140	65.9 + j18.2	69.2 – j19.8	4.08 + j1.52	31.6	44.2	26	53.8	–8
2170	69.5 + j20.2	69.1 – j20.1	3.94 + j1.55	31.7	44.2	27	55.3	–9

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	69.5 + j18.1	67.0 – j19.9	4.38 + j1.42	29.5	44.8	30	53.4	–12
2140	65.9 + j18.2	65.6 – j21.2	4.45 + j1.31	29.4	44.9	31	54.2	–11
2170	69.5 + j20.2	65.5 – j20.8	4.24 + j1.26	29.5	44.9	31	55.2	–12

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 15. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1A} = 24 mA, I_{DQ2A} = 149 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	69.5 + j18.1	74.2 – j19.6	2.36 + j3.84	32.7	42.3	17	61.2	–12
2140	65.9 + j18.2	73.0 – j21.6	2.42 + j3.87	32.6	42.3	17	62.1	–11
2170	69.5 + j20.2	72.4 – j21.5	2.60 + j3.58	32.6	42.8	19	63.2	–11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	69.5 + j18.1	70.8 – j20.0	2.62 + j3.53	30.7	43.5	22	60.9	–15
2140	65.9 + j18.2	69.3 – j21.7	2.66 + j3.46	30.6	43.5	23	61.8	–15
2170	69.5 + j20.2	69.5 – j21.7	2.48 + j3.34	30.6	43.5	22	63.0	–16

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

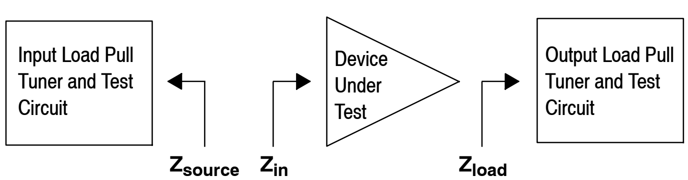


Table 16. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 43 mA, V_{GS2B} = 1.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	63.5 + j9.31	67.9 – j12.2	2.29 + j0.28	27.7	46.3	43	54.8	–15
2140	68.4 + j14.6	70.3 – j18.9	2.35 + j0.19	27.6	46.3	43	54.0	–15
2170	73.3 + j22.8	72.1 – j25.6	2.32 + j0.09	27.6	46.3	43	54.0	–16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	63.5 + j9.31	67.3 – j18.4	2.42 + j0.19	25.6	46.9	49	55.2	–19
2140	68.4 + j14.6	68.2 – j25.0	2.50 + j0.10	25.6	46.8	48	54.3	–19
2170	73.3 + j22.8	68.6 – j31.3	2.55 – j0.04	25.5	46.8	48	53.9	–21

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

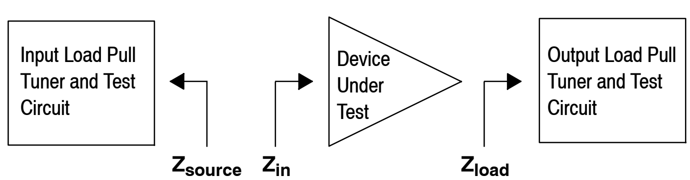
Table 17. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ1B} = 43 mA, V_{GS2B} = 1.3 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	63.5 + j9.31	71.0 – j8.08	1.53 + j1.79	28.3	44.6	29	64.0	–20
2140	68.4 + j14.6	74.6 – j15.1	1.51 + j1.73	28.2	44.5	28	63.3	–21
2170	73.3 + j22.8	76.8 – j23.1	1.67 + j1.62	28.2	44.8	30	62.8	–22

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	63.5 + j9.31	70.4 – j13.3	1.61 + j1.61	26.4	45.5	35	63.1	–26
2140	68.4 + j14.6	72.6 – j20.3	1.57 + j1.51	26.3	45.5	35	62.4	–26
2170	73.3 + j22.8	74.0 – j27.8	1.67 + j1.49	26.3	45.4	35	61.9	–28

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

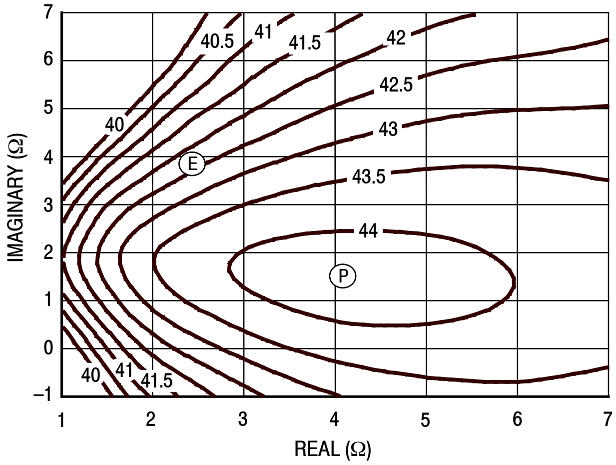


Figure 30. P1dB Load Pull Output Power Contours (dBm)

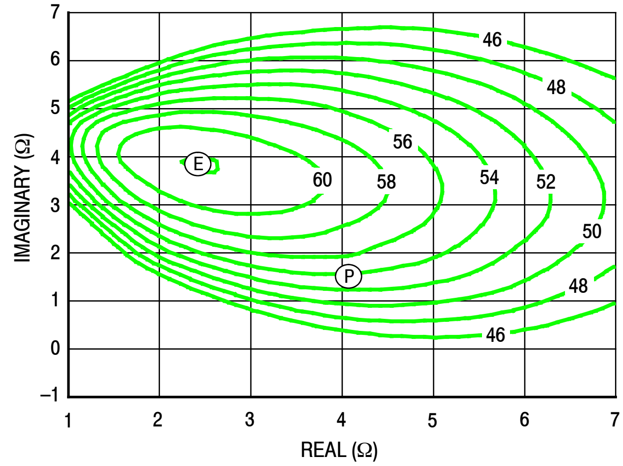


Figure 31. P1dB Load Pull Efficiency Contours (%)

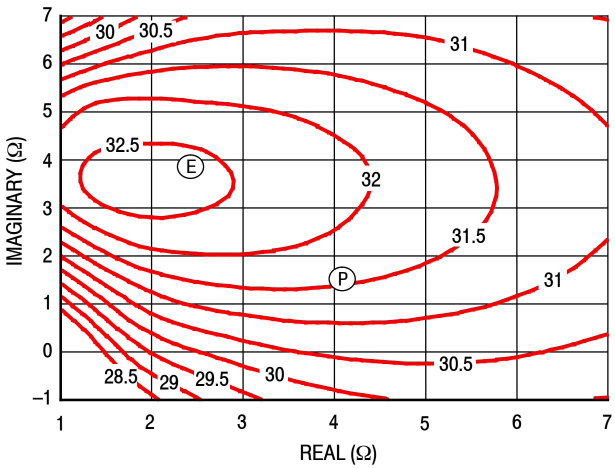


Figure 32. P1dB Load Pull Gain Contours (dB)

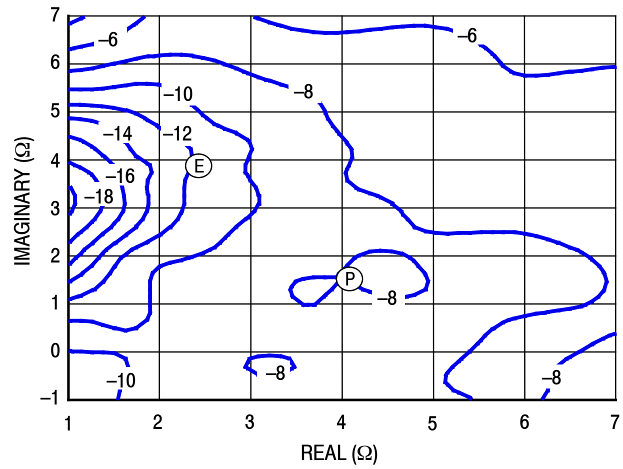


Figure 33. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power
E = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz

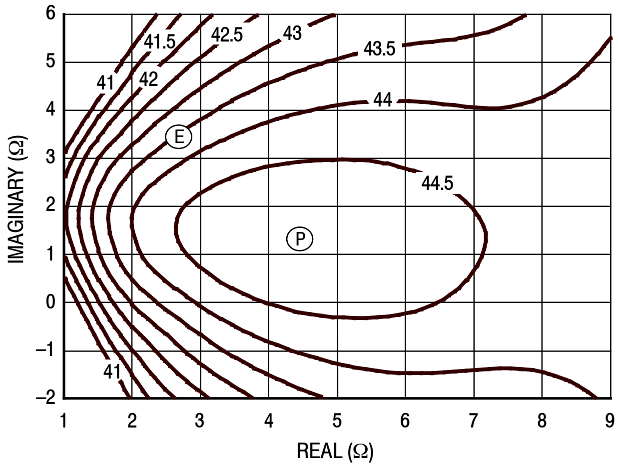


Figure 34. P3dB Load Pull Output Power Contours (dBm)

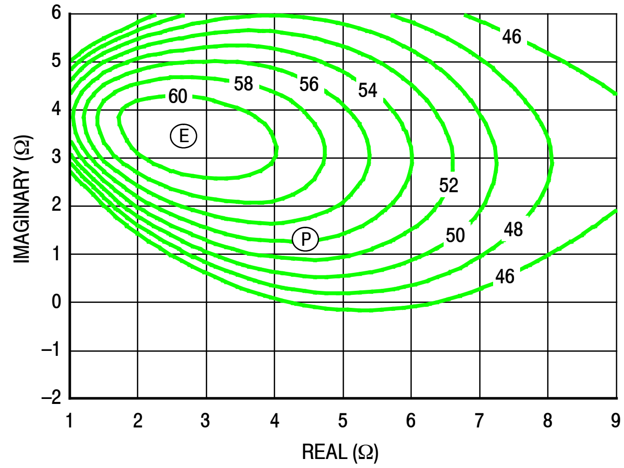


Figure 35. P3dB Load Pull Efficiency Contours (%)

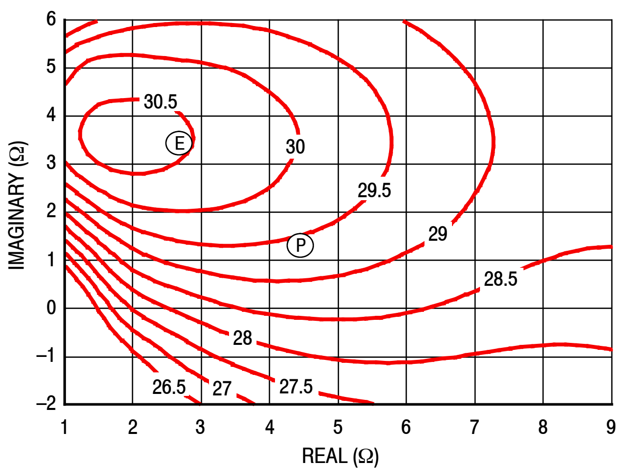


Figure 36. P3dB Load Pull Gain Contours (dB)

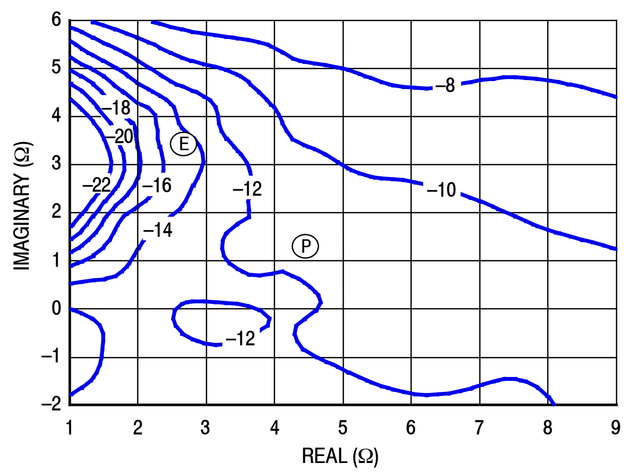


Figure 37. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

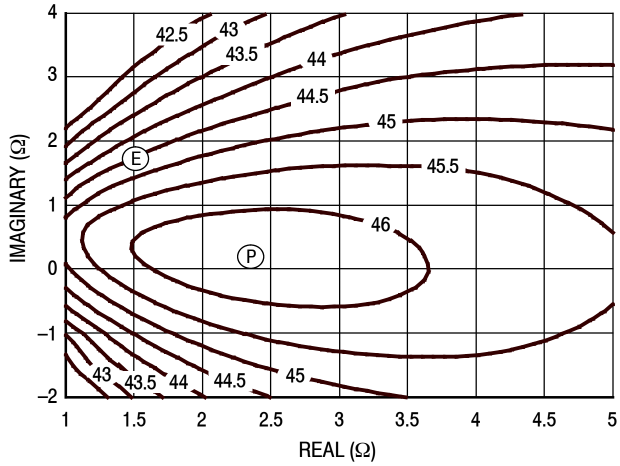


Figure 38. P1dB Load Pull Output Power Contours (dBm)

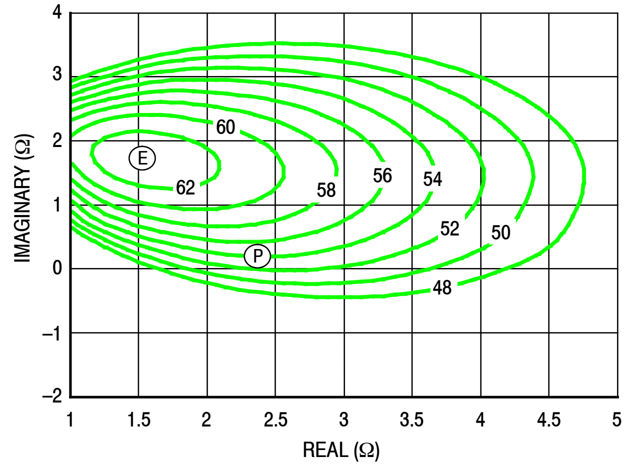


Figure 39. P1dB Load Pull Efficiency Contours (%)

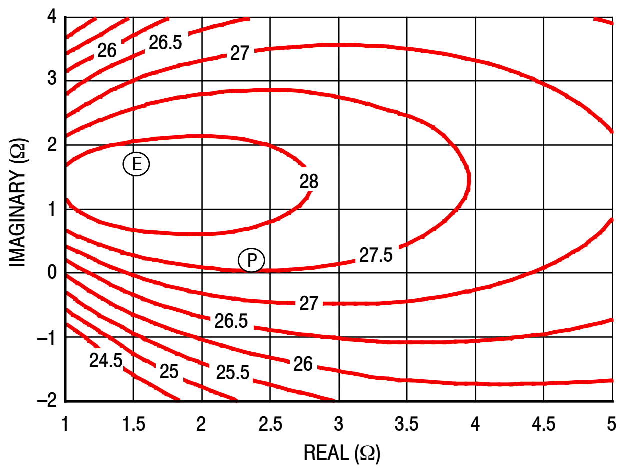


Figure 40. P1dB Load Pull Gain Contours (dB)

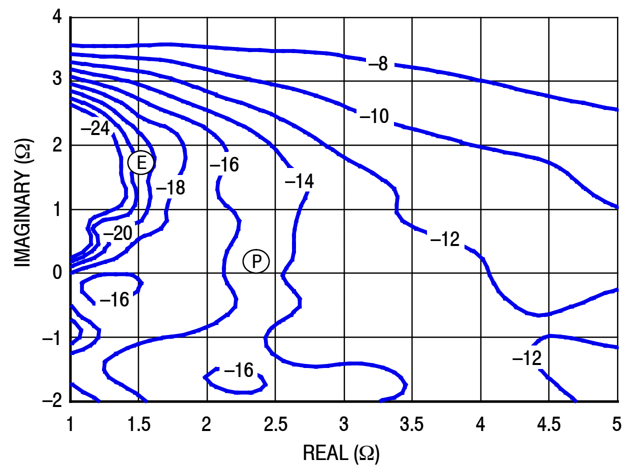


Figure 41. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

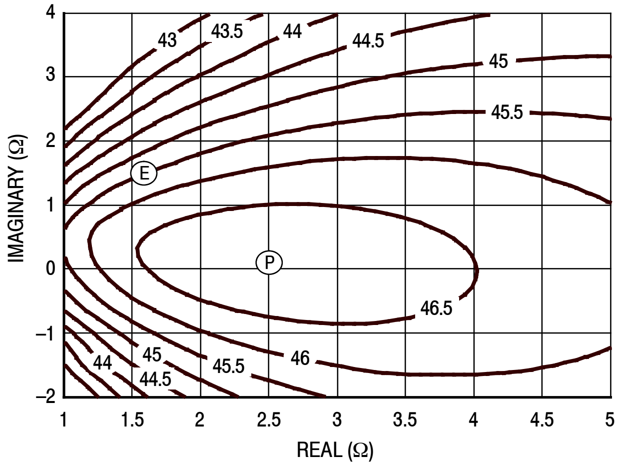


Figure 42. P3dB Load Pull Output Power Contours (dBm)

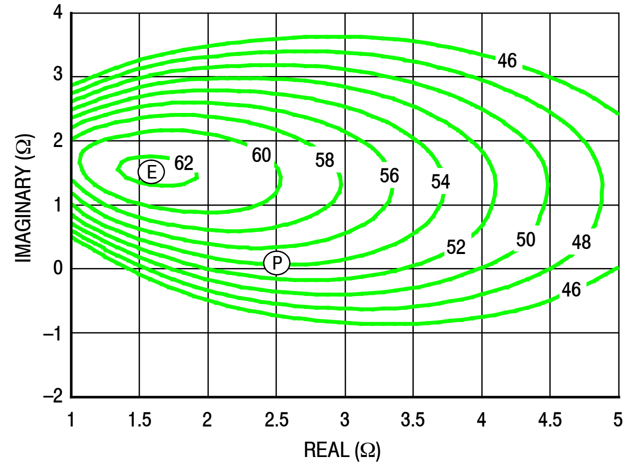


Figure 43. P3dB Load Pull Efficiency Contours (%)

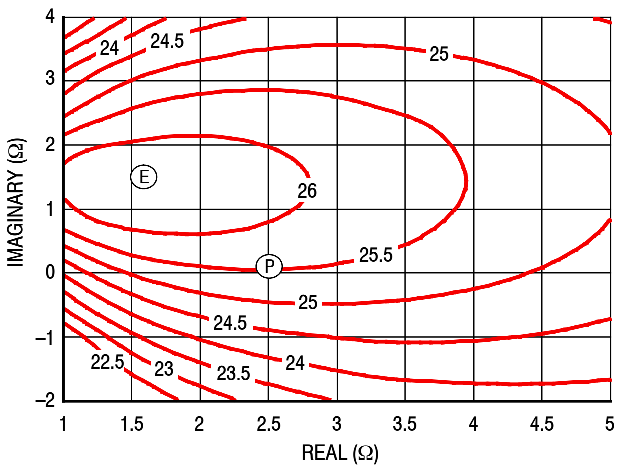


Figure 44. P3dB Load Pull Gain Contours (dB)

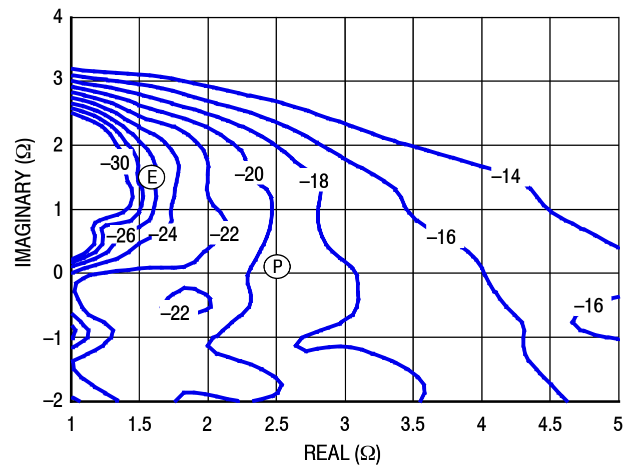


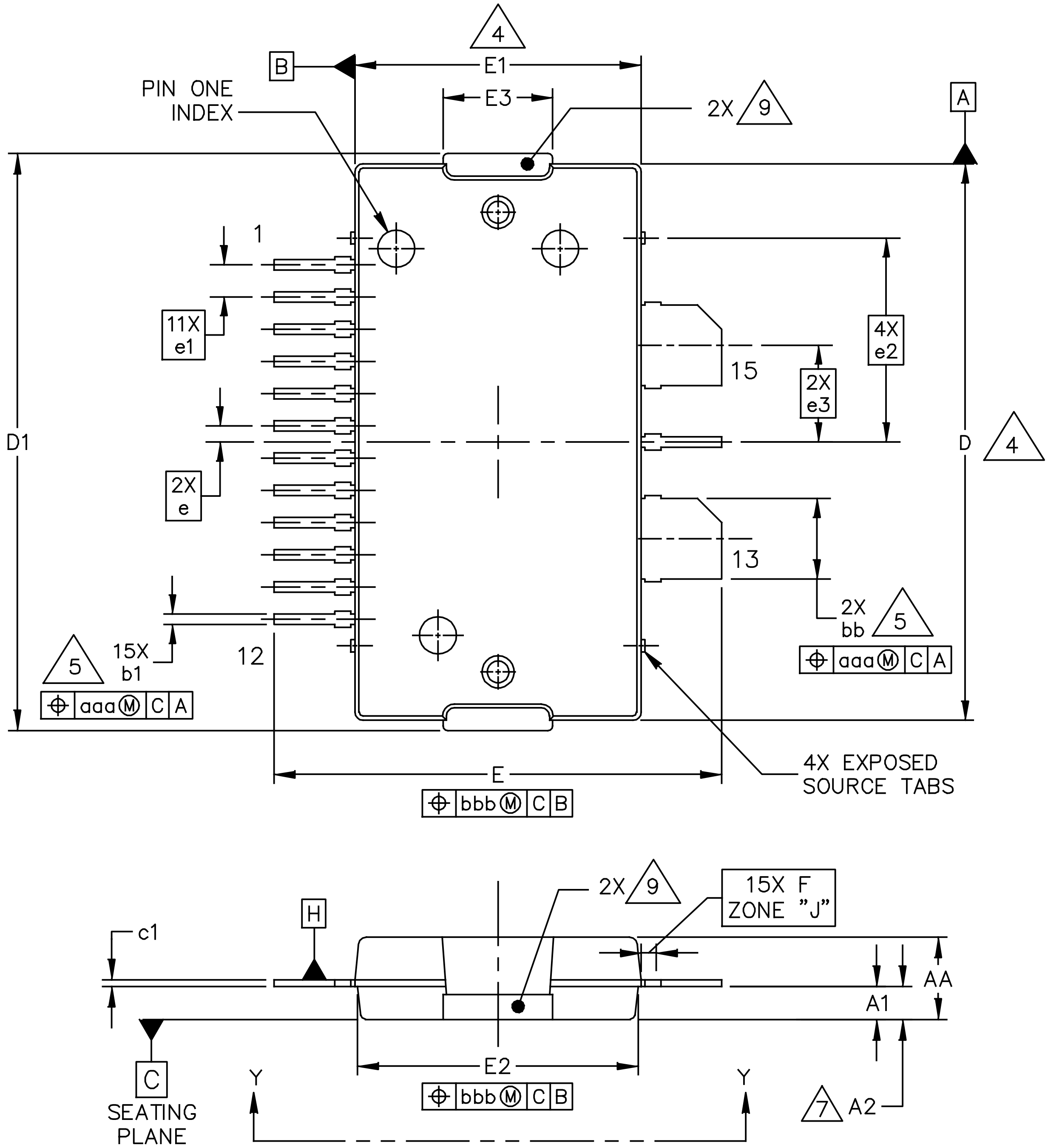
Figure 45. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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TITLE: TO–270WB–15	DOCUMENT NO: 98ASA00630D REV: 0	
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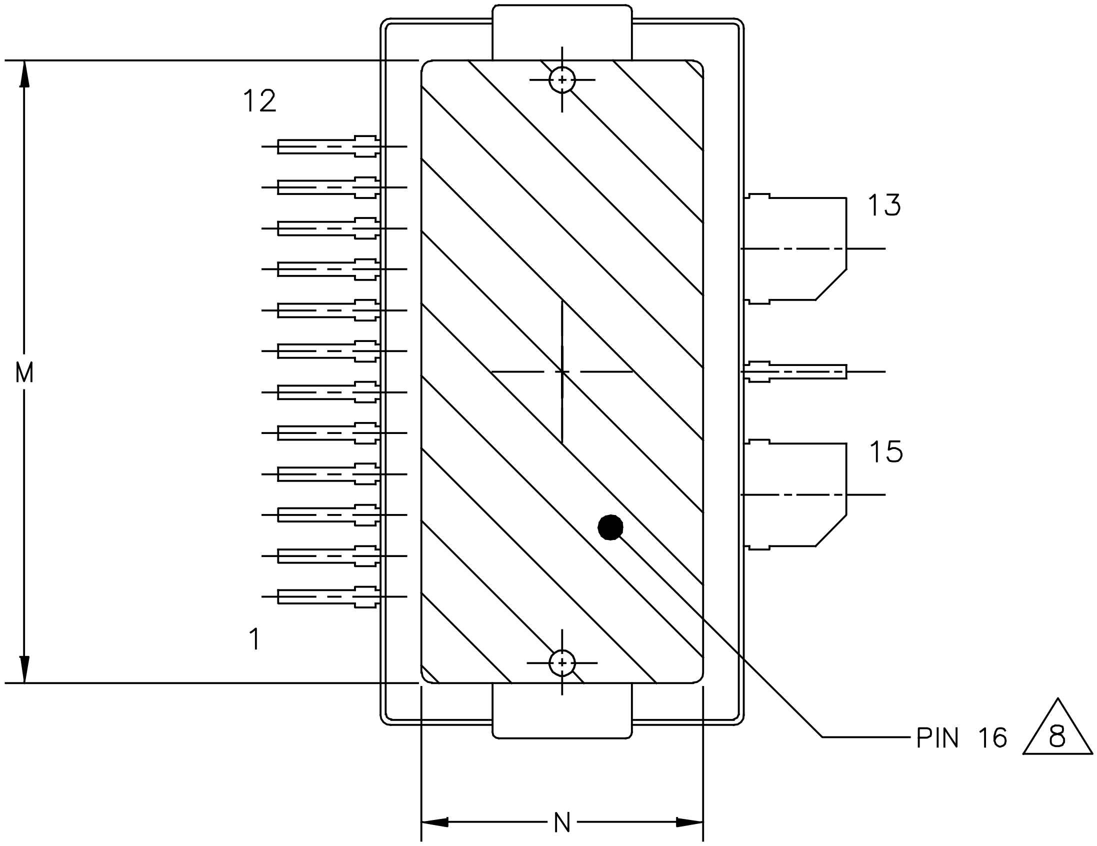

VIEW Y–Y

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	17 JUN 2014	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.039	.043	0.99	1.09	N	.270	----	6.86	----
A2	.040	.042	1.02	1.07	bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.551	.559	14.00	14.20	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

MECHANICAL OUTLINE

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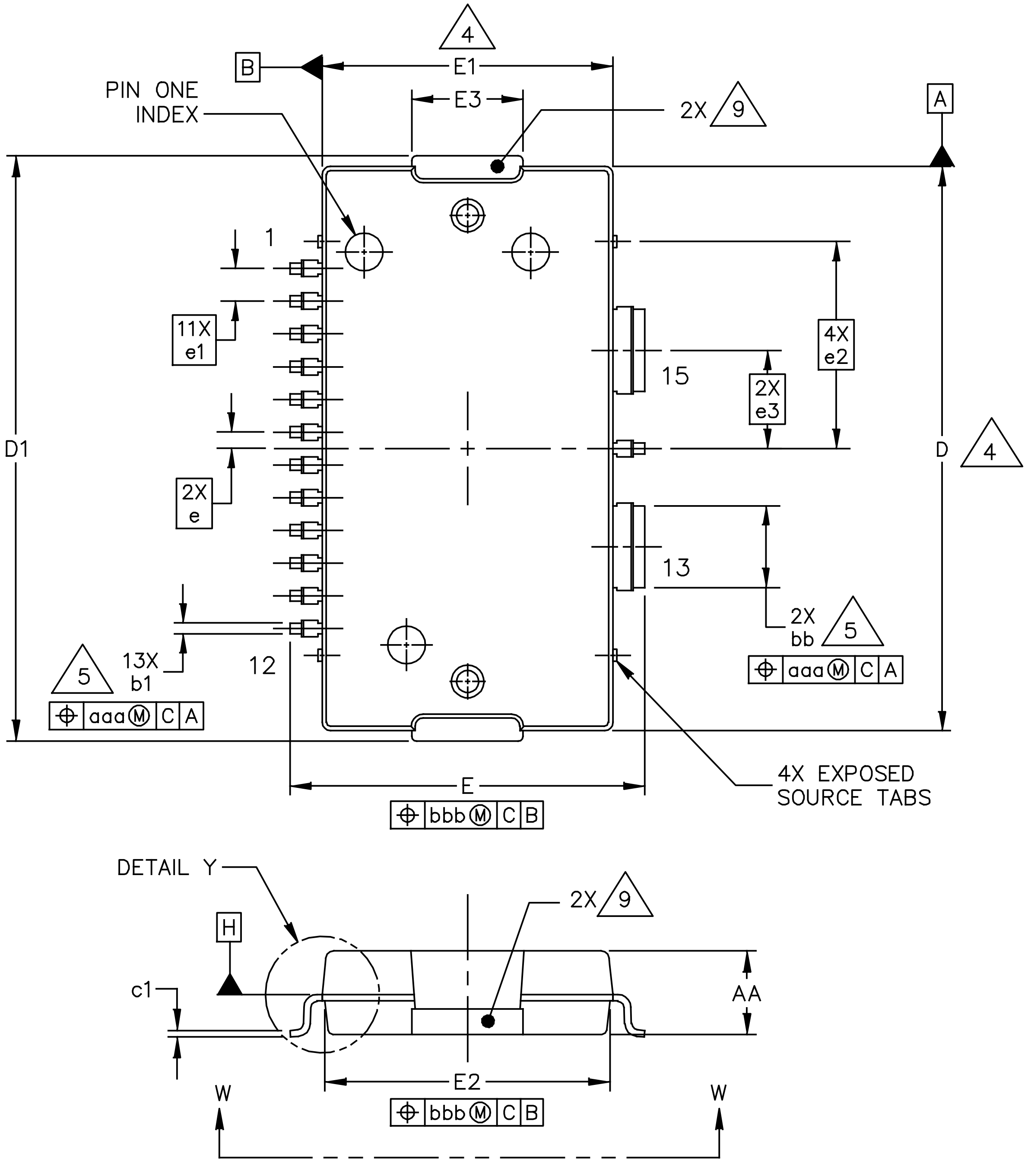

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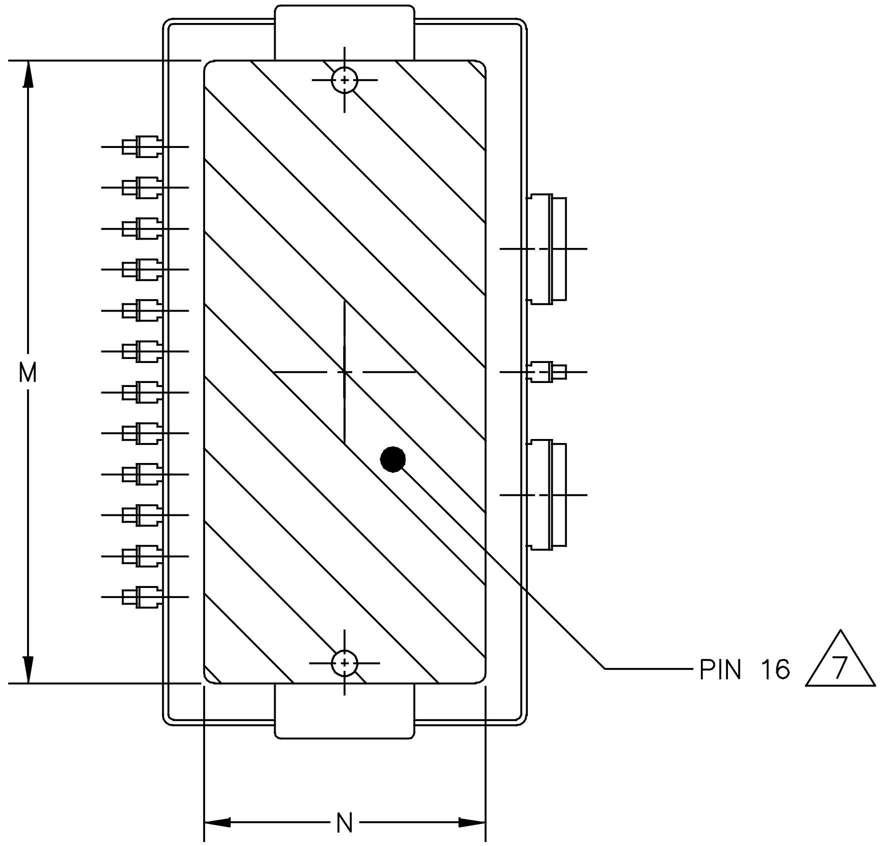
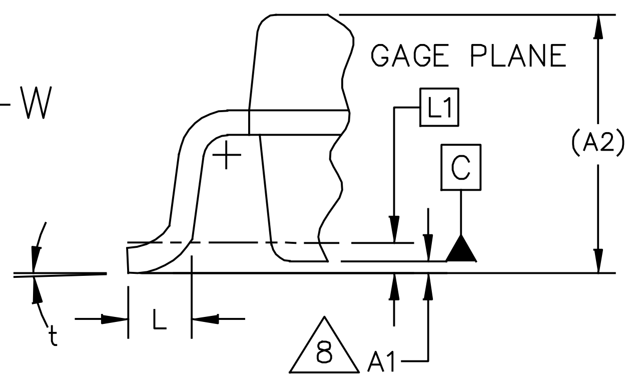
	17 JUN 2014	



VIEW W—W



DETAIL "Y"

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		17 JUN 2014

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	M	.600	----	15.24	----
A1	.001	.004	0.03	0.10	N	.270	----	6.86	----
A2	(.105)		(2.67)		bb	.097	.103	2.46	2.62
D	.688	.692	17.48	17.58	b1	.010	.016	0.25	0.41
D1	.712	.720	18.08	18.29	c1	.007	.011	0.18	0.28
E	.429	.437	10.90	11.10	e	.020 BSC		0.51 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.253 INFO ONLY		6.43 INFO ONLY	
E3	.132	.140	3.35	3.56	e3	.120 BSC		3.05 BSC	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
					bbb	.008		0.20	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2016	• Initial release of data sheet

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Rev. 0, 2/2016