±2.0A DDR Termination Regulator

■ FEATURES

- Meets DDR-SDRAM Power Supplies
- ±2A Source and Sink Current
- Supply Voltage 2.7 to 5.5V
- VREF Voltage Accuracy VDDQ×0.49 to 0.51
- VTT Voltage Accuracy VREF±40mV
- Status at EN Low VTT Output: OFF (Discharge)
  VREF Output: Active
- Correspond to external VREF source
- Correspond to MLCC
- Thermal Shutdown Protection
- Power Good (PG)
- Over Current Protection
- Under Voltage Lock Out (UVLO)
- VTT discharge function
- Package NJW4118MJE: EQFN16-JE

■ GENERAL DESCRIPTION

The NJW4118 is a sink/source (±2A) termination regulator for DDR-SDRAM

The NJW4118 contains a high-speed operational amplifier that provides excellent transient response.

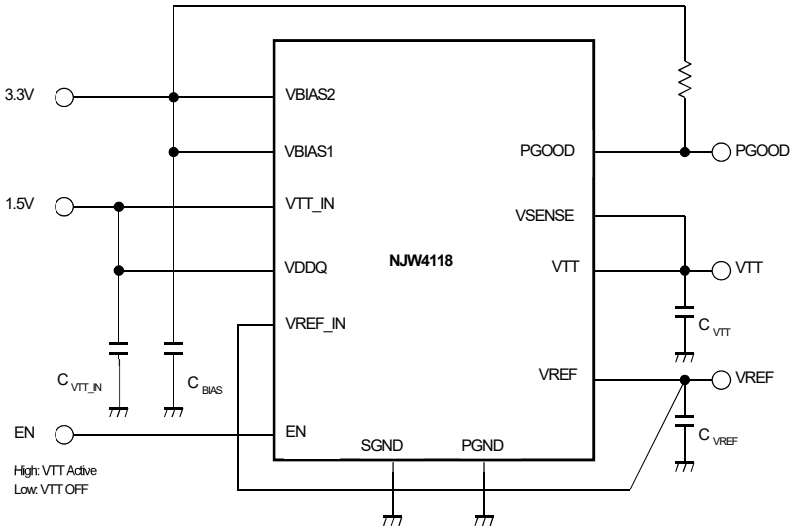
The NJW4118 can configure the two patterns of VREF + VTT output or VTT standalone output by change of wiring.
Even if VREF is generated outside, VTT is able to subordinate to VREF because there is VREF_IN Pin.
When using at VTT standalone, it is possible to contribute to low power consumption because VREF circuit can be completely stopped.

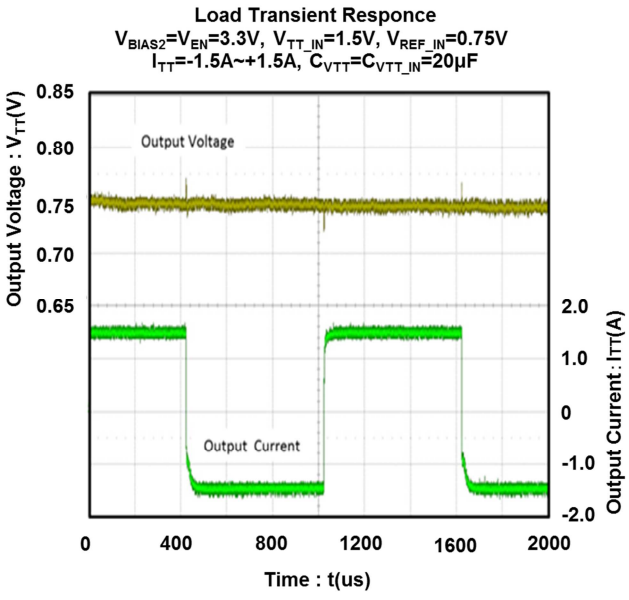
Regarding the EN function, each output becomes as the following status: VREF is Active and VTT is OFF (Discharge) at EN=Low.

■ TARGET APPLICATION

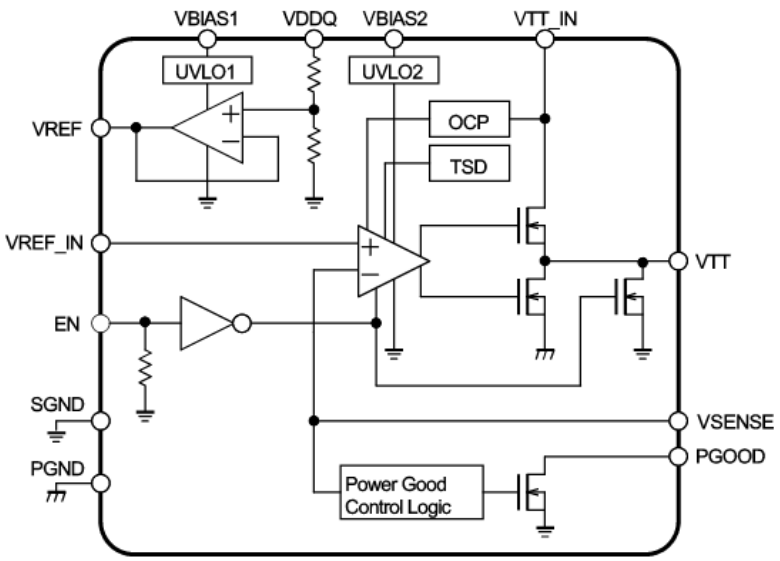
- Automotive
- Industrial Equipment
  and other.

■ APPLICATION

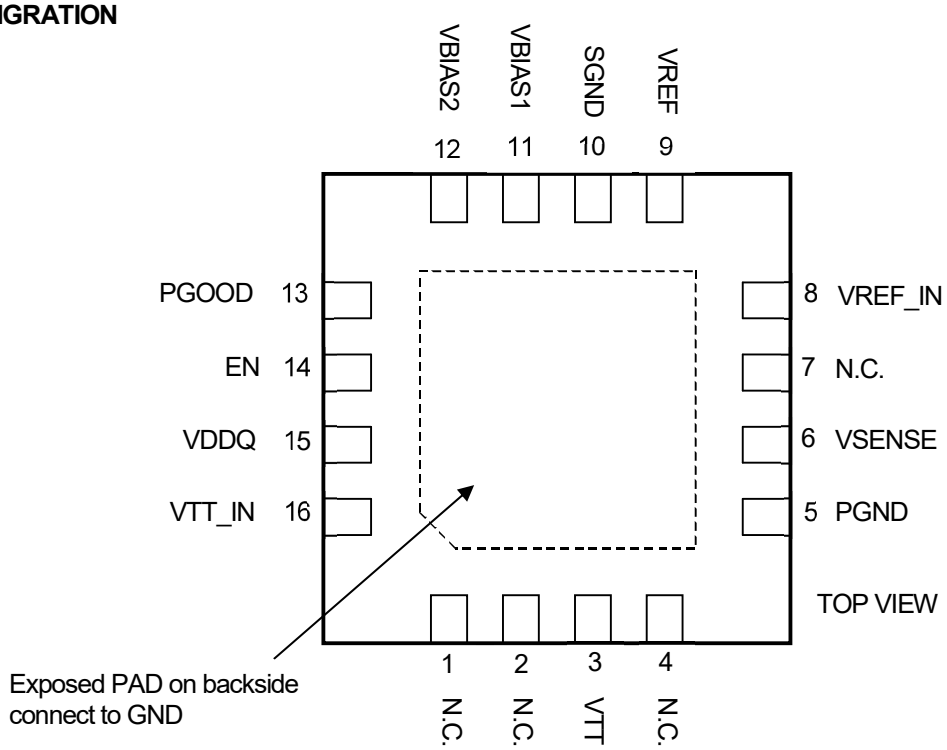




■ BLOCK DIAGRAM

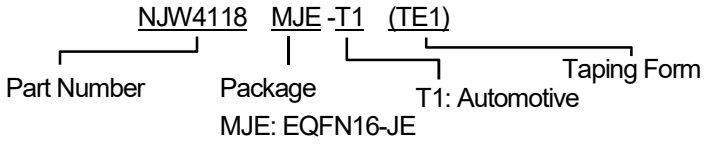


■ PIN CONFIGRATION



Pin number	Name	Function	Pin number	Name	Function
1	N.C.	N.C.	9	VREF	VREF output
2	N.C.	N.C.	10	SGND	Signal ground
3	VTT	VTT Output	11	VBIAS1	VREF circuit power supply input
4	N.C.	N.C.	12	VBIAS2	Termination circuit power supply input
5	PGND	Power ground	13	PGOOD	Power good output
6	VSENSE	VTT sense input (Should be connected to C_{VTT} or the + pin of load)	14	EN	Enable control input
7	N.C.	N.C.	15	VDDQ	VDDQ input
8	VREF_IN	VREF input	16	VTT_IN	Power supply input for VTT

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	AUTO MOTIVE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4118MJE-T1(TE1)	EQFN16-JE	yes	yes	yes	Sn2Bi	4118T1	17	1500

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum rating	Unit
VTT_IN pin voltage	V_{TT_IN}	-0.3 to +4	V
VBIAS1 pin voltage	V_{BIAS1}	-0.3 to +7	V
VBIAS pin voltage 端子電圧	V_{BIAS2}	-0.3 to +7	V
VDDQ pin voltage	V_{DDQ}	-0.3 to +7	V
EN pin voltage	V_{EN}	-0.3 to +7	V
VREF_IN 端子電圧	V_{REF_IN}	-0.3 to +7	V
Power Dissipation (Ta=25°C) EQFN16-JE	P_D	720(1)	mW
		1800(2)	
Junction temperature	Tj	-40 to +150	°C
Operating temperature	Topr	-40 to +125	°C
Storage temperature	Tstg	-50 to +150	°C

(1): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2layers, with Exposed Pad)
(2): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4layers, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
VBIAS1 pin Voltage (3)	V_{BIAS1}	2.7 to 5.5	V
VBIAS2 pin Voltage (3)	V_{BIAS2}	2.7 to 5.5	V
VTT_IN pin Voltage(4)	V_{TT_IN}	V_{DDQ}	V
VDDQ pin Voltage (5)	V_{DDQ}	1.14 to 2.55	V
EN pin Voltage	V_{EN}	0 to 5.5	V
VREF_IN pin Voltage	V_{REF_IN}	$0.5 \times V_{DDQ}$	V

(3): You should use under the condition of $V_{BIAS} > V_{TT}+1.95V$.
(4): If using a voltage of VTT_IN less than 1.5V, the maximum output current of V_{TT} is limited
(5): You should apply the same voltage as VDDQ of DDR.

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{BIAS1}=3.3V, V_{BIAS2}=3.3V, V_{DDQ}=1.5V, V_{TT_IN}=1.5V, V_{EN}=3.3V, T_a=25°C, C_{BIAS}=1µF, C_{VTT_IN}=20µF, C_{VREF}=1µF, C_{VTT}=20µF)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Quiescent Current						
VBIAS1 Quiescent Current	I_{BIAS1}	V_{EN}=3.3V, I_{REF}=0mA	-	50	100	µA
		V_{EN}=3.3V, I_{REF}=0mA Ta=-40°C to 125°C	-	-	100	
VBIAS2 Quiescent Current	I_{BIAS2_1}	V_{EN}=3.3V, I_{TT}=0mA	-	2	3.2	mA
		V_{EN}=3.3V, I_{TT} =0mA Ta=-40°C to 125°C	-	-	3.6	
	I_{BIAS2_2}	V_{EN}=3.3V, I_{TT}=2.0A	-	3	4.2	mA
		V_{EN}=3.3V, I_{TT} =2.0A Ta=-40°C to 125°C	-	-	4.6	
VBIAS2 Quiescent Current in Stand-by	I_{BIAS2_STB}	V_{EN}=0V, I_{TT}=0mA (Include I_{BIAS1})	-	100	140	µA
		V_{EN}=0V, I_{TT}=0mA (Include I_{BIAS1}) Ta=-40°C to 125°C	-	-	160	
VTT_IN Quiescent Current	I_{VTT_IN}	I_{TT}=0mA	-	-	1	µA
		I_{TT}=0mA Ta=-40°C to 125°C	-	-	5	
Reference Block						
Reference Output Voltage (DDR2)	V_{REF2}	V_{BIAS1}=V_{BIAS2}=5.0V V_{DDQ}=V_{TT_IN}=1.8V I_{REF}= -1mA to 1mA	V_{DDQ} × 0.49	V_{DDQ} × 0.5	V_{DDQ}× 0.51	V
		V_{BIAS1}=V_{BIAS2}=5.0V V_{DDQ}=V_{TT_IN}=1.8V I_{REF}= -1mA to 1mA Ta=-40°C to 125°C	V_{DDQ} × 0.49	-	V_{DDQ}× 0.51	
Reference Output Voltage (DDR3)	V_{REF3}	V_{BIAS1}=V_{BIAS2}=3.3V V_{DDQ}=V_{TT_IN}=1.5V I_{REF}= -1mA to 1mA	V_{DDQ} × 0.49	V_{DDQ} × 0.5	V_{DDQ}× 0.51	V
		V_{BIAS1}=V_{BIAS2}=3.3V V_{DDQ}=V_{TT_IN}=1.5V I_{REF}= -1mA to 1mA Ta=-40°C to 125°C	V_{DDQ} × 0.49	-	V_{DDQ}× 0.51	
Reference Source Current	I_{REF_H}		1	-	-	mA
		Ta=-40°C to 125°C	1	-	-	
Reference Sink Current	I_{REF_L}		1	-	-	mA
		Ta=-40°C to 125°C	1	-	-	
VDDQ Input Impedance	Z_{VDDQ}		-	100	-	kΩ

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{BIAS1}=3.3V, V_{BIAS2}=3.3V, V_{DDQ}=1.5V, V_{TT_IN}=1.5V, V_{EN}=3.3V, T_a=25°C,
C_{BIAS}=1µF, C_{VTT_IN}=20µF, C_{VREF}=1µF, C_{VTT}=20µF)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Termination Output Block						
VTT Output Voltage (DDR2)	V_{TT2}	V_{BIAS1}=V_{BIAS2}=5.0V V_{DDQ}=V_{TT_IN}=1.8V I_{TT}= -2.0A to 2.0A	V_{REF} - 40m	V_{REF}	V_{REF} +40m	V
		V_{BIAS1}=V_{BIAS2}=5.0V V_{DDQ}=V_{TT_IN}=1.8V I_{TT}= -2.0A to 2.0A Ta=-40°C to 125°C	V_{REF} - 40m	-	V_{REF} +40m	
VTT Output Voltage (DDR3)	V_{TT3}	V_{BIAS1}=V_{BIAS2}=3.3V V_{DDQ}=V_{TT_IN}=1.5V I_{TT}= -2.0A to 2.0A	V_{REF} - 40m	V_{REF}	V_{REF} +40m	V
		V_{BIAS1}=V_{BIAS2}=3.3V V_{DDQ}=V_{TT_IN}=1.5V I_{TT}= -2.0A to 2.0A Ta=-40°C to 125°C	V_{REF} - 40m	-	V_{REF} +40m	
VTT Source Current Limit	I_{TTLIM_H}		2	3.5	-	A
		Ta=-40°C to 125°C	2	-	-	
VTT Sink Current Limit	I_{TTLIM_L}		2	3.5	-	A
		Ta=-40°C to 125°C	2	-	-	
High Side-MOSFET $R_{DS(ON)}$	R_{ON_H}	Source, I_{TT}=2.0A(VTT to GND)	-	260	380	mΩ
		Source, I_{TT}=2.0A(VTT to GND) Ta=-40°C to 125°C	-	-	380	
Low Side-MOSFET $R_{DS(ON)}$	R_{ON_L}	Sink, I_{TT}=2.0A (VTT_IN to VTT)	-	260	380	mΩ
		Sink, I_{TT}=2.0A (VTT_IN to VTT) Ta=-40°C to 125°C	-	-	380	
VREF_IN Input Current	I_{REF_IN}	V_{REF_IN}=0.75V I_{TT}=0mA	-	-	4.8	µA
		V_{REF_IN}=0.75V I_{TT}=0mA Ta=-40°C to 125°C	-	-	5.5	
VSENSE Input Current	I_{SENSE}	V_{SENSE}=0.75V	-	-	2.6	µA
		V_{SENSE}=0.75V Ta=-40°C to 125°C	-	-	3.5	
Discharge FET ON Resistance	R_{DISCH}	V_{REF_IN}=0V, VTT=0.3V V_{EN}=0V	-	6	-	Ω

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{BIAS1}=3.3V, V_{BIAS2}=3.3V, V_{DDQ}=1.5V, V_{TT_IN}=1.5V, V_{EN}=3.3V, T_a=25°C, C_{BIAS}=1µF, C_{VTT_IN}=20µF, C_{VREF}=1µF, C_{VTT}=20µF)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable Control Block						
High Level Threshold Voltage	V_{THH_EN}	V_{EN}=L→H	1.6	-	-	V
		V_{EN}=L→H Ta=-40°C to 125°C	1.6	-	-	
Low Level Threshold Voltage	V_{THL_EN}	V_{EN}=H→L	-	-	0.6	V
		V_{EN}=H→L Ta=-40°C to 125°C	-	-	0.6	
Enable Current	I_{EN}	V_{EN}=1.6V	-	3	12	µA
		V_{EN}=1.6V Ta=-40°C to 125°C	-	-	12	
UVLO Block						
UVLO1 ON Threshold Voltage	V_{UVLO1_ON}	V_{BIAS1}=L→H	2.2	2.35	2.5	V
		V_{BIAS1}=L→H Ta=-40°C to 125°C	2.2	2.35	2.5	
UVLO1 Hysteresis	V_{UVLO1_HYS}	V_{BIAS1}=H→L	-	70	-	mV
UVLO2 ON Threshold Voltage	V_{UVLO2_ON}	V_{BIAS2}=L→H	2.2	2.35	2.5	V
		V_{BIAS2}=L→H Ta=-40°C to 125°C	2.2	2.35	2.5	
UVLO2 Hysteresis	V_{UVLO2_HYS}	V_{BIAS2}=H→L	-	70	-	mV
Power Good Block						
High Level Detection Voltage	V_{THH_PG}	Measured at V_{SENSE} pin	106	111	116	%
		Measured at V_{SENSE} pin Ta=-40°C to 125°C	106	-	116	
Low Level Detection Voltage	V_{THL_PG}	Measured at V_{SENSE} pin Rising	84	89	94	%
		Measured at V_{SENSE} pin Rising Ta=-40°C to 125°C	84	-	94	
Low Level Detection Voltage Hysteresis	V_{HYS_PG}	V_{SENSE} Falling	-	-5	-	%
Leak Current at OFF state	I_{LEAK_PG}	V_{SENSE}=V_{REF_IN} PGood=V_{BIAS2}	-	-	1	µA
		V_{SENSE}=V_{REF_IN} PGood=V_{BIAS2} Ta=-40°C to 125°C	-	-	1	
Power Good ON Resistance	R_{ON_PG}	I_{PG}=4mA	-	15	-	Ω

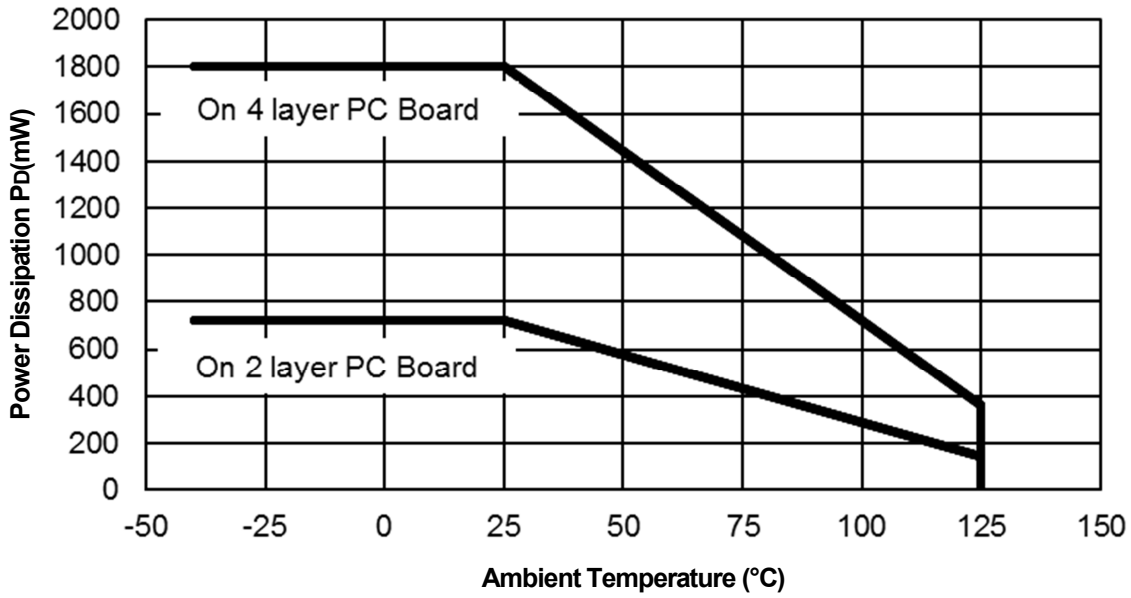
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient Thermal resistance	θja	173 (6) 68 (7)	°C/W
Junction-to-Top of package Characterization parameter	ψjt	20 (6) 10 (7)	°C/W

(6): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2layers, with Exposed Pad)
(7): Mounted on glass epoxy board.
(101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4layers, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

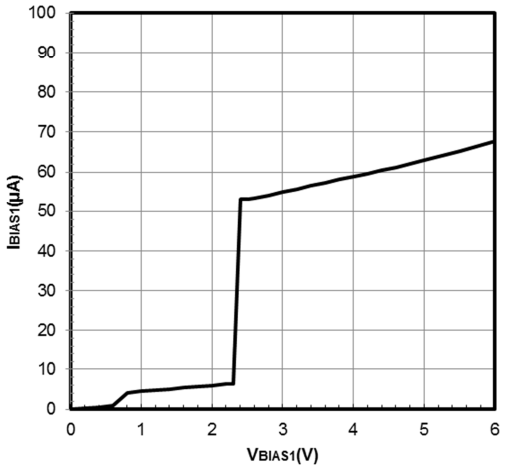
NJW4118 (EQFN16 Package)
Power Dissipation vs. Ambient Temperature
(Topr=-40°C to +125°C Tj=to 150°C)



■ TYPICAL CHARACTERISTICS

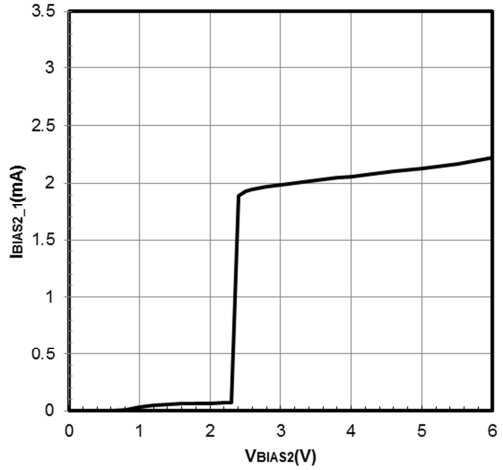
IBIAS1 vs. VBIAS1

VBIAS2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2, Ta=25℃



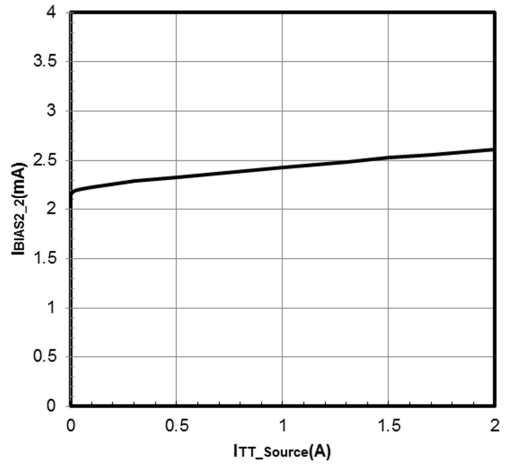
IBIAS2_1 vs. VBIAS2

VBIAS1=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2,CVTT=10μFx2, Ta=25℃



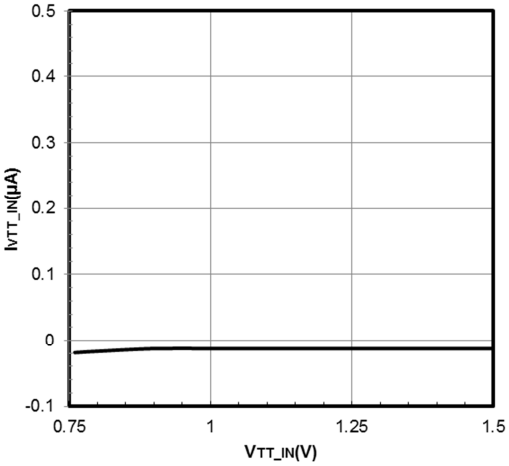
IBIAS2_2 vs. ITT_Source

VBIAS1_2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2, Ta=25℃



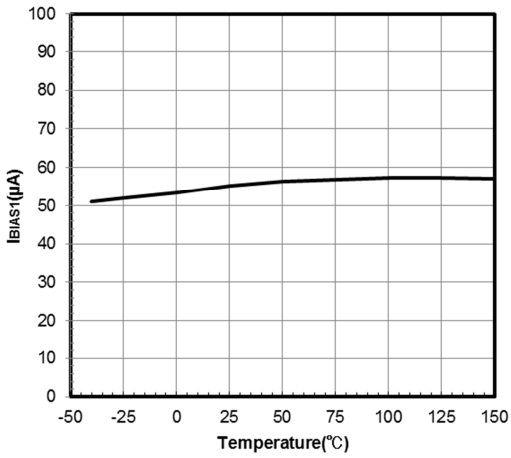
IVTT_IN vs. VTT_IN

VBIAS1_2=VEN=3.3V, VDDQ=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2, Ta=25℃



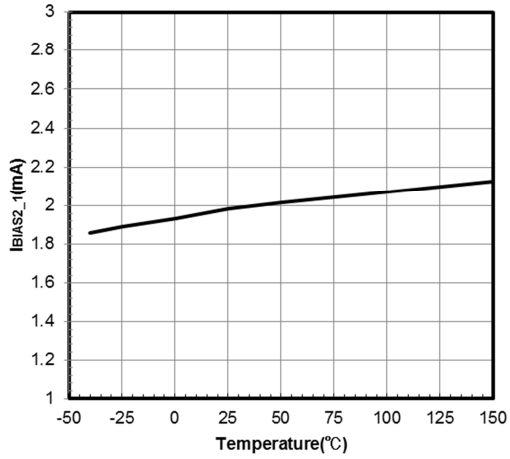
IBIAS1 vs. Temperature

VBIAS1_2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



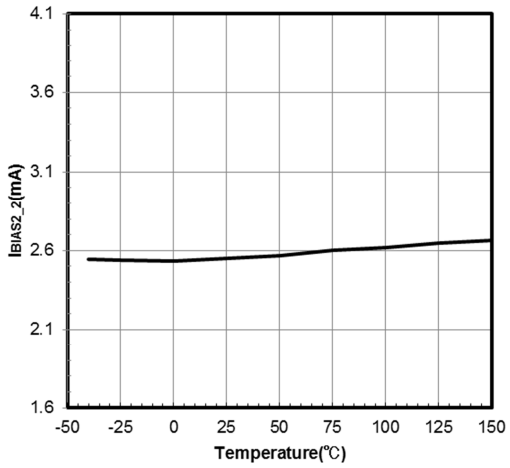
IBIAS2_1 vs. Temperature

VBIAS1_2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2

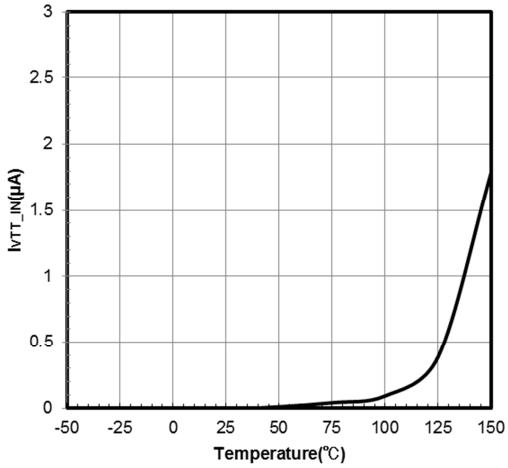


■ TYPICAL CHARACTERISTICS

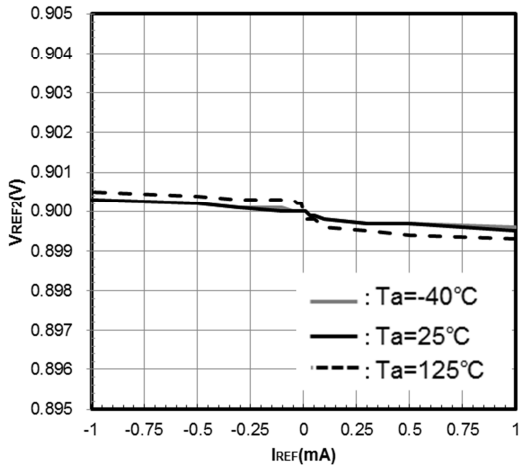
IBIAS2_2 vs. Temperature
VBIAS1_2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



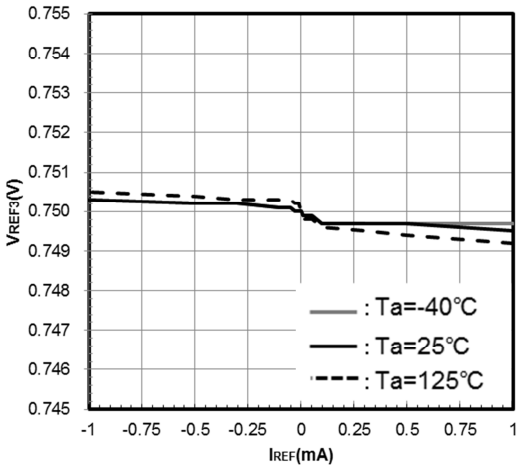
IVTT_IN vs. Temperature
VBIAS1_2=VEN=3.3V, VDDQ=VTT_IN=1.5V, VREF=VREF_IN, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



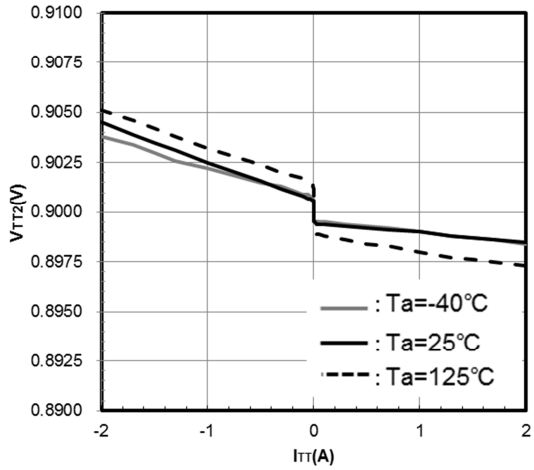
VREF2 vs. IREF (DDR2)
VBIAS1=VBIAS2=VEN=5.0V, VDDQ=VTT_IN=1.8V
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



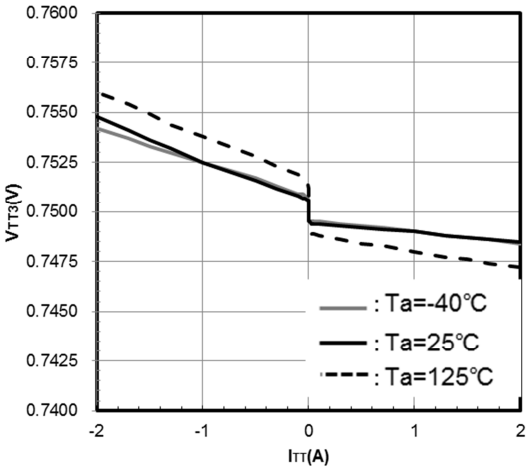
VREF3 vs. IREF (DDR3)
VBIAS1=VBIAS2=VEN=3.3V, VDDQ=VTT_IN=1.5V
CBIAS=1.0μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



VTT2 vs. ITT (DDR2)
VBIAS2=VEN=5.0V, VTT_IN=1.8V, VREF_IN=0.9V, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



VTT3 vs. ITT (DDR3)
VBIAS2=VEN=3.3V, VTT_IN=1.5V, VREF_IN=0.75V, VTT=VSENSE
CBIAS=1μF, CREF=1μF, CVTT_IN=10μFx2, CVTT=10μFx2



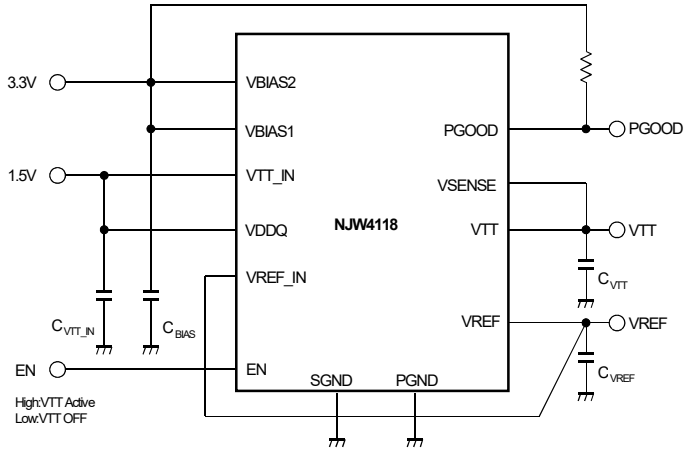
■ PIN DISCRIPTION

Pin No.	Name	Function
1	N.C.	Non Connection
2	N.C.	Non Connection
3	VTT	VTT Output
4	N.C.	Non Connection
5	PGND	Power Ground
6	VSENSE	VTT sense input (Should be connected to C_{VTT} or the + pin of load)
7	N.C.	Non Connection
8	VREF_IN	VREF input for VTT
9	VREF	VREF Output. The output voltage is 1/2 of the voltage input to the VDDQ pin.
10	SGND	Signal Ground
11	VBIAS1	VREF circuit power supply input
12	VBIAS2	Termination circuit power supply input
13	PGOOD	Power good output .Connect a pull-up resistor.
14	EN	Enable control input
15	VDDQ	VDDQ input
16	VTT_IN	Power supply input for VTT

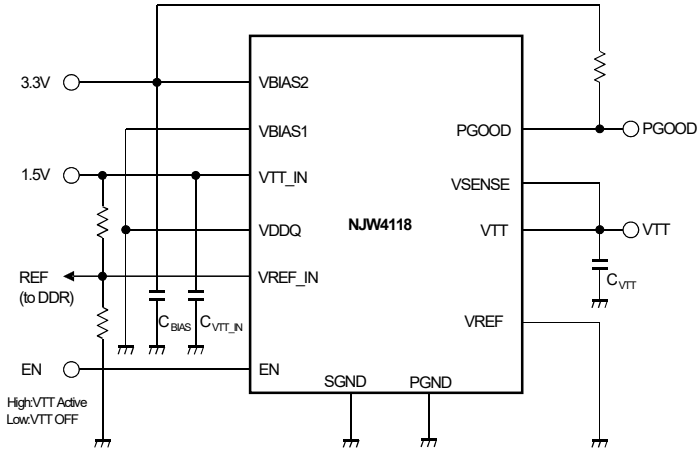
Technical Information

■ TYPACAL APPLICATIONS (DDR3)

・Using Internal Vref.



・Using external Vref.



- Input Capacitor C_{VTT_IN}・C_{BIAS}

  Input Capacitor C_{VTT_IN}・C_{BIAS} are required to prevent oscillation and reduce power supply ripple for applications when high power supply impedance or a long power supply line.

  Therefore, use the recommended value; C_{VTT_IN}=20μF,C_{BIAS}=1μF or larger and should connect between GND and each pin(*1) as shortest path as possible to avoid the problem.

  (*1 each pin: VTT_IN,VDDQ,VBIAS1,VBIAS2)

  Regarding C_{VTT_IN}, in order to cope with rapid transient variation of VTT pin, please select a capacitor of low ESR and ESL. It is recommended that you use to connect the two parallel GRM21BR70J106KE76L(Murata Co., Ltd.).

- Output Capacitor C_{VTT}・C_{VREF}

  Output capacitor C_{VTT}・C_{VREF} are required for a phase compensation of the internal error amplifier.

  The capacitance and the Equivalent Series Resistance (ESR) influence to stable operation of the regulator.

  Using smaller C_{VTT}・C_{VREF} may cause excess output noise or oscillation of the regulator due to lack of the phase compensation.

  Therefore, use the recommended value; C_{VTT}=20μF,C_{VREF}=1μF or larger and should connect between VTT – GND and VREF - GND as shortest path as possible for stable operation.

  On the other hand, using larger C_{VTT}・C_{VREF} reduces output noise and ripple output, and also improves output transient response when a load rapidly changes.

  Regarding C_{VTT}, in order to correspond to the loop stability and rapid transients, please select a capacitor of low ESR and ESL. It is recommended that you use to connect to the two parallel GRM21BR70J106KE76L (Murata Co., Ltd.).

  In addition, you should consider varied characteristics of a capacitor (a frequency characteristic, a temperature characteristic, a DC bias characteristic and so on) and unevenness peculiar to a capacitor supplier enough.

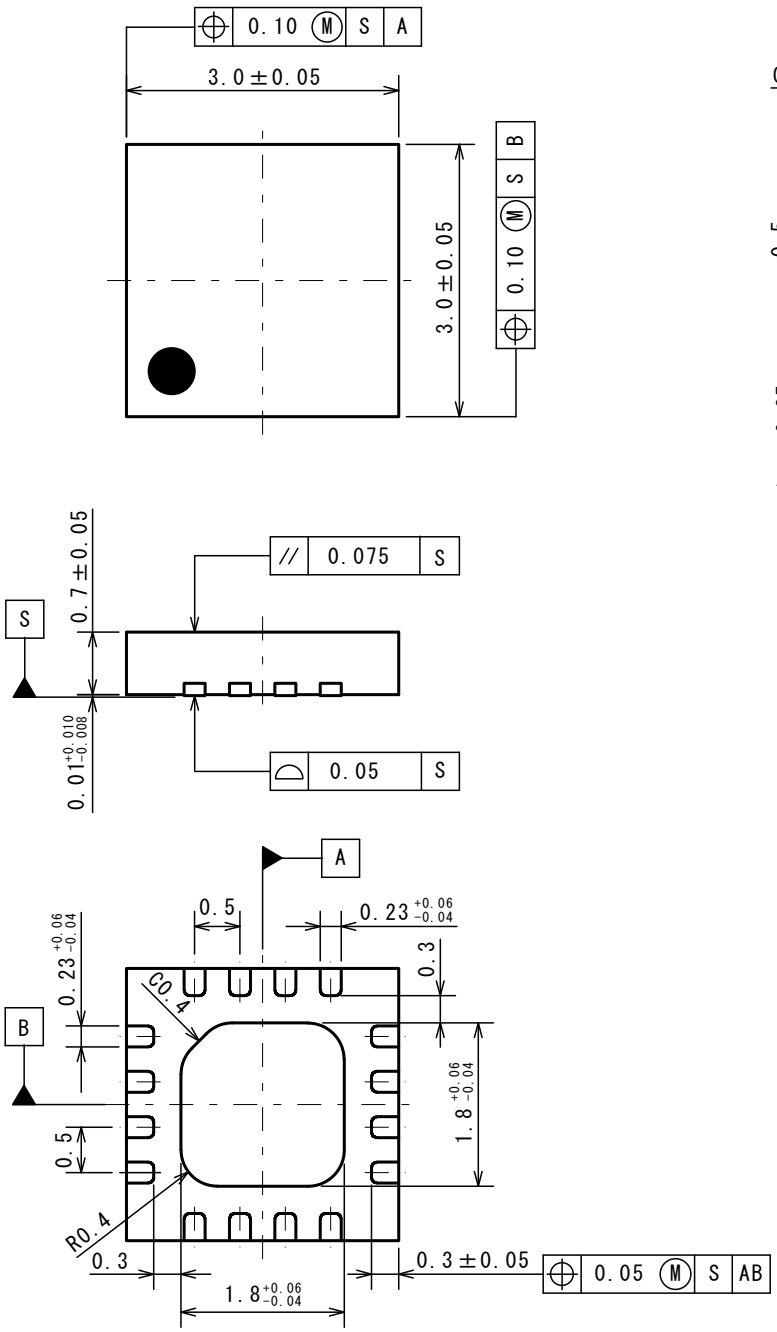
- Regarding the GND line, it is preferred to separate the power system and the signal system in order to prevent influence of a resistance of layout pattern and a voltage variation by large current, and use single ground point. Also the GND line of external parts should be considered in the same way.

  The layout pattern of GND should be designed to be low impedance.

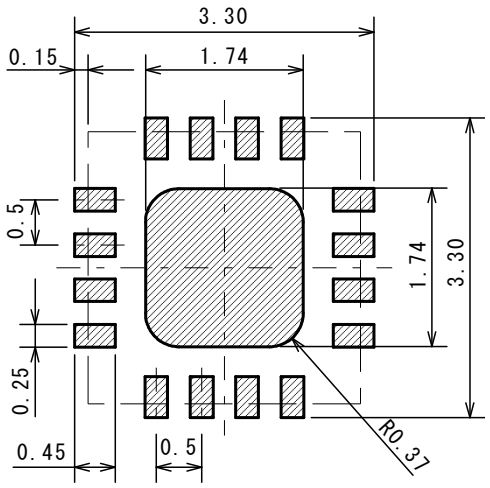
EQFN16-JE

Unit: mm

■PACKAGE DIMENSIONS



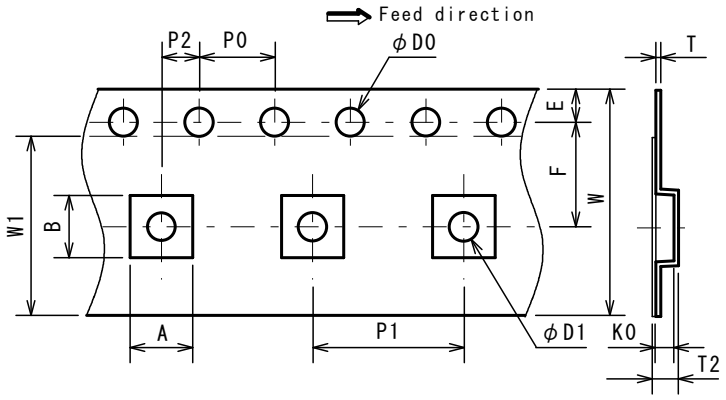
■EXAMPLE OF SOLDER PADS DIMENSIONS



■PACKING SPEC

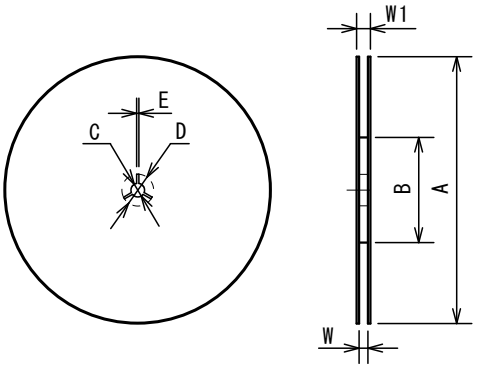
Unit: mm

TAPING DIMENSIONS



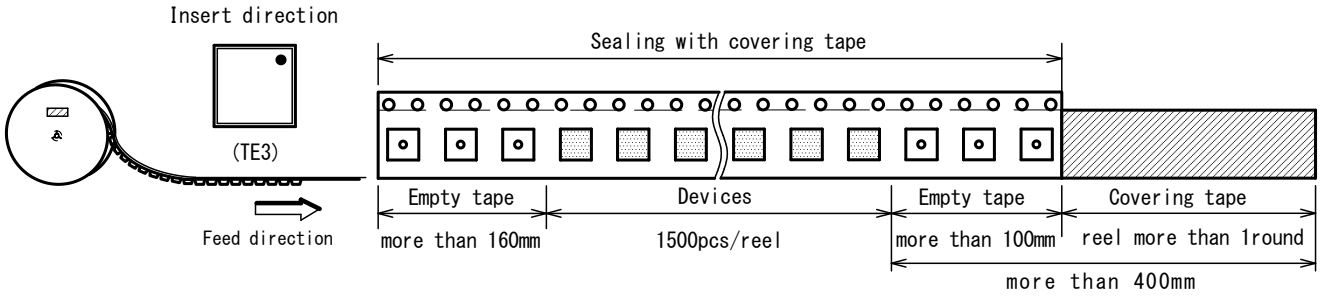
SYMBOL	DIMENSION	REMARKS
A	3.3±0.1	BOTTOM DIMENSION
B	3.3±0.1	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	1.3±0.07	
K0	0.9±0.05	
W	$12.0^{+0.3}_{-0.1}$	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

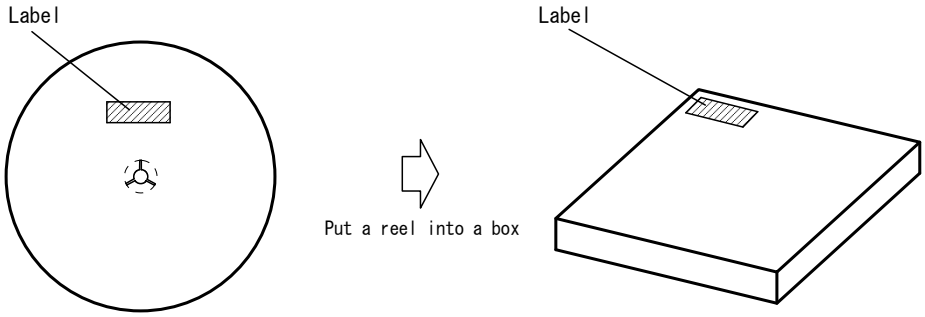


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-3.0}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	$13^{+1.0}_{0}$
W1	15.4±1.0

TAPING STATE



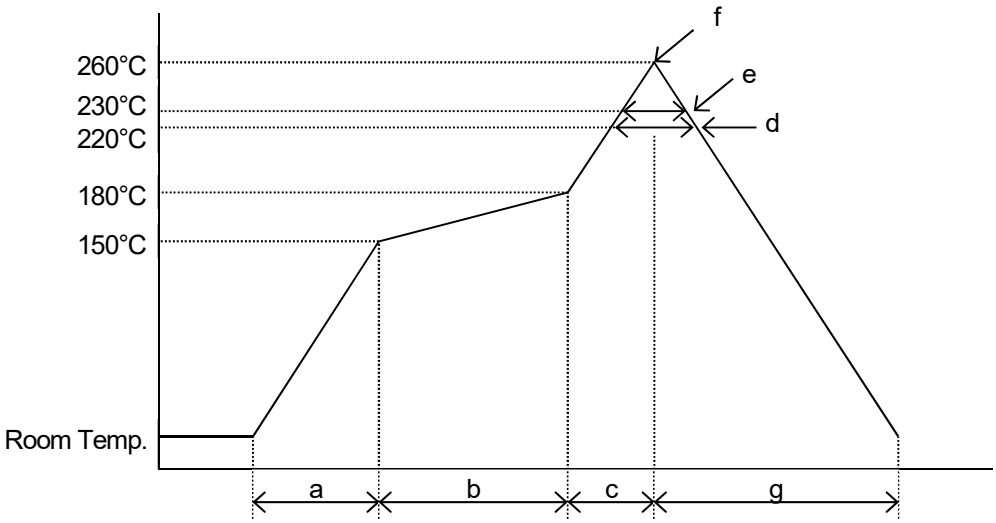
PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a: Temperature ramping rate	: 1 to 4°C /s
b: Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c: Temperature ramp rate	: 1 to 4°C /s
d: 220°C or higher time	: Shorter than 60s
e: 230°C or higher time	: Shorter than 40s
f: Peak temperature	: Lower than 260°C
g: Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■ **REVISION HISTORY**

DATE	DIVISION	CHANGES
3. Apr. 2018	Ver.1.0	New Release

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