Voice Switched Speakerphone Circuit with Speaker Amplifier

■ GENERAL DESCRIPTION

The **NJW1128** is a Voice Switched Speakerphone Circuit. It includes all of functions processing a high quality hands–free speakerphone system, such as the necessary amplifiers (Mic , Receive ,Line, Speaker), attenuators, level detectors functions.

The **NJW1128** is controllable independently power-down of the speaker amplifier and the entire IC excluding the speaker amplifier.

All external capacitors are sufficient small so that ceramic capacitors are applied.

■ PACKAGE OUTLINE

NJW1128FR3

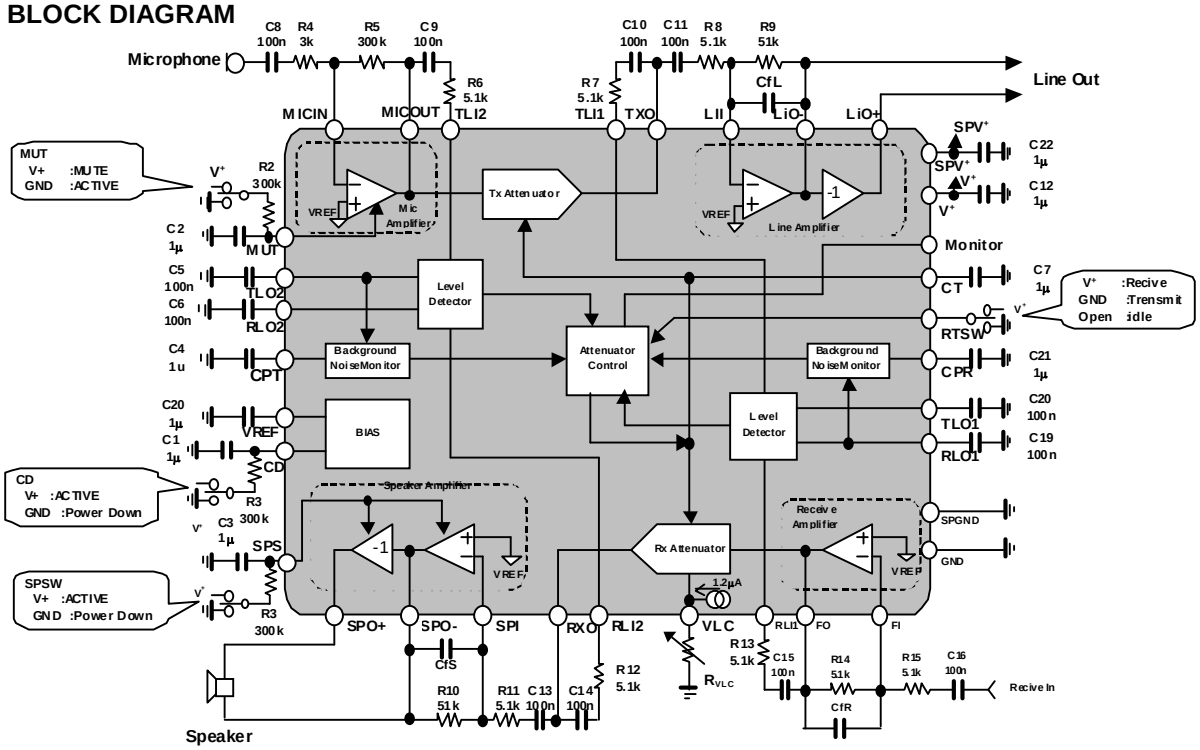
■ APPLICATION

- Video Door Phone
- Conference System
- Wireless Application
- Security System

■ FEATURES

- Operating voltage range 3.9 to 5.5V
- Attenuator gain range between Transmit and Receive 52dB
- Speaker amplifier
- Microphone amplifier with mute function
- Force to Receive, Transmit, or Idle modes
- Mode –watching monitor
- Background noise monitor for each path
- 4-point signal sensing
- Chip disable Pin powers down the entire IC excluding the speaker amplifier
- Speaker switch Pin power down the speaker amplifier
- Microphone and Receive Amplifiers pinned out for flexibility
- Package Outline LQFP48-R3

■ BLOCK DIAGRAM



■ **ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_+	7	V
Power Dissipation	P_D	1,330(Note1)	mW
Operating Temperature Range	Topr	-40 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C
Maximum Input Voltage	V_{IMAX}	0 ~ V^+ (Note2)	V

(Note1) EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting

■ **OPERATING VOLTAGE**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+	-	3.9	5.0	5.5	V

■ **ELECTRICAL CHARACTERISTICS** ($Ta=25°C, V^+=5V$, MUT=CD=SPSW= ACTIVE ,RTSW=OPEN, $R_{VLC}=0\Omega$, MIC Amplifier Gv=0dB, Receive Amplifier Gv=0dB)

●Power Supply

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	I_{CC1}	RX-mode (Receive)	2.0	3.5	6.0	mA
Operating Current 2	I_{CC2}	TX-mode (Transmit)	2.0	3.5	6.0	mA
Operating Current 3	I_{CC3}	Idle-mode (Standby)	2.0	3.5	6.0	mA
Operating Current 4	I_{CC4}	Idle-mode (Standby) , SPSW=PD	1.0	2.5	4.0	mA
Operating Current 5	I_{CC5}	CD=PD,SPSW=PD	0.5	1	1.5	mA
Reference Voltage	V_{REF}	Idle-mode (Standby)	2.2	2.5	2.8	V

●Receive Attenuator(RxIN=200Vrms,Receive Amplifier Gv=0dB)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Receive Attenuator Gain 1	G_{R1}	RX-mode (Receive)	3.0	6.0	9.0	dB
Receive Attenuator Gain 2	G_{R2}	TX-mode (Transmit)	-50	-46	-42	dB
Receive Attenuator Gain 3	G_{R3}	Idle-mode (Standby), CRT=CPR=V^+	-23	-20	-17	dB
Range R to T mode	dG_R	RX-mode – TX-mode	47	52	57	dB
Dynamic DC offset	G_{RDC}	RX-mode – TX-mode (DC)	-50	-	50	mV
Volume control range	G_{RVR}	RX-mode,$R_{VLC}=0\Omega$-100kΩ	35	45	55	dB

●Transmit Attenuator (TxIN=200Vrms,Mic.amplifier Gv=0dB)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transmit Attenuator Gain 1	G_{T1}	TX-mode (Transmit)	3.0	6.0	9.0	dB
Transmit Attenuator Gain 2	G_{T2}	RX-mode (Receive)	-50	-46	-42	dB
Transmit Attenuator Gain 3	G_{T3}	Idle-mode, (Standby) CRT=CPR=V^+	-23	-20	-17	dB
Range R to T mode	dG_T	TX-mode – RX-mode	47	52	57	dB
Dynamic DC offset	G_{TDC}	TX-mode – RX-mode (DC)	-50	-	50	mV

●MIC Amplifier(TxIN=1mVrms,Gv=40dB,R_L=5.1kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage	V_{MOS}	R5=300kΩ, $V_{MOS}=V_{MCI}-V_{MCO}$	-50	0.0	50	mV
Input Bias Current	I_{MBIAS}		-	30	-	nA
Voltage Gain 1	G_{VM1}	f=1kHz	-	40	-	dB
Voltage Gain 2	G_{VM2}	f=20kHz	-	36	-	dB
Maximum Output Voltage	V_{MMAX}	THD=1%	1.0	-	-	Vrms
Maximum Attenuation	G_{MMUTE}	MUT=MUTE	-70	-73	-	dB

●Receive Amplifier (RxIN=1mVrms,Gv=40dB,R_L=5.1kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage	V_{ROS}	R14=300kΩ, $V_{FOS}=V_{FI}-V_{FO}$	-50	0.0	50	mV
Input Bias Current	I_{RBIAS}		-	30	-	nA
Voltage Gain 1	G_{VR1}	f=1kHz	-	40	-	dB
Voltage Gain 2	G_{VR2}	f=20kHz	-	36	-	dB
Maximum Output Voltage	V_{RMAX}	THD=1%	1.0	-	-	Vrms

●Line Amplifier (LINEIN=50mVrms, G_V=26dB,R_L=1.2kΩ)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage	V_{LOS}	R9=51kΩ	-50	0.0	50	mV
Input Bias Current	I_{RBIAS}		-	30	-	nA
Voltage Gain 1	G_{vL1}	f=1kHz	-	26	-	nA
Voltage Gain 2	G_{vL2}	f=20kHz	-	25	-	nA
Gain Bandwidth	G_{LBW}	RL=600Ω,LIO	-	1.5	-	MHz
Closed Loop Gain	G_{LC}	RL=1.2kΩ,LIO- to LIO+	-0.5	0	0.5	dB
Maximum Output Voltage	V_{LMAX}	RL=1.2kΩ,THD=1%	2.0	-	-	Vrms
Total Harmonic Distortion	THD_{LN}	G_V=20dB, RL=1.2Ω	-	-	0.5	%

●Speaker Amplifier (SPIN=50mVrms, G_V=26dB,R_L=32Ω)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage	V_{SPOS}	R10=51kΩ	-50	0.0	50	mV
Input Bias Current	I_{SBIAS}		-	0	-	nA
Voltage Gain 1	G_{VSP1}	f=1kHz	-	26	-	dB
Voltage Gain 2	G_{VSP2}	f=20kHz	-	24	-	dB
Voltage Gain 3	G_{VSP3}	f=1kHz, G_{VSP}=6dB,RL=8Ω	-	6	-	dB
Voltage Gain 4	G_{VSO4}	f=20kHz, G_{VSP}=6dB,RL=8Ω	-	4	-	dB
Closed Loop Gain	G_{LC}	SPO- to SPO+	-0.6	0	0.6	dB
Maximum Output Power	Po_{MAX1}	f=1kHz, RL=32Ω,THD=3%	200	300	-	mW
	Po_{MAX2}	f=1kHz, RL=8Ω,THD=3%	300	500	-	mW
Total Harmonic Distortion	THD_{SP1}	VIN=50mVrms,f=1KHz, RL=32Ω,G_{VD}=26dB		-	1.0	%
	THD_{SP2}	VIN=500mVrms,f=1KHz, RL=8Ω,G_{VD}=6dB	-	-	1.0	%

●MONITOR TERMINAL (MON)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
R_X-mode	Rx	-	V^+-0.6	-	V^+	V
T_X-mode	Tx	-	GND	-	0.6	V
Idle-mode	Idle	No Signal	2.4	2.5	2.6	V
Maximum Output Current	I_{MON}	Rx-mode / Tx-mode	-	0.9	-	mA

■ LOGIC CONTROL

●SW CHARACTERISTICS 1 (CD,MUT,SPSW)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL1}	-	-	-	0.3	V
High Level Input Voltage	V_{IH1}	-	1.5	-	-	V

●SW CHARACTERISTICS 2 (RTSW)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL2}	-	-	-	0.3	V
High Level Input Voltage	V_{IH2}	-	V^+-0.3	-	-	V

■ FUNCTION

●CD

INPUT VOLTAGE	STATUS	OPERATION
V_{IH}	ACTIVE	NJW1128 is active.
V_{IL}	PD	NJW1128 is shutdown except Speaker Amplifier.

●MUT

INPUT VOLTAGE	STATUS	OPERATION
V_{IH}	MUTE	The microphone input is mute.
V_{IL}	ACTIVE	The microphone input is active.

●SPSW

INPUT VOLTAGE	STATUS	OPERATION
V_{IH}	ACTIVE	The Speaker Amplifier is Active.
V_{IL}	PD	The Speaker Amplifier is Shutdown.

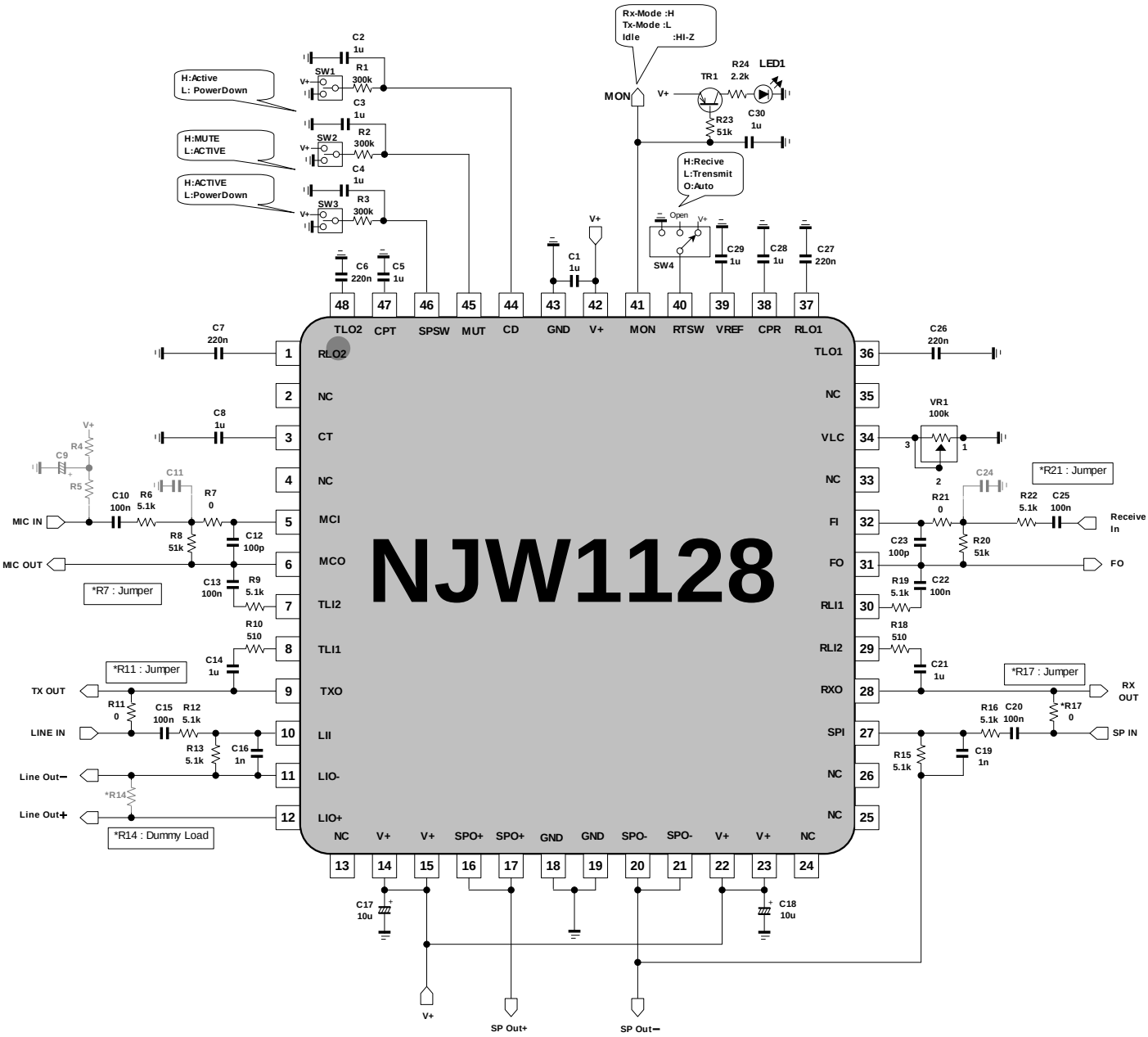
●RTSW

INPUT VOLTAGE	STATUS	OPERATION
V_{IH}	Receive	Force to Receive mode.
OPEN	AUTO	Receive mode and Transmit mode are automatically switched.
V_{IL}	Transmit	Force to Transmit mode.

●R_{VLC} (34pin)

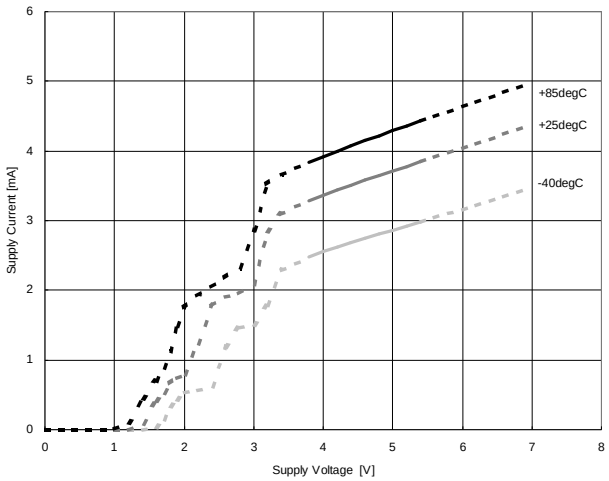
IMPEDANCE	STATUS	OPERATION
0	Vol_{MAM}	The Receive attenuator Volume is maximum.
100kΩ	Vol_{MIN}	The Receive attenuator Volume is minimum.

■ APPLICATION CIRCUIT

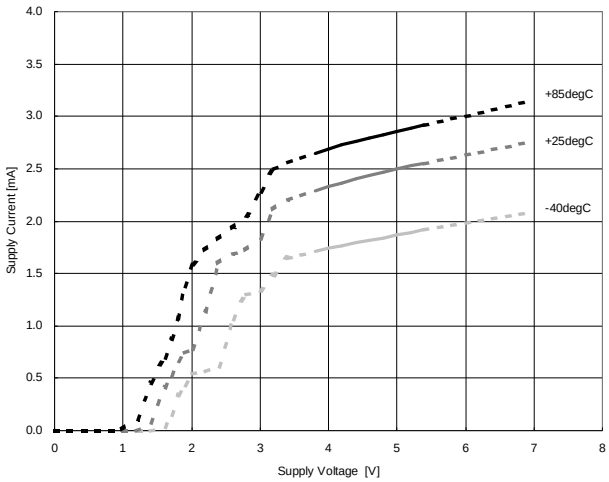


■ TYPICAL CHARACTERISTICS

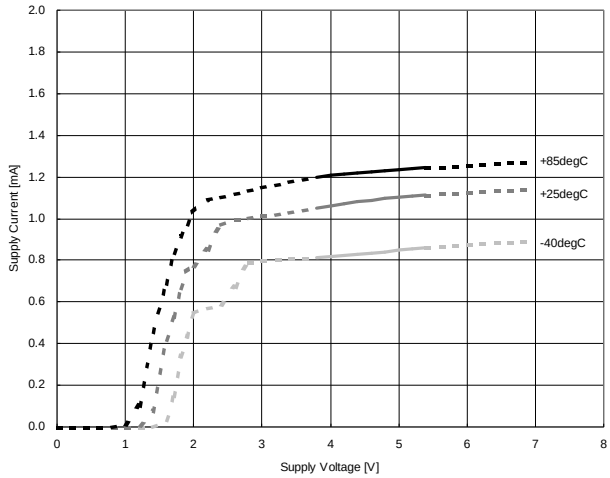
Supply Current vs Supply Voltage
No Signal , Supply Current 1



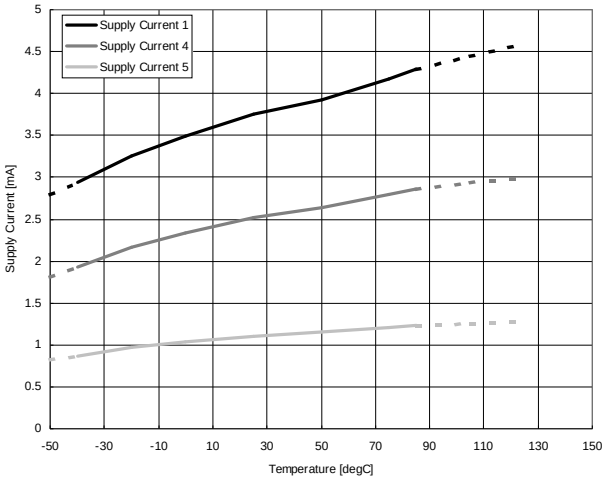
Supply Current vs Supply Voltage
No Signal , Supply Current 4



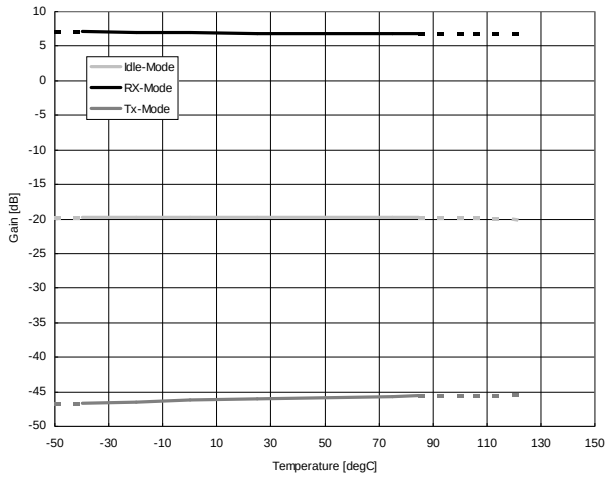
Supply Current vs Supply Voltage
No Signal , Supply Current 5



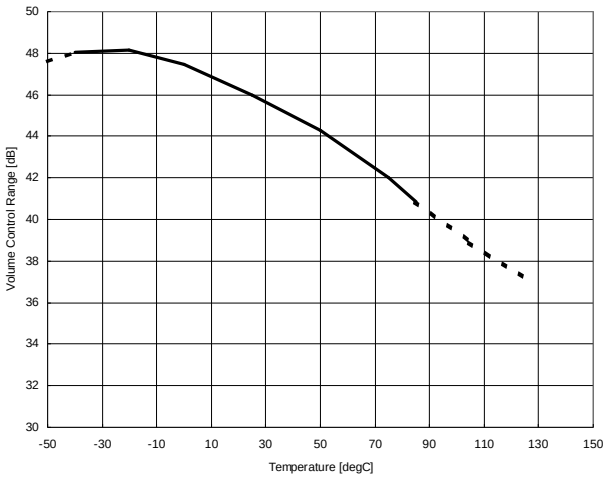
Supply Current vs Temperature
V+ =5.0V , No Signal



RxAtt Gain vs Temperature
V+ =5.0V , RecieveAmp : 0dB , RL=5.1kΩ

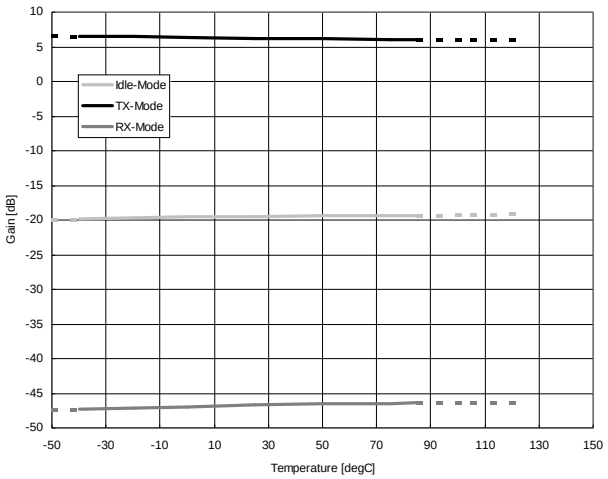


RxAtt Gain vs Temperature
V+ =5.0V , Rx-Mode , RecieveAmp : 0dB , RL=5.1kΩ

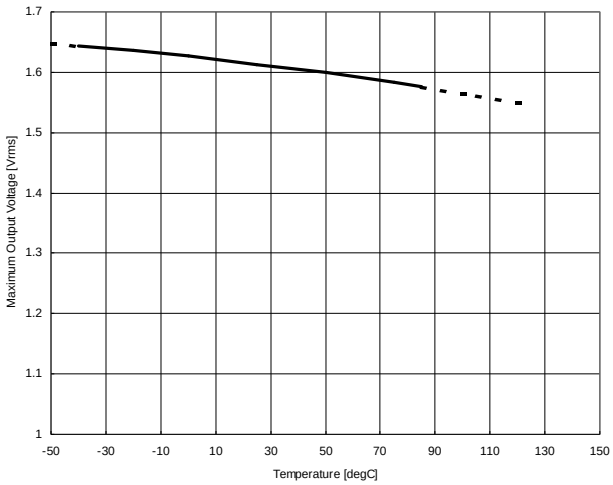


■ TYPICAL CHARACTERISTICS

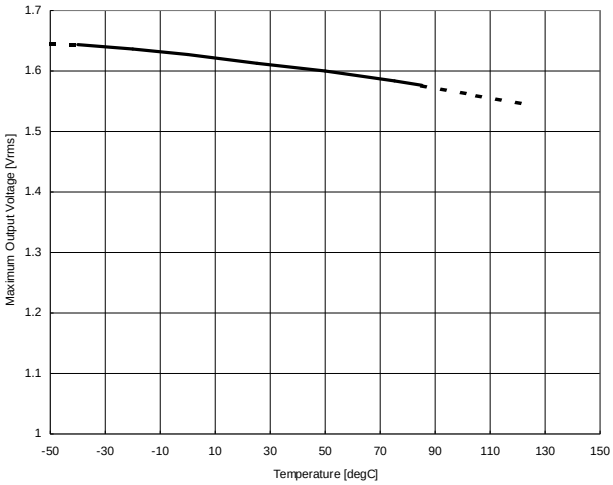
TxAtt Gain vs Temperature
V+ = 5.0V , MicAmp : 0dB , RL=5.1kΩ



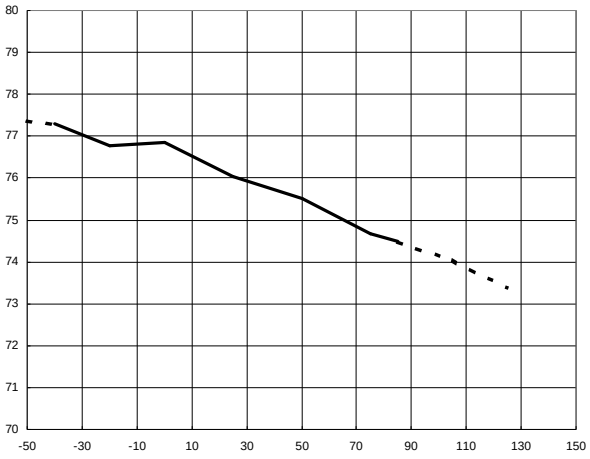
RecieveAmp Maximum Output Voltage vs Temperature
V+ = 5.0V , f = 1kHz Rf = 300kΩ , Gv=40dB , RL=5.1kΩ , THD+N = 1% , BW=400Hz-30kHz



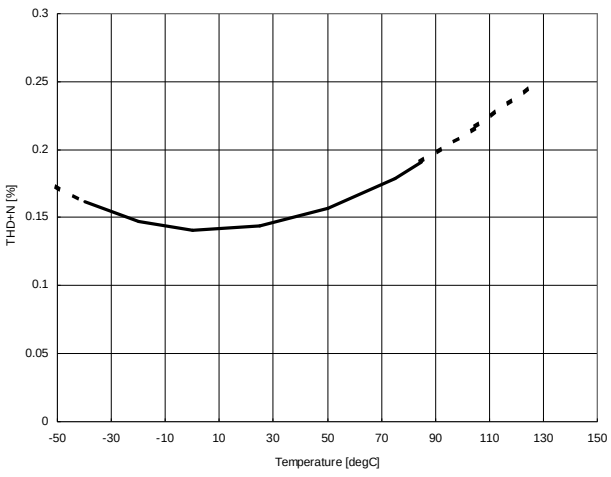
MicAmp Maximum Output Voltage vs Temperature
V+ =5.0V , f = 1kHz , Rf = 300kΩ , Gv=40dB , RL=5.1kΩ , THD+N = 1% , BW=400Hz-30kHz



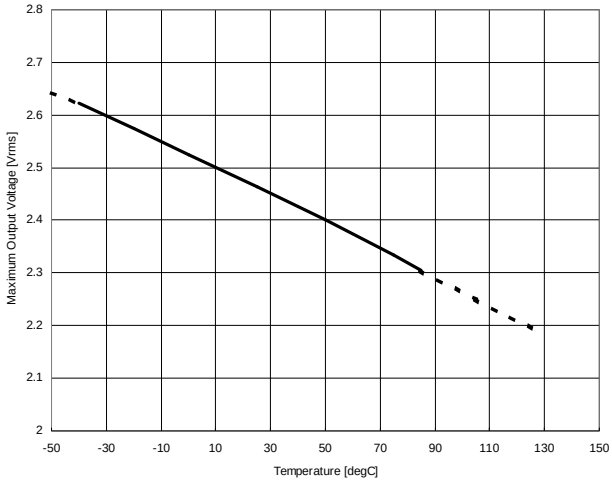
MicAmp Mute Range vs Temperature
V+ =5.0V , Rf = 300kΩ , Gv=40dB , RL=5.1kΩ , A-Weighting



LineAmp THD vs Temperature
V+ =5.0V , f = 1kHz , Rf = 51kΩ , Gv=26dB , Vin = 50mVrms , RL=1.2kΩ , BW=400Hz-30kHz

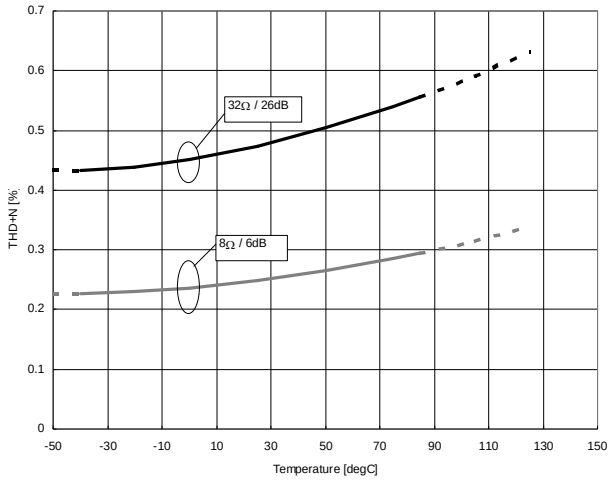


LineAmp Maximum Output Voltage vs Temperature
V+ =5.0V , f = 1kHz , Rf = 51kΩ , Gv=26dB , RL=1.2kΩ , THD+N = 1% , BW=400Hz-30kHz

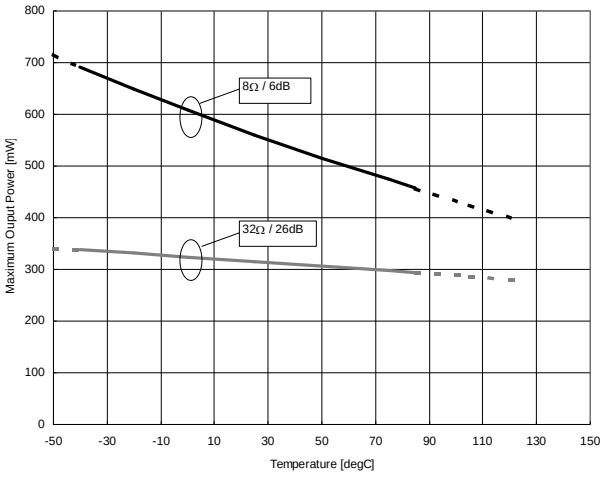


■ TYPICAL CHARACTERISTICS

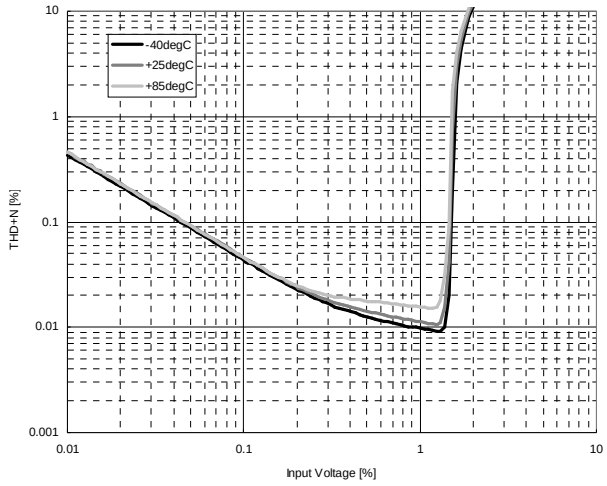
Speaker Amp THD vs Temperature
V+ =5.0V , f = 1kHz , BW=400Hz-30kHz



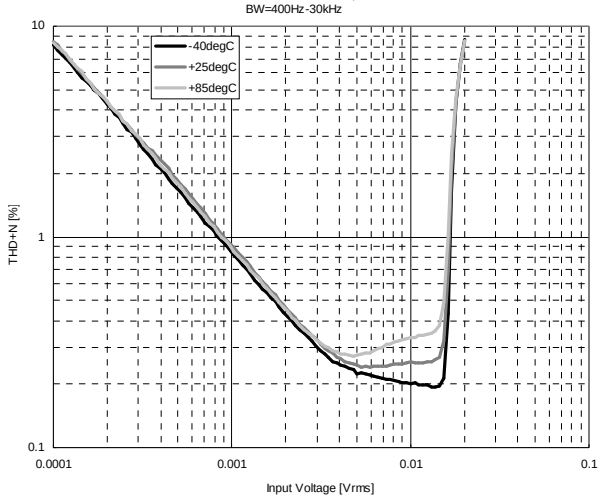
Speaker Amp Maximum Output Power vs Temperature
V+ =5.0V , f = 1kHz , THD+N = 3% , BW=400Hz-30kHz



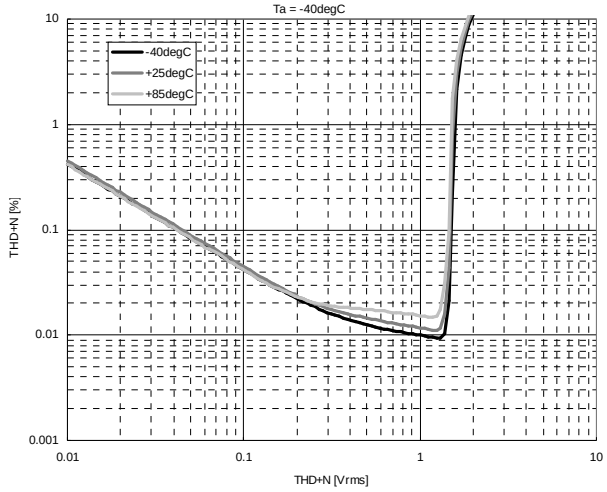
Receive Amp THD+N vs Input Voltage
V+ = 5.0V , f = 1kHz Rf = 3kΩ , Ri=3kΩ , Ci = 1μF , Gv=0dB , RL=5.1kΩ , BW=400Hz-30kHz



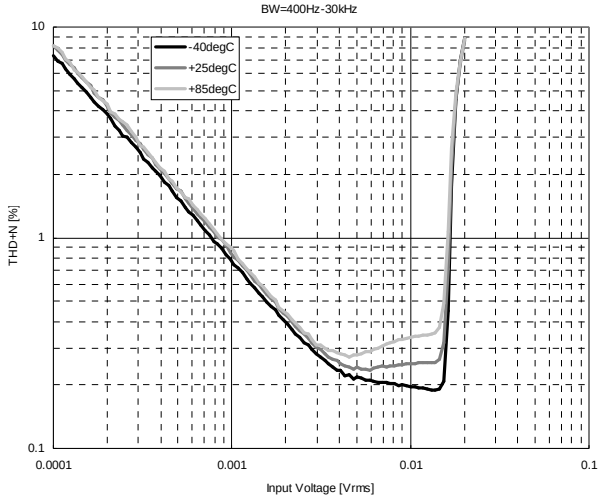
Receive Amp THD+N vs Input Voltage
V+ = 5.0V , f = 1kHz Rf = 300kΩ , Ri=3kΩ , Ci = 1μF , Gv=40dB , RL=5.1kΩ , BW=400Hz-30kHz



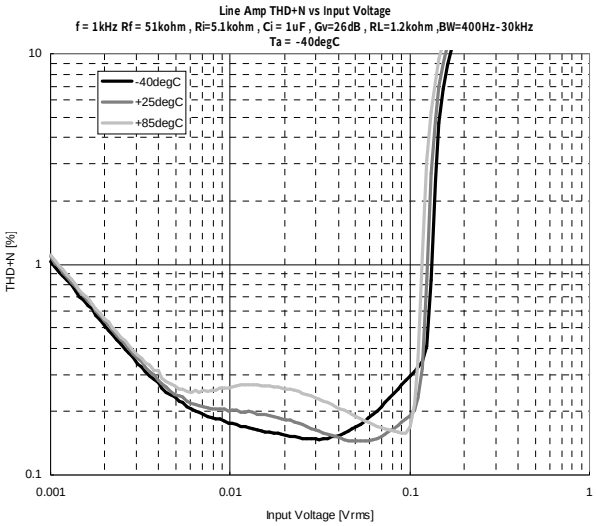
Mic Amp THD+N vs Input Voltage
f = 1kHz Rf = 3kohm , Ri=3kohm , Ci = 1uF , Gv=0dB , RL=5.1kohm ,BW=400Hz-30kHz
Ta = -40degC

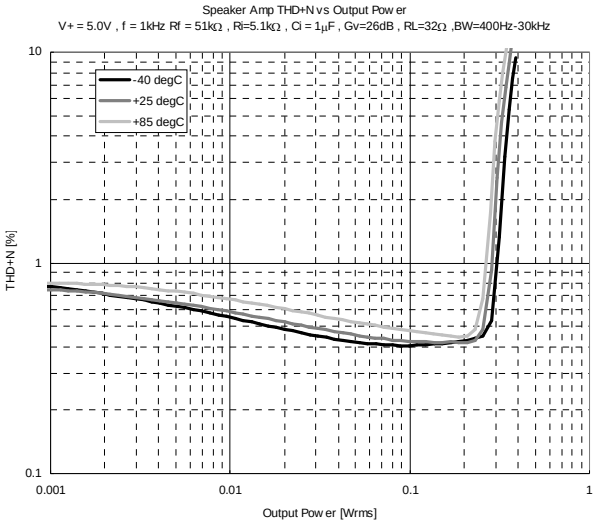


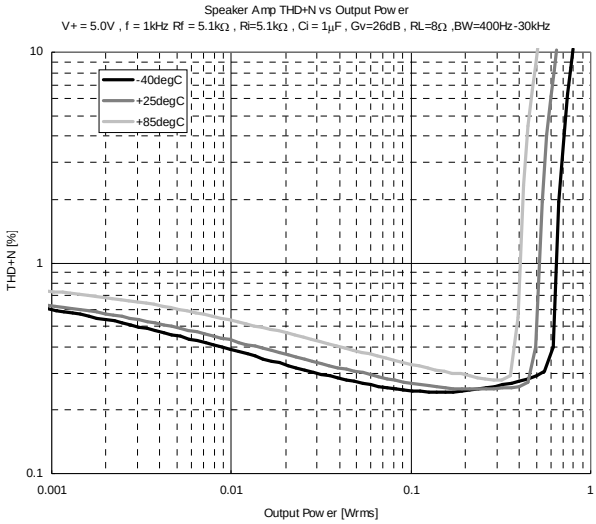
Mic Amp THD+N vs Input Voltage
V+ = 5.0V , f = 1kHz Rf = 300kΩ , Ri=3kΩ , Ci = 1μF , Gv=40dB , RL=5.1kΩ , BW=400Hz-30kHz

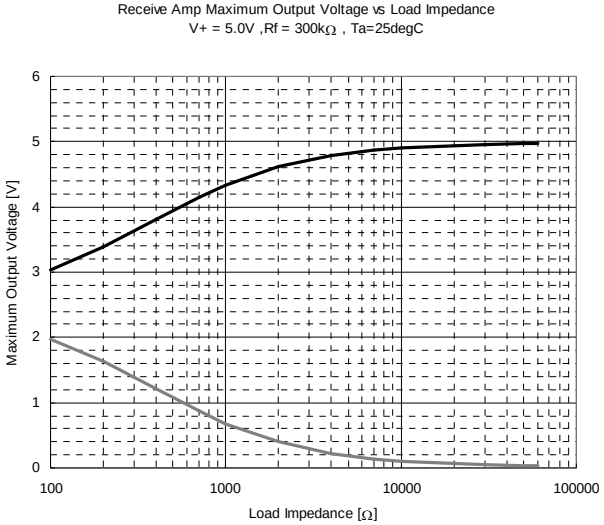


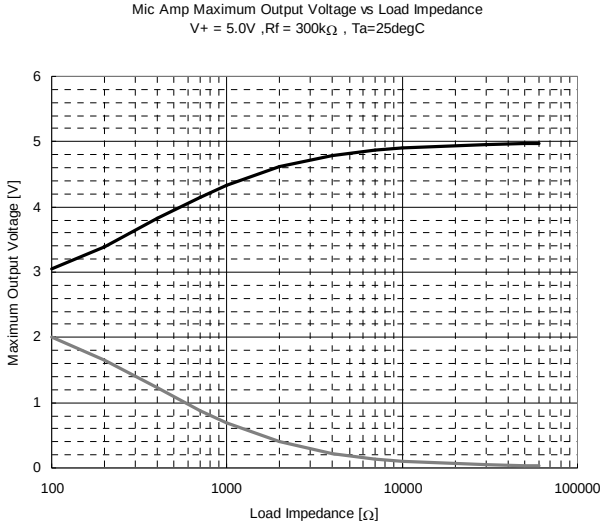
■ TYPICAL CHARACTERISTICS





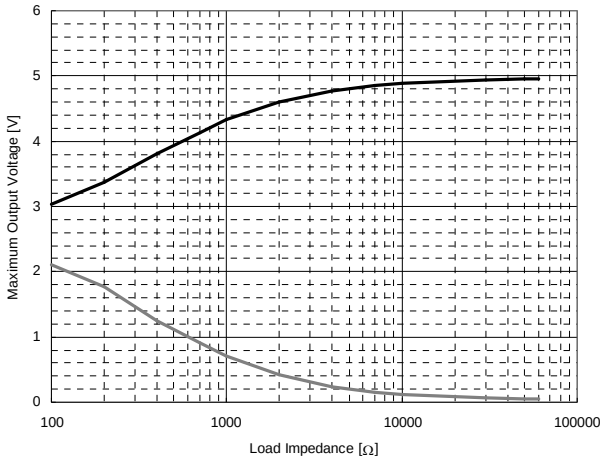




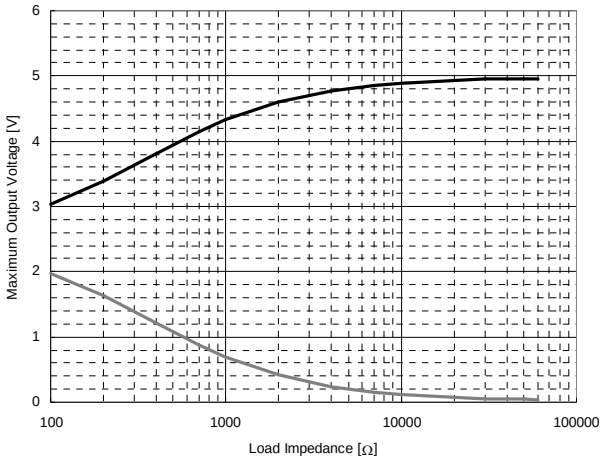


■ TYPICAL CHARACTERISTICS

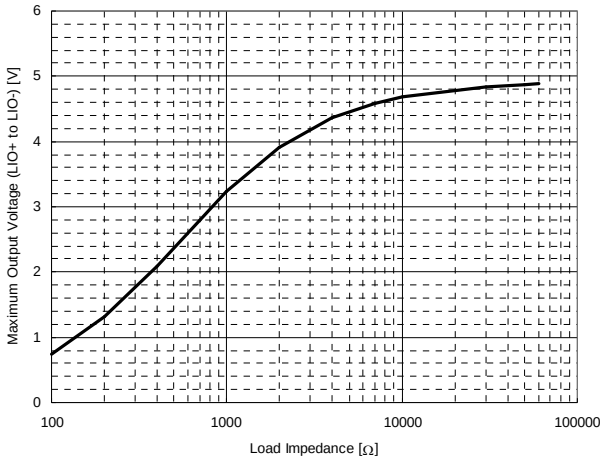
Rx Att Maximum Output Voltage vs Load Impedance
V+=5.0V , Ta=25degC



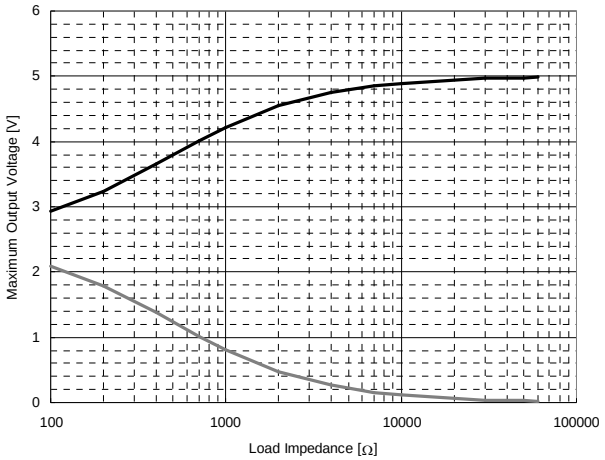
Tx Att Maximum Output Voltage vs Load Impedance
V+=5.0V , Ta=25degC



Line Amp Maximum Output Voltage vs Load Impedance
V+ = 5.0V ,Rf = 51kΩ , Ta=25degC

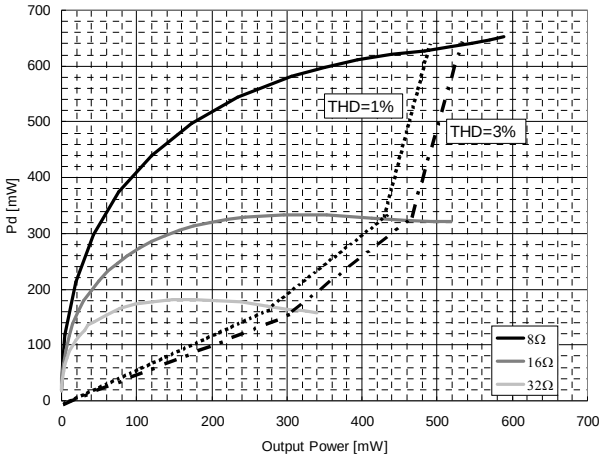


Monitor out Maximum Output Voltage vs Load Impedance
V+=5.0V , Ta=25degC

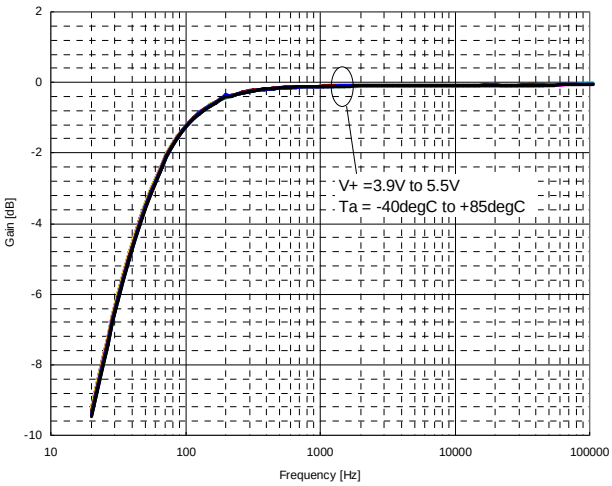


■ TYPICAL CHARACTERISTICS

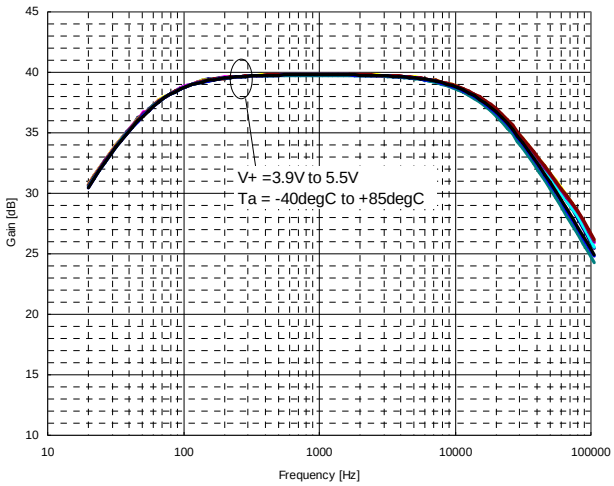
Pd vs Output Power
V+=5.0V , f=1kHz , Gv=6dB , BW=400Hz-30kHz , Ta=25degC



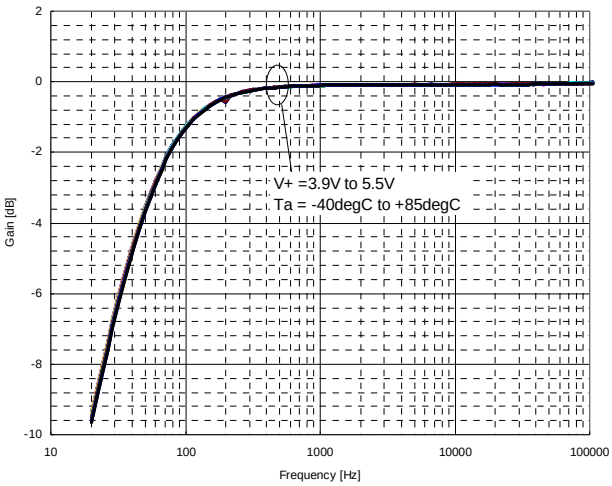
RecieveAmp Voltage Gain vs Frequency
Vin = 100mVrms , Rf = 3kΩ , Ri = 3kΩ , Ci = 1μF , Gv=0dB , RL=5.1kΩ



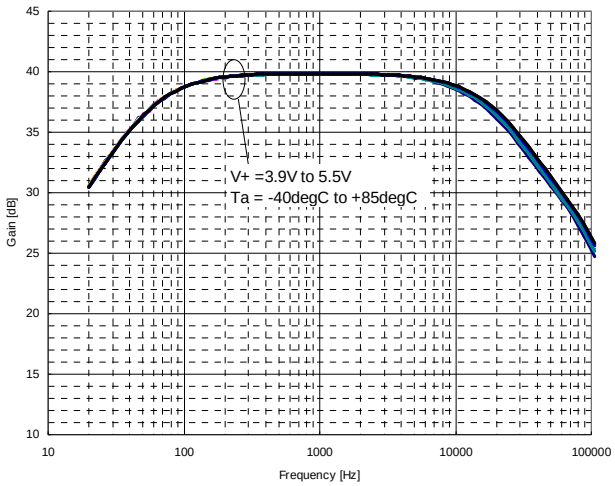
RecieveAmp Voltage Gain vs Frequency
Vin = 1mVrms , Rf = 300kΩ , Ri = 3kΩ , Ci = 1μF , Gv=40dB , RL=5.1kΩ



Mic Amp Voltage Gain vs Frequency
Vin = 100mVrms , Rf = 3kΩ , Ri = 3kΩ , Ci = 1μF , Gv=0dB , RL=5.1kΩ

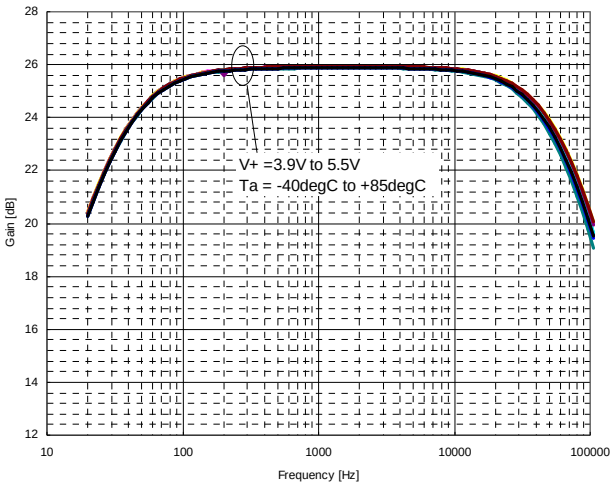


Mic Amp Voltage Gain vs Frequency
Vin = 1mVrms , Rf = 300kΩ , Ri = 3kΩ , Ci = 1μF , Gv=40dB , RL=5.1kΩ

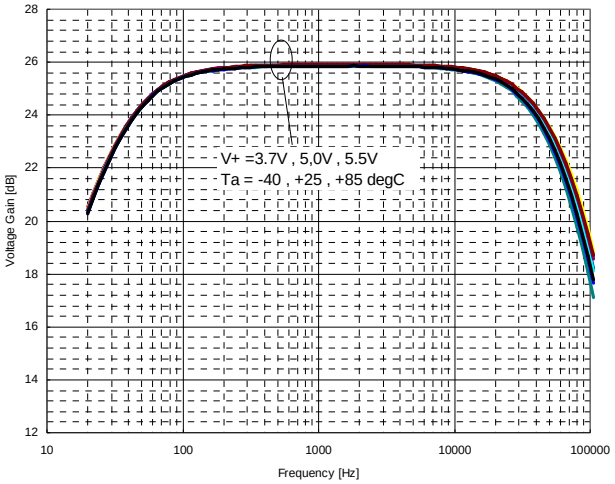


■ TYPICAL CHARACTERISTICS

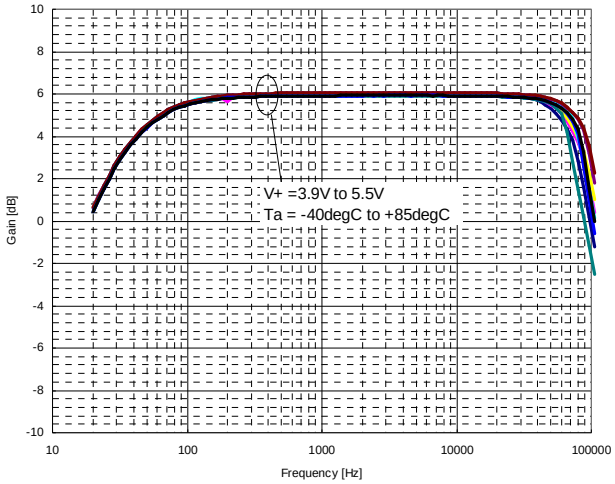
Line Amp Voltage Gain vs Frequency
Vin = 50mVrms , Rf = 51kΩ , Ri = 5.1kΩ , Ci = 1μF , Gv=26dB , RL=1.2kΩ



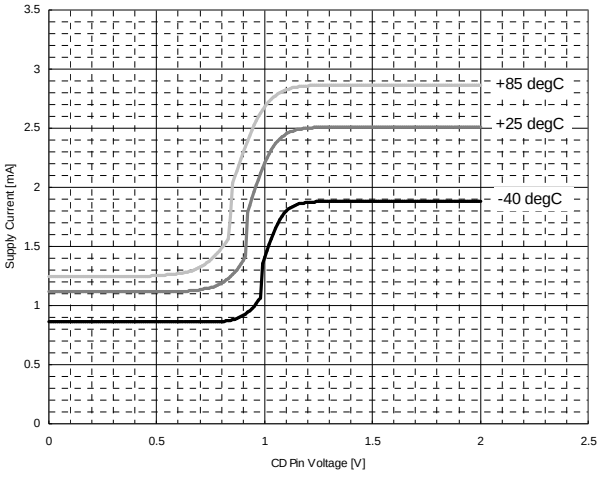
Speaker Amp Voltage Gain vs Frequency
Vin = 50mVrms , Rf = 51kΩ , Ri = 5.1kΩ , Ci = 1μF , Gv=26dB , RL=32Ω



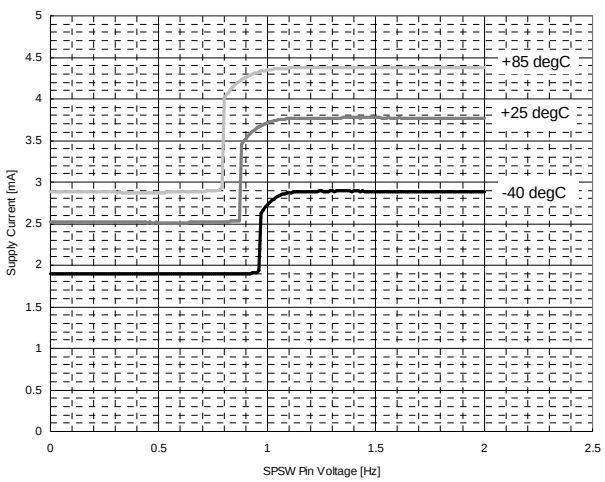
Speaker Amp Voltage Gain vs Frequency
Vin = 500mVrms , Rf = 5.1kΩ , Ri = 5.1kΩ , Ci = 1μF , Gv=6dB , RL=8Ω



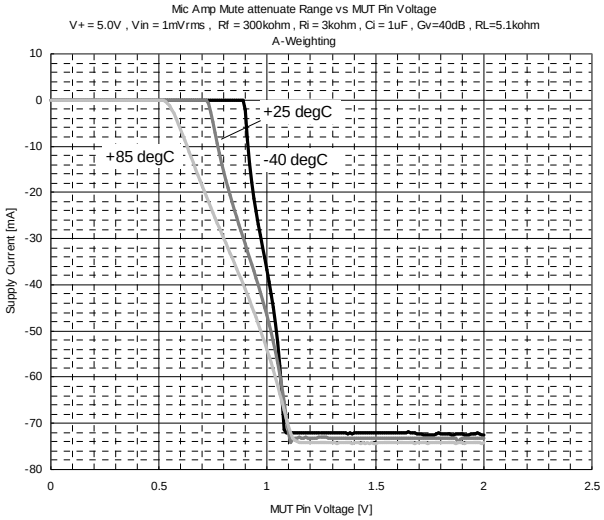
Supply Current vs CD Pin Voltage
V+ = 5.0V , SPSW = PD , RTSW = Open , no Signal

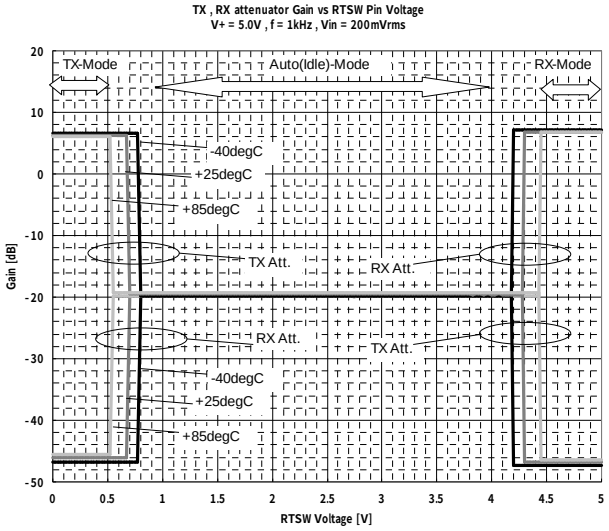


Supply Current vs SPSW Pin Voltage
V+ = 5.0V , CD = Active , RTSW = Open , no Signal



■ TYPICAL CHARACTERISTICS





■APPLICATION NOTES

■GENERAL DESCRIPTION

The **NJW1128** is a Voice Switched Speakerphone Circuit. The **NJW1128** includes all of functions processing a high quality hands–free speakerphone system, such as the necessary amplifiers (Microphone amplifier , Receive amplifier, Line amplifier ,and speaker Amplifier), attenuators, level detectors .

The **NJW1124** detects a signal to judges which path is talking. After that, the one side path is active, another path is attenuated. This is half-duplex system. Appropriate operating keeps closed loop gain less than 0dB, and that prevents acoustic coupling.

All external capacitors are sufficient small so that ceramic capacitors are applied.

The resister and capacitor values in Fig.0.1 below are references. For correct operating, check in actual condition as possible as you can. And adjust the levels input each detectors.
On this application notes, Base unit is defined as the unit included the **NJW1128**.

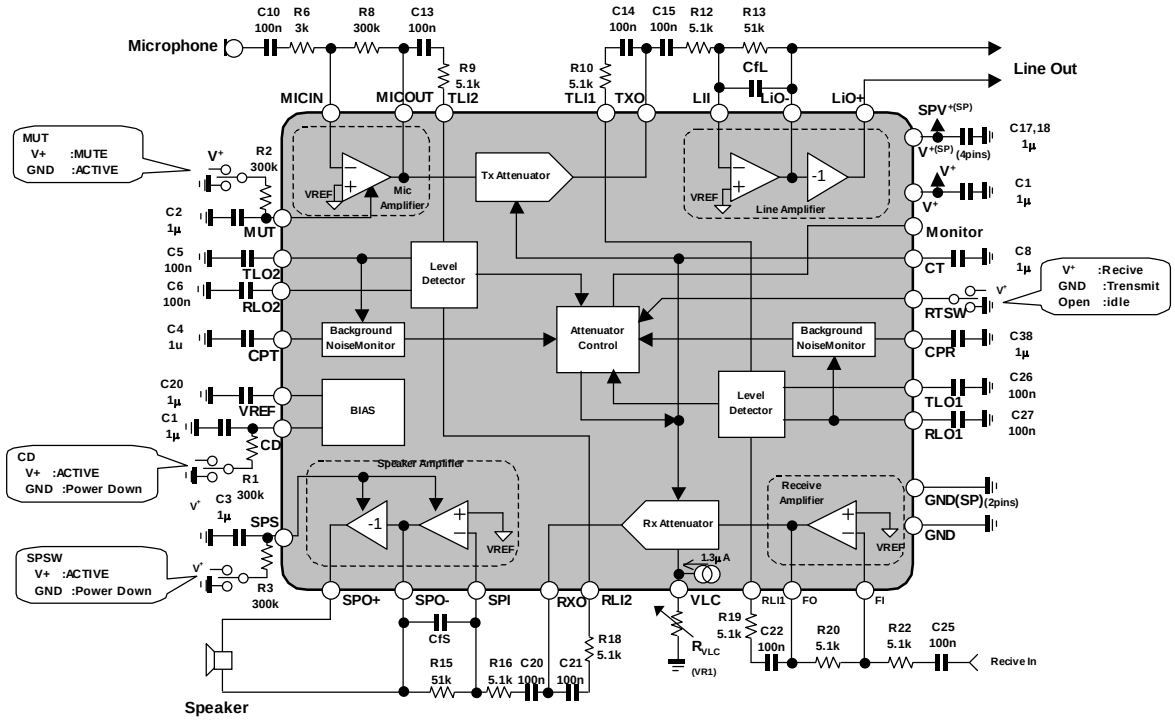


Fig.0.1 NJW1128 Block diagram

The resistance and capacitor value above is just one example.
Certain Half-duplex operation are not guaranteed.
Best value depends on your microphone, speaker, and chassis.
Understand NJW1128 operation and select appropriate value.

<Evaluation-Board Circuit>

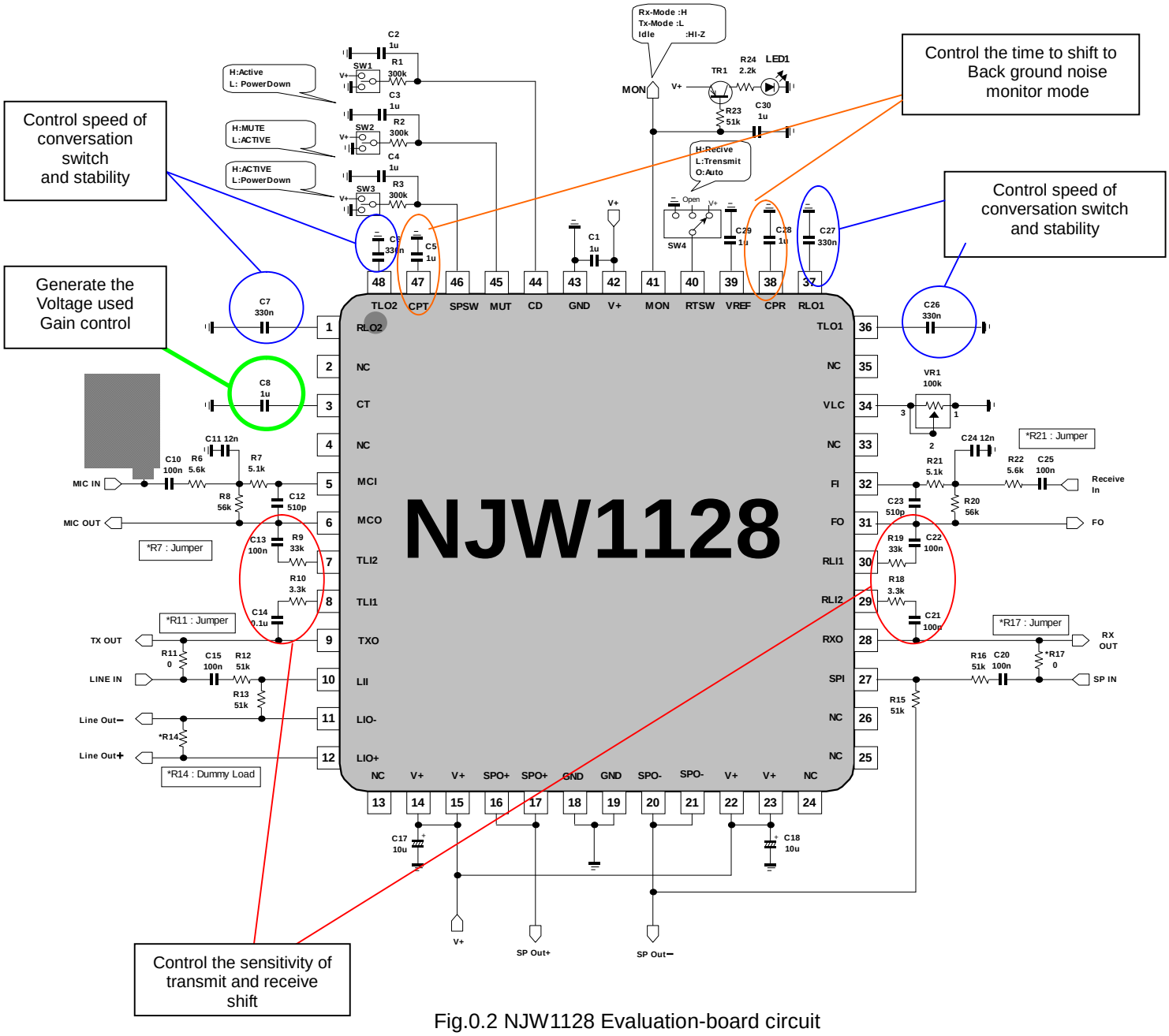


Fig.0.2 NJW1128 Evaluation-board circuit

<Power Supply Wiring layout>

42pin is sensitive for power supply ripple. Thus, ripple should be less than 10mVp-p.
Please use regulator for stable power supply.

1,42pin, other V+ pin, and 43pin(GND) should have lower common impedance as possible.

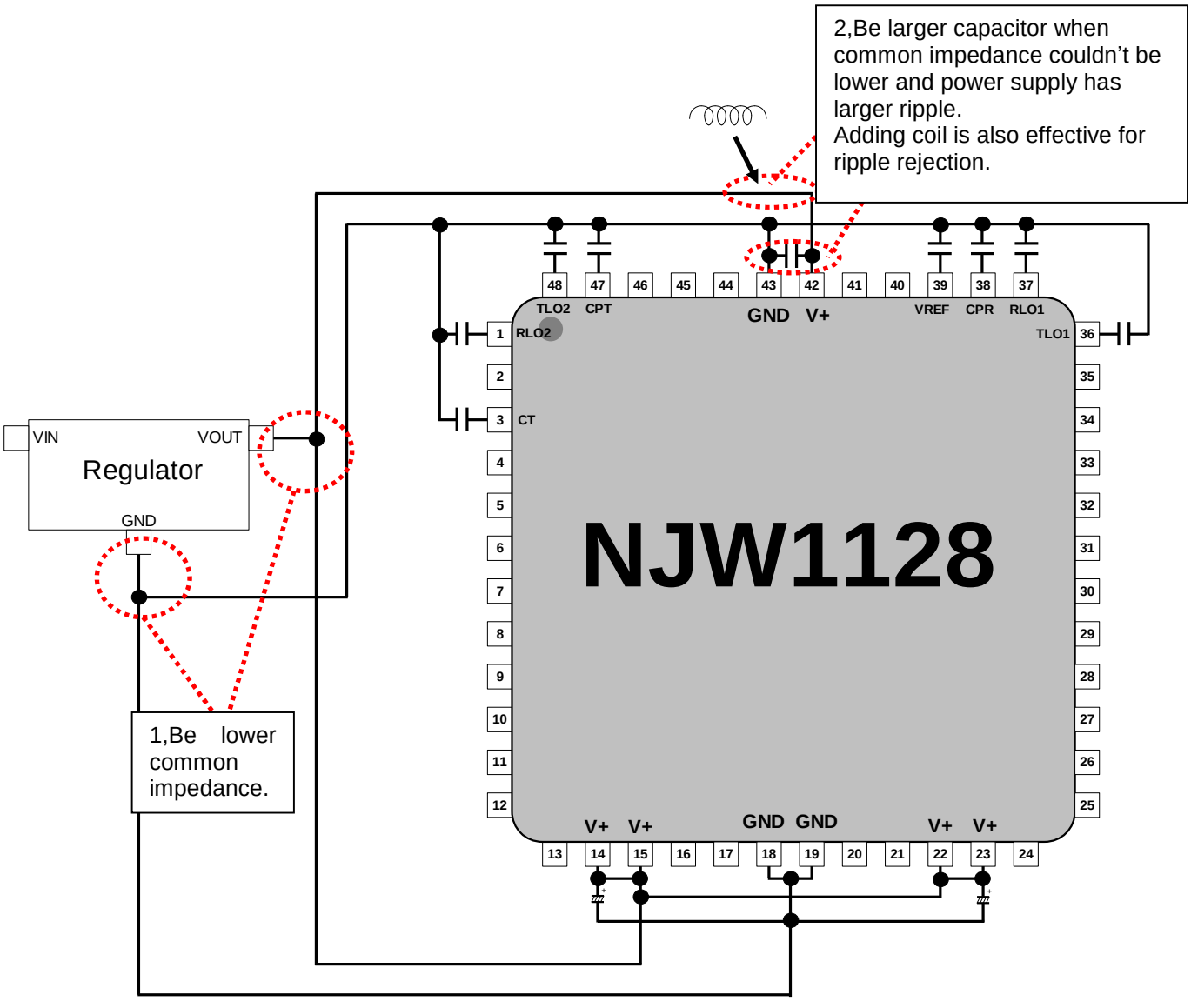
2,Large capacitor between 42pin and 43pin, in case of that common impedance couldn't be lower and power supply has larger ripple.

And, adding coil in front of bypass capacitor of 42pin is also effective for ripple rejection.

Supply same power source to 42pin and 14,15,22,23 pin. They are not able to use on different voltage.
Connect de-coupling capacitor to 14,15,22,23 pin.

43pin and 18,19pin should be connected to GND.
All V^+pin and GND pin should be connected for normal operating. Don't be Open.

Wire lower impedance GND side of capacitor connected to VREF,CPT,CPR,TL01,TL02,RL01,RL02,and CTpin as possible.



[Operating mode]
NJW1128 equips operating modes below.
Fig.0.4 shows simple NJW1128 diagram.

<Tx mode> signal input to mic. In(Transmit side)
Tx Attenuator sets +6dB, signal go route.1 though mic in to line amp.
At same time, route.2 sets –46dB to stop signal.

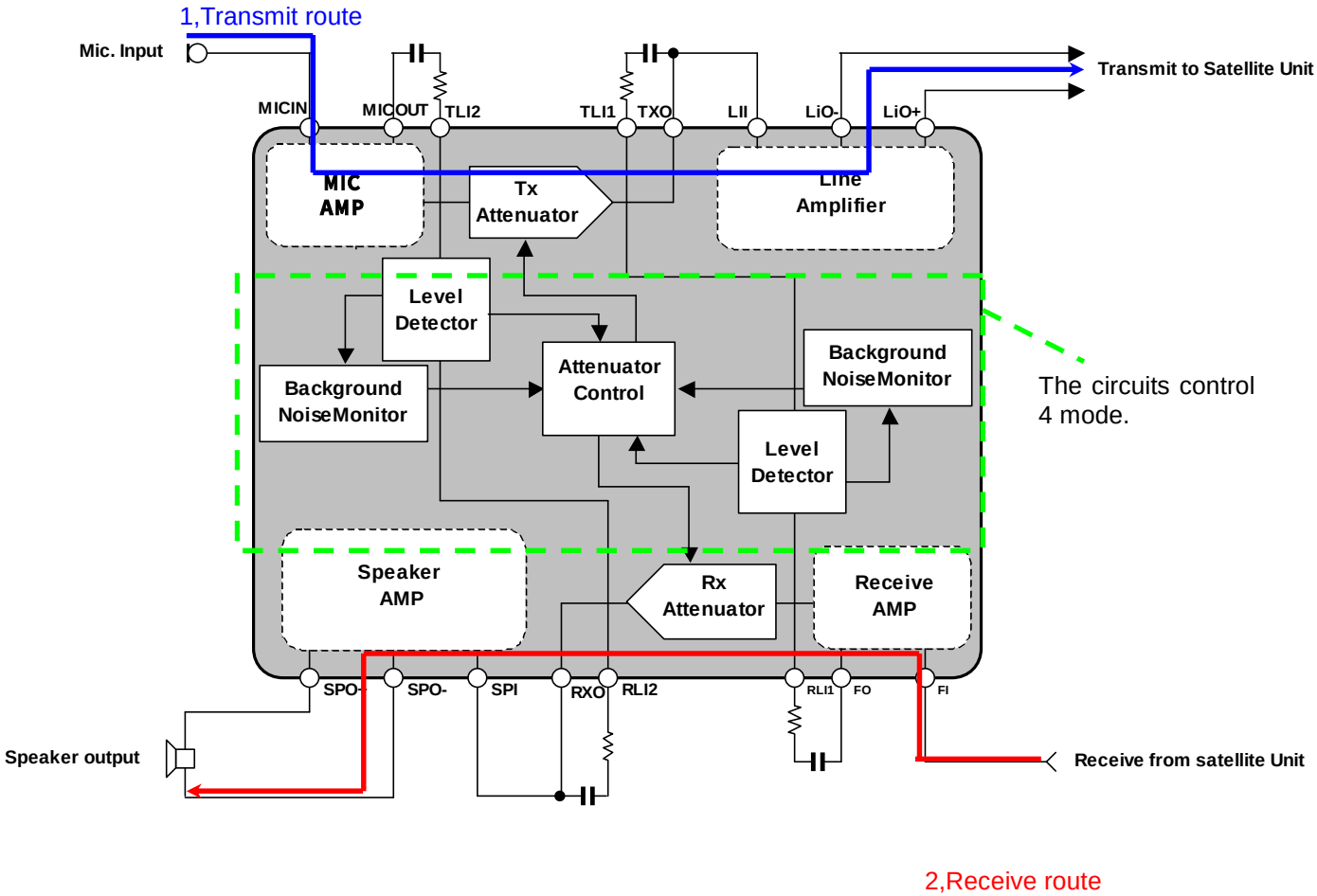
<Rx mode> signal input to Receive. In(Receive side)
Rx Attenuator sets +6dB, signal go route.2 though mic in to line amp.
At same time, route.1 sets –46dB to stop signal.

<Slow idle mode> environmental noise input or no signal input

continuous signal input to mic.input or receive input, or both input no signal
Rx attenuator and Tx attenuator set both –20dB.
Then, shifting transmit mode or receive mode to half conversation(both route -20dB) gradually.

<Fast idle mode> Transmit and Receive input at the same time.
To Mic.input and Receive input signal input at the same time, Rx attenuator and Tx attenuator set both –20dB. route1 and 2 shift half conversation(both route –20dB). Shifting transmit mode or receive mode to half conversation(both route -20dB) sharply.

We recommend forming filter of mic.amp and receive amp. to filtering some frequency we don't need.
That realizes to stable conversation.



[2wire-4wire convert circuit]

NJW1128 2wire application should be mixed or isolated by 2wire-4wire convert circuit
Fig0.5 shows conceptual diagram of 2wire - 4wire convert circuit.
Each impedance meeting this condition doesn't transmit VIN1toVout1 and VIN2toVout2.
That means transmit side signal doesn't leak to receive side, opposite side too.
This circuit enable to transmit and receive by 2wire.

$$Z_{14} = \frac{Z_{12} \times Z_{13}}{Z_{11}}$$

$$Z_{24} = \frac{Z_{22} \times Z_{23}}{Z_{21}}$$

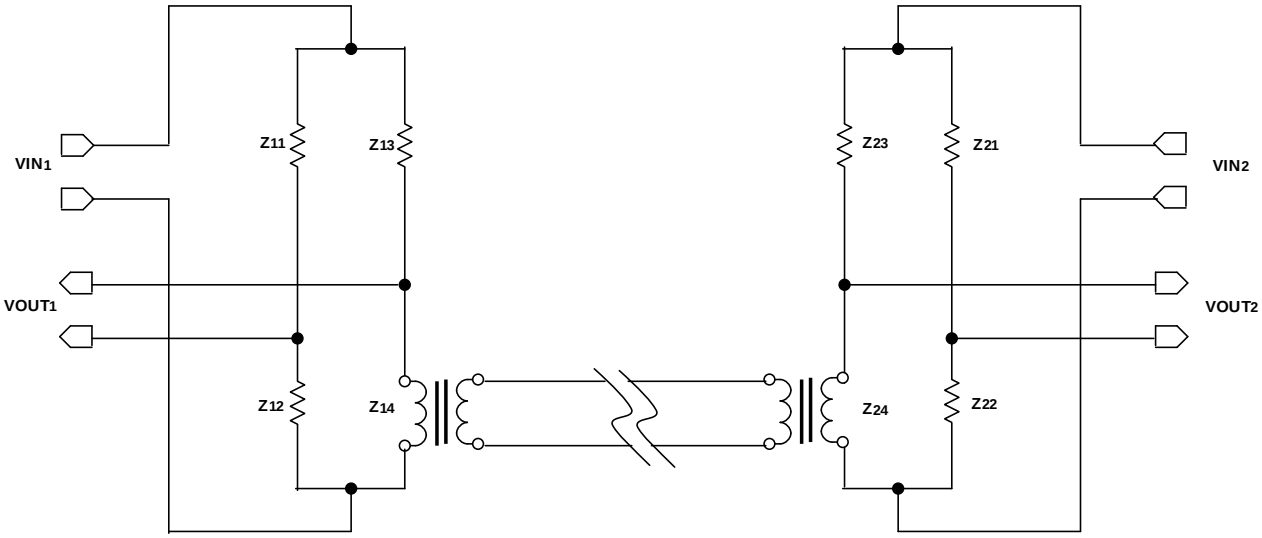


Fig.0.5 2wire-4wire convert circuit Conceptual diagram

Fig.6 shows 2wire –4wire convert circuit consisted of line amp of NJW1128 and Hybrid transformer.
Impedance matching Z1 and Z2 enable to operate normally..

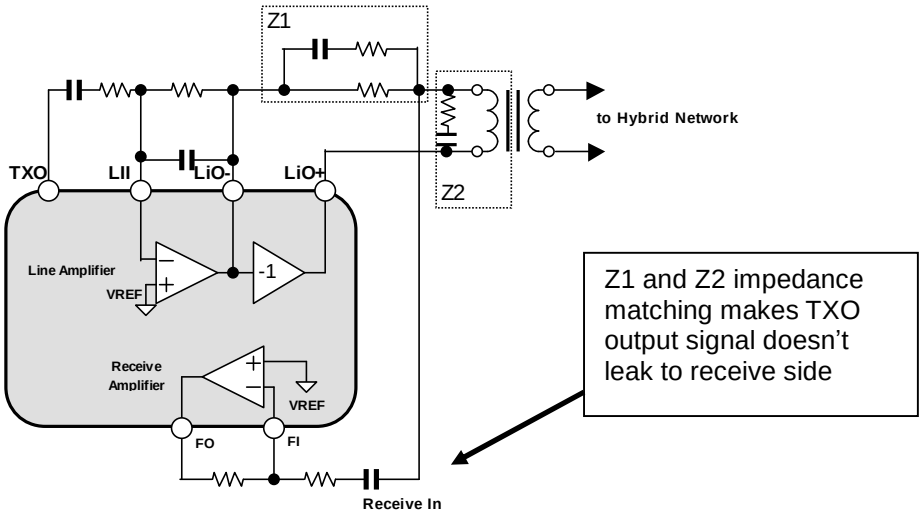


Fig.0.6 2wire –4wire convert circuit consisted of line amp of NJW1128 and Hybrid transformer

More details about equal circuit consisted of Tr or power supply superimposed circuit , refer to other technical book on phone line.

[Thermal Design]
Notice of thermal design on Speaker Amplifier.

Fig.0.7 shows Maximum power dissipation of NJW1128(LQFP48-R3) and Ambient temperature Ta.
Test condition is EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting and EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 4layer, FR-4) mounting.

Calculate appropriate P_D to be lower than Pdmax(maximum Power dissipation).
Fig.0.8 shows PD and Speaker output power .

Actual Pdmax depends on your PCB type, PCB size, wiring. Consider appropriate thermal design.

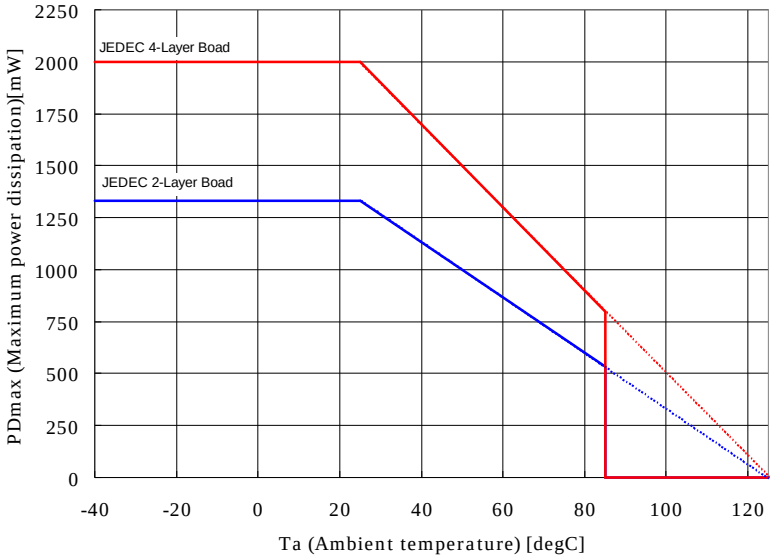


Fig.0.7 NJW1128(LQFP48-R3) $P_D$max and Ta

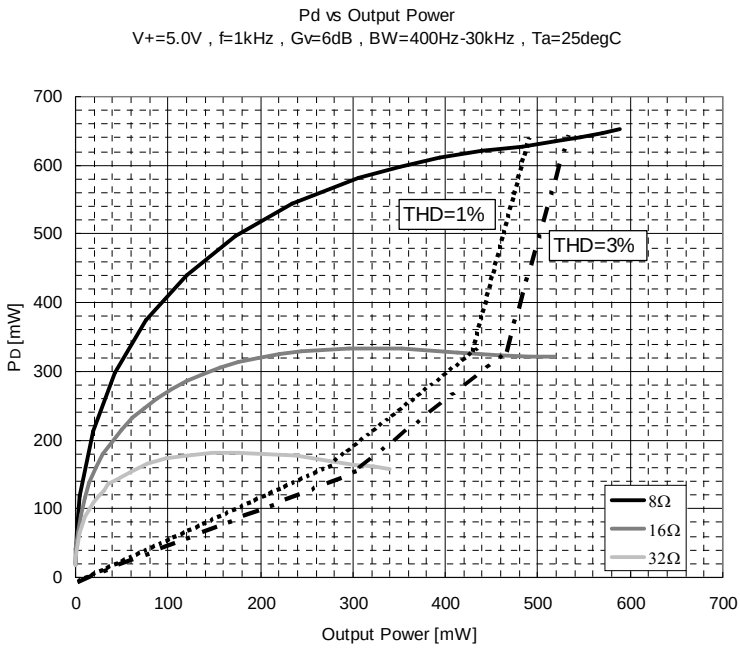


Fig.0.8 NJW1128 P_D and Speaker output power

1.Receive Attenuator

Receive Attenuator has 3 modes depending on base and satellite unit condition.

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Receive Attenuator Gain 1	G_{R1}	RX-mode (Receive)	3.0	6.0	9.0	dB
Receive Attenuator Gain 2	G_{R2}	TX-mode (Transmit)	-43	-46	-50	dB
Receive Attenuator Gain 3	G_{R3}	Idle-mode (Standby),CPT=CPR=V^+	-17	-20	-23	dB

1.Receive Attenuator Gain 1 , (Receive mode :Gain=+6dB)
Condition: Receive the signal from satellite unit, and no transmit the signal to satellite unit.

2. Receive Attenuator Gain 2 , (Transmit mode :Gain=-46dB)
Condition: Transmit the signal to satellite unit, and no receive signal from satellite unit.

3. Receive Attenuator Gain 3 , (Idle mode :Gain=-20dB)
Condition: Both lines are attenuated (-20dB).

Receive attenuator mode depends on level controller detection mode.

Volume Control

Receive Attenuator includes Volume Control.
Volume is controlled by resister value connected to VCL pin.
Fig.2 shows Volume attenuate vs. Resister value.
Volume max.(0dB) : 0Ω,
Volume min. (-40dB): 100kΩ .

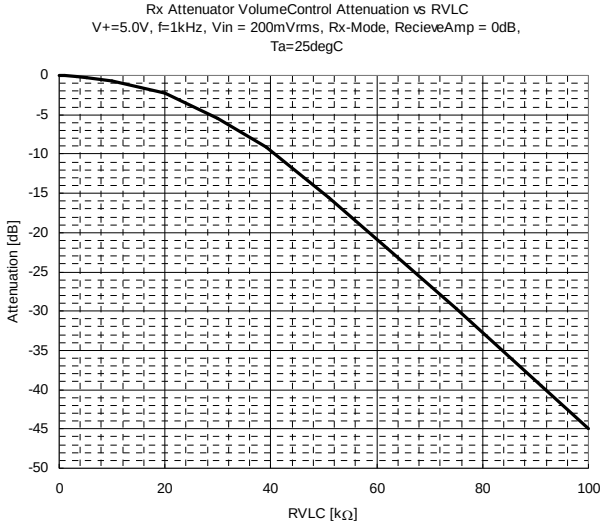


Fig.2 Volume vs. Resister

2.Transmit Attenuator

Transmit Attenuator has 3 modes depending on base and satellite unit condition.

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Transmit Attenuator Gain 1	G_{T1}	RX-mode (Receive)	3.0	6.0	9.0	dB
Transmit Attenuator Gain 2	G_{T2}	TX-mode (Transmit)	-43	-46	-50	dB
Transmit Attenuator Gain 3	G_{T3}	Idle-mode (Standby),CPT=CPR=V^+	-17	-20	-23	dB

1.Transmit Attenuator Gain 1 , (Transmit mode :Gain=+6dB)
Condition: Transmit the signal to satellite unit, and No receive the signal from satellite unit.

2. Transmit Attenuator Gain 2 , (Transmit mode :Gain=-46dB)
Condition: No Transmit the signal to satellite unit, and Receive the signal from satellite unit.

3. Transmit Attenuator Gain 3 , (Idle mode :Gain=-20dB)
Condition: Both lines are attenuated (-20dB)

Transmit attenuator mode depends on level controller detection mode.
Transmit Attenuator doesn't equip Volume Control.

3.Microphone Amplifier(Transfer Block)

Microphone Amplifier is an operational Amplifier amplifying the signal from microphone to line level.
Fig.3 shows Block Diagram of Mic.Amp..
Non-inverting input keeps reference voltage inside. Mic.Amp is used as inverting amplifier. The Gain should be 40dB or less. Mic.amp equips Mute function.

GND to 0.3V:Active
1.5V to V+:Mute

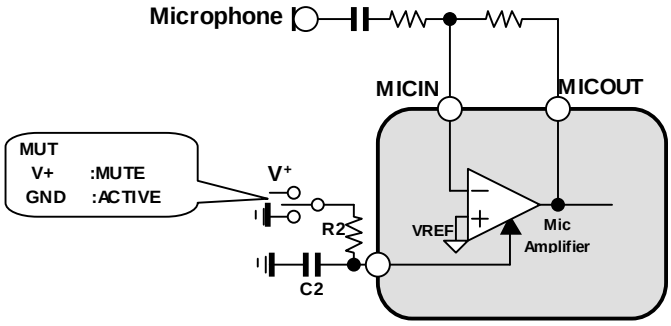


Fig.3.1 mic amp application example

Table.3.1 mic amp application external parts

External Parts	Purpose	Recommend value	Explanation	Note
C10	DC decoupling	100n～10μF	-	C10 and R6 create LPF (fc=1/2πR6*C10)
R8	Gain Setting	3k～300kΩ	Gv = R8/R6	Recommend Gv<40dB
R6			Input impedance=R6	
R2	Pop-noise reduction	10k～300kΩ	MUTE/ACTIVE swithing pop-noise reduction	
C2		100n～1μF		

Table 3.2 mic. amp mute logic

MUTE pin Voltage		Condition
VIH	>1.5V	MUTE
VIL	<0.3V	ACTIVE

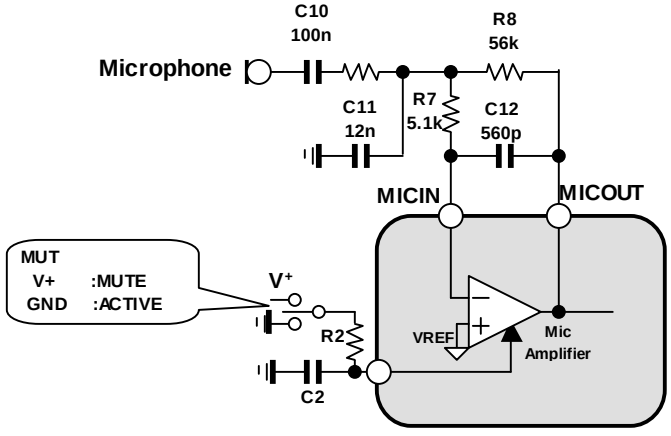


Fig.3.2 mic amp application example(Gv=20dB,fc=4kHz LPF)

Mic amp is also used creating multiple feedback LPF,HPF,BPF.Fig.3 shows Block Diagram of Mic.Amp (Gv=20dB,fc=4kHz LPF). Frequency except Conversation band should be remove by mic amp filter for stable operating. Refer note.2 about Filter value at the end of this application note.

4.Receive Amplifier(Receive Block)

Receive Amplifier is an operational Amplifier receiving the signal from satellite unit.
Fig.4 shows Block Diagram of Mic.Amp Block Non-inverting input keeps reference voltage inside.
Receive Amp is used as inverting amplifier. The Gain should be 40dB or less.
Receive Amplifier doesn't equip Mute function.

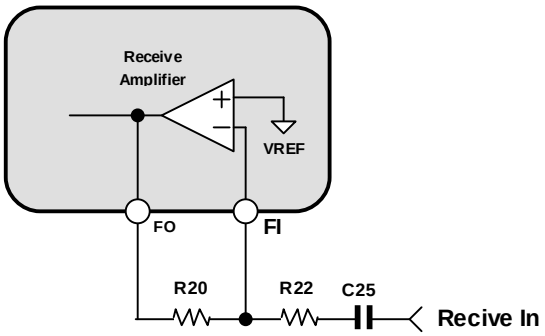


Fig.4.1 Receive amplifier application example

Table.4.1 Recieve amp external parts

External Parts	Purpose	Recommend Value	Explanation	Note
C25	DC-decoupling	100n to 10μF	-	C25 and R22 create LPF (fc=1/2πR22*C25)
R20 R22	Gain setting	3k to 300kΩ	Gv = R20/R22 Input impedance=R22	Recommend Gv<40dB

Receive amp is also used creating multiple feedback LPF,HPF,BPF.
Fig.4.2 shows application example of Receive amplifier (Gv=20dB,fc=4kHz LPF,-40dB/deg).
Frequency except Conversation band should be remove by mic amp filter for stable operating.

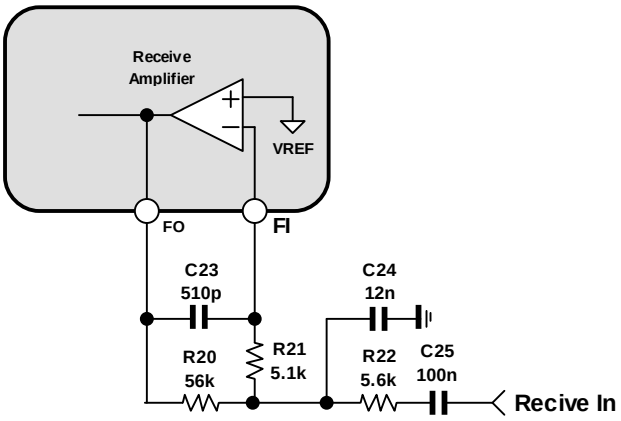


Fig.4.2 Receive amplifier application example (Gv=20dB,fc=4kHz LPF)

5.Line Amplifier(Transfer Block)

Line Amplifier transmits the signal from Tx attenuator to satellite unit. Line Amplifier consists of two operational Amplifiers.
First Amplifier non-inverting input keeps reference voltage inside. First Amplifier is used as inverting amplifier.
Second Amplifier includes –1 fixed Gain.
These two amplifiers enable to differential output from single-ended signal.

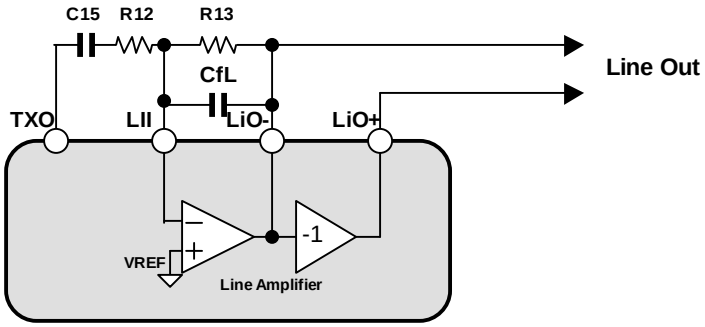


Fig.5.1 Line Amplifier Block

Table.5.1 Line amp external parts

External Parts	Purpose	Recommend Value	Explanation	Note
C15	DC-decoupling	100n to 10μF	-	C15 and R12 create LPF (fc=1/2πR12*C15)
R13 R12	Gain setting	3k to 300kΩ	Gv=R13/R12 Input impedance=R12	Recommend Gv<40dB
CfL	Prevent oscillation	10p to100pF	Need when oscillate due to wire length and inductance. Normally not required.	-

Line Amplifier may oscillates, long transmission path becoming large capacitive load. In this case, add ceramic capacitor (10p to 100p) between LII and LIO-.
LIO+,LIO- should not be short to GND. LIO+,LIO- terminal are biased to V+/2).

Line amp differential output enable to create hybrid circuit.
Refer to 2wire-4wire convert circuit.

Fig.5.2 show forbidden circuit example. Line output must not be connected with GND even AD coupling.

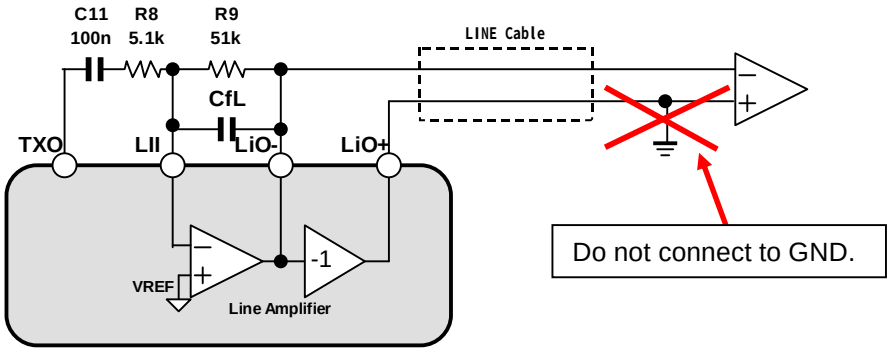


Fig.5.2 Forbidden Circuit

6.Speaker Amplifier(Receive Block)

Speaker Amplifier amplifies the signal from Rx attenuator and drives speaker on Receive block .
Speaker Amplifier consists of two operational Amplifiers.

First Amplifier's non-inverting input keeps reference voltage inside. First Amplifier is used as inverting amplifier.
Second Amplifier includes –1 fixed Gain.
These two amplifiers enable to differential output(BTL output) from single-ended signal.

Speaker impedance should be more than 8Ω.

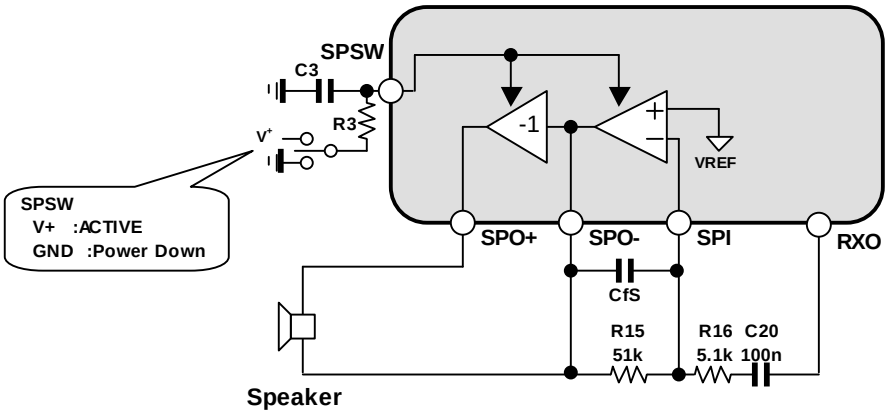


Fig. 6.1Speaker amplifier application.

External Parts	Purpose	Recommend Value	Explanation	Note
C20	DC-decoupling	100n to 10μF	-	C20 and R16 create LPF (fc=1/2πR16*C20)
R15	Gain setting	3k to 300kΩ	Gv=R16/R15 Input impedance=R12	Recommend Gv<40dB
R16				
CfL	Prevent oscillation	10p to 100pF	Need when oscillate due to wire length and inductance. Normally not required.	-

Reducing pop-noise on Power-on, first start up on Power Down mode , after 1 to 3 sec later, activate SPSW.

Adding capacitor and resistor in series between SPO- and SPO+ for phase compensation may improve oscillation characteristics depending on speaker type and inductance of wiring.
Resistor should be 10 to 20Ω, capacitor should be 1 to 100nF.

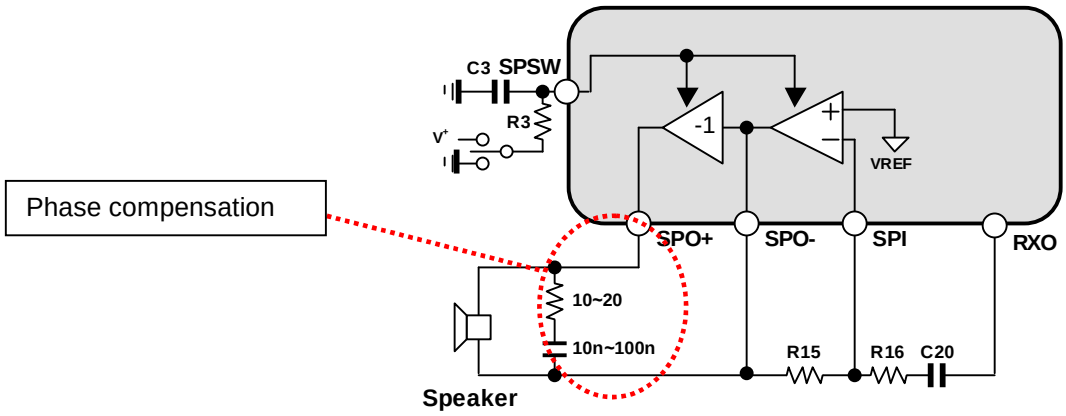


Fig.6.2 improve oscillation circuit

Fig.6.3 shows forbidden circuit example.
Speaker Amplifier output must not be connect to GND even AC-couplung.

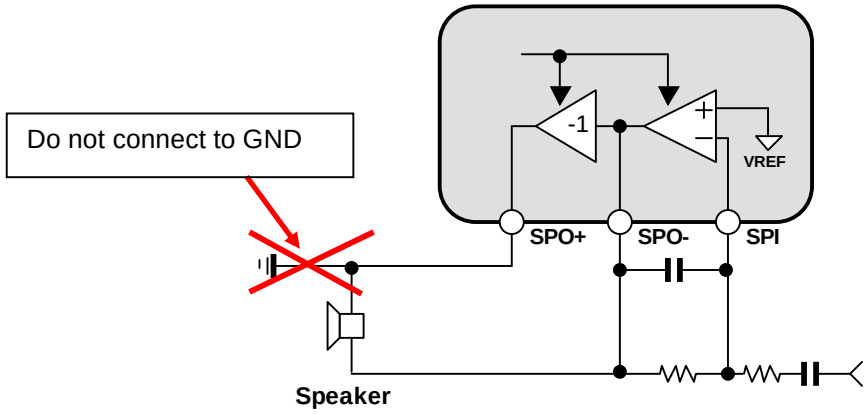


Fig.6.3 Forbidden Circuit

7.Monitor Terminal
Monitor Terminal switches Voltage mode depends on NJW1124 condition.
Fig.7 shows Monitor terminal Block diagram

Receive mode:SW-R is on,SW-T is off. Monitor output is Hi(V+).
Transmit mode:SW-R is off,SW-T is on. Monitor output is Lo(GND)
Idle mode: mode:SW-R is off,SW-T is off. Monitor output is Hi-impedance.

Fig.7 shows test circuit block diagram.
SW-R,SW-T include 300Ω (typ.V+=5V). Refer to typical characteristics data on datasheet about output level vs. Load impedance.

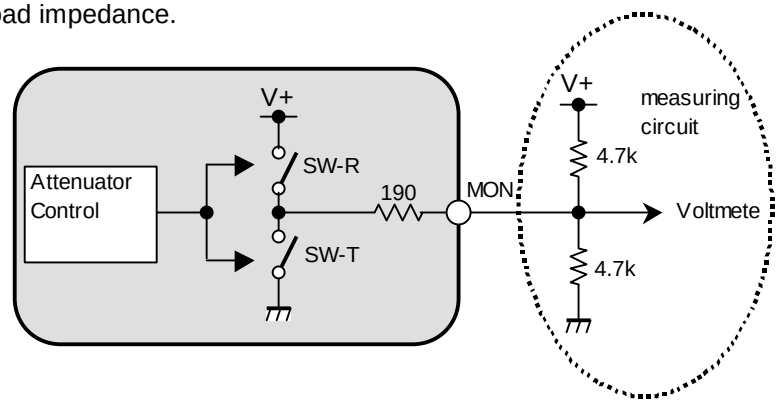


Table7.1 Monitor terminal condition

Mode	SW-R	SW-T
Tx Mode	OFF	ON
Rx Mode	ON	OFF
FAST Idle Mode	OFF	OFF
SLOW Idle Mode	OFF	OFF

Fig.7 Monitor terminal test circuit block diagram

8.Level Detector Block

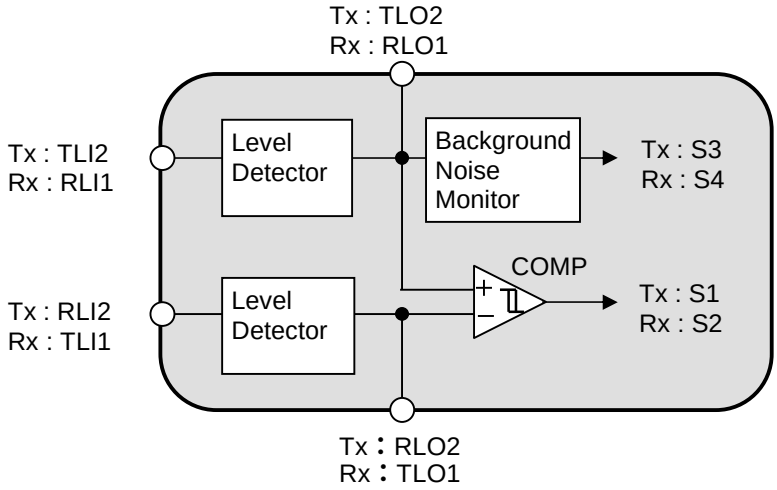
The **NJW1124** includes Level Detector Block on transmit block and receive block.
Level Detector Block consists of two same detectors and back ground noise monitor.
Fig.8(a) shows Level Detector block.
The signal(S1 to S4) output each detector transmits to attenuator controller to change the mode.
Next 8.1 and 8.2 explain each detector and Background Noise Monitor operation details.
About S1 to S4 signals, refer to 8 part.,

Level detector
Compare mic.amp output level(Transmit side) with receive attenuator output level or speaker output(Receive side)
Compare Receive amp output level(Receive side) with Transmit attenuator output level or speaker output (Transmit side)

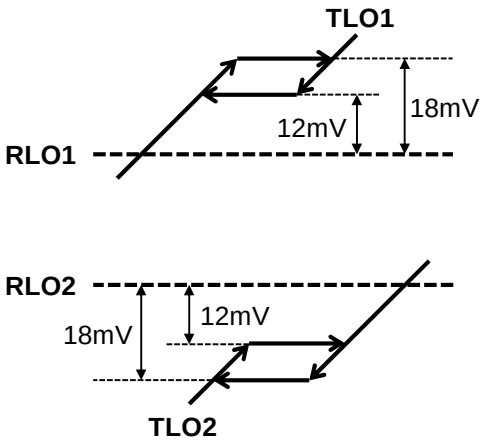
Mic amp output level ••• LI2
Receive attenuator •••RLI2
Receive amo output •••RLI1
Transmit attenuator •••TLI1

NJW1128 detects these 4point to judge transmit or receive, and input or no signal.

Comparator include 18mV hysteresis.
Logic switches being level difference more than 18mV.
Fig.8(b) shows hysteresis of the comparator.



(a) block diagram



(b) hysteresis of the comparator

Fig.8 Level detector

Table8 Truth table

S1	S2	S3	S4	Mode
Tx	Tx	1	X	Tx Mode
Tx	Rx	y	y	FAST Idle Mode
Rx	Tx	y	y	FAST Idle Mode
Rx	Rx	X	1	Rx Mode
Tx	Tx	0	X	SLOW Idle Mode
Tx	Rx	0	0	SLOW Idle Mode
Rx	Tx	0	0	SLOW Idle Mode
RX	Rx	X	0	SLOW Idle Mode

S1 ：Result comparing RLO2 and TLO2
(RLI2 and TLI2···Detecting Base Unit side)
RLO2>TLO2 [Rx]
TLO2>RLO2 [Tx]
S2 ：Result comparing RLO1and TLO1
(RLI1 and TLI1···Detecting Satellite Unit side)
RLO1>TLO1 [Rx]
TLO1>RLO1 [Tx]
S3＆S4 ：Output Background Noise Monitor
[1]:Detecting signal
[0]:Judging noise
[x]：Don.t Care
[y]：Both C3 and C4 is not 0.

8.1.Level Detector Circuit

Level detector circuit detects sound signal on each detecting point.Fig.8.1 shows level detector circuit.
Equation 8.1.1 shows voltages on each detecting point Vin and Vo(Voltage difference between Ref).

$$Vo = 0.026 \times Ln\left(\frac{\frac{Vin}{Ri} + 0.54\times10^{-6}}{0.54\times10^{-6}}\right) \quad \text{[unit : Volt]} \quad \cdots \quad (8.1.1)$$

For example, Vin=200mVrms(283mVpeak),Ri=10kΩ, Vo=103mV.
Equation 8.1.1 shows **input impedance Ri decides sensitivity level.**
Choose appropriate value Ci creating HPF with Ri. Cut off frequency is decided Ci and Ri.
Isink=Vin/Ri(input current to detect circuit) should be less than 1mA.
Minimum Ri value is more than 1kΩ. Recommend more than 5kΩ

Unwanted frequency signal should be cut by LPF,HPF,BPF created by mic.amp or receive amp..
Refer to note:2 part about more detail.

The capacitor connected to TLO1.2,RLO1.2 retains detected voltage level Vo.
The charging completes immediately. The discharge completes slowly I3=0.3μA.
Equation below defines δVo discharge

$$\delta Vo = -3\times10^{-7} / Co \quad \textbf{[unit : V/sec]} \quad \cdots \quad \textbf{(8.1.2)}$$

For example, Co=0.33μF, δVc=-0.909V/sec.

Level detector is half wave rectifier. It discharges in no detecting half cycle.
Thus, too small Co value deteriorates Vo rectify characteristic so background noise monitor wouldn't work.
Too large Co lengthen keeping time, so it lengthen transmit / receiver switching time.
And also long keeping time minifies level difference, it cause background noise monitor always judge input signal noise.
Please select appropriate Co value by adjusting actual product (more than 0.05μF).

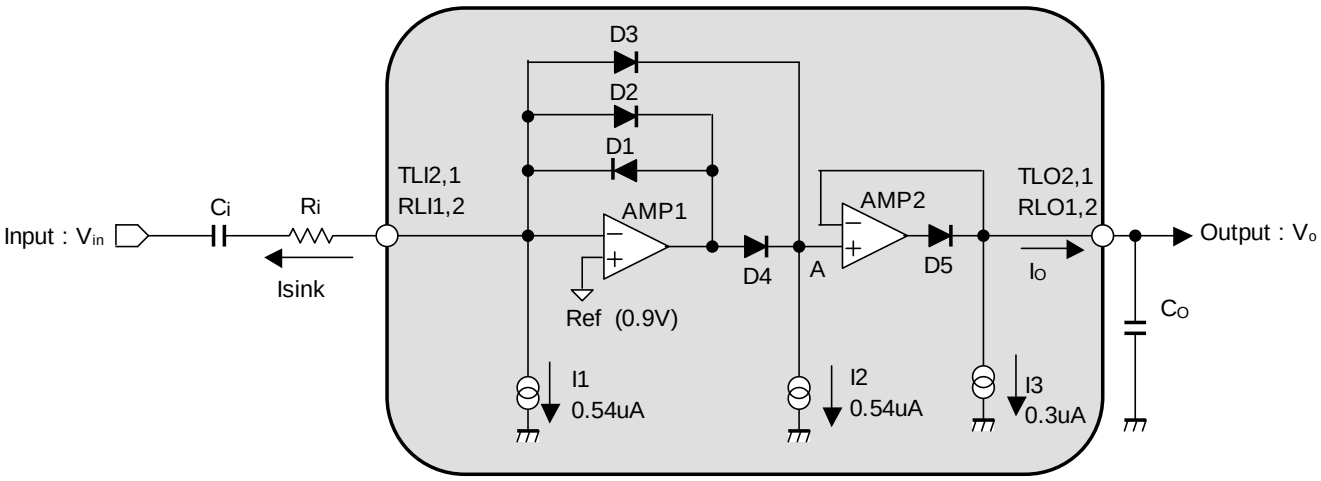


Fig.9.1 Level detector circuit diagram

External Parts	Purpose	Recommend Value	Explanation	Note
Cin	DC-decoupling	100n to 1μF	-	Cin and Rin create HPF
Rin	V-I Convert	5k to 100 kΩ	Iin=Vin/Rin	Iin > 100μF Each detector Input current should be same.
Co	Keep voltage level	0.05 to 1.0 μF	δVC=-0.3μA	Recommend low current leakage capacitor. Low value capacitor deteriorated rectifier characteristics.

8.2.Back Ground Noise Monitor

Background Noise Monitor judges whether the input signal is noise or sound (voice) by TLO2 and RLO2 voltage, and change the mode.
The **NJW1124** includes the Background noise monitor on transmit side and receive side.
Fig.9.2 shows Block diagram of Background noise monitor.

Background Noise Monitor inputted from TLO2 or RLO1, operates as follows.

1,On initial state, inverted input is 46mV higher voltage than non-inverted input. COMP output is 0(Lo).
2,When signal input to TLO2 or RLO1, COMP non-inverted input is inputted 2.7 times amplified TLO2 or RLO1 signal.
3,Then, if AMP1 output is higher than 36mV meaning COMP hysteresis, COMP output is 1(Hi).
4,At the same time, CPT and CPR is charged through AMP2.
5, Ccp voltage rises gradually in a certain gradient. Finally, the voltage becomes 46mV higher than AMP1 output.
6,When Ccp voltage reach 36 mV higher than AMP1, COMP output change to 0(Lo).

Operation detail is below.

[①,②]
The voltage difference between TLO2 or RLO1 and Ref is amplified 8.6dB on AMP1.
The signal from AMP1 inputs 2nd stage AMP2 and comparator (COMP) non-inverting input.
The signal from AMP2 having 46mV offset voltage inputs COMP inverting input.
COMP inverting voltage is 46mV higher than AMP1 output.
Thus, on initial state COMP output is 0(Lo), inputting signal COMP output shift to 1(Hi).

[③～⑥]
At the same time, 0.8μA internal current source charges external capacitor, until the C_{CP} voltage reach 46mV higher than AMP2 input voltage.

The equivalent below shows C_{CP} voltage charging gradient.

$$\Delta V_{CCP} = 0.8 \times 10^{-7} / C_{CP} \ [V/sec]$$

For example, C_{CP}=1μF,ΔV_{CP}=0.8V/sec.
The COMP non-inverting input voltage reach 36mV meaning COMP hysteresis higher than inverting, COMP output 0(Lo).

Fig. 8.2.2(a) shows operation of 1~6 explained before.
Fig. 8.2.2(b) shows operation inputting intermittent signal or large shift signal.
Back ground noise monitor judges that certain continued signal is noise.

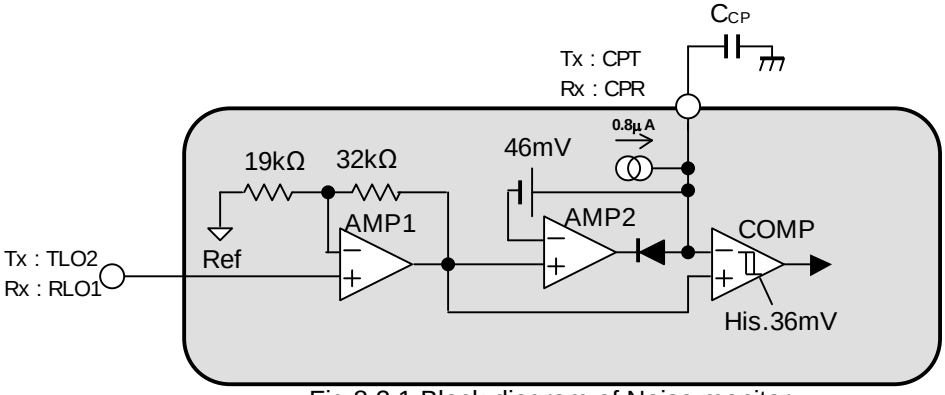
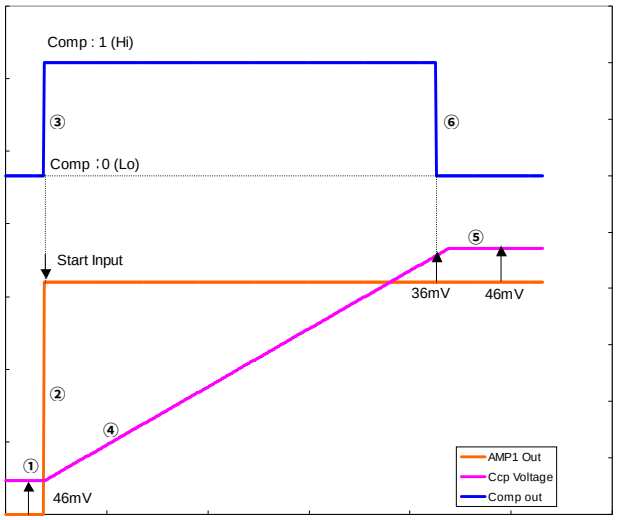
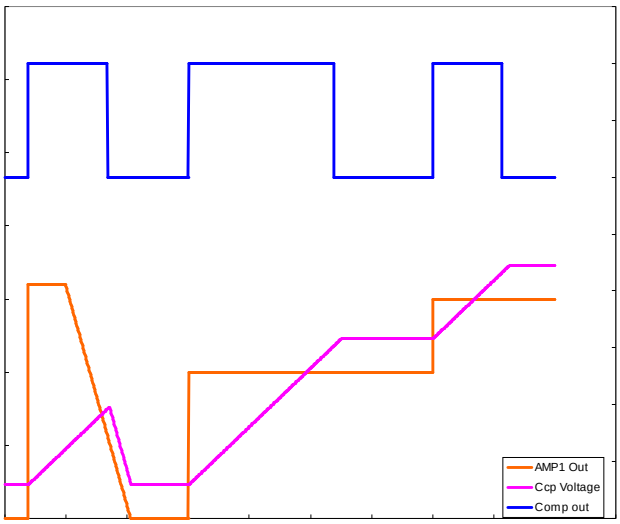


Fig.8.2.1 Block diagram of Noise monitor

External Parts	Purpose	Recommend Value	Explanation	Note
Ccp	Noise Detect	100nF to 1.0 μF	-	Decide the time detecting noise.



(a)Certain continued input signal example



(b) intermittent signal or large shift signal example

8.2.2 Operation of Noise monitor

9.Attenuator Controller

Attenuator Controller controls each mode(Transmit or Receive or idle) by the signal(S1 to S4) from level detector according as table.9.1 below
Fig.9.1 shows Attenuator Controller block diagram.
Table9.1 shows Switch ON/OFF condition truth table on each mode.

CT pin charge external C_{TR} to being VREF=+78mV or –78mV on Tx-mode or Rx-mode(S_{tx}=ON, S_{RX}ON,S_{IDLE}=ON).
Internal 12μA current source circuit charges $C_{CT.}$ Gradient is calculated below.

$\Delta V_{CCP} = 1.2 \times 10^{-5} / C_{CT}$ [V/sec] (9.1)

for example, C_{CT}=1μF, ΔV_{CCP}=12V/sec.
78mV voltage difference takes approximately 6.5msec.

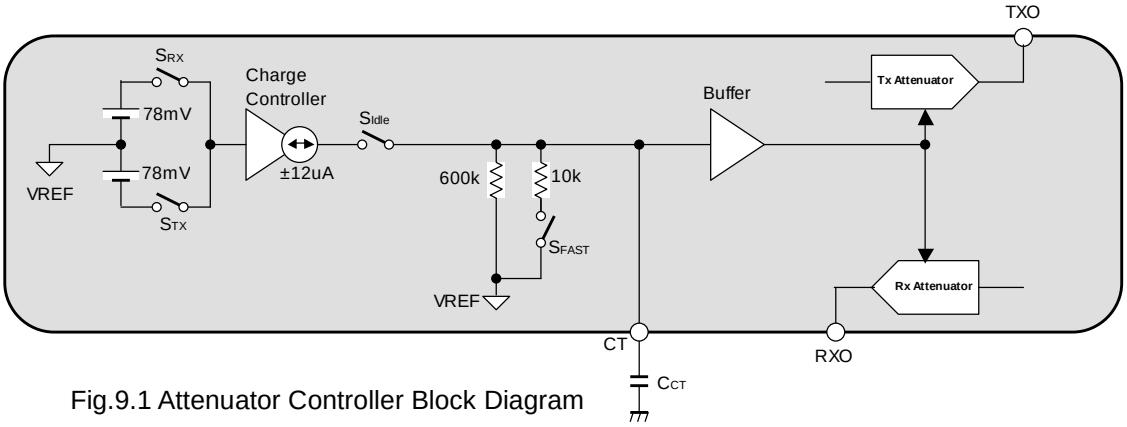


Fig.9.1 Attenuator Controller Block Diagram

Table.9.1 Attenuator Controller Truth Table

Mode	S_{RX}	S_{TX}	S_{Idle}	S_{FAST}
Tx Mode	OFF	ON	ON	OFF
Rx Mode	ON	OFF	ON	OFF
FAST Idle Mode	OFF	OFF	OFF	ON
SLOW Idle Mode	OFF	OFF	OFF	OFF

Idle mode: S_{TX}=OFF,S_{RX}=OFF, Sidle=OFF
Fast Idle mode: S_{FAST}=ON
Slow Idle mode: S_{FAST}=OFF

CT voltage become VREF voltage with time constant.
Time constant is below.

$\tau = RxC_{CT}$ [Sec] 9.2

R is 600kΩ on SLOW idle mode, 10kΩ on FAST mode.

Buffered CT pin voltage(V_{CT}) controls Tx attenuator and Rx attenuator directly.
V_{CT} is calculated below. ($G_{AT(TX)}$ =Gain of Tx attenuator, $G_{AT(RX)}$ =Gain of Rx attenuator,)

$$G_{AT(TX)} = 20Log\left[0.1\times\exp\left\{-\frac{(V_{CT}-VREF)}{0.026}\right\}\right] \quad \text{[unit : dB]} \quad (9.3)$$

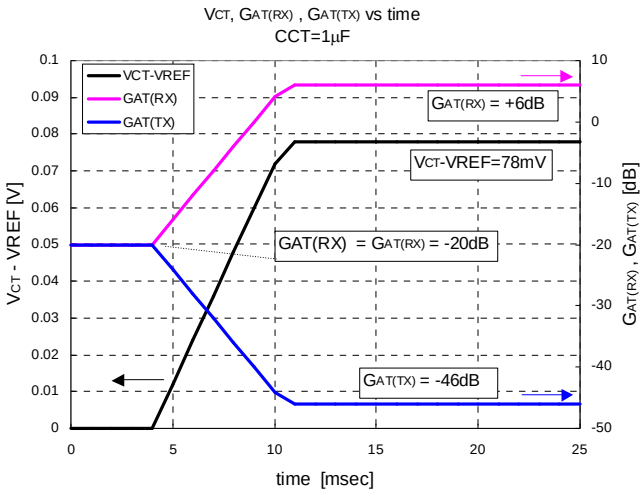
$$G_{AT(RX)} = 20Log\left[0.1\times\exp\left\{\frac{(V_{CT}-VREF)}{0.026}\right\}\right] \quad \text{[unit : dB]} \quad \cdots \quad (9.4)$$

For example, V_{CT} =Vref + 78mV on Rx-mode,
Results are $G_{AT(RX)}$ = -46dB , $G_{AT(RX)}$ = +6dB.

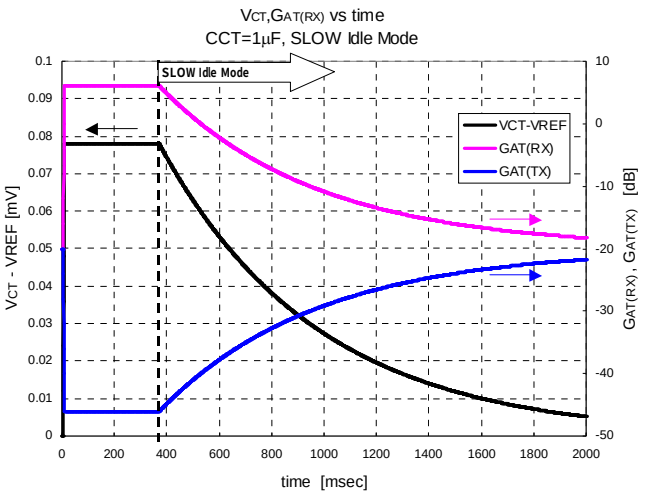
V_{CT} =Vref on idle-mode,
Results are $G_{AT(RX)}$ = -20dB , $G_{AT(RX)}$ = -20dB.

Fig,9,1,2(a),(b) shows these operating.

For adjusting, before adjust CT capacitor value, First, adjust TLI1,2 or RLI1,2 resistance value.
Second, adjust CPT,CPR capacitor value.
If after adjust 2 method adjust is not enough, adjust CT pin capacitor 1μF to other value.
(Fast attenuating or shifting is too slow.)



(a) V_{CT} Response example



(b) Response to SLOW idle mode

Fig.9.2 Attenuator Controller Operation

When measuring CT pin, use high impedance measuring equipment (recommend more than 1GΩ), because CT pin is high impedance and attenuator is very sensitive to CT pin voltage.
Dust and Condensation may prevent normal operation.

10.RT Switch

RTSW shifts the mode forcibly. RTSW changes the CTpin voltage forcibly to shift the mode.
Ex.9 shows the response to RTSW.

Table 10.1 RTSW Truth Table

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low Level Input Voltage	V_{IL}	0	-	0.3	V
High Level Input Voltage	V_{IH}	V^+-0.3	-	V^+	V

Table 10.2 NJW1128 mode and RTSW condition

Condition	Symbol	Operation
V_{IH}	Rx Mode	Receive mode priority.
OPEN ※	AUTO	Receive mode and Transmit mode are automatically switched.
V_{IL}	Tx Mode	Transmit mode priority.

※ Open or V+/2 voltage.

RTSW shifts the mode forcibly. Table.10.2 and 10.2 shows the response to RTSW.

It independent on input level and signal input or not. RTSW change the mode .
The mode doesn't change when RTSW working.

RTSW Detecting voltage switches Force Transmit mode, priority Receive mode, Auto mode(normal hands-free mode).
Fig.10.1 shows internal circuit block.
Table 10.3 and 10.4 shows Switching Operation.

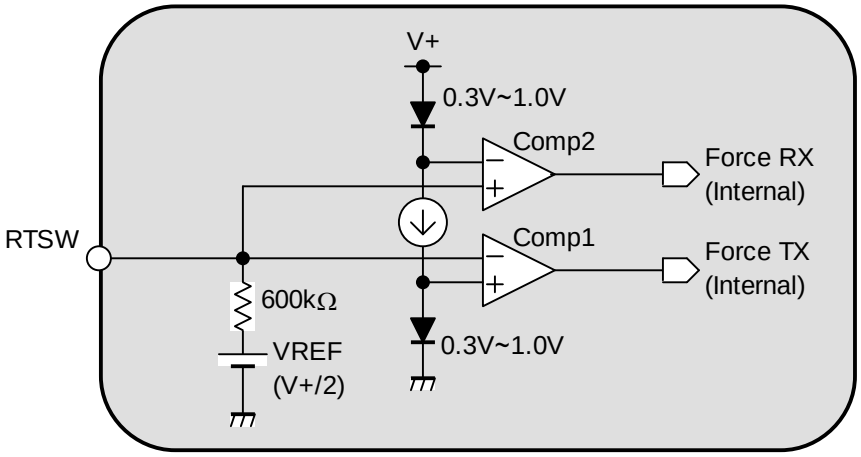


Fig.10.1 Internal circuit of RTSW

Table10.3 Truth Table RTSW voltage

RTSW Voltage	Force Rx	Force Tx
GND ~ 0.3V	Lo	Hi
0.3V ~ 1.0V	Lo	transition range
1.0V ~ (V+ -1.0V)	Lo	Lo
(V+ -1.0V) ~ (V+ -0.3V)	transition range	Lo
(V+ -0.3V) ~ V+	Hi	Lo

Table 10.4 Operating mode

Force RX	Force TX	Mode
Lo	Lo	Auto Mode
Lo	Hi	Tx Mode
Hi	Lo	Rx Mode
Hi	Hi	not supported

Notes:1
To reduce Pop-Noise of power-on and off.

Appropriate power supply sequence reduces pop-noise.

Initial condition: No power supply.
SPSW=MUT=GND(less than 0.3V), CD=V+

[Power-on sequence]
1.Power-on NJW1128. Concurrently the circuit which connected to Receive In and Mic. in power on.
2.After 1 sec, Activate Speaker Amp of NJW1128(SPSW GND to V+)

[Power-off sequence]
1.Speaker Amplifier shift standby mode (SPSW V+ to GND).
2.NJW1128 power off. Concurrently, the circuit which connected to Receive In and Mic.amp power off

Notes:2:
Filter circuit using Receive amplifier, Mic. Amplifier, Line amplifier.

Receive amplifier, Mic. Amplifier, Line amplifier enable to form active filter circuit which is 1st order or 2nd order, HPF or LPF or BPF.
Example is below. Example shows that receive amplifier version, but mic.amp and line amp also are able to create filter on same way.

1.1st order HPF,LPF circuit example
Fig.2.1 shows 1st order (-6dB/oct) HPF, LPF circuit.
Combining HPF formed by Co and R1, and LPF formed by C1 and R2, forms BPF.
(Co should be also used typical application as DC decoupling.)

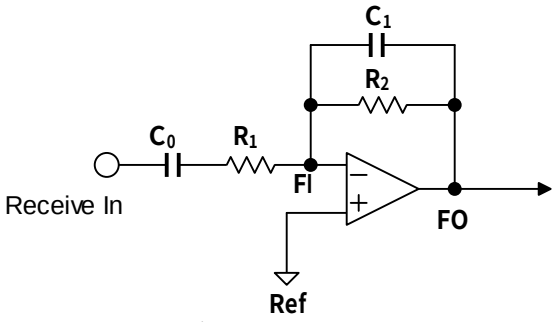
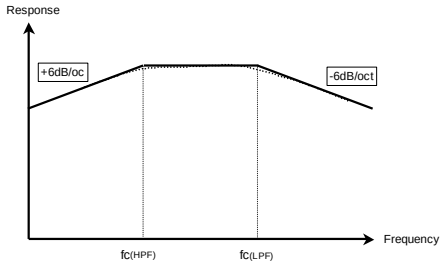


Fig.2.1 1st order HPF,LPF circuit example

$$f_{C(HPF)} = \frac{1}{2\pi C_0 R_1}$$

$$f_{C(LPF)} = \frac{1}{2\pi C_1 R_2}$$



2. 2nd order LPF circuit example
Fig.2.2 shows 2nd order (-12dB/oct) LPF circuit.
Same as 1st order filter, Co should be used as DC decoupling. It works as BPF.
C2 selecting arbitrarily, Butterworth filter forming coefficient is as below.

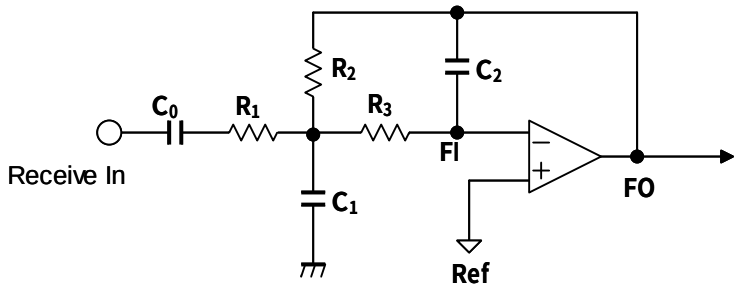


Fig.2.2 2nd order LPF circuit example

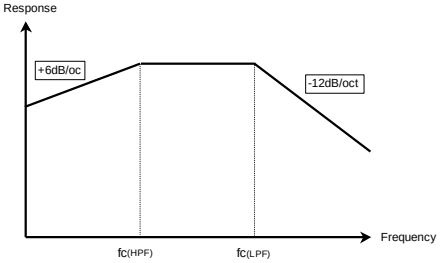
$$R_1 = \frac{1}{2\sqrt{2}G\pi f_{C(LPF)} C_2}$$

$$R_2 = \frac{1}{2\sqrt{2}\pi f_{C(LPF)} C_2}$$

$$R_3 = \frac{1}{2\sqrt{2}(G+1)\pi f_{C(LPF)} C_2}$$

$$C_1 = 2(G+1)C_2$$

$$G : Gain$$



$f_{C(HPF)}$ is same as 1st order type above

Fig.2.3 shows LPF(Gain=20dB,$fc_{(LPF)}$=4kHz) circuit example.

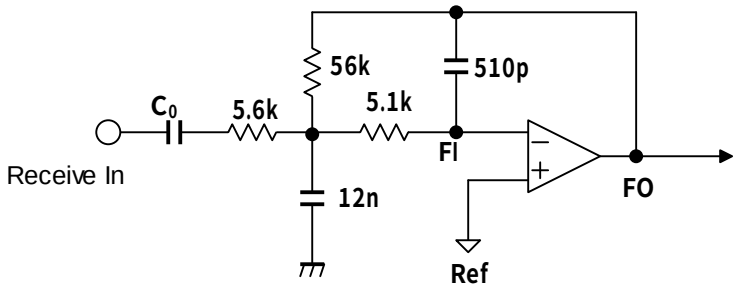


Fig.2.3 2nd order LPF circuit example
Gain=20dB,$fc_{(LPF)}$ = 4kHz, Butterworth filter

3.2nd order HPF circuit example

Fig.2.4 shows 2st order (+12dB/oct) HPF circuit.
Co=C2, Butterworth filter forming coefficient is as below.

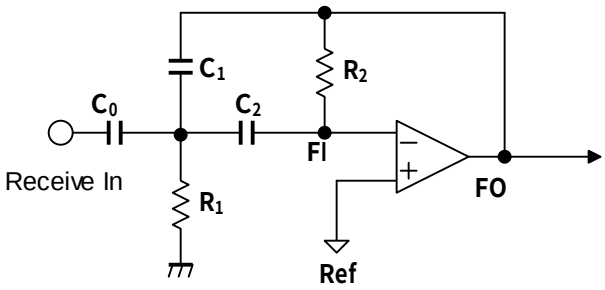


Fig.2.4 2nd order HPF circuit example.

$$R_1 = \frac{\sqrt{2}}{2\pi f_{C(HPF)} C_0 (2 + 1/G)}$$

$$R_2 = \frac{2G + 1}{2\pi f_{C(HPF)} C_0}$$

$$C_1 = \frac{C_0}{G}$$

$$C_0 = C_2$$

$$G : Gain$$

Fig.2.5 shows HPF(Gain=20dB,$fc_{(LPF)}$=200Hz) circuit example.

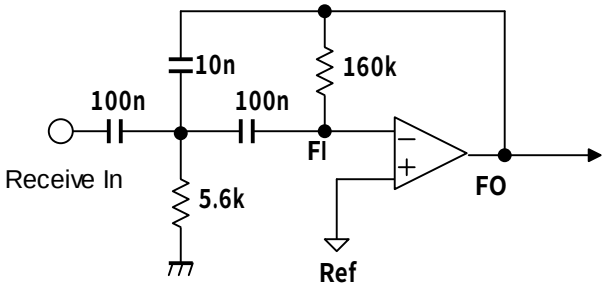


Fig.2.5 2nd order HPF circuit example.
Gain=20dB,$Fc_{(HPF)}$=200Hz, Butterworth filter

3.1nd order BPF circuit example

Fig.2.6 shows 1st order (+12dB/oct) HPF circuit.
Butterworth filter forming coefficient is as below.

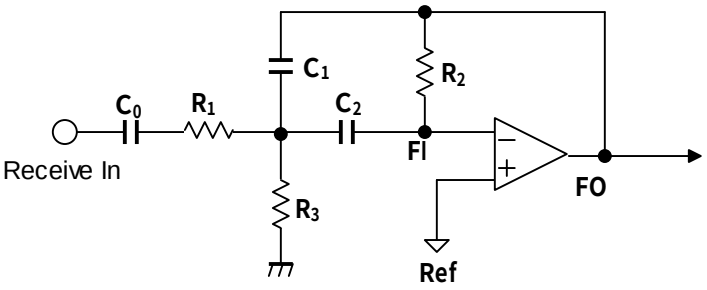


Fig.2.6 1nd order BPF circuit example.

$$R_1 = \frac{R_2}{2G}$$

$$R_3 = \frac{R_1 R_2}{4Q^2 R_1 - R_2}$$

$$R = \frac{R_1 R_3}{R_1 + R_3}$$

$$C_1 = C_2 = \frac{1}{2\pi f_{C(BPF)} \sqrt{R_3 R}}$$

$$Q : Quality Factor$$

$$G : Gain$$

Actually, it also works as HPF.
Fig.2.7 shows BPF(Gain=20dB,$fc_{(LPF)}$=1kHz,Qyality Factor=3) circuit example.

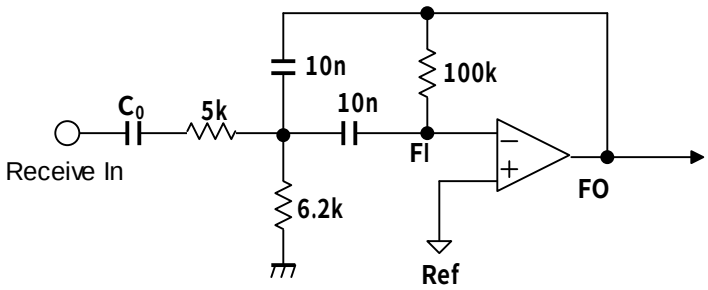


Fig.2.7 1nd order BPF circuit example.
Gain=20dB,$fc_{(HPF)}$=1kHz, Quality Factor=3

Notes:3
Other application.

1.Disable Background Noise Monitor

Fig.8.2.1 shows stopping Background Noise Monitor function.
Being CPT,CPR pin voltage lower than AMP1(0.3V~0.6V) output voltage keep Comp output '1'.
This can stop to shift background noise monitor mode, even if continued signal input. It means keeping transmit mode or receive mode.
However, when transmit and receive signal input at the same time, shift to Fast idle mode.

Fig3.1 shows Stopping Background noise monitor block diagram.

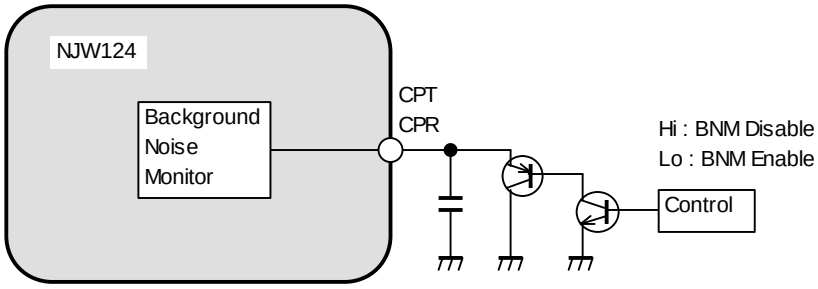


Fig3.1 Background Noise Monitor mode Enable/Disable control

1. Supply Vref (reference voltage) to other circuit
Vref circuit including NJW1128 is not able to supply reference voltage directly.
Supplying Vref needs external Buffer amp.(Op.amp) like Fig.3.31 below.
Supplying Without Buffer amp. causes deteriorate cross talk and abnormal operation by external circuit influence.

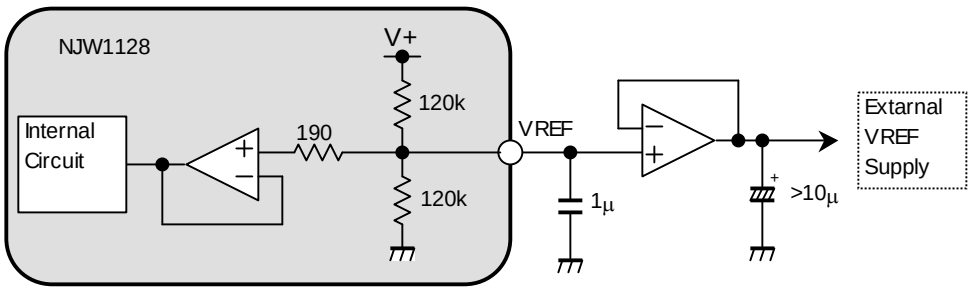


Fig.3.3.1 Supply Vref(Reference Voltage) to external circuit 1

In case that Buffer amp can't prepare, make Vref circuit outside NJW1128 by resistor and capacitor like Fig.3.3.2.

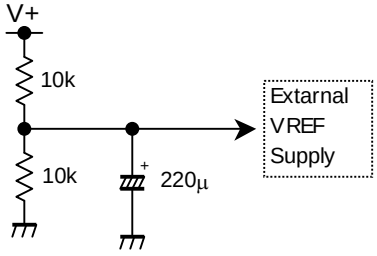


Fig.3.3.2 Supply Vref(Reference Voltage) to external circuit 2

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