

Low phase noise Fundamental Quartz Crystal Oscillator IC

■FEATURES($V_{DD}=3.3V$, $f_0=49.152MHz$, $T_a=25^{\circ}C$)

- Phase noise -103dBc/Hz(Typ.) @10Hz Offset
-163dBc/Hz(Typ.) @1kHz Offset
- RMS Jitter 0.05psec(Typ.) @12kHz to 20MHz
- Oscillation Frequency 20MHz to 50MHz(Fundamental)
- Operating Voltage 1.62V to 3.63V
- Operating Current 9.0mA(Typ.) @ $C_L=15pF$.
- 3-State Output Buffer
- Oscillation Capacitors C_g and C_d on-chip
- Operation Temperature $-40^{\circ}C$ to $+125^{\circ}C$
- Package Outline DFN6-G1(ESON6-G1)

■GENERAL DESCRIPTION

The **NJU6385** is a C-MOS quartz crystal oscillator IC (20MHz to 50MHz) realized very low phase noise. It is consisted of an oscillation amplifier and 3-state output buffer.

The NJU6385 in low voltage operation features low phase noise, it is suitable for a master-clock generator into a D-A converter of digital audio system.

■APPLICATION

- Car Audio / Car Navigation System
- Home Audio
- Portable Audio
- USB DAC

■PIN CONFIGURATION

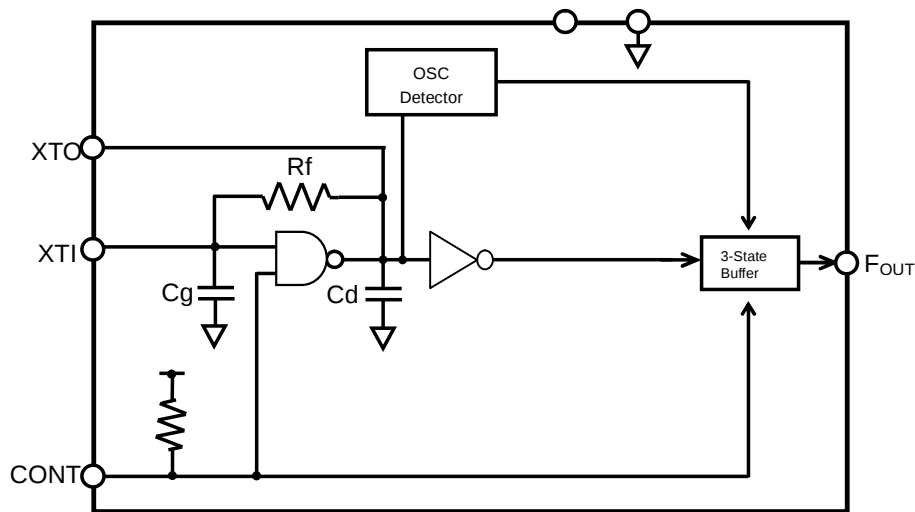
Parts Number	NJU6385KG1
Package Outline	DFN6-G1(ESON6-G1)(*)
Pin Function	TOP View

(*)Connect to exposed pad to V_{SS} or OPEN

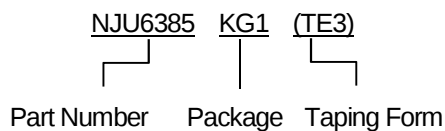
■TERMINAL DISCREPTION

SYMBOL	FUNCTION
CONT	Oscillation and 3-state Output Buffer Control
	CONT F_{OUT}
	H or OPEN Frequency Output
	L Oscillation Stop and High impedance Output
XTI XTO	Quartz Crystal Connection terminals
V_{SS}	GND terminal ($V_{SS}=0V$)
F_{OUT}	Frequency Output terminal (3-State Output Buffer)
V_{DD}	Power Supply terminal $V_{DD}=1.62$ to $3.63V$

■BLOCK DIAGRAM



■PRODUCT NAME INFORMATION



■ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.6 to +6.0	V
Input Voltage	V_{IN}	-0.6 to $+V_{DD}+0.6$ and $\leq 6.0V$	V
Output Voltage	V_O	-0.6 to $V_{DD}+0.6$	mV
Input Current	I_{IN}	± 10	mA
Output Terminal Input Voltage	I_O	± 25	mV
Power Dissipation($T_a=25^\circ C$) DFN6-G1(ESON6-G1) ⁽²⁾	P_D	(2-layer / 4-layer) 420 / 1200	mW
Junction Temperature	T_{jmax}	+150	$^\circ C$
Operating Temperature Range	T_{opr}	-40 to +125	$^\circ C$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ C$

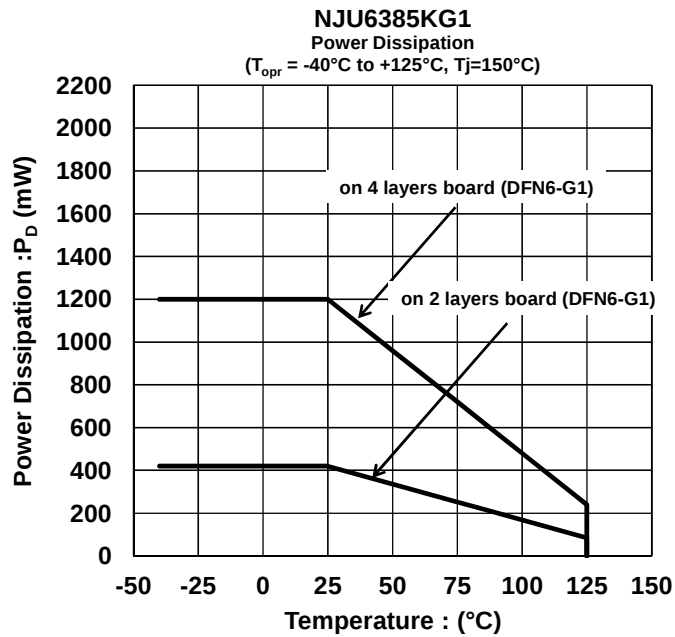
(1) If the LSI used condition above the absolute maximum ratings, the LSI may be destroyed. Use beyond the electric characteristics conditions will cause mal-function and poor reliability.

(2) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

■POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ELECTRICAL CHARACTERISTICS⁽⁴⁾

($T_a=25^{\circ}\text{C}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	$f_{OSC}=50\text{MHz}$	1.62	-	3.63	V
Input Voltage	V_{IN}	CONT	0	-	3.63	V
Output Voltage	V_{OUT}	F_{OUT}	0	-	V_{DD}	V
Output Frequency Stability	df/f	$V_{DD}\pm 10\%$	-	± 1	-	ppm

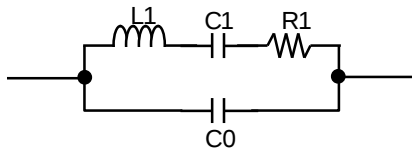
$(V_{DD}=1.62 \text{ to } 3.63\text{V}, V_{SS}=0\text{V}, T_a=25^\circ\text{C})$

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Current	I_{DD}	$f_0=49.152\text{MHz}$ No load TEST CIRCUIT(1) ⁽³⁾ $F_{OUT}=49.152\text{MHz}$	$V_{DD}=1.8\text{V}$	-	1.8	2.9	mA
			$V_{DD}=2.5\text{V}$	-	3.3	4.8	
			$V_{DD}=3.3\text{V}$	-	5.5	7.7	
		$f_0=49.152\text{MHz}$ $C_L=15\text{pF}$ TEST CIRCUIT(1) ⁽³⁾ $F_{OUT}=49.152\text{MHz}$	$V_{DD}=1.8\text{V}$	-	3.1	4.1	
			$V_{DD}=2.5\text{V}$	-	5.1	6.6	
			$V_{DD}=3.3\text{V}$	-	7.9	9.9	
Stand-by Current	I_{STB}	TEST CIRCUIT(1) ⁽³⁾ CONT= V_{SS}	$V_{DD}=1.8\text{V}$	-	3.0	25.0	μA
			$V_{DD}=2.5\text{V}$	-	5.0	30.0	
			$V_{DD}=3.3\text{V}$	-	9.0	35.0	
H Level Output Voltage	V_{OH}	TEST CIRCUIT(2) ⁽³⁾		$V_{DD}-0.4$	-	-	V
L Level Output Voltage	V_{OL}	TEST CIRCUIT(2) ⁽³⁾		-	-	0.4	V
H Level Input Voltage	V_{IH}	TEST CIRCUIT(3) ⁽³⁾		$0.7V_{DD}$	-	-	V
L Level Input Voltage	V_{IL}	TEST CIRCUIT(3) ⁽³⁾		-	-	$0.3V_{DD}$	V
Input Current	I_{IN}	TEST CIRCUIT(4) ⁽³⁾ , $V_{DD}=1.62\text{V}$, CONT= V_{DD}		-	-	+65	nA
		TEST CIRCUIT(4) ⁽³⁾ , $V_{DD}=1.62\text{V}$, CONT= V_{SS}		-	-	-0.5	μA
		TEST CIRCUIT(4) ⁽³⁾ , $V_{DD}=3.63\text{V}$, CONT= V_{DD}		-	-	+150	nA
		TEST CIRCUIT(4) ⁽³⁾ , $V_{DD}=3.63\text{V}$, CONT= V_{SS}		-10	-	-	μA
3-state Off Leakage Current	I_{OZ}	TEST CIRCUIT(5) ⁽³⁾ CONT= V_{SS} , $F_{OUT}=V_{DD}$ or V_{SS}		-	-	± 1	μA
Feedback Resistance	R_f			35	50	65	k Ω
Built-In Oscillator Capacitance	C_g	$f_{OSC}=50\text{MHz}$		-	8	-	pF
	C_d	$f_{OSC}=50\text{MHz}$		-	17	-	pF
Oscillation Frequency	F_{OSC}	Recommendation ⁽⁴⁾		-	-	50	MHz
Output Signal Symmetry	SYM	$C_L=15\text{pF}$, @ $V_{DD}/2$		45	50	55	%
Phase Noise	SSB	$f_{OSC}=49.152\text{MHz}$ $V_{DD}=1.8\text{V}$	10Hz Offset	-	-103	-	dBc /Hz
			1kHz Offset	-	-158	-	
			Floor	-	-166	-	
		$f_{OSC}=49.152\text{MHz}$ $V_{DD}=3.3\text{V}$	10Hz Offset	-	-103	-	
			1kHz Offset	-	-163	-	
			Floor	-	-172	-	
Output Signal rise Time	T_r	TEST CIRCUIT(1) ⁽³⁾ $0.1V_{DD}$ to $0.9V_{DD}$	$V_{DD}=1.8\text{V}$	-	3.1	4.7	ns
			$V_{DD} \geq 2.5\text{V}$	-	1.8	2.7	ns
Output Signal fall Time	T_f	TEST CIRCUIT(1) ⁽³⁾ $0.9V_{DD}$ to $0.1V_{DD}$	$V_{DD}=1.8\text{V}$	-	2.8	4.2	ns
			$V_{DD} \geq 2.5\text{V}$	-	1.8	2.7	ns
Output Disable Time	t_{POZ}	TEST CIRCUIT(6) ⁽³⁾		-	-	200	ns
Output Enable Time	t_{PZO}	TEST CIRCUIT(6) ⁽³⁾		-	-	1	ms
Oscillation Start-Up Time	t_{OSC}	TEST CIRCUIT(1) ⁽³⁾		-	-	1	ms

(3) Decoupling capacitor over than 0.01 μF ceramic capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

(4) NJR's standard crystal is used for measurement of the oscillation frequency range and it does not guarantee oscillation. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS)

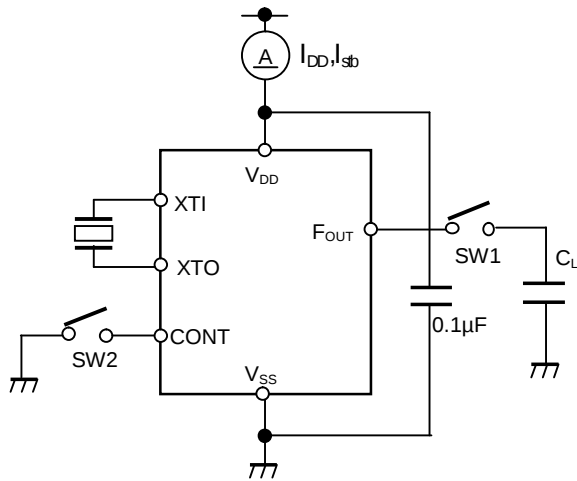
■EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS



f[MHz]	R1[Ω]	L1[mH]	C1[fF]	C0[pF]
49.152	17.7	3.83	2.74	1.23

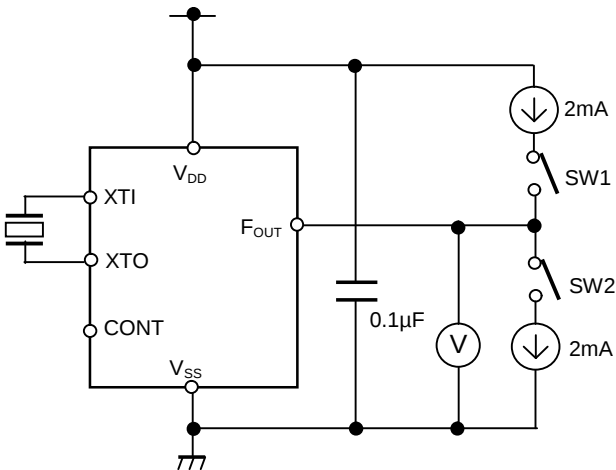
■ TYPICAL TEST CIRCUIT

(1) Operating Current, Stand-by Current, Output Signal rise / Fall Time, Oscillation Start-Up Time



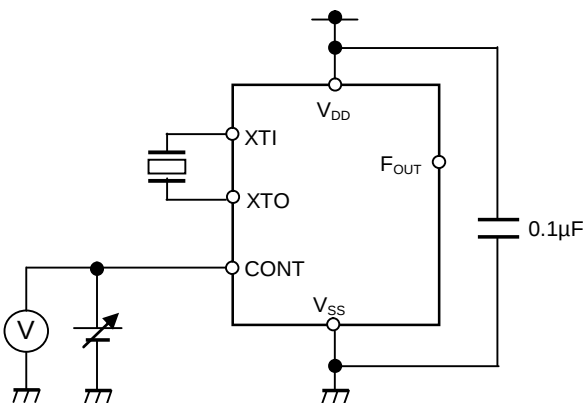
PARAMETER	SW1	SW2
$I_{DD}(C_L=0pF)$	OFF	OFF
$I_{DD}(C_L=15pF)$	ON	OFF
I_{sb}	ON or OFF	ON
SYM, t_k , t_f	ON	OFF
t_{osc}	ON	OFF

(2) High-level / Low-level Output Voltage (V_{OH} / V_{OL})



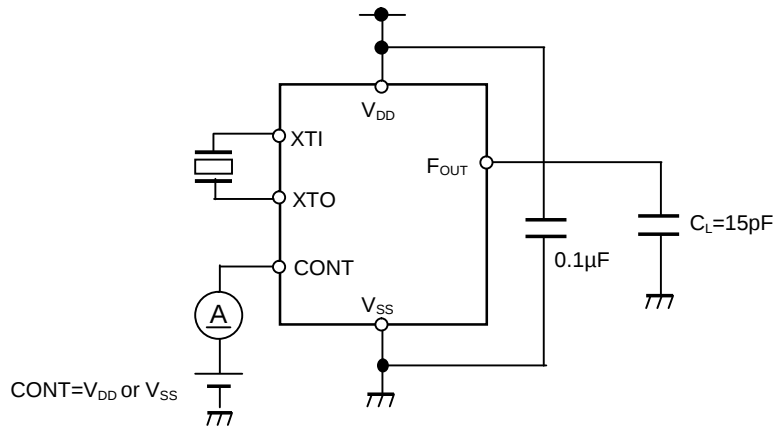
PARAMETER	SW1	SW2
V_{OH}	OFF	ON
V_{OL}	ON	OFF

(3) High-level / Low-level Input Voltage (V_{IH} / V_{IL})

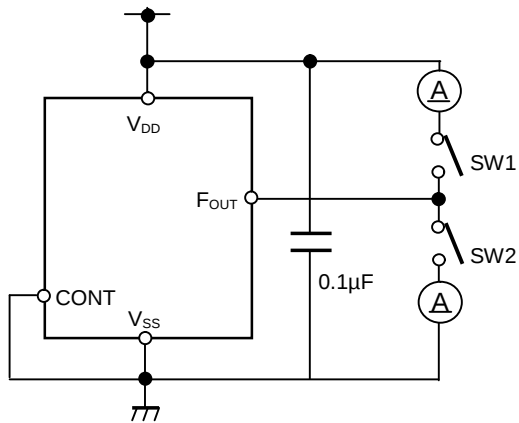


PARAMETER	F_{OUT}
$CONT \geq 0.7V_{DD}$	Oscillation
$CONT \leq 0.3V_{DD}$	Stop

(4) Input Current (I_{IN})

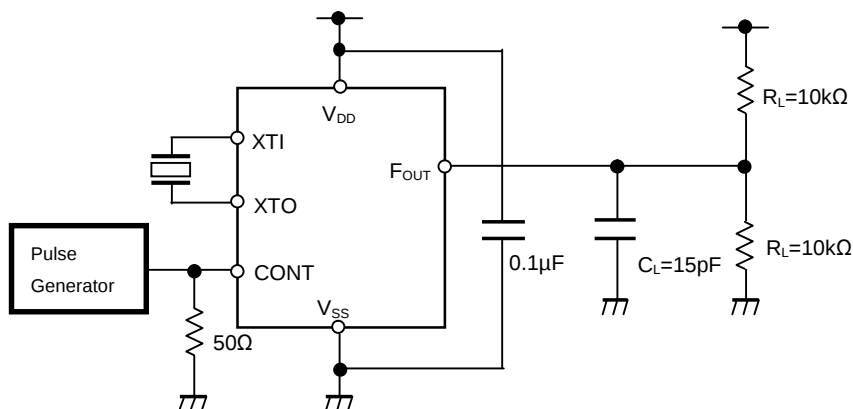


(5) 3-State Off Leakage Current (I_{OZH}/I_{OZL})



PARAMETER	SW1	SW2
I_{OZH}	OFF	ON
I_{OZL}	ON	OFF

(6) Output Disable Time, Output Enable Time (T_{POZ}/T_{PZO})



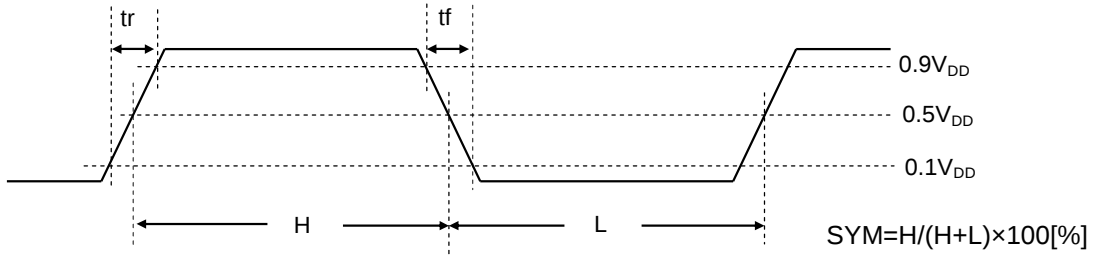
■TIMING CHART


Fig.1 Output Signal Rise Time: t_r , Output Signal Fall Time: t_f , Output Symmetry: SYM

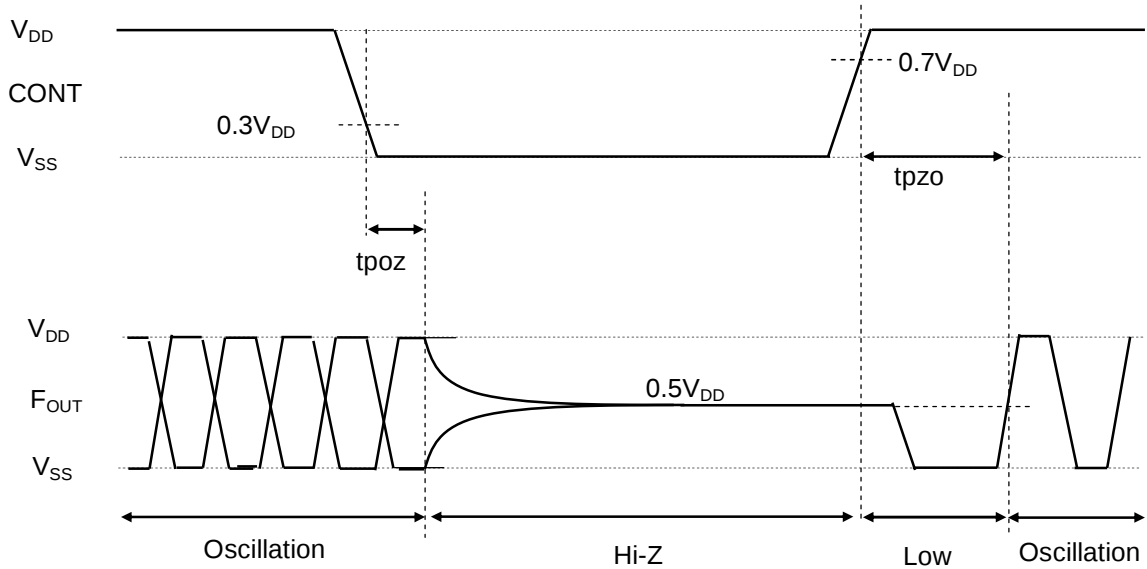


Fig.2 Output Disable time: $tpoz$, Output Enable time: $tpzo$, Timing Chart

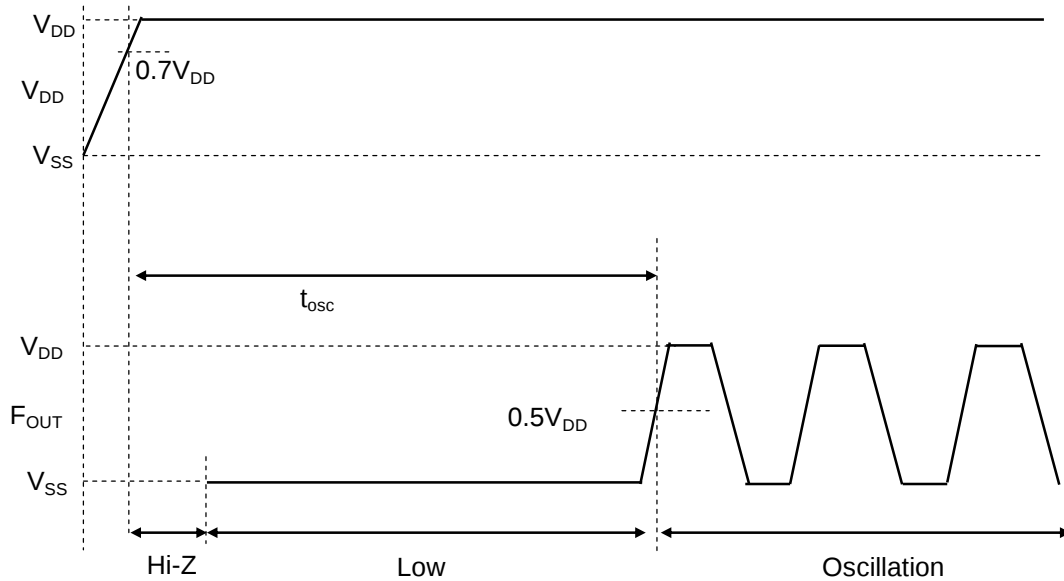
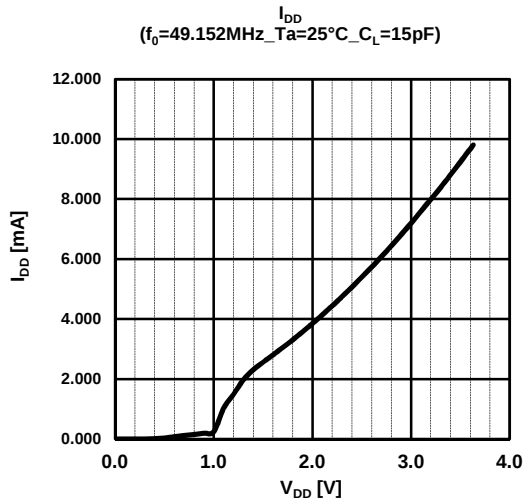


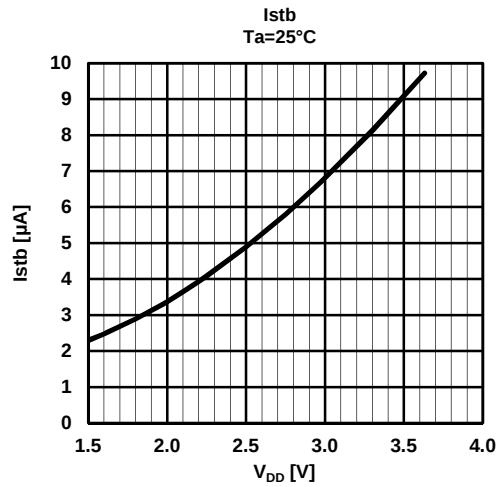
Fig.3 Oscillation Start time: t_{osc}

■ TYPICAL CHARACTERISTICS

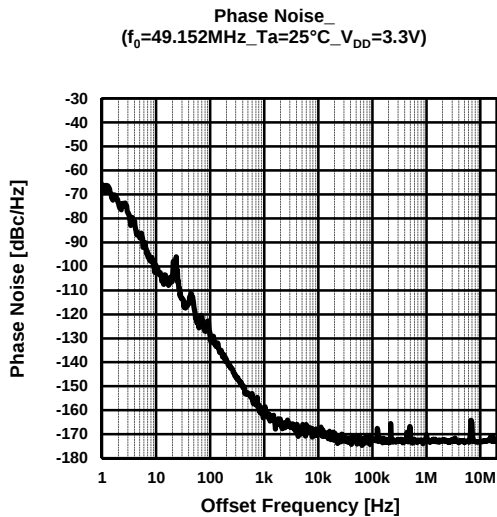
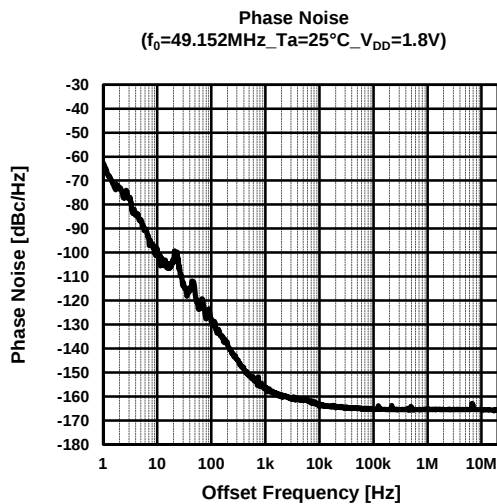
• Operating Current



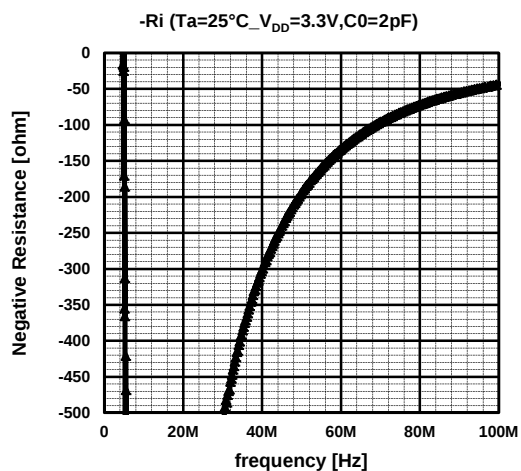
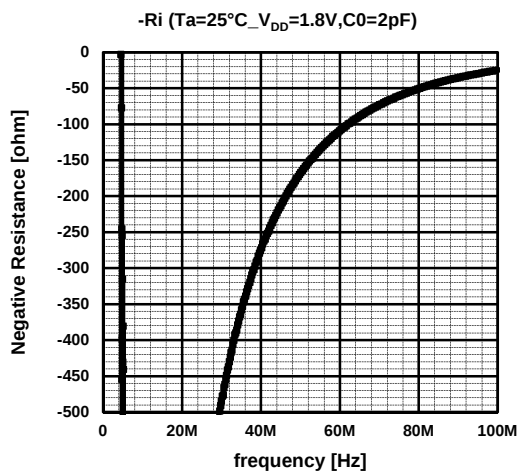
• Stand-by Current



• Phase Noise

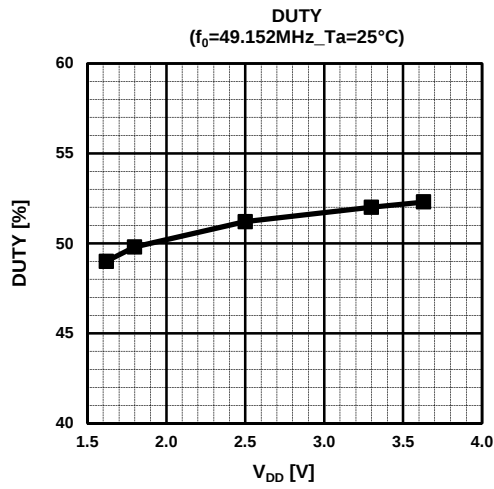


• Negative Resistance

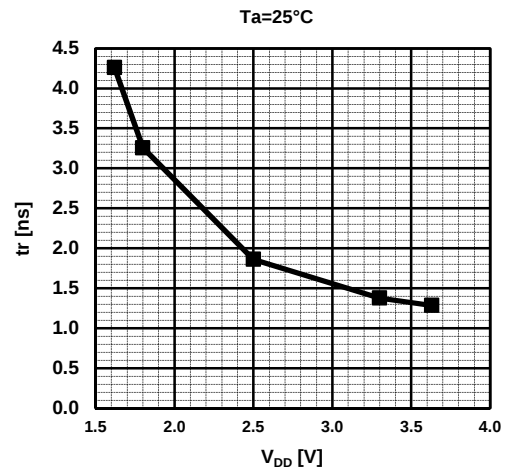


Note; A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

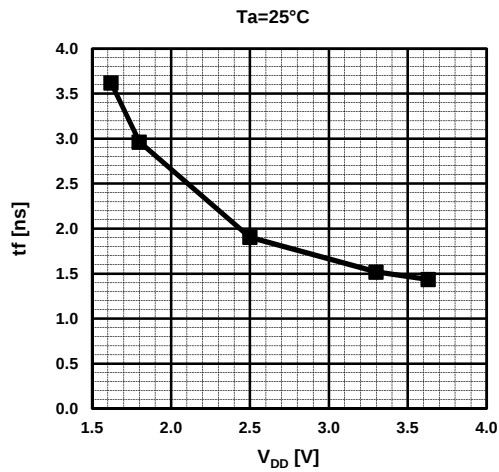
• Output Signal Symmetry



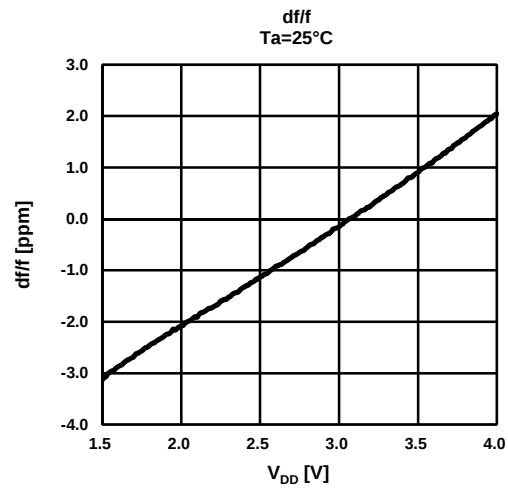
• Output Signal rise Time



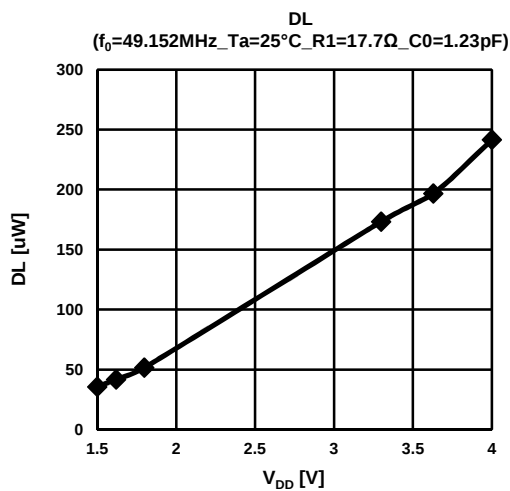
• Output Signal fall Time



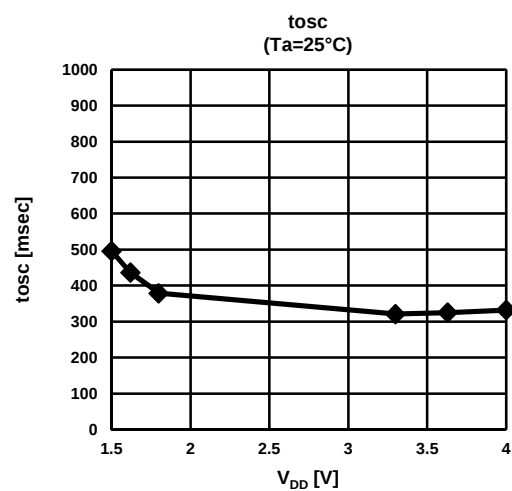
• Output Frequency Stability



• Drive Level



• Oscillation Start-Up Time



■Application Note

FUNCTIONAL DESCRIPTION

•Standby Function

When CONT Terminal is “Low”, the F_{OUT} Terminal output is High impedance.

CONT	F_{OUT}	Oscillator
High(Open)	Frequency output	Normal operation
Low	High impedance	Stop

When not using Stand-by function, CONT terminal is recommended to connect to V_{DD} .

•Built-in Variable Pull-up Resistance of CONT terminal

The built-in pull-up resistance value of CONT Terminal changes in response to the input level. When CONT is “Low” level, the pull-up resistance value is large to reduce the current consumption by the resistance. When CONT is open or connected to V_{DD} , the pull-up resistance value is small to decrease the input susceptibility to external noise. It works to prevent an unexpectedly stopping of the output by external noise.

Choice of crystal at notice

Standard crystal unit example

	Dxx2520xx
Frequency Range	30 to 54 MHz
Overtone Order	Fundamental

Equivalent Series Resistance	50Ω max.
Drive Level	10μW (Max. 200μW)
Load Capacitance	8, 12, 15 pF

- This range is related to crystal oscillation IC.

Equivalent Series Resistance: Equivalent resistance of crystal unit when series resonance.(refer to perspective of $-R_i$)

Drive Level: Loading condition of crystal resonator, which is determined by electric current or power.

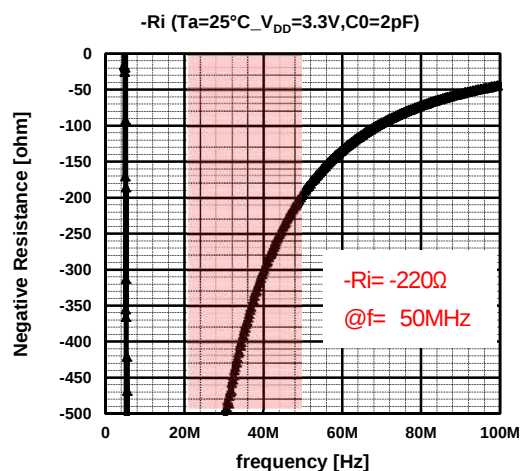
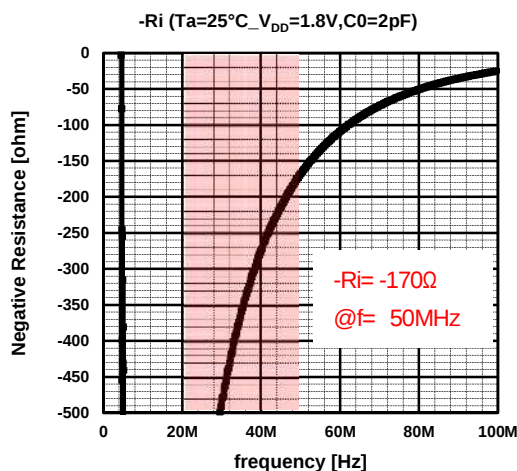
(refer to perspective of drive level)

Load Capacitance: The effective external capacitance that determines the resonance frequency of a crystal resonator.

(refer to A formula of load capacitance.)

Perspective of $-R_i$

■ :NJU6385 Oscillation Frequency Range.(20MHz to 50MHz)

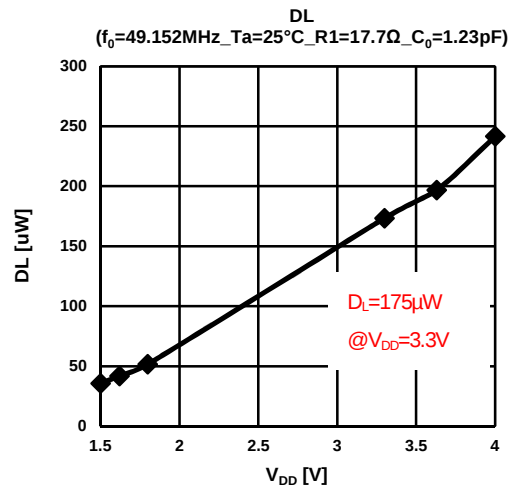


Note: A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

Perspective of Drive Level

According to graph, $D_L = 200\mu W$ at $V_{DD} = 3.3V$, $f = 49.1592MHz$

We recommend the high drive level crystal unit. example $200\mu W$ [max.]



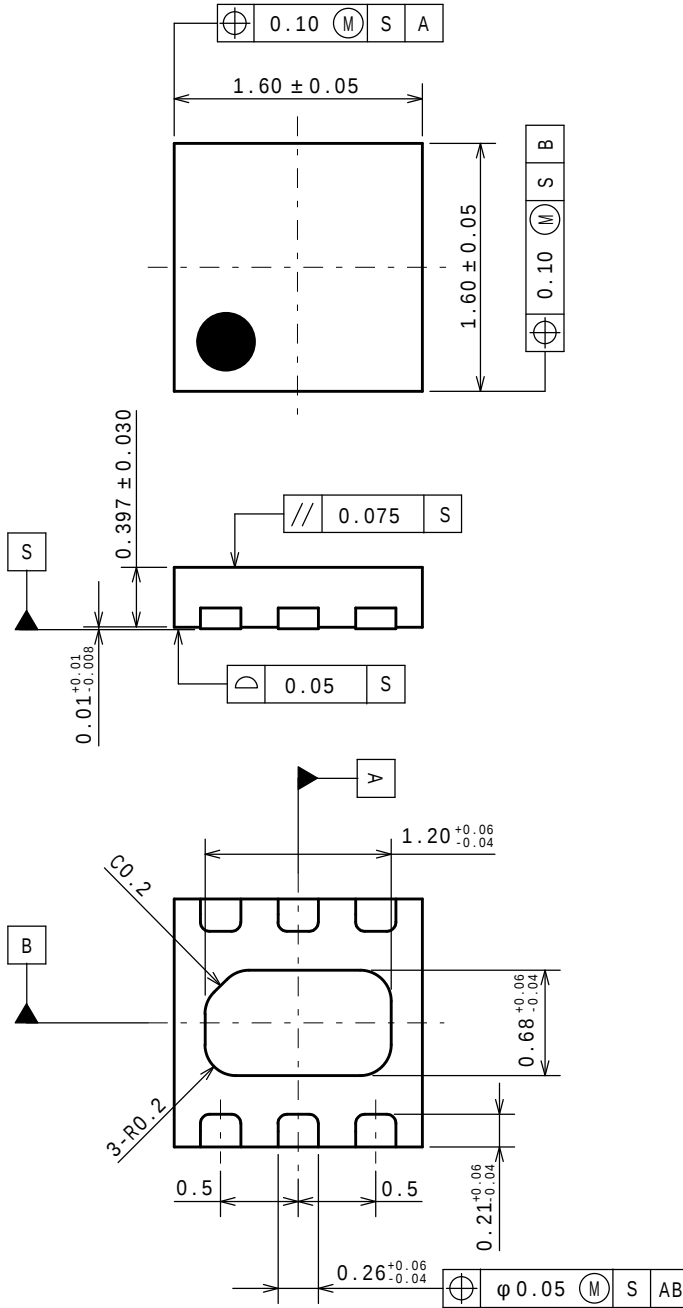
A formula of Load Capacitance. (In case of internal capacitance of NJU6385)

$$C_L = C_g \times C_d / (C_g + C_d) = 8pF \times 17pF / (8pF + 17pF) \approx \underline{5.44pF} \quad \leftarrow \text{Load Capacitance of crystal unit.}$$

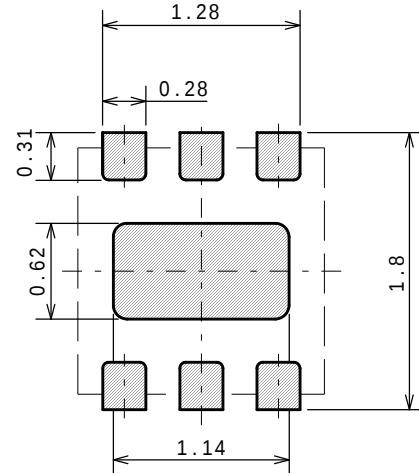
DFN6-G1(ESON6-G1)

Unit: mm

■PACKAGE DIMENSIONS

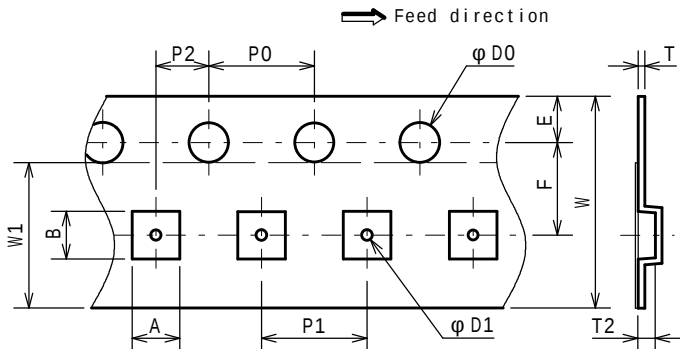


■EXAMPLE OF SOLDER PADS DIMENSIONS



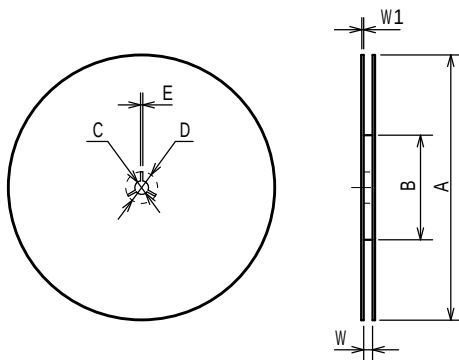
PACKING SPEC

TAPING DIMENSIONS



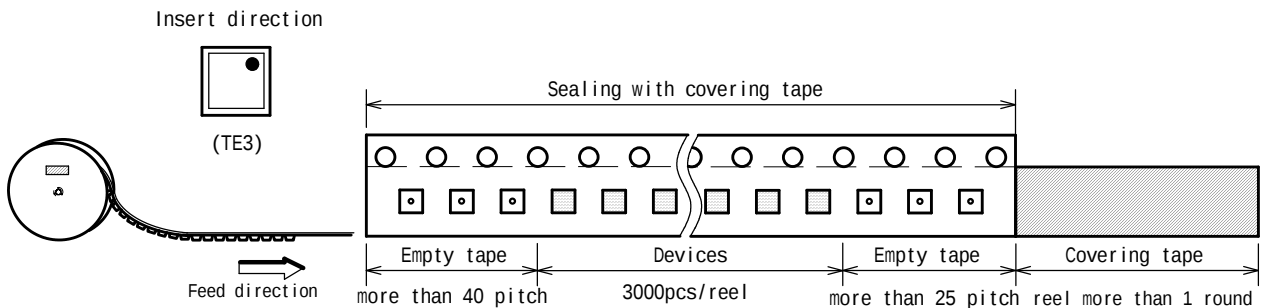
SYMBOL	DIMENSION	REMARKS
A	1.85 ± 0.05	BOTTOM DIMENSION
B	1.85 ± 0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_0$	
D1	0.5 ± 0.1	
E	1.75 ± 0.1	
F	3.5 ± 0.05	
P0	4.0 ± 0.1	
P1	4.0 ± 0.1	
P2	2.0 ± 0.05	
T	0.25 ± 0.05	
T2	0.65 ± 0.05	
W	8.0 ± 0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

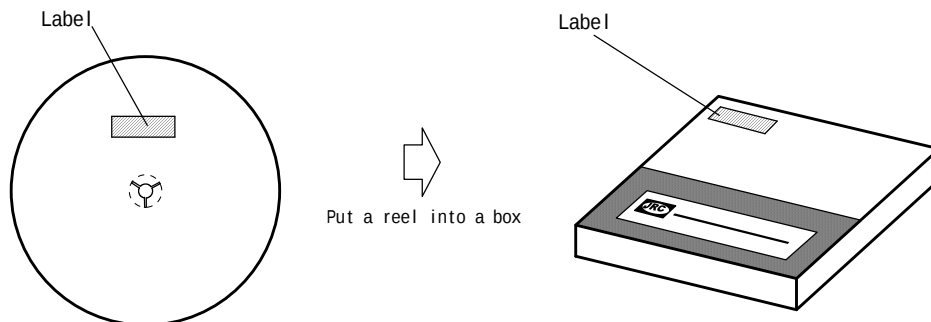


SYMBOL	DIMENSION
A	$\phi 180^{+0}_{-1.5}$
B	$\phi 60^{+1}_0$
C	$\phi 13 \pm 0.2$
D	$\phi 21 \pm 0.8$
E	2 ± 0.5
W	$9^{+0.3}_0$
W1	1.2

TAPING STATE

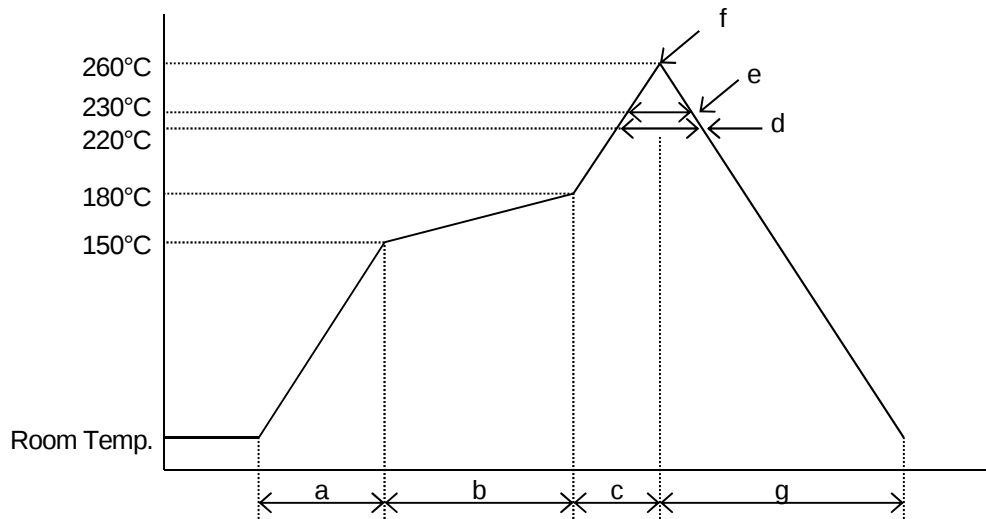


PACKING STATE



■RECOMMENDED MOUNTING METHOD

*Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4°C/s
- b: Pre-heating temperature : 150 to 180°C
- time : 60 to 120s
- c: Temperature ramp rate : 1 to 4°C/s
- d: 220°C or higher time : Shorter than 60s
- e: 230°C or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260°C
- g: Temperature ramping rate : 1 to 6°C/s

*The temperature indicates at the surface of mold package.

■REVISION HISTORY

Date	Revision	Changes
24.Apr.2018	Ver.0	First edition
06.Jun.2018	Ver.1	P.6, P.7 ■ TYPICAL TEST CIRCUIT : Replacement of TYPICAL CIRCUIT
		P.8 ■ TIMING CHART: Unification of terms. (Change to SYM from DUTY)
12.Feb.2019	Ver.2	P.11, P.12 ■ Application Note: In addition, Chose select crystal unit

[CAUTION]

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 - Equipment Used in the Deep Sea
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 - Various Safety Devices
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8. Warning for handling Gallium and Arsenic (GaAs) Products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.



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