

STEPPER MOTOR CONTROLLER / DRIVER

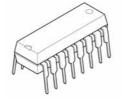
■ GENERAL DESCRIPTION

The NJM2671 is a two-phase unipolar stepping motor driver with a motor output of a maximum of 60 V and a maximum current of 500 mA.

The Step&Dir (Pulse Input) system of the motor controller enables simple switching between half and full step modes.

A high voltage of 60 v and wide power voltage supply range makes possible use with high-speed motor applications and the high voltage improves reliability.

■ PACKAGE OUTLINE







NJM2671E2 (SOP16-E2)

■ FEATURES

- Maximum motor power supply voltage: 60 V
- Continuous output current: 2 ch x 500 mA
- Internal driver and phase logic
- External phase logic reset terminal (RESET)
- Phase origin monitoring output terminal (MO)
- Thermal shutdown circuit
- Package DIP16, SOP16-E2 JEDEC 300mil

■ PIN CONFIGURATIONS

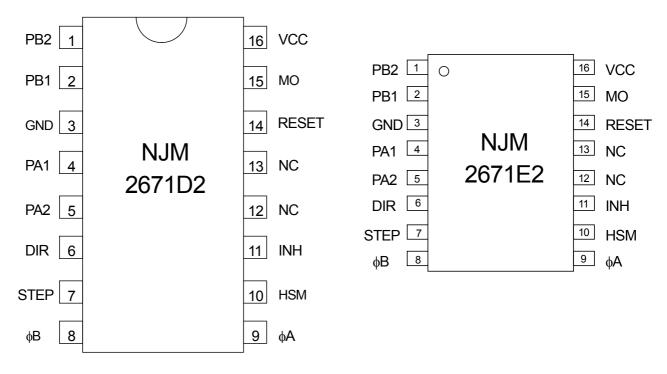


Fig.1 Pin Configurations

■ BLOCK DIAGRAM

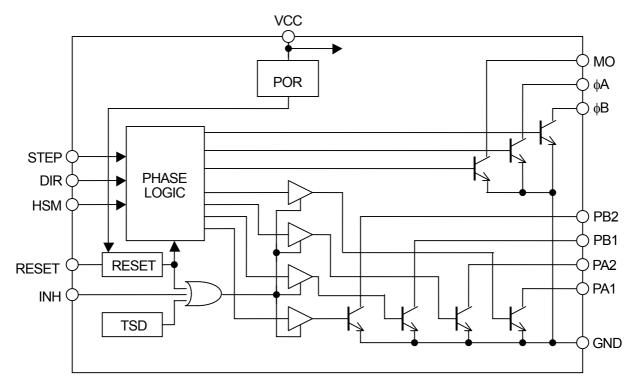


Fig.2 Block Diagram

■ PIN DESCRIPTION

Pin	Pin name	Description
1	PB2	B2 phase output with a maximum 500 mA sinking open collector output
2	PB1	B1 phase output with a maximum 500 mA sinking open collector output
3	GND	Vcc ground power supply terminal
4	PA1	A1 phase output with a maximum of 500 mA sinking open collector
5	PA2	A2 phase output with a maximum of 500 mA sinking open collector
6	DIR	Direction command input for determining motor turning direction
7	STEP	Motor stepping pulse input, phase logic operation triggered by negative
		edge of STEP signal
8	φВ	0 current sequence monitor output for B phase in half step mode
9	φА	0 current sequence monitor output for A phase in half step mode
10	HSM	Half/full step mode switching input
		H level in full step mode and L level in half step mode
11	INH	Phase output off input, all phase output is off at H level
12	NC	Not connected
13	NC	Not connected
14	RESET	Phase logic initial input
15	MO	Phase output initial status detection output
16	Vcc	Logic unit power supply voltage terminal

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	PIN No.	SYMBOL	MIN.	MAX.	UNIT	NOTE
Phase Output Voltage	1,2,4,5	V_{PCEO}	0	60	V	
Phase Output Current	1,2,4,5	I _P	0	500	mA	
Logic Supply Voltage	16	V _{CC}	0	7	V	
Logic Input Voltage Range	6,7,10,11,14	Vı	-0.3	6	V	
Logic Input Current	6,7,10,11,14	l _l	-10	1	mA	
Logic Output Current	8,9,15	Io	-	6	mA	
Junction TSOPerature Range		Tj	-40	+150	°C	
Operating TSOPerature		Topr	-40	85	°C	
Storage TSOPerature		Tstg	-50	150	°C	
DIP16 Package		P_{D}	-	1.6	W	
SOP16 Package		P_{D}	-	1.3	W	

■ RECOMMENDED OPERATING CONDITIONS

(Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Phase Output Voltage	V_{PCEO}	10	-	55	V	
Phase Output Current	l _P	0	-	350	mA	
Logic Supply voltage	Vcc	4.75	5	5.25	V	
Junction TSOPerature Range	Tj	-20	-	+125	°C	
Set-up Time	ts	400	-	-	ns	
Step Pulse Range	t _P	800	-	1	ns	
Reset Pulse Range	t _R	800	-	-	ns	

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General						
Supply Current	I _{CC} 1	INH=LOW	-	45	60	mA
Зирріу Сипені	I _{CC} 2	INH=HIGH	-	12	-	mA
Thermal Shutdown TSOPerature	TSD	-	-	170	-	°C
Phase Output						
Saturation Voltage	V _{PCE Sat}	lo=350mA	-	-	0.85	V
Leak Current	I _{PL}	-	-	-	500	μА
Turn-ON / Turn OFF Time	td	Vi=2.4V	-	-	3	μS
Logic Input						
H Level Input Voltage	V _{IH}	-	2.0	-	-	V
L Level Input Voltage	V _{IL}	-	-	-	0.8	V
H Level Input Current	I _{IH}	V _I =2.4V	-	-	-20	μΑ
L Level Input Current	I _{IL}	V _I =0.4V	-400	-	-	μΑ
Logic Output	•		•	•	•	
Saturation Voltage	V _{O Sat}	lo=1.6mA	-	-	0.6	V

■ TYPICAL APPLICATION

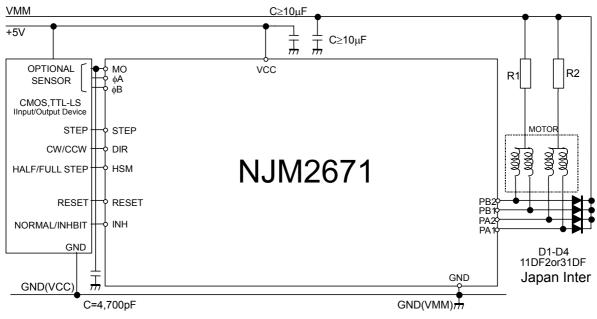


Fig.3

■ Function description

The NJM2671 is a high-performance low-voltage driver system for driving stepping motors with unipolar winding.

SOPloying a general-purpose STEP&DIR motion controller, it can easily control a stepping motor when combined with a pulse generator.

The phase output is as high as 60 V max. This prevents the phase output voltage margin of the motor from being exceeded, which is a common problem with unipolar winding systems and also simplifies the design of power control circuits during phase turn off.

■ Logic input

All inputs are LS-TT compatible. When the logic input is open, the circuit recognizes any open logic inputs as H level. The NJM2671 has built-in phase logic for optimum control of the stepping motor.

• STEP - Stepping pulse

The built-in phase logic sequencer goes UP on every negative edge of the STEP signal (pulse). In full step mode, the pulse turns the stepping motor at the basic step angle. In half step mode, two pulses are required to turn the motor at the basic step angle.

The DIR (direction) signal and HSM (half/full mode) are latched to the STEP negative edge and must therefore be established before the start of the negative edge. Note the setup time ts in Figure 4.

• DIR - direction

The DIR signal determines the step direction. The direction of the stepping motor depends on how the NJM2671 is connected to the motor. Although DIR can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge. See the timing chart in Figure 4.

HSM – half/full step mode switching

This signal determines whether the stepping motor turns at half step or full step mode. The built-in phase logic is set to the half step mode when HSM is low level. Although HSM can be modified this should be avoided since a misstep of 1 pulse increment may occur if it is set simultaneous with the negative edge. See

the timing chart in Figure 4.

• INH - phase output off

All phase output is turned off when INH goes high reducing power consumption (consumption current).

RESET

A two-phase stepping motor repeats the same winding energizing sequence every angle that is a multiple of four of the basic step. The phase logic sequence is repeated every four pulses in the full step mode and every eight pulses in the half step mode.

RESET forces to initialize the phase logic to sequence start mode.

When RESET is at L level, the phase logic is initialized and the phase output is turned off.

When RESET recovers to H level, the phase output resumes the energizing pattern output at sequence start of phase logic. Refer to Figure 5 for a reset timing chart.

■POR – power on and reset function

The internal power-on and reset circuit, which is connected to Vcc, resets the phase logic and turns off phase output when the power is supplied to prevent missteps.

Each time the power is turned on, the energizing pattern of phase logic at sequence start is output.

■ Phase output unit

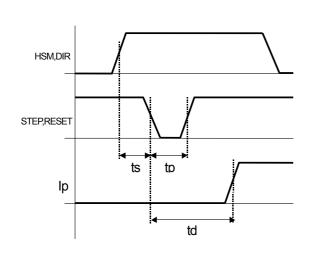
The phase output unit is composed of four open collector transistors that are directly connected to the stepping motor as shown in Figure 3.

■ ΦA, ΦB bi-polar phase logic output

This ΦA , ΦB output is a signal generated by the phase logic for external monitoring to determine whether the energizing sequence is 1-phase or 2-phase energizing. Missteps normally occur unless the switch from half step to full step mode is performed appropriately. Use of ΦA , ΦB output switches HSM in 2-phase energizing status ($\Phi A = \Phi B = L$ level) enables switching between the half and full step modes without missteps.

■ MO – origin monitor

At sequence start of the phase logic or after POR or external RESET, an L level output is made to indicate to external devices that the energizing sequence is in initial status.



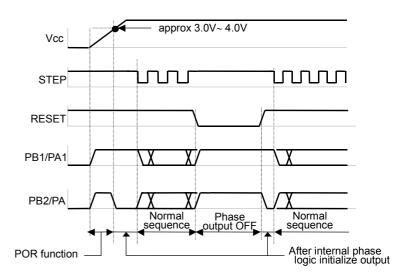


Fig.4 Timing chart

Fig.5 POR and external reset timing

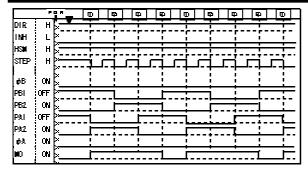


Fig. 6-1 Full step mode and CS sequence

STEP	POR	1	2	3	4
PB1	OFF	OFF	ON	ON	OFF
PB2	ON	ON	OFF	OFF	ON
PA1	OFF	ON	ON	OFF	OFF
PA2	ON	OFF	OFF	ON	ON

Fig. 6-2 Sequence table

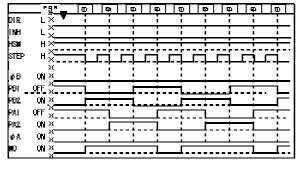


Fig. 7-1 Full step mode, C CW sequence

STEP	POR	1	2	3	4
PB1	OFF	ON	ON	OFF	OFF
PB2	ON	OFF	OFF	ON	ON
PA1	OFF	OFF	ON	ON	OFF
PA2	ON	ON	OFF	OFF	ON

Fig. 7-2 Sequence table

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DIR	Тн≿	7									_
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HSM	LX						i			i	
STEP	H ×−		ШП	Ш-	ЩП	_		_=		Щ	_
фΒ	ON X										
PBI	OFF XT										_
P62	ON X										
PAI	OFF XT										_
P92	ON X										_
φA	ON X								ı		_
MO	ON X										

Fig. 8-1 Half step mode and CW sequence

STEP	POR	1	2	3	4	5	6	7	8
PB1	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
PB2	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
PA1	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
PA2	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON

Fig. 8-2 Sequence table

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INH		× ×—			;							
HSW		\widetilde{x}	i	i	i	i	i	i	i	i	i	
STEP		×== ×		ΙĹ	П		шi	шİ	Дĺ	ഥ	Дĺ	
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φВ	ON					_ ;				:		
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P#12	ON	×	Ī	<u>-</u>		:						
φà		×	!			Ħ						
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Fig. 9-1 Half step mode, C CW sequence

STEP	POR	1	2	3	4	5	6	7	8
PB1	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
PB2	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
PA1	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
PA2	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	ON

Fig. 9-2 Sequence table

		₹."	O 5	5 G	i [4	3 E	9 5	9 [8	D 8) (0)	П
DIR] н	.									
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HSM	L	R	i :							i	
STEP	Н	Ş 	L		口口		Ш	Ц.	П	Щ	
øΒ	ON	}	1 1			į					
PBI	OFF	Š 									=
P62	OFF										_
PAI	OFF	5 .									_
P#2	OFF	R	.								=
φà	ON	<u> </u>							!		
MO	ON	<u> </u>	J								_

Fig. 10 Half step mode, INH sequence

■ Application examples

• Logic input unit

The circuit handles an open state in the logic input unit as an H level input. Unused input units should be fixed at Vdd level to maximize noise resistance characteristics.

Phase output unit

The phase output unit is provided with a power sink to enable unipolar drive of stepping motor windings. The resistor connected to the common line of the winding determines the maximum motor power.

To protect output transistors from kickback power, a high-speed free wheeling diode is required. A example solution is shown in Figures 11 to 14.

ΦA, ΦB bi-polar phase logic output

ΦA, ΦB are open collector outputs that go high when the phase output in the half step mode is set to current output off. A pull-up resistor is required to ensure appropriate power supply voltage. (5 k ohm recommended for Vcc 5 V logic).

■ I/O signal sequence in each drive mode

Timing charts for I/O signals in each drive mode are shown in Figures 6 to 10. The left side shows input and output signals after POR.

■ Precautions

- 1. Do not remove ICs or PCBs when power is supplied.
- 2. Note that some stepping motors may generate excessive voltages even when free wheeling diode is used.
- 3. Select a stepping motor with the required power rating to obtain the required torque.
 - Generally, the higher the input voltage of the stepping motor, the higher rpm it will produce. When the supply voltage is higher than stepping motor rated voltage, a current limit resistor must be used to connect the common winding to the power supply. Use the L/R time constant of the resistor to obtain optimum high-speed rpm characteristics from the stepping motor.
- 4. Do not use motor power supplies (without an output capacitor) with a serial diode. Nor use ground lines with common impedance with Vcc, instead make a one point ground connection using the ground terminal (pin 3) of the IC.
- 5. To reverse motor rotation, reverse PA and PA2 (or PB1 and PB2) stepping motor connections.
- 6. Drive circuit

High-performance stepping motor operation requires that the windings are energized speedily at phase turn on, and that energizing is quickly turned off at turn off.

7. Phase turnoff problems

The drive circuit may be damaged if the kickback voltage induced when the energizing of the windings is turned off (when winding current is turned off) is not adequately suppressed. Refer to the turn-off circuit described in Figures 11 to 14.

8. Using an MO output

Hazard may occur at the MO output terminal in half step mode. Check the output waveform and connect a 1,000 pF or higher ceramic capacitor between the MO terminal (pin 15) and the GND terminal (pin 3).

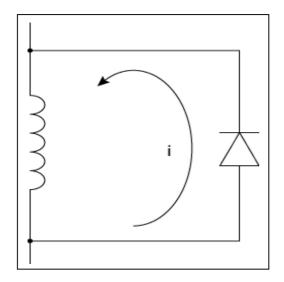


Fig. 11 Diode and turn off circuit

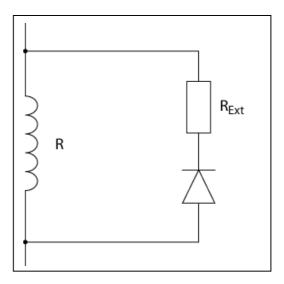


Fig. 12 Resistor and turn off circuit

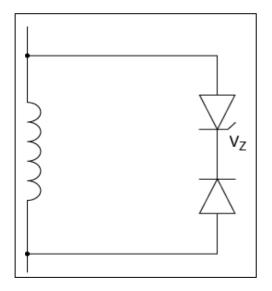


Fig. 13 Zener diode and turn off circuit

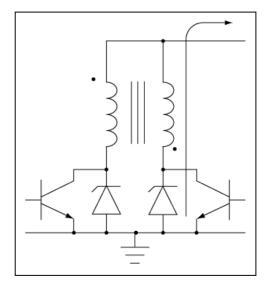


Fig. 14 Power regeneration and turn off circuit

■ ELECTRICAL CHARACTERISTICS EXAMPLES

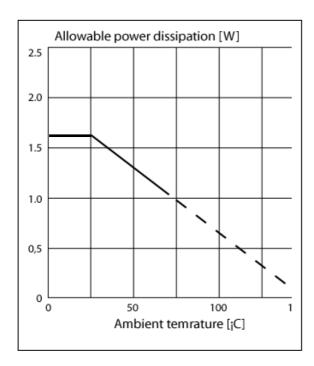


Fig. 15 Ambient tSOPerature vs. allowable power dissipation characteristics example

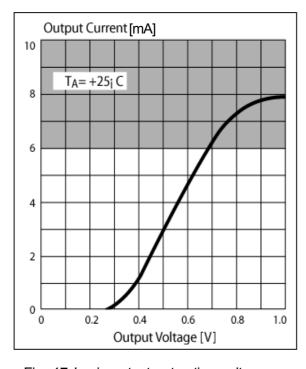


Fig. 17 Logic output saturation voltage vs. output current characteristics example

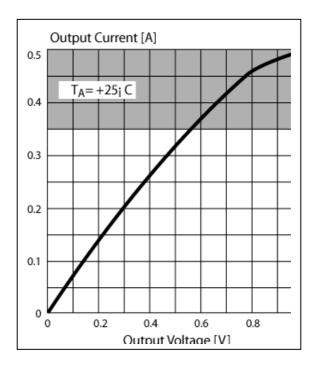


Fig. 16 Phase output saturation voltage vs. output current characteristics example

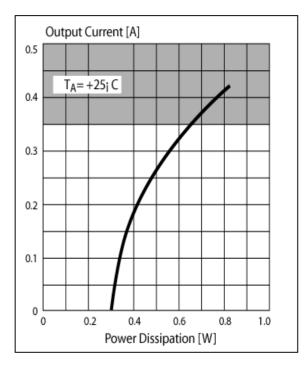


Fig. 18 Allowable dissipation vs. phase output current characteristics (@ full step)

MEMO

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