

Ultra low current consumption SPDT switch

■FEATURES

- Low control voltage 1.6 V min.
- Low current consumption 0.1 µA typ.
- Low insertion loss 0.45 dB typ. @f = 920 MHz
- High isolation

■APPLICATION

switching applications

BLOCK DIAGRAM (DFN6-75)

- 30 dB typ. @f = 920 MHz +30 dBm typ. @f = 920 MHz
- P-0.1dB 1.0 mm x 1.0 mm, t = 0.375 mm
- Small package

LPWA (SIGFOX, LoRaWAN, Wi-SUN) applications

Antenna switching, path switching, general purpose

RoHS compliant and Halogen Free, MSL1

■GENERAL DESCRIPTION

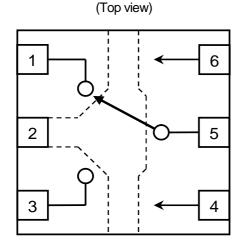
The NJG1816K75 is a 2 bit control SPDT switch GaAs MMIC suited for LPWA applications.

The NJG1816K75 operates at low control voltage from 1.6 V. The NJG1816K75 is the best choice for IoT devices with battery operation because of ultra low current consumption.

The small and thin DFN6-75 package is adopted.

■PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION
1	P1	RF terminal
2	NC(GND)	Ground terminal
3	P2	RF terminal
4	VCTL2	Control signal input terminal
5	PC	RF terminal
6	VCTL1	Control signal input terminal



■FUNCTIONAL DESCRIPTION

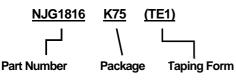
"H" = VCTL(H), "L" = VCTL(L)

ON Path	VCTL1	VCTL2
PC-P1	L	н
PC-P2	Н	L

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■ PRODUCT NAME INFORMATION



ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN- FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1816K75	DFN6-75	Yes	Yes	Ni/Pd/Au	5	1.2	5,000

■ ABSOLUTE MAXIMUM RATINGS

$T_a = 25^{\circ}C, Z_s = Z_l =$				
PARAMETER	SYMBOL	RATINGS	UNIT	
RF input power ⁽¹⁾	P _{IN}	+30	dBm	
Control voltage	V _{CTL}	4.5	V	
Power dissipation ⁽²⁾	PD	380	mW	
Operating temperature	T _{opr}	-40 to +105	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

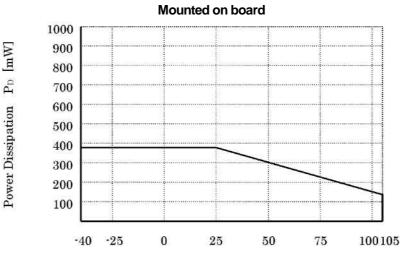
(1): $V_{CTL}(L) = 0 V$, $V_{CTL}(H) = 1.8 V$, on state port

(2): Mounted on four-layer FR4 PCB with through-hole (76.2 \times 114.3 mm), T_i = 150 °C

■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation [PD], a special attention should be paid in designing of thermal radiation.)



Power Dissipation – Ambient Temperature Characteristic

Ambient Temperature Ta [°C]

■ ELECTRICAL CHARACTERISTICS (DC CHARACTERISTICS)

VCTL(H) = 1.8 V, VCTL(L) = 0 V, Ta = 25°C, Zs = ZI = 50 Ω , with application circuit						
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Control voltage (HIGH)	Vcī⊾(H)	VCTL1, VCTL2 terminal	1.6	1.8	4.0	V
Control voltage (LOW)	V _{CTL} (L)	VCTL1, VCTL2 terminal	-0.2	-	0.2	V
Control current	ICTL		-	0.1	2.0	μA

■ ELECTRICAL CHARACTERISTICS (RF CHARACTERISTICS)

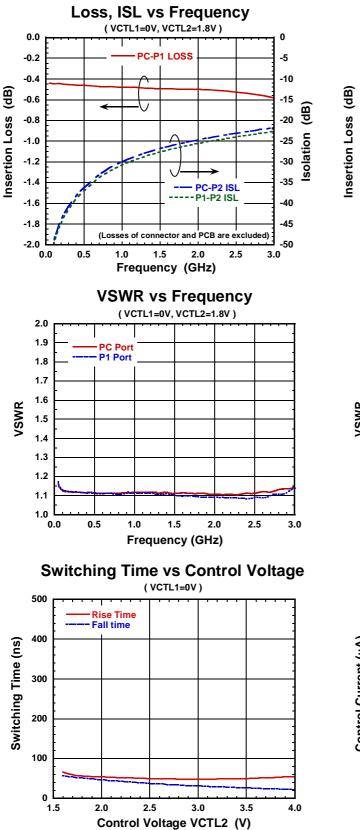
VCTL(H) = 1.8 V, VCTL(L) = 0 V, Ta = 25°C, Zs = ZI = 50 Ω , with application circuit

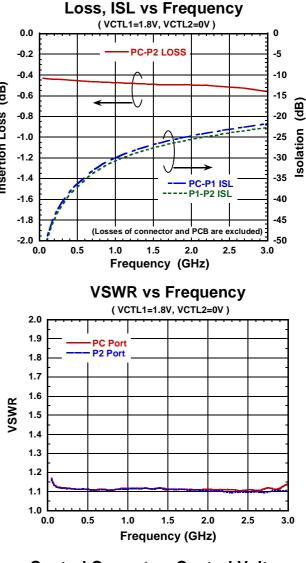
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion loss	LOSS	f = 920 MHz	-	0.45	0.65	dB
Isolation	ISL	f = 920 MHz	26	30	-	dB
Input power at 0.1 dB compression point	P-0.1dB	f = 920 MHz	+25	+30	-	dBm
VSWR	VSWR	f = 920 MHz	-	1.1	1.4	-
Switching time	Tsw	50% Vcт∟ to 10%/90% RF	-	100	300	ns

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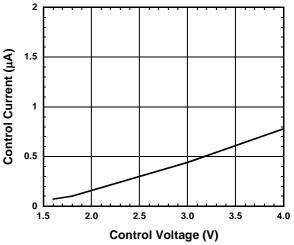


ELECTRICAL CHARACTERISTICS





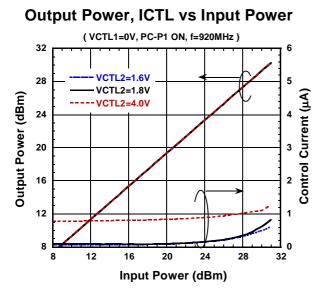
Control Current vs Control Voltage



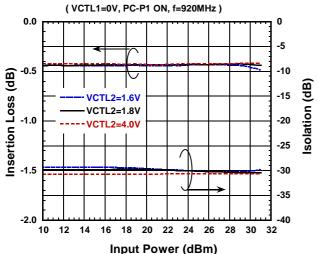
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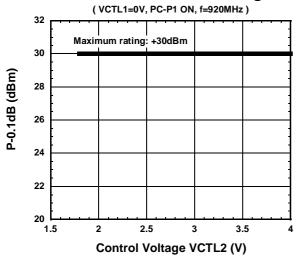
■ ELECTRICAL CHARACTERISTICS



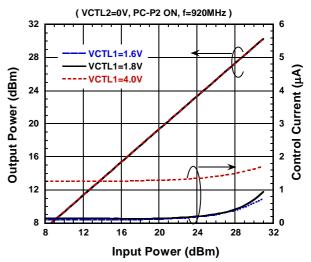
Insertion Loss, Isolation vs Input Power



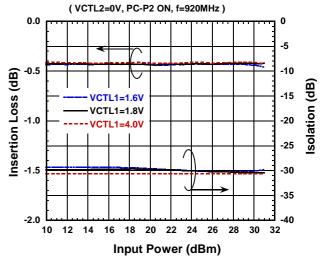
P-0.1dB vs Control Voltage



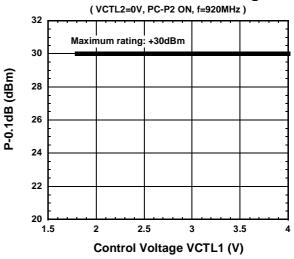
Output Power, ICTL vs Input Power



Insertion Loss, Isolation vs Input Power



P-0.1dB vs Control Voltage



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75

100

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100

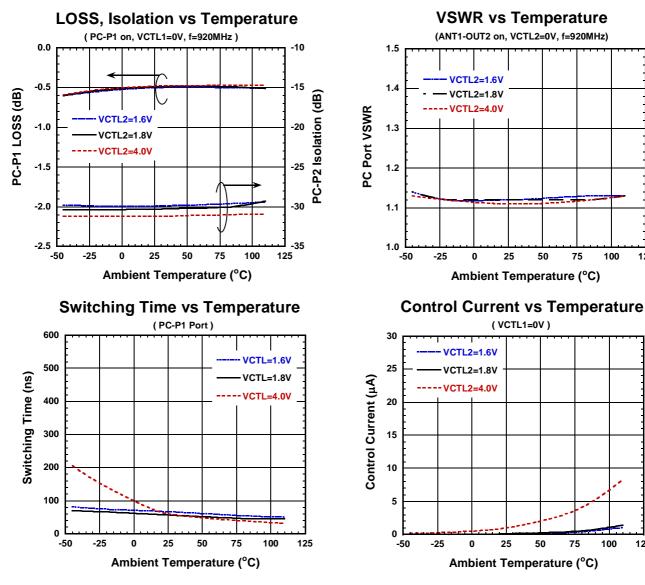
125

75

125



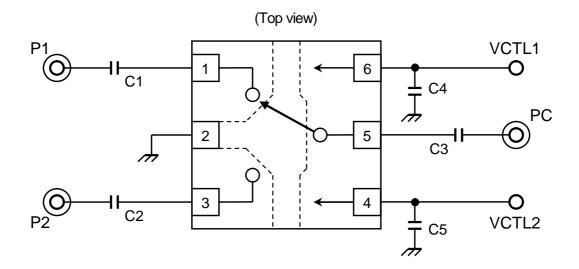
■ ELECTRICAL CHARACTERISTICS



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■ APPLICATION CIRCUIT



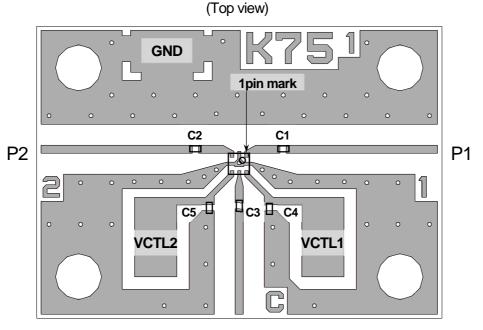
■ PARTS LIST

Part ID	Value	Notes
C1 to C3	1000 pF	MURATA (GRM03)
C4 to C5	10 pF	MURATA (GRM03)

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■ EVALUATION BOARD



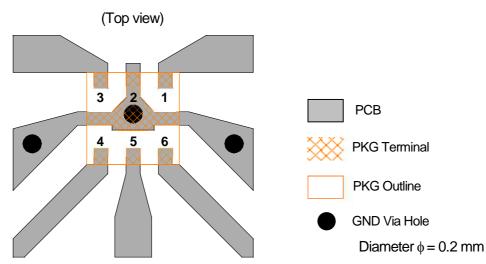


Losses of PCB and connectors, $Ta = +25^{\circ}C$

Frequency (MHz)	Loss (dB)
920	0.22

PCB: FR-4
t = 0.2 mm
MICROSTRIP LINE WIDTH: 0.4 mm (Zo = 50 Ω)
PCB SIZE: 19.4 x 14.0 mm

■ PCB LAYOUT GUIDELINE



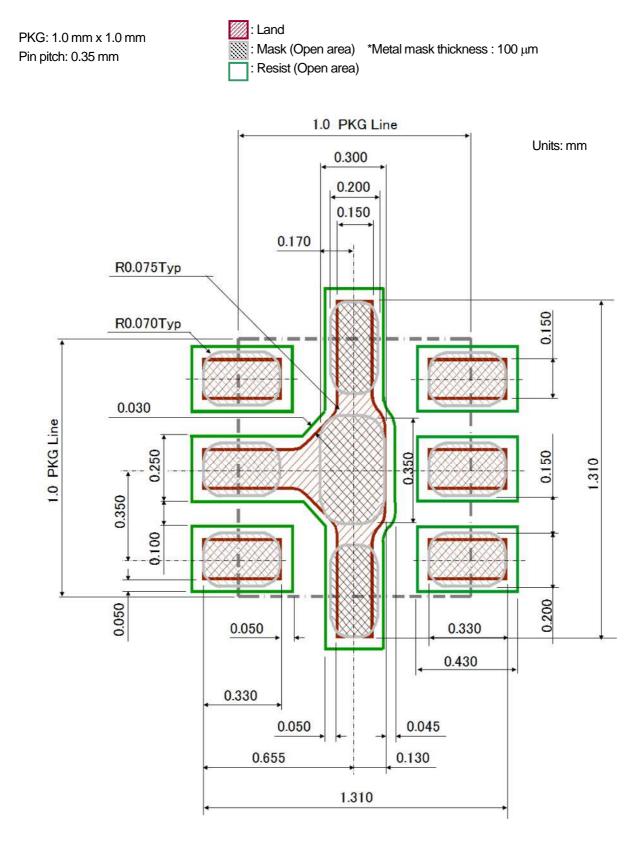
■ PRECAUTIONS

- [1] The DC blocking capacitors (C1, C2, C3) should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
- [2] For avoiding the degradation of RF performance, the bypass capacitors (C4, C5) should be placed as close as possible to VCTL terminals.
- [3] For good RF performance, exposed pad should be connected to PCB ground plane of substrate, and through –holes should be placed near the IC.

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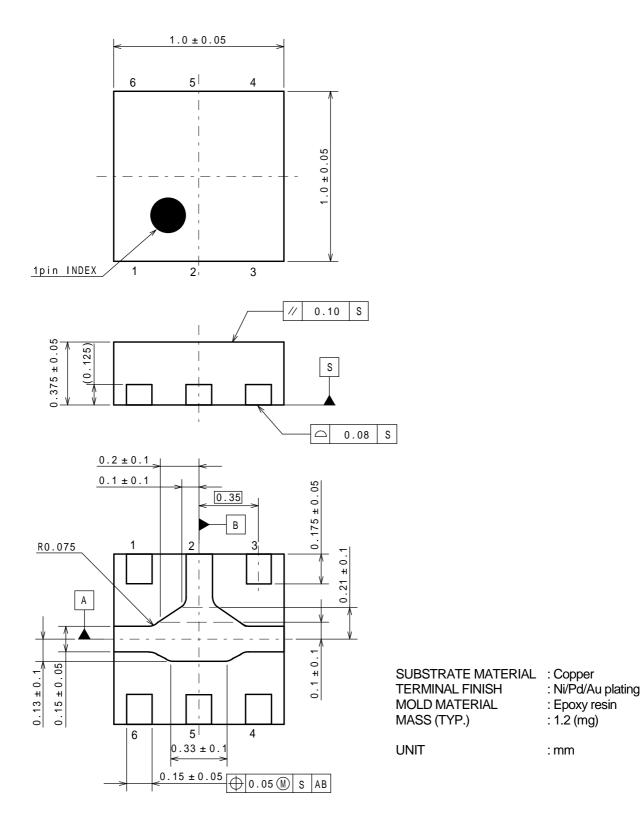
■ RECOMMENDED FOOTPRINT PATTERN (DFN6-75)



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■ PACKAGE OUTLINE (DFN6-75)

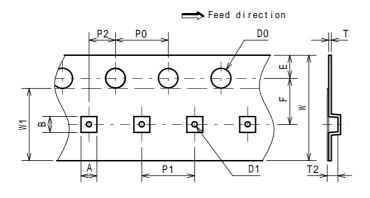


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Units: mm

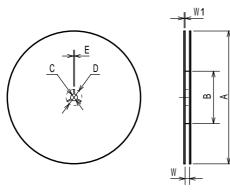
■ PACKING SPECIFICATION (DFN6-75)

TAPING DIMENSIONS



SYMBOL	DIMENSION	REMARKS
А	1.19 ^{+0.04} -0.01	BOTTOM DIMENSION
В	1.19 ^{+0.04}	BOTTOM DIMENSION
DO	1.5 ^{+0.1}	
D1	0.5 ± 0.05	
E	1.75 ± 0.1	
F	3.5 ± 0.05	
P0	4.0 ± 0.1	
P1	4.0 ± 0.1	
P2	2.0 ± 0.05	
Т	0.18 ± 0.05	
T2	0.69 ± 0.1	
W	8.0±0.1	
W1	5.5 ± 0.1	THICKNESS 60 µ max

REEL DIMENSIONS

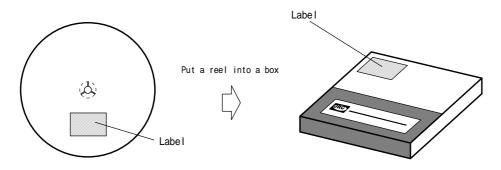


SYMBOL	DIMENSION
Α	180 _3
В	60 ⁺¹
С	13±0.2
D	21 ± 0.8
E	2±0.5
W	9±0.3
W1	1.2

TAPING STATE

Insert dire	ection Se	aling with covering tape	>	
(TE1)				
	👞 🔰 Empty tape	Devices	Empty tape	Covering tape
Feed dire	ection 150 to 200mm	5000pcs/reel	150 to 200mm	600 to 800mm

PACKING STATE



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[CAUTION]

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