

Low Noise Amplifier with Bypass for LTE

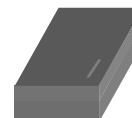
■ GENERAL DESCRIPTION

NJG1169UX2 is low noise amplifier with bypass switch for LTE which covers frequency from 728 to 960MHz.

The NJG1169UX2 has a LNA pass-through function to select LNA active mode or bypass mode, and this IC achieves high gain, low noise figure and high linearity. Integrated ESD protection device on each port achieves excellent ESD robustness.

A very small and ultra-thin package of EPFP6-X2 is adopted.

■ PACKAGE OUTLINE



NJG1169UX2

■ APPLICATIONS

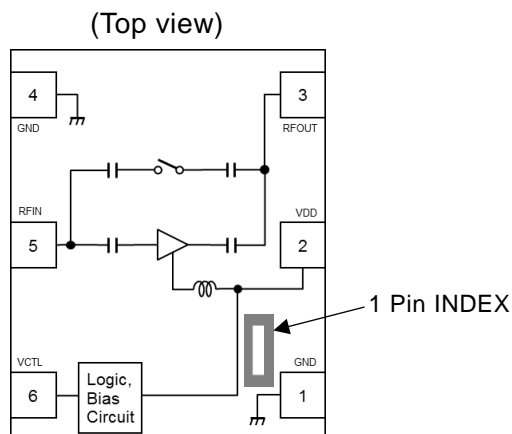
LTE receive application

RF front-end modules, smartphones, data cards and others mobile application

■ FEATURES

- Operating frequencies 728 to 960MHz
- Operating voltage 1.5 to 3.3V
- Low current consumption 4.8/4.0mA typ. @ $V_{DD}=2.8/1.8V$
- High Gain 12.5dB typ. @ $V_{DD}=2.8V$, $f=880MHz$
- Low Noise figure 0.8dB typ. @ $V_{DD}=2.8V$, $f=880MHz$
- High IIP3 0dBm typ. @ $V_{DD}=2.8V$, $f=880MHz$
- Insertion loss in bypass mode 2.5dB typ. @ $V_{DD}=2.8V$, $f=880MHz$
- Ultra Small package size EPFP6-X2 (Package size: 1.1mm x 0.7mm x 0.37mm typ.)
- RoHS compliant and Halogen Free
- MSL1

■ PIN CONFIGURATION



Pin Connection

1. GND
2. VDD
3. RFOUT
4. GND
5. RFIN
6. VCTL

■ TRUTH TABLE

"H"= $V_{CTL}(H)$ "L"= $V_{CTL}(L)$

V_{CTL}	Mode
L	Bypass mode
H	LNA active mode

Note: Specifications and description listed in this datasheet are subject to change without notice

■ ABSOLUTE MAXIMUM RATINGS

General condition: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply voltage	V_{DD}		5.0	V
Control voltage	V_{CTL}		5.0	V
Input power	P_{in}	$V_{DD}=2.8\text{V}$	+15	dBm
Power dissipation	P_D	4-layer FR4 PCB with through-hole (101.5x114.5mm), $T_j=150^{\circ}\text{C}$	430	mW
Operating temperature	T_{opr}		-40 to +105	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS 1 (DC)

General condition: $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\Omega$

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		1.5	-	3.3	V
Control voltage (High)	$V_{CTL(H)}$		1.3	1.8	3.3	V
Control voltage (Low)	$V_{CTL(L)}$		0	0	0.3	V
Operating current 1	I_{DD1}	RF OFF, $V_{DD}=2.8\text{V}$ $V_{CTL}=1.8\text{V}$	-	4.8	8.0	mA
Operating current 2	I_{DD2}	RF OFF, $V_{DD}=1.8\text{V}$ $V_{CTL}=1.8\text{V}$	-	4.0	7.5	mA
Operating current 3	I_{DD3}	RF OFF, $V_{DD}=2.8\text{V}$, $V_{CTL}=0\text{V}$	-	15	60	μA
Operating current 4	I_{DD4}	RF OFF, $V_{DD}=1.8\text{V}$, $V_{CTL}=0\text{V}$	-	10	60	μA
Control current	I_{CTL}	RF OFF, $V_{CTL}=1.8\text{V}$	-	7	20	μA

■ ELECTRICAL CHARACTERISTICS 2 (LNA active mode)

General Condition: $V_{DD}=2.8V$, $V_{CTL}=1.8V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 1	Gain1	Exclude PCB & connector losses(0.13dB)	10.0	12.5	15.0	dB
Noise figure 1	NF1	Exclude PCB & connector losses(0.06dB)	-	0.8	1.2	dB
Input power at 1dB gain compression point 1(1)	P-1dB (IN)1(1)		-10.0	+1.0	-	dBm
Input 3rd order intercept point 1(1)	IIP3_1(1)	$f1=f_{RF}$, $f2=f_{RF}+1MHz$, $P_{IN}=-24dBm$	-6.0	0	-	dBm
Gain settling time1(1)	Ts1(1)	Bypass to LNA active mode To be within 1dB of the final gain	-	2.0	5.0	μs
Gain settling time1(2)	Ts1(2)	LNA active to Bypass mode To be within 1dB of the final Insertion loss	-	1.0	4.0	μs
RF IN Return loss1(1)	RLi1(1)		6.0	11.0	-	dB
RF OUT Return loss1(1)	RLo1(1)		6.0	11.0	-	dB

■ ELECTRICAL CHARACTERISTICS 3 (Bypass mode)

General Condition: $V_{DD}=2.8V$, $V_{CTL}=0V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss1	Loss1	Exclude PCB & connector losses(0.13dB)	-	2.5	4.0	dB
Input power at 1dB gain compression point 1(2)	P-1dB (IN)1(2)		0	+10.0	-	dBm
Input 3rd order intercept point 1(2)	IIP3_1(2)	$f1=f_{RF}$, $f2=f_{RF}+1MHz$, $P_{IN}=-5dBm$	0	+15.0	-	dBm
RF IN Return loss1(2)	RLi1(2)		6.0	10.0	-	dB
RF OUT Return loss1(2)	RLo1(2)		4.0	6.5	-	dB

■ ELECTRICAL CHARACTERISTICS 4 (LNA active mode)

General Condition: $V_{DD}=1.8V$, $V_{CTL}=1.8V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small signal gain 2	Gain2	Exclude PCB & connector losses(0.13dB)	-	12.0	-	dB
Noise figure 2	NF2	Exclude PCB & connector losses(0.06dB)	-	0.8	-	dB
Input power at 1dB gain compression point 2(1)	P-1dB (IN)2(1)		-	-2.0	-	dBm
Input 3rd order intercept point 2(1)	IIP3_2(1)	$f1=f_{RF}$, $f2=f_{RF}+1MHz$, $P_{IN}=-24dBm$	-	-0.5	-	dBm
Gain settling time2(1)	Ts2(1)	Bypass to LNA active mode To be within 1dB of the final gain	-	2.0	-	μs
Gain settling time2(2)	Ts2(2)	LNA active to Bypass mode To be within 1dB of the final Insertion loss	-	1.0	-	μs
RF IN Return loss2(1)	RLi2(1)		-	10.0	-	dB
RF OUT Return loss2(1)	RLo2(1)		-	10.0	-	dB

■ ELECTRICAL CHARACTERISTICS 5 (Bypass mode)

General Condition: $V_{DD}=1.8V$, $V_{CTL}=0V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit

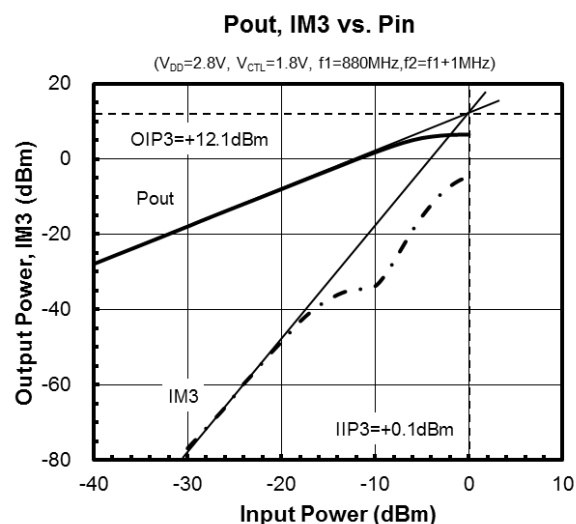
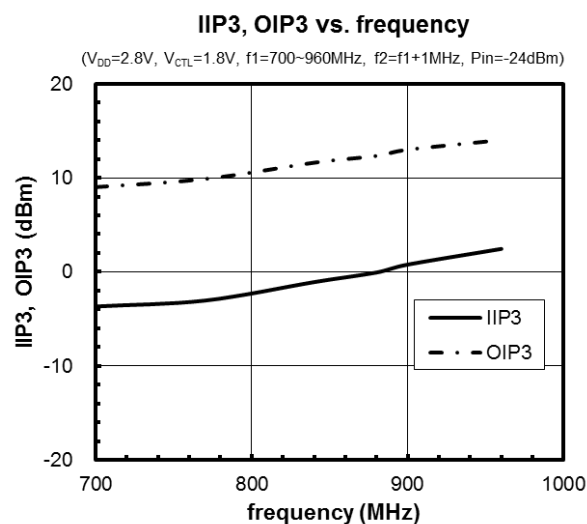
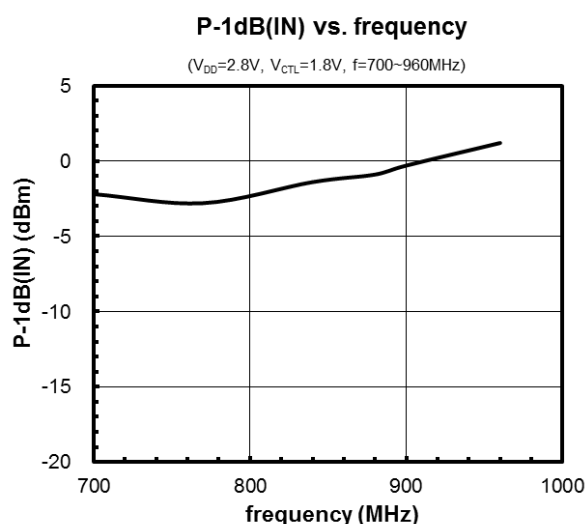
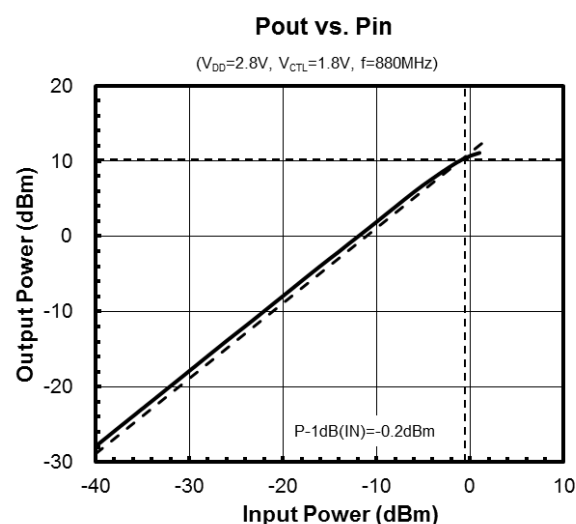
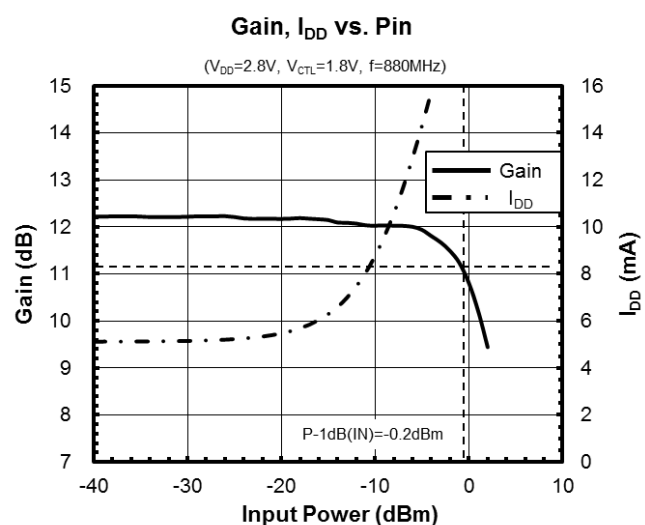
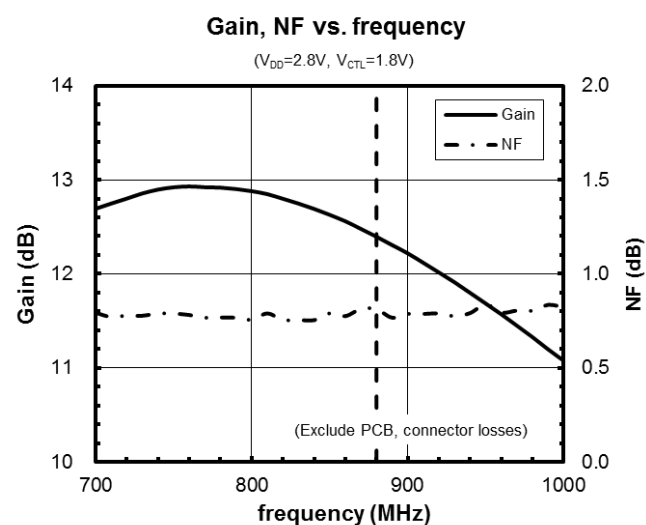
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss2	Loss2	Exclude PCB & connector losses(0.13dB)	-	2.5	-	dB
Input power at 1dB gain compression point 2(2)	P-1dB (IN) 2(2)		-	+10.0	-	dBm
Input 3rd order intercept point 2(2)	IIP3_2(2)	$f1=f_{RF}$, $f2=f_{RF}+1MHz$, $P_{IN}=-5dBm$	-	+15.0	-	dBm
RF IN Return loss 2(2)	RLi2(2)		-	9.0	-	dB
RF OUT Return loss 2(2)	RLo2(2)		-	6.0	-	dB

■ TERMINAL INFORMATION

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. This terminal should be connected to the ground plane as close as possible for excellent RF performance.
2	VDD	Supply voltage terminal. Please connect bypass capacitor C1 with ground as close as possible.
3	RFOUT	RF output terminal. This terminal requires no DC blocking capacitor since this IC has internal output matching circuit including DC blocking capacitor.
4	GND	Ground terminal. This terminal should be connected to the ground plane as close as possible for excellent RF performance.
5	RFIN	RF input terminal. This terminal requires only a matching inductor L1, and does not require DC blocking capacitor.
6	VCTL	Control voltage terminal.

■ ELECTRICAL CHARACTERISTICS (LNA active mode)

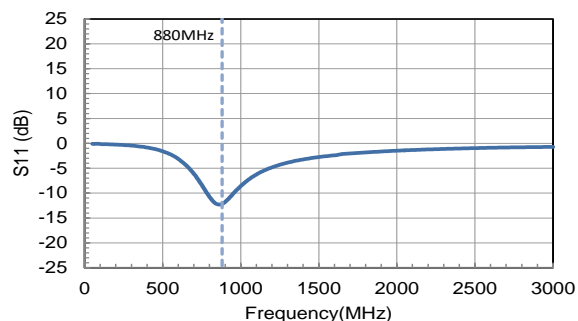
Conditions: $V_{DD}=2.8V$, $V_{CTL}=1.8V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit



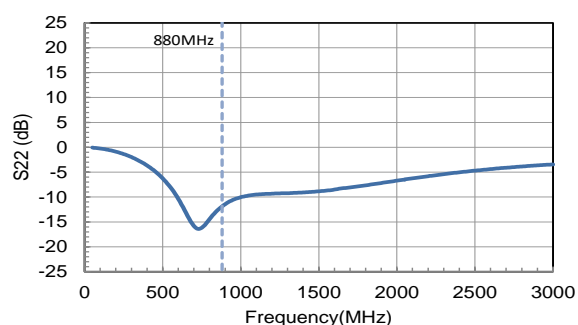
■ ELECTRICAL CHARACTERISTICS (LNA active mode)

Conditions:

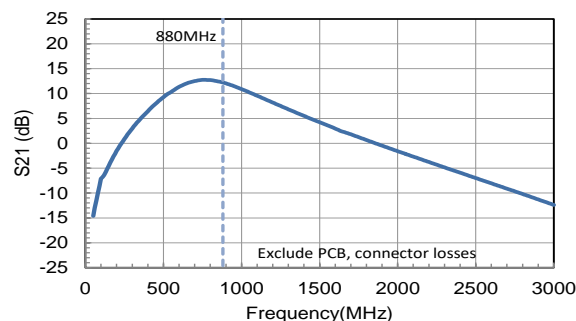
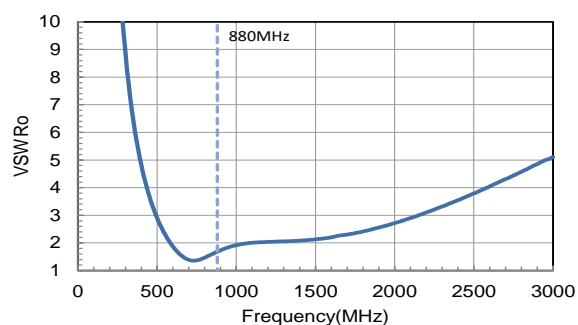
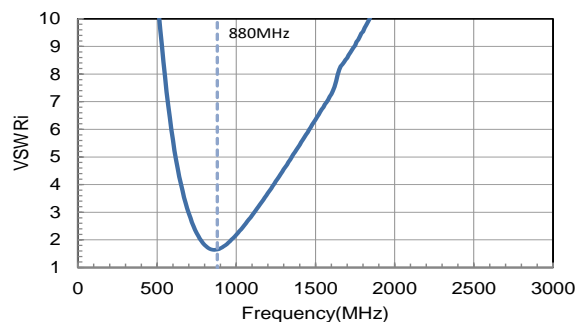
$V_{DD}=2.8V$, $V_{CTL}=1.8V$, $f_{RF}=50$ to $3000MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit



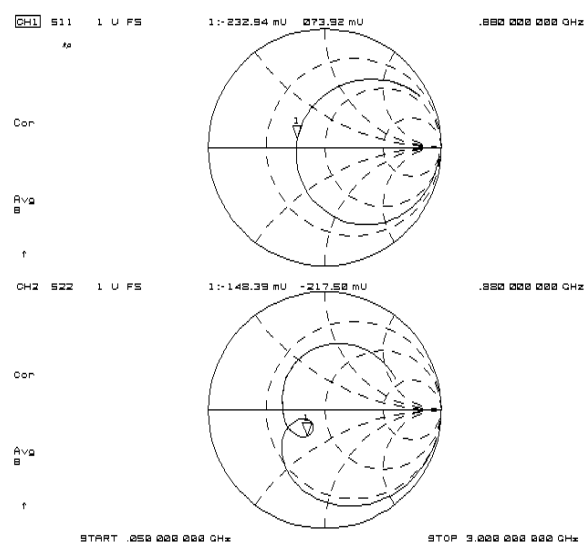
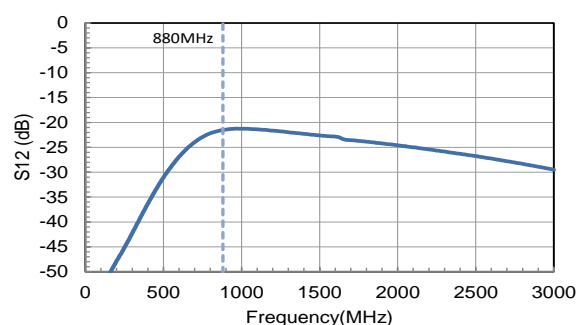
S11, S22



VSWRi, VSWRo



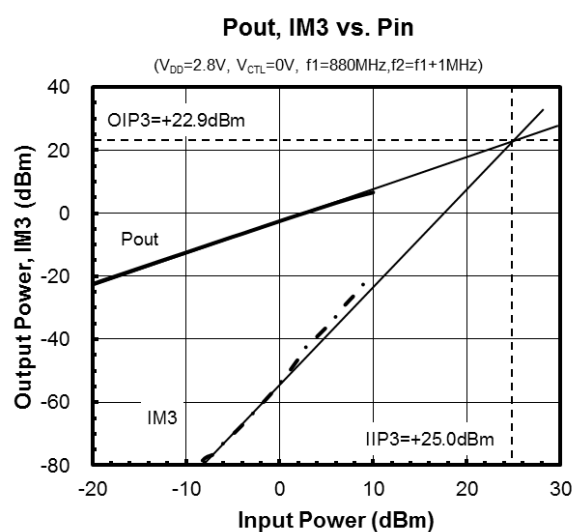
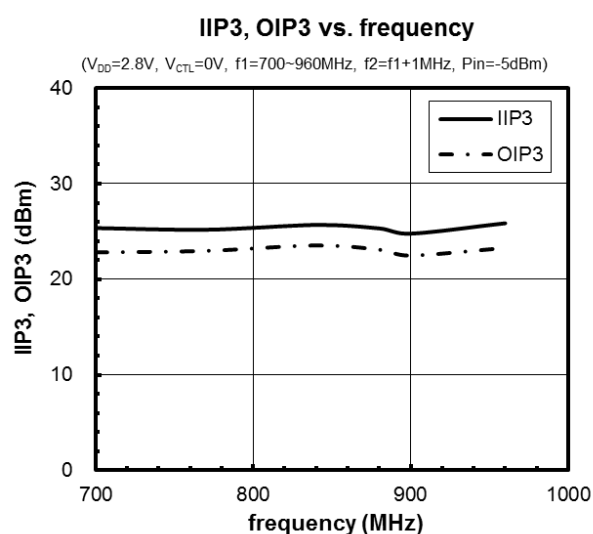
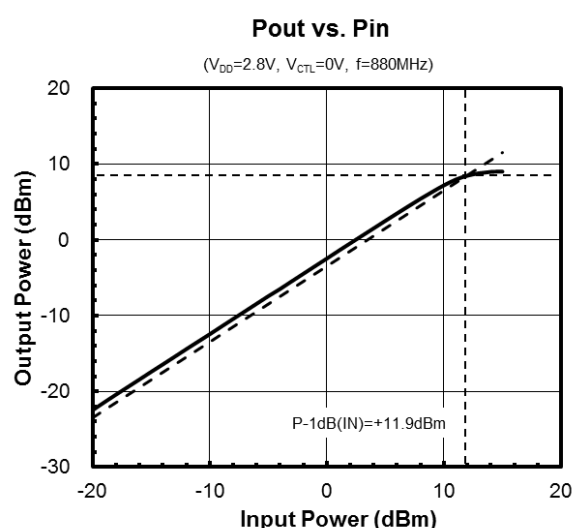
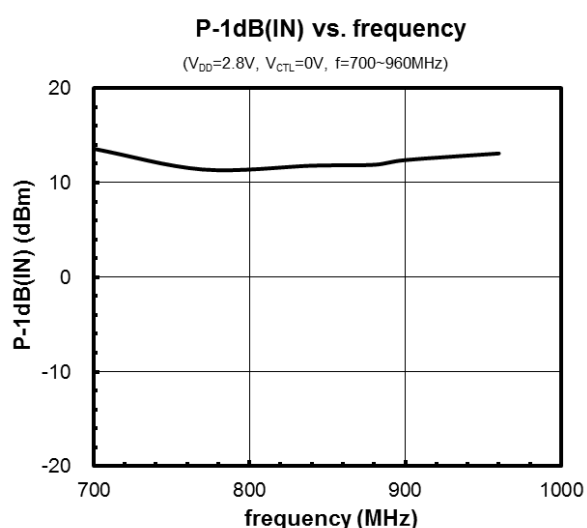
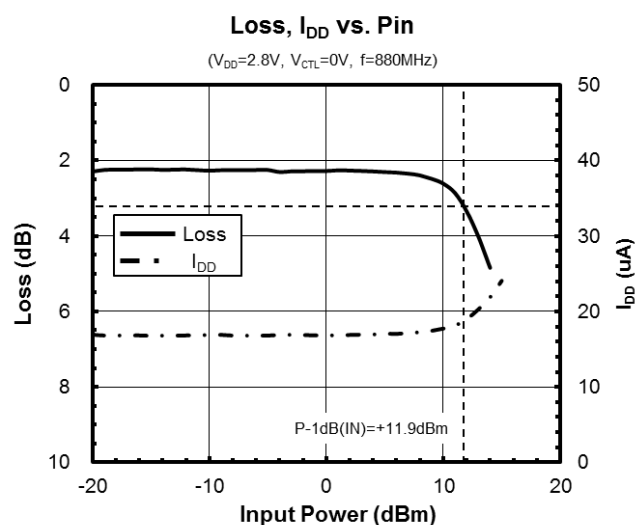
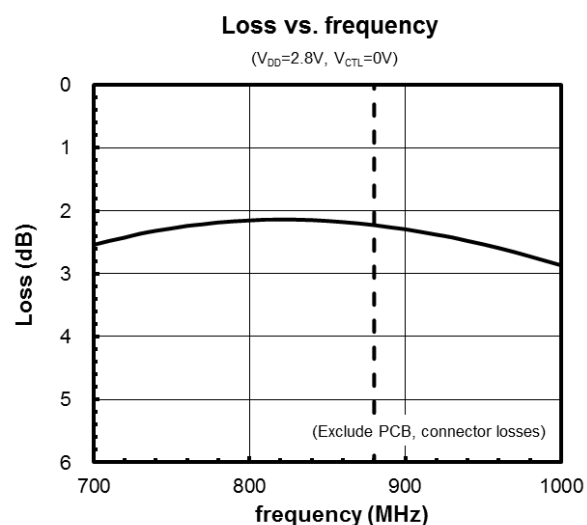
S21, S12



Zin, Zout

■ ELECTRICAL CHARACTERISTICS (Bypass mode)

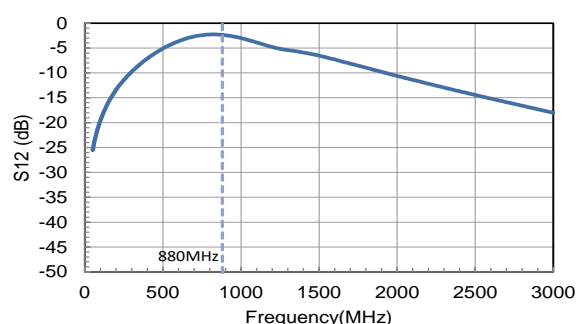
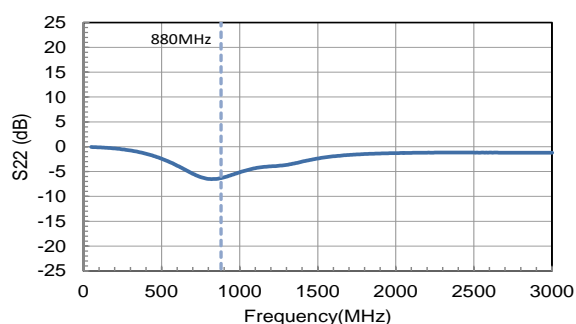
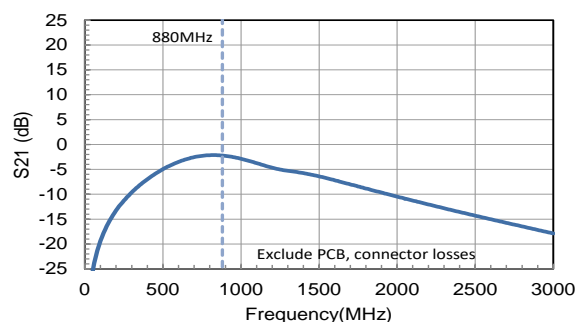
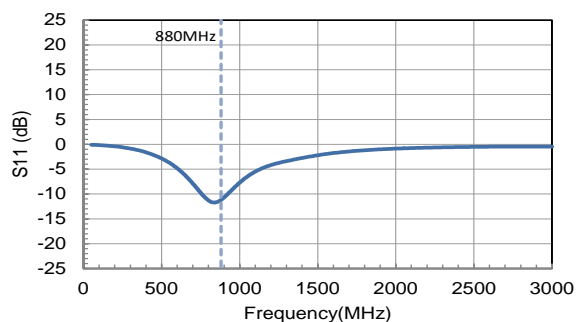
Conditions: $V_{DD}=2.8V$, $V_{CTL}=0V$, $f_{RF}=880MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_L=50\Omega$, with application circuit



■ ELECTRICAL CHARACTERISTICS (Bypass mode)

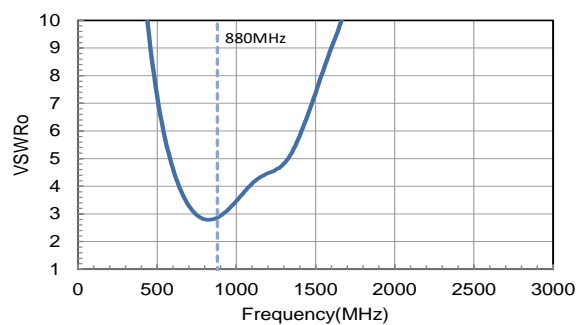
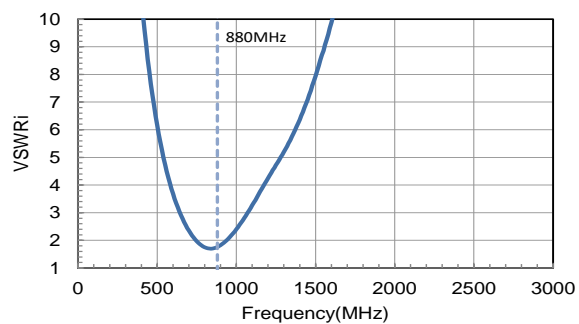
Conditions:

$V_{DD}=2.8V$, $V_{CTL}=0V$, $f_{RF}=50$ to $3000MHz$, $T_a=+25^{\circ}C$, $Z_s=Z_l=50\Omega$, with application circuit

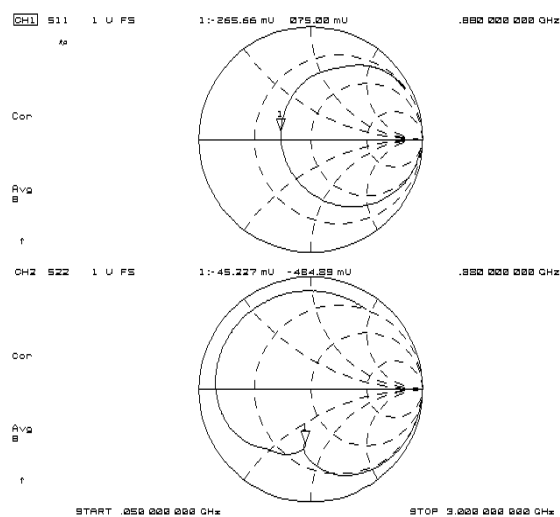


S11, S22

S21, S12



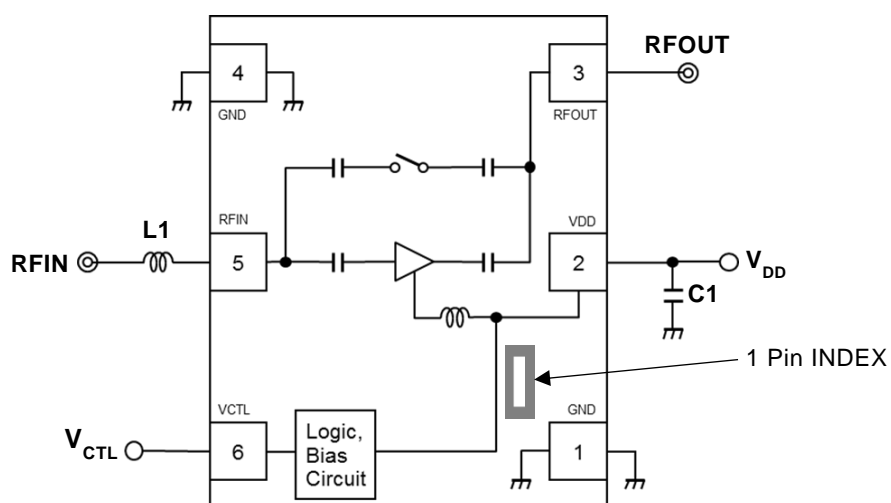
VSWRi, VSWRo



Zin, Zout

APPLICATION CIRCUIT

(Top View)



PARTS LIST

Parts ID	Value	Manufacture
L1	16nH	LQW15AN_00 Series (MURATA)
C1	1000pF	GRM03 Series (MURATA)

■ MEASUREMENT BLOCK DIAGRAM

Measuring instruments

NF Analyzer : Keysight N8975A
Noise Source : Keysight 346A

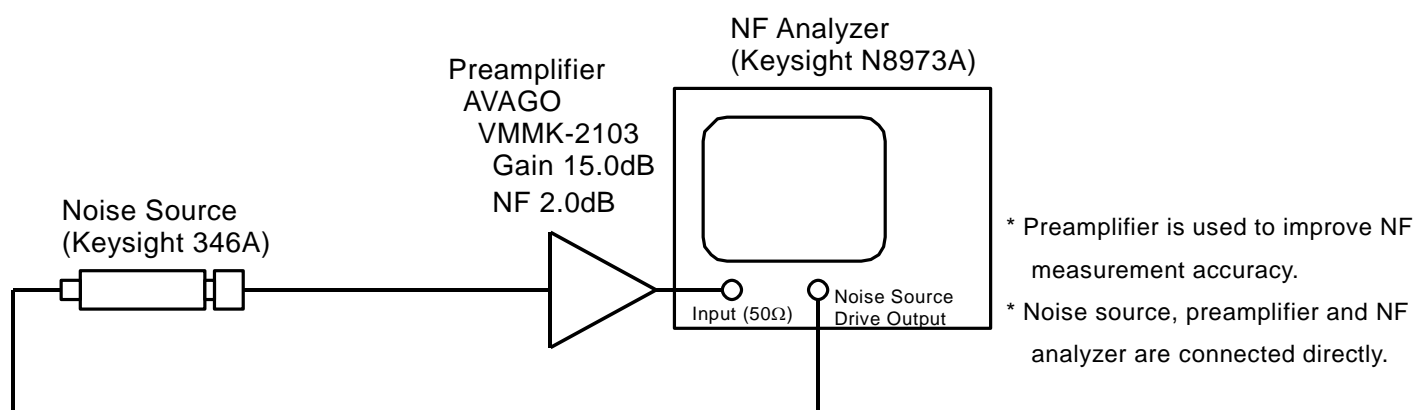
Setting the NF analyzer

Measurement mode form

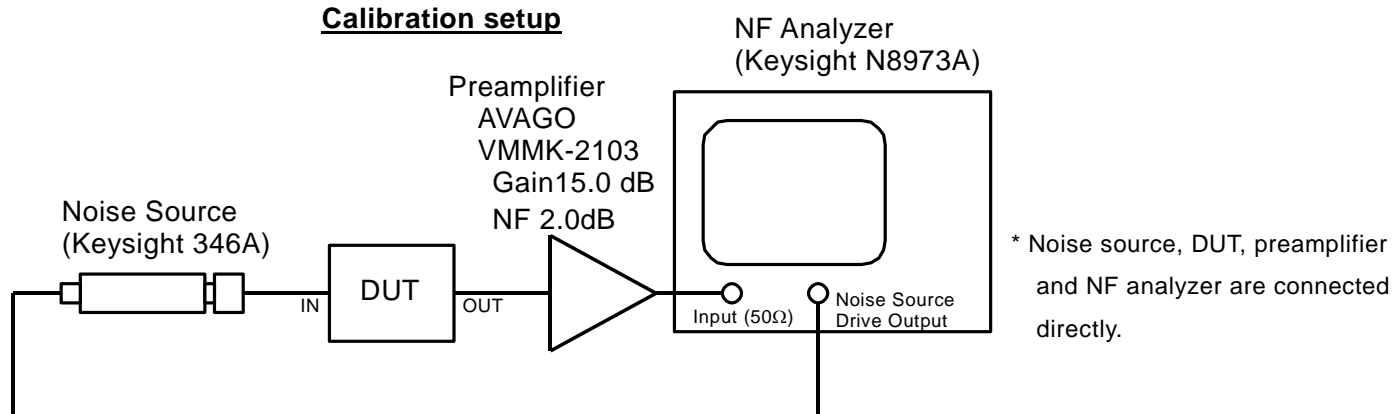
Device under test : Amplifier
System downconverter : off

Mode setup form

Sideband : LSB
Averages : 8
Average mode : Point
Bandwidth : 4MHz
Loss comp : off
Tcold : setting the temperature of noise source (305.15K)

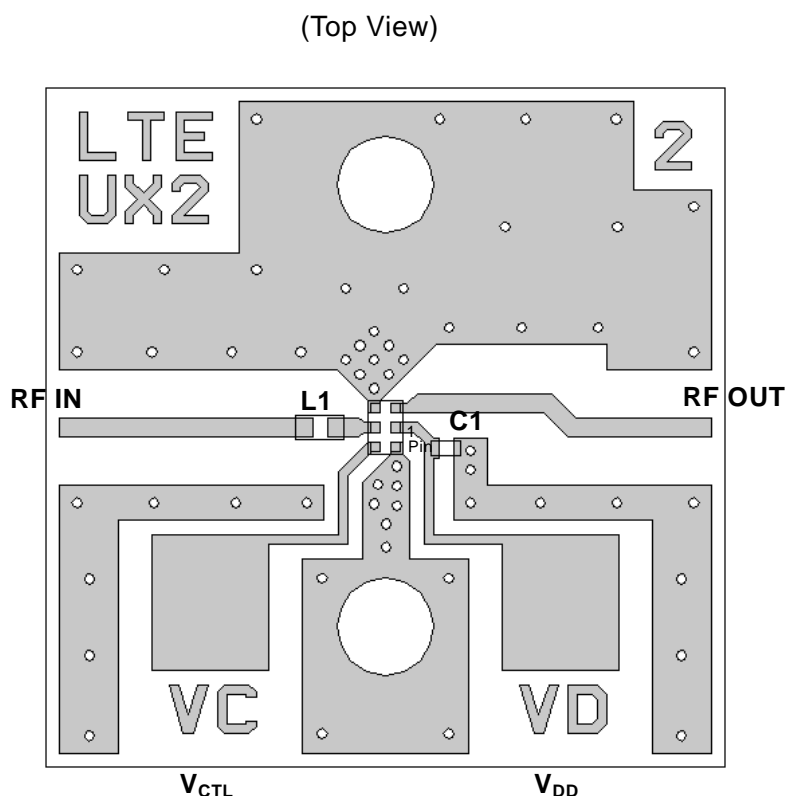


Calibration setup



Measurement Setup

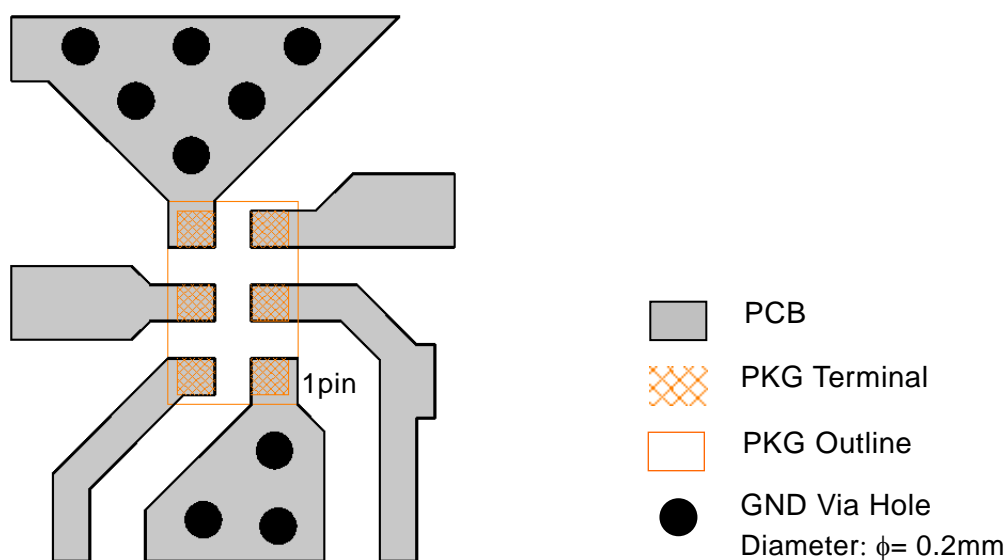
■ EVALUATION BOARD



PCB Information

Substrate:	FR-4
Thickness:	0.2mm
Microstrip line width:	0.4mm ($Z_0=50\Omega$)
Size:	14.0mm x 14.0mm

■ PCB LAYOUT GUIDELINE






PRECAUTIONS

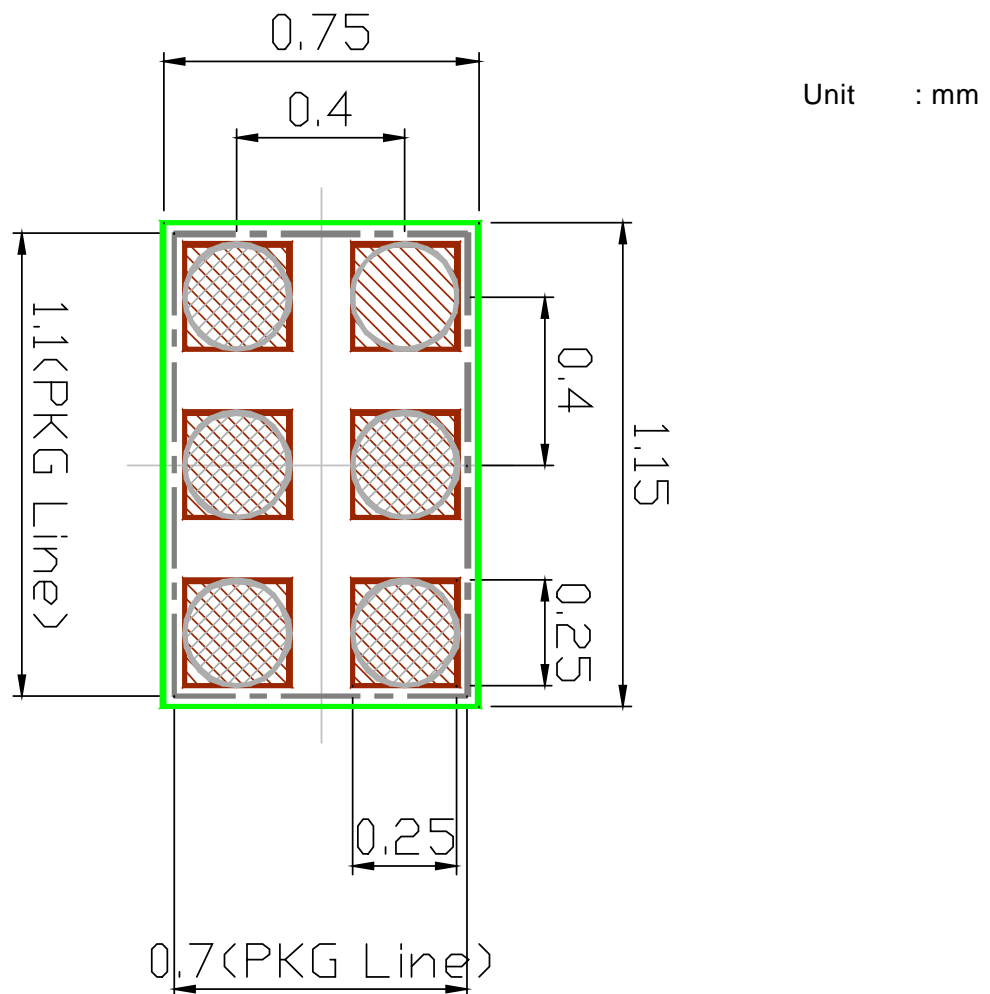
- All external parts should be placed as close as possible to the IC.
- For good RF performance, all GND terminals must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.

RECOMMENDED FOOTPRINT PATTERN (EPFFP6-X2 PACKAGE)

PKG: 1.1mm x 0.7mm

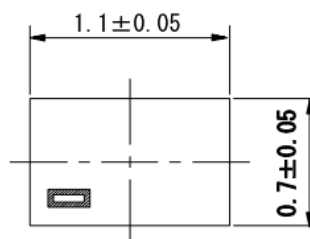
Pin pitch: 0.4mm

-  : Land
-  : Mask (Open area) *Metal mask thickness: 100μm
-  : Resist (Open area)

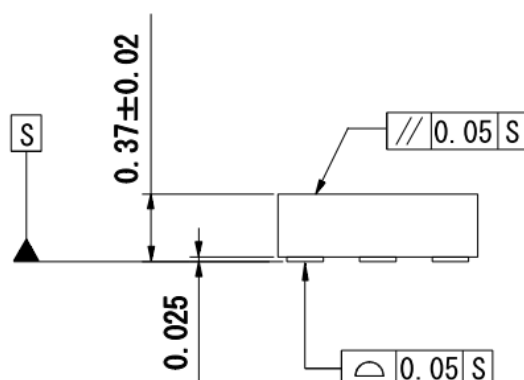


■ PACKAGE OUTLINE (EPFFP6-X2)

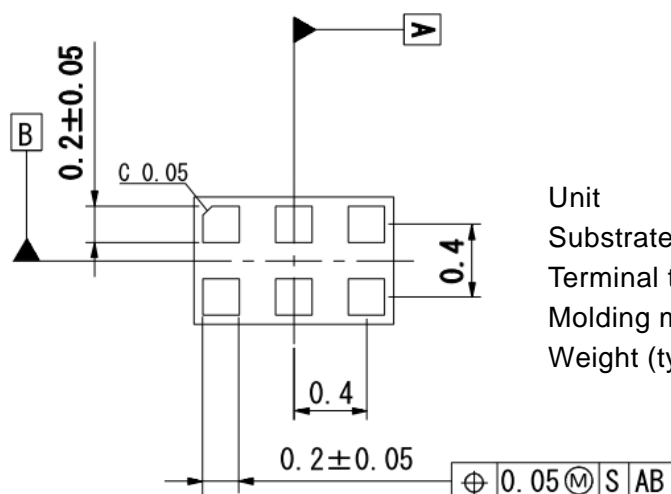
TOP VIEW



SIDE VIEW



BOTTOM VIEW



Unit	: mm
Substrate	: FR4
Terminal treat	: Ni/Pd/Au
Molding material	: Epoxy resin
Weight (typ.)	: 0.7mg

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NJR:](#)

[NJG1169UX2-TE1](#)