CEL California Eastern Laboratories

Evaluation Board Document

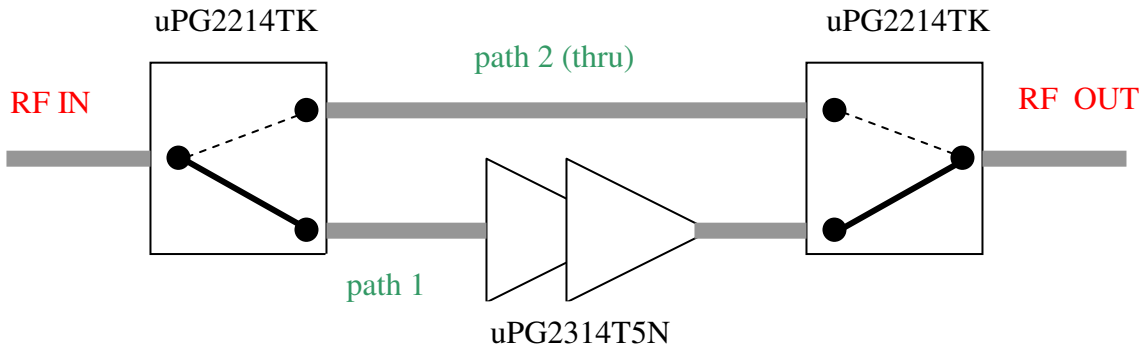
µPG2314T5N-ZBT-EV-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- Circuit Schematic and Assembly Drawing
- Appendix: Evaluation Board Document of the uPG2314T5N-EVAL-A

Circuit Description:

This evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2314T5N power amplifier and RF switch uPG2214TK for a "range extension" application at 2.4GHz ISM band (such as for Bluetooth or ZigBee applications). The circuit provides two paths for a transmit signal of a Bluetooth or Zigbee RF transceiver: either through the amplifier or direct pass through two switches. The functional diagram of this board is shown below:



The two paths are selected by the logic levels at the two control pin-connectors, Vcont1 and Vcont2, (refer to the schematic for the connector designation) according to the following truth table:

Vcont1	**Vcont2**	**Path 1 (PA)**	**Path 2 (Thru)**
3.0 V	0 V	ON	OFF
0 V	3.0 V	OFF	ON

The matching and bias circuits for the uPG2314T5N are the same as those used in the CEL's evaluation circuit board, uPG2314T5N-EVAL-A. For more information on the PA circuit design, refer to the Evaluation Board Document of uPG2314T5N-EVAL-A in the appendix.

The PCB is FR4 four layer board. The top and bottom dielectric layers are 8mils thick. The total board thickness is 62mils. The dielectric constant of FR4 is 4.3.

Typical Performance Data

Path 1:

Test conditions:

F=2.45GHz, Vcc=Ven=3V

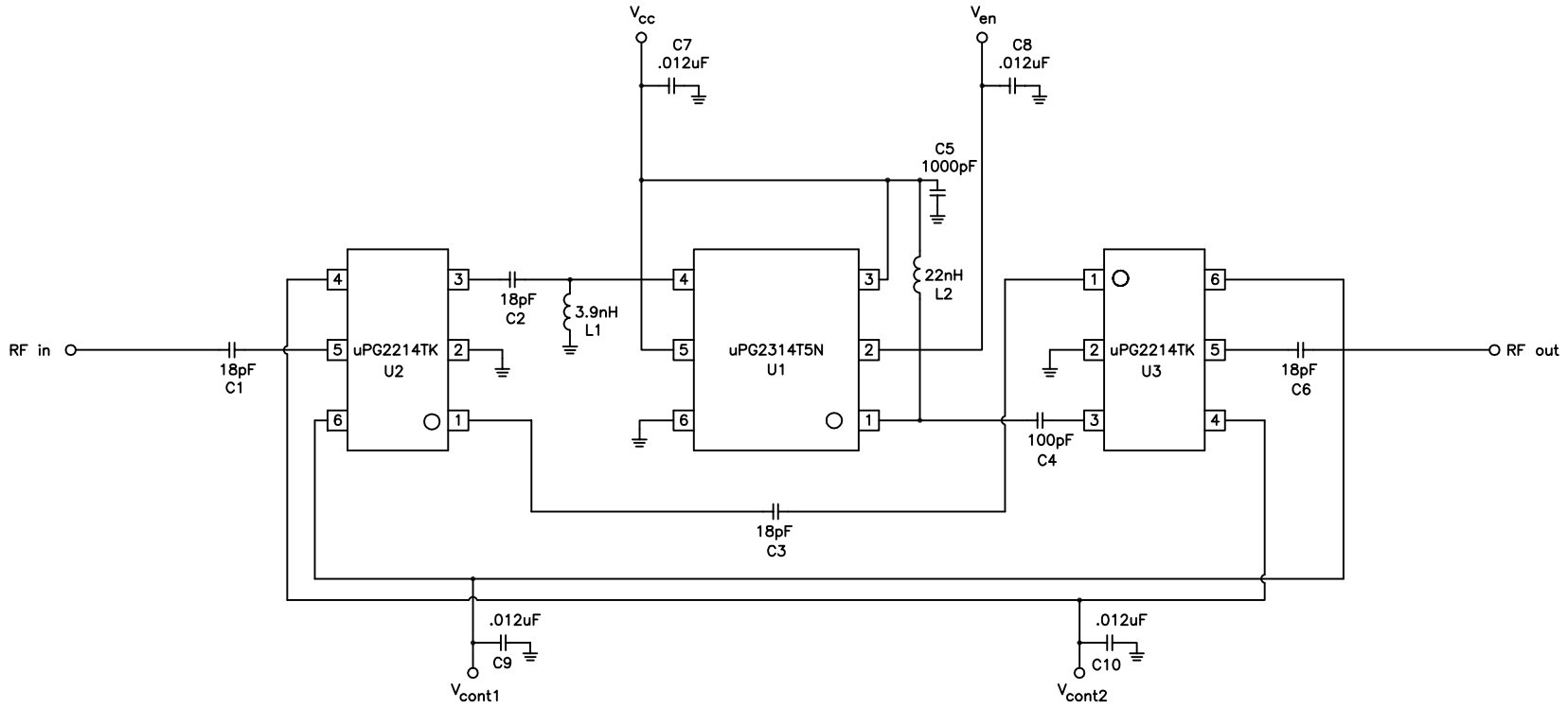
The output power Pout, supply current Ic and gain as a function of input power Pin are shown in the following table.

Pin (dBm)	Pout (dBm)	Gain (dB)	Ic (mA)
-20	1.7	21.7	23
-19	2.7	21.7	24
-18	3.7	21.7	24
-17	4.6	21.6	24
-16	5.6	21.6	25
-15	6.5	21.5	25
-14	7.5	21.5	26
-13	8.4	21.4	27
-12	9.3	21.3	28
-11	10.2	21.2	29
-10	11.1	21.1	31
-9	12.0	21.0	33
-8	12.9	20.9	35
-7	13.8	20.8	37
-6	14.7	20.7	40
-5	15.6	20.6	44
-4	16.5	20.5	47
-3	17.2	20.2	51
-2	17.9	19.9	56
-1	18.5	19.5	60
0	18.9	18.9	63
1	19.3	18.3	67
2	19.5	17.5	69
3	19.6	16.6	71
4	19.7	15.7	72

Path 2:

The insertion loss of the “thru” path is 1.2dB.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	LQP03TN22NJ00	L2	0201 22nH IND +/-5% MURATA	11
1	LQP0603T3N9C	L1	0201 3.9nH IND +/-0.3nH MURATA	10
4	GRM0335C1E180JD01	C1,C2,C3,C6	0201 18pF CAP +/-5% MURATA	9
1	GRM033R71C101KD01	C4	0201 100pF CAP +/-5% MURATA	8
2	GRM033R71C102KD01	C5	0201 1000pF CAP +/-5% MURATA	7
4	X7R0603HTTD123K	C7,C8,C9,C10	0603 .012uF CAP KOA	6
5	2340-6111 TG	P1,P2,P3,P4,P5	PIN HEADER 3M	5
2	142-0711-821	J1,J2	SMA FEMALE CONNECTOR E.F.JOHNSON	4
1	uPG2314T5N	U1	NEC GaAs Pwr Amplifier uPG2314T5N	3
2	uPG2214TK	U2,U3	NEC GaAs SPDT Switch uPG2214TK	2
1	CL-101893	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING

MATERIAL

FINISH

APPROVALS		
Drawing by:	Hugues de Saint Salvy	2006/01/23
Designed by:	Hugues de Saint Salvy	2006/01/06
Checked by:		
Project Engineer:		
Quality Control:		

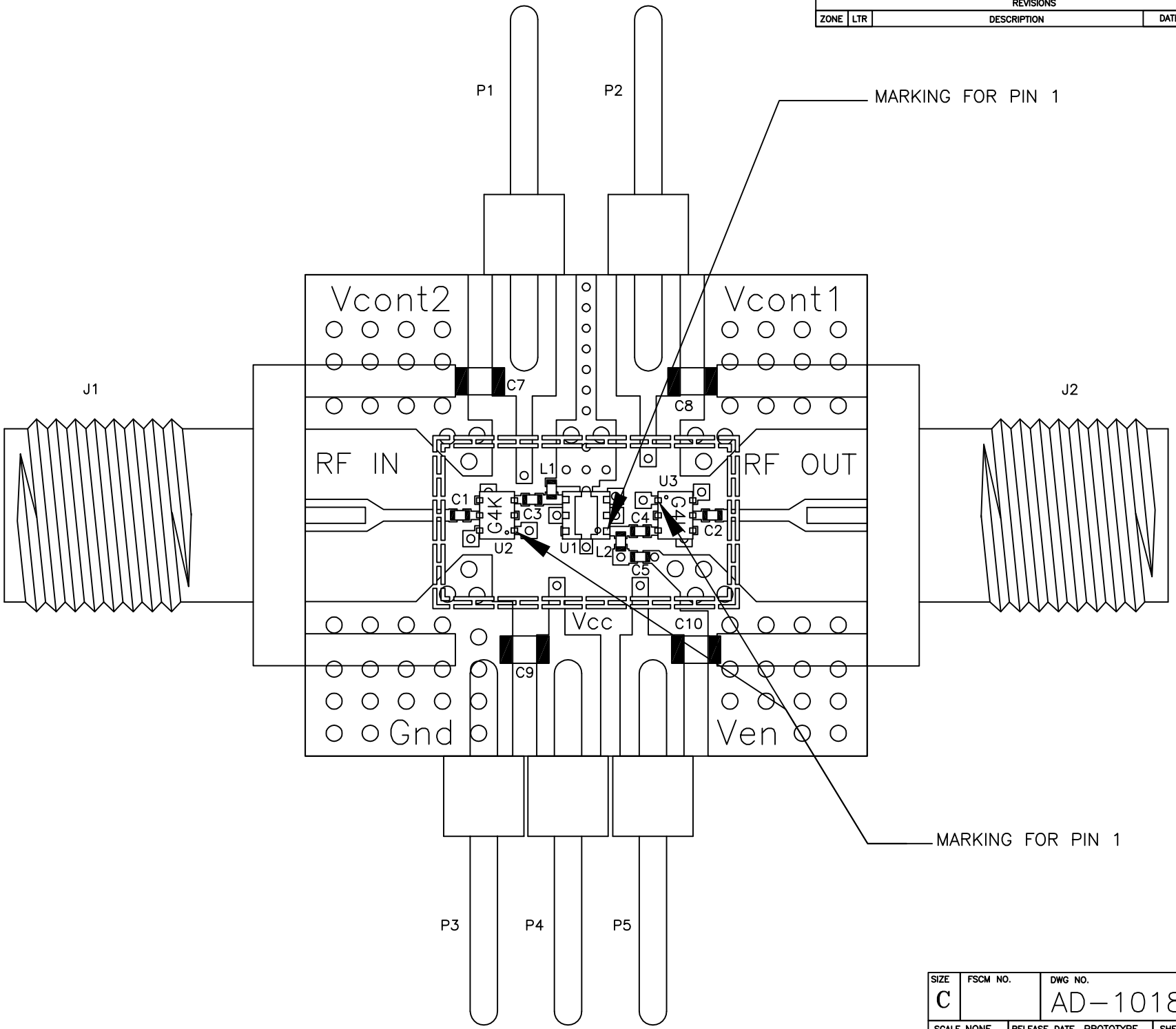
CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
uPG2314T5N-ZBT-EV-A
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101893	-

SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 1 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



SIZE	FSCM NO.	DWG NO.	REV
C		AD–101893	–
SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 2 OF 3	

CEL California Eastern Laboratories

Evaluation Board Document

µPG2314T5N-EVAL-A

Evaluation Board

- Bias and Matching Circuits
- Output Power Control
- PCB Information
- Typical Performance
- Schematic and Assembly Drawing

Matching and Bias Circuits

As shown in the circuit schematic on the next page, the uPG2314T5N requires relatively simple matching circuits. The inductor L1 is for input matching and should be placed close to the device. At the output essentially no matching circuit is required. L2 functions as an RF choke and C2 is DC block capacitor.

The uPG2314T5N is a two stage PA. The first stage bias is through Vcc1. A small section of transmission line between the device and the bypass capacitor, C1, is needed to provide enough isolation between RF and DC paths.

Output Power Control

The output power of uPG2314T5N can be adjusted by the voltage on Vcont pin. The control curve is shown on the data sheet. To turn off the PA, Vbias+Venable pin should be set to 0V.

PCB Information

The PCB is Getek two layer board. The board thickness is 28mil.

Typical Performance

Refer to the data sheet for typical performance curves.

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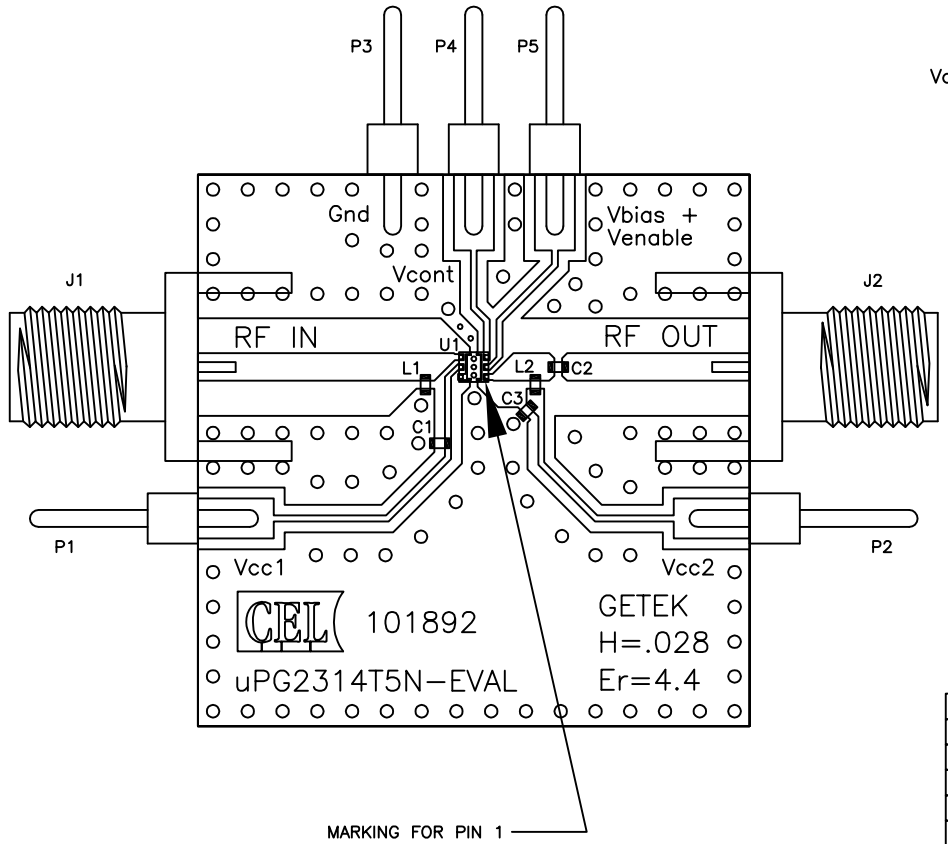
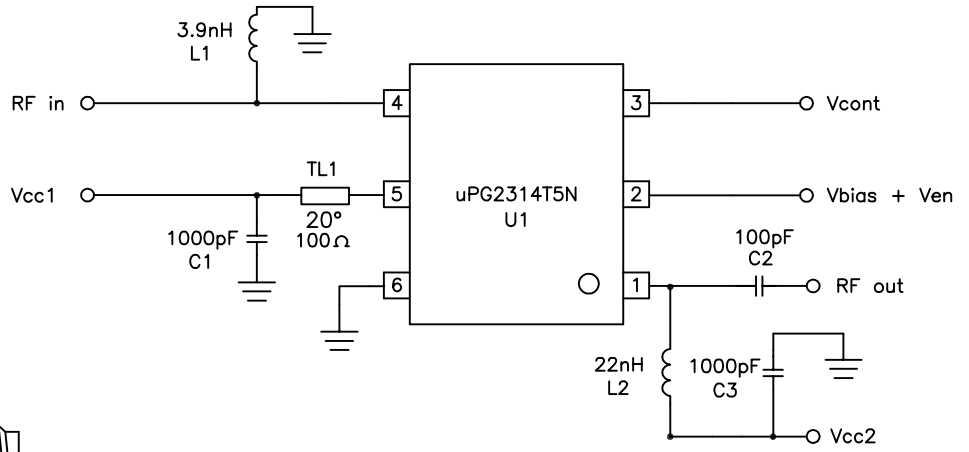
ZONE	LTR	DESCRIPTION	DATE	APPROVED





QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	LQG15HS22NJ02	L2	0402 22nH IND +/-5% MURATA	9
1	LQG15HS3N9S02	L1	0402 3.9nH IND +/-0.3nH MURATA	8
1	GRM1555C1H101JZ01D	C2	0402 100pF CAP +/-5% MURATA	7
2	GRM1555C1H102JA01D	C1,C3	0402 1000pF CAP +/-5% MURATA	6
		TL1	100 Ω ,20 ° @ 2.45GHz	5
5	2340-6111 TG	P1,P2,P3,P4,P5	PIN HEADER 3M	4
2	142-0701-841	J1,J2	SMA FEMALE CONNECTOR E.F.JOHNSON	3
1	uPG2314T5N	U1	NEC GaAs PA uPG2314T5N	2
1	CL-101892	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

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APPROVALS		
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Designed by:	Hugues de Saint Salvy	2005/12/14
Checked by:		
Project Engineer:		
Quality Control:		

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4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
uPG2314T5N-EVAL-A
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101892	-

SCALE 2:1 | RELEASE DATE PROTOTYPE | SHEET 1 OF 1

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