CEL California Eastern Laboratories

Evaluation Board Document

µPG2250T5N-EVAL-A

Evaluation Board

- Circuit Description
- Performance data
- Circuit schematic and assembly drawing

Circuit Description

The circuit schematic and assembly drawing are shown on the last two pages.

Matching and Bias Circuits

The inductor L1 is for input matching and should be placed close to the device.

The output matching is realized mainly with the capacitor C6. C6 can be placed as close as possible to the device without much sacrifice of the performance when the layout space is tight. On the other hand the output power can be increased by a fraction of dB by moving C6 away from the device. The trace length between C6 and the device on this evaluation board is about 100 mil. Because of the gradual change in its width, the effect of this section of trace cannot be simply represented by a set of parameters of transmission line impedance and electrical length. It is recommended that the designer leave some space for tuning on this trace length in the initial prototype board layout if an optimal output power is desirable.

The uPG2250T5N has three gain stages, each being biased by an external voltage supply. The DC feed lines are not completely isolated from the RF path on the chip, and as a result care needs to be taken in the board layout for these DC lines.

The inductor L2 on the Vdd1 line provides the DC feed for the first stage and is part of the inter-stage matching between stage 1 and 2 as well. The value of this inductor may need to be adjusted on the application board to have the optimized performance. Generally it should be placed close to the device and immediately followed by the capacitor C2 as shown in the assembly drawing of this evalboard.

The length of trace TL1 on the Vdd2 line has significant impact on the output power and the value shown in the schematic should be used in the application board layout.

The inductor L3 is for the last stage DC feed and functions as an RF choke. Its value and location are not critical.

The three shunt capacitors on the DC lines (C2, C8 and C9) provide a low RF impedance at their respective locations. Their value should be in the range of 10 to 30pF. These low RF impedance spots adequately isolate the RF circuit from the rest of DC feed lines beyond the point of shunt capacitors. This arrangement is particularly beneficial in transferring the evaluation circuit to the end products because the RF characteristic of a DC feed line usually cannot be well controlled in a practical board design. The other three 0.01uF capacitors, C1, C3 and C5, are general bypass capacitors and the user can select their values and locations according the design requirements.

PCB Material

The PCB is Getek two layer board. The board thickness is 28mil.

Typical Performance Data

Test Conditions:

f=2.45GHz; Pin= -5dBm; Vcont =1.8V

For $V_{DD1,2,3}$ =1.8V

Quiescent current Idsq: 55mA;

Output Power Pout: 21dBm;

Supply Current I_{DD}: 130mA;

Efficiency PAE: 55%;

For $V_{DD1,2,3}$ =3V

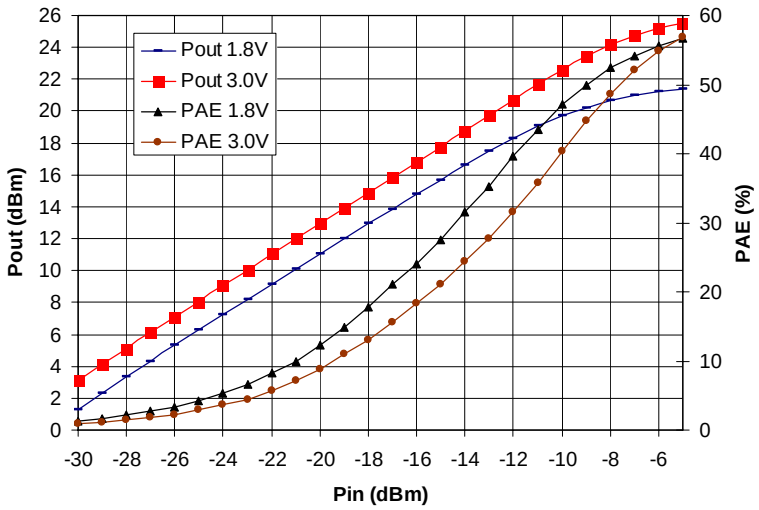
Quiescent current Idsq: 80mA;

Output Power Pout: 25dBm;

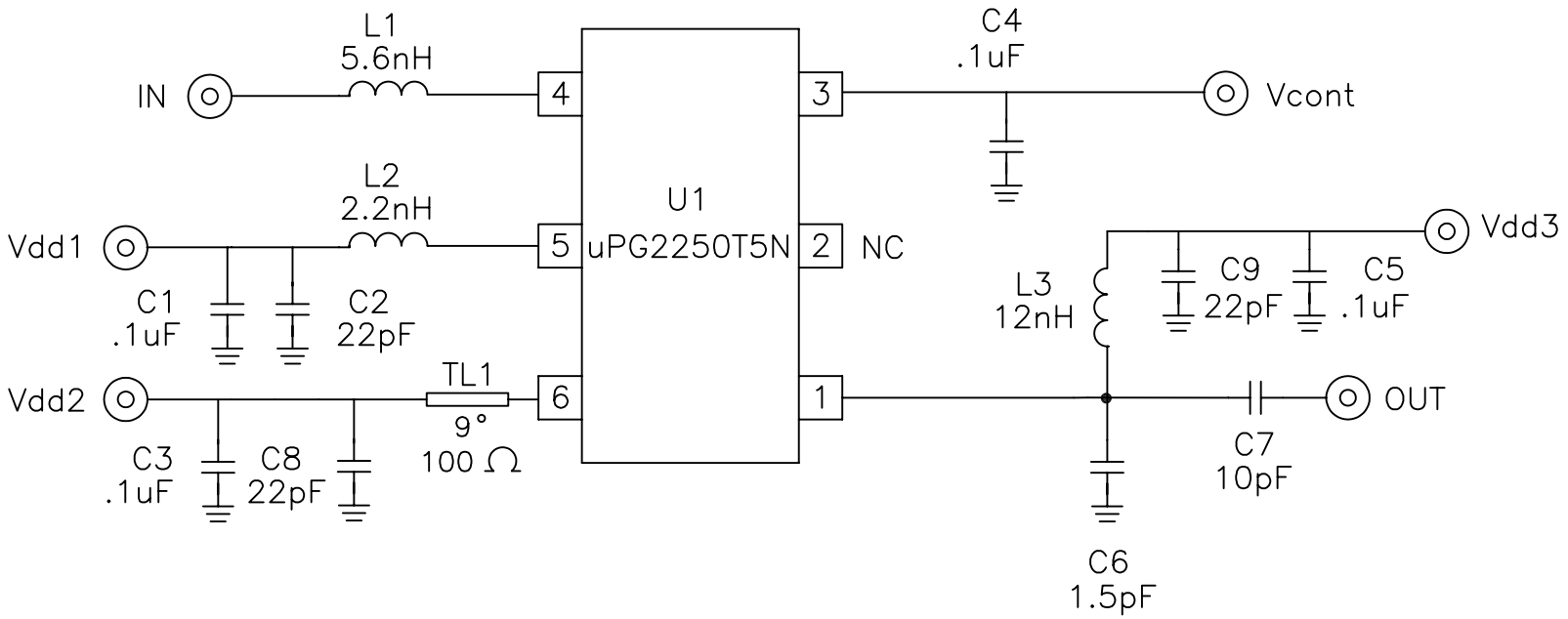
Supply Current I_{DD}: 200mA;

Efficiency PAE: 55%;

Pout and PAE vs Pin are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	LQG15HS12NJ02	L3	0402 12nH IND MURATA	13
1	LQG15HS2N2S02	L2	0402 2.2nH IND MURATA	12
1	LQG15HS5N6S02	L1	0402 5.6nH IND MURATA	11
1	GRM1555C1H100JZ01B	C7	0402 10pF CAP MURATA	10
1	GRM1555C1H1R5CZ01D	C6	0402 1.5pF CAP MURATA	9
3	GRM1555C1H220JZ01B	C2,C8,C9	0402 22pF CAP MURATA	8
4	GRM155R71E104KA01D	C1,C3,C4,C5	0402 .1uF CAP MURATA	7
		TL1	100 Ω ,9° @ 2.45GHz	6
5	2340-6111 TG	P1-P5	PIN HEADER 3M	5
2	142-0701-841	J1,J2	SMA FEMALE CONNECTOR E.F.JOHNSON	4
1	uPG2250T5N	U1	NEC uPG2250T5N	3
1	CL-101919	DRAWING	COMPONENT LAYOUT DRAWING	2
1	N/A	PCB	PCB MANUFACTURED BY NETWORK PCB	1

PARTS LIST

APPROVALS		
Drawing by: MDONG	5/13/2010	
Designed by: MDONG	5/13/2007	
Checked by:		
Project Engineer:		
Quality Control:		

CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
UPG2250T5N-EVAL-A
SCHEMATIC BOM

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101919	

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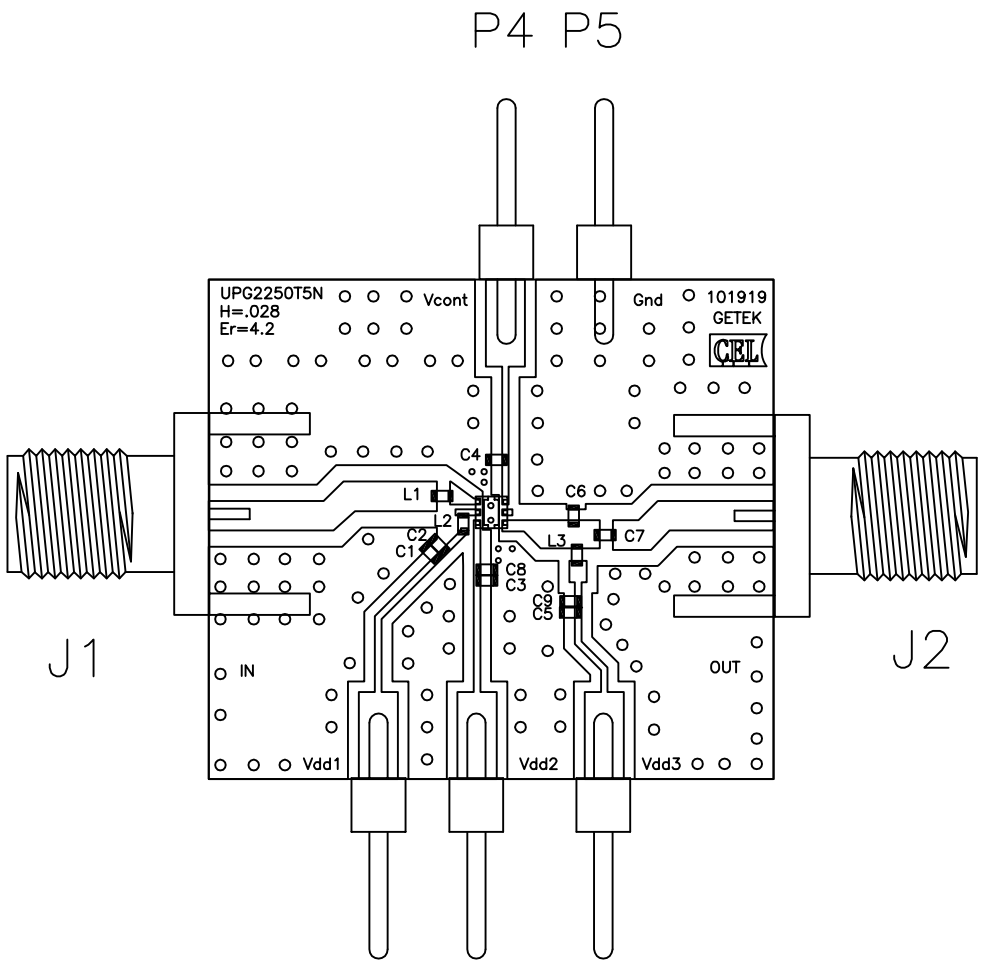
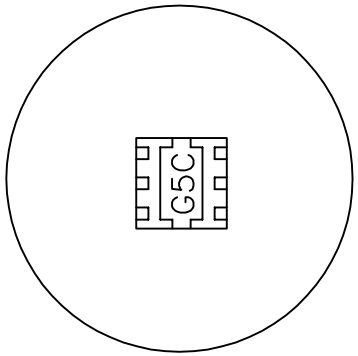
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





APPROVALS		
Drawing by: BMU	01/03/2007	
Designed by: BMU	01/03/2007	
Checked by:		
Project Engineer:		
Quality Control:		

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TITLE:
UPG2250T5N-EVAL-A
ASSEMBLY_DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101919	-

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Mouser Electronics

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