

PE426525

Document Category: Product Specification

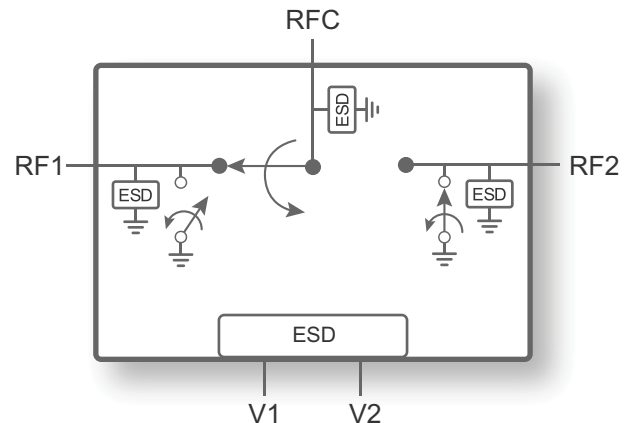
UltraCMOS® SPDT RF Switch, 9 kHz–60 GHz



Features

- Wideband support up to 60 GHz
- Low insertion loss
 - 1.3 dB @ 26.5 GHz
 - 1.7 dB @ 45 GHz
 - 1.9 dB @ 50 GHz
 - 2.7 dB @ 60 GHz
- Fast switching time of 8 ns
- High port to port isolation
 - 41 dB @ 26.5 GHz
 - 38 dB @ 45 GHz
 - 37 dB @ 50 GHz
 - 36 dB @ 60 GHz
- –55 °C to +125 °C operating temperature support
- High linearity: IIP3 of 48 dBm
- Flip-chip die, pin-to-pin compatible to the PE42524 and the PE42525

Figure 1 • PE426525 Functional Diagram



Applications

- Harsh industrial applications
- Applications that require extended temperature support in the range of –55 °C to +125 °C

Product Description

The PE426525 is a HaRP™ technology-enhanced reflective SPDT RF switch die that supports a wide frequency range from 9 kHz to 60 GHz. This wideband flip-chip switch is pin compatible to the PE42524 and the PE42525. It delivers low insertion loss, fast switching time and high isolation in the operating temperature of –55 °C to +125 °C. It is ideal for applications that require extended temperature support within this range, such as harsh industrial applications. At 50 GHz, the PE426525 exhibits 1.9 dB insertion loss and 37 dB isolation. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE426525 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology.

Peregrine's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • Absolute Maximum Ratings for PE426525

| Parameter/Condition | Min | Max | Unit |
|--|------|---------------|------|
| Control voltage (V1, V2) | −3.6 | 3.6 | V |
| RF input power (RFC–RFX, 50Ω) | | Fig. 2 | dBm |
| Maximum junction temperature | | +150 | °C |
| Storage temperature range | −65 | +150 | °C |
| ESD voltage HBM ^(*) | | | |
| All pins | | 600 | V |
| RF pins to GND | | 1000 | V |
| Note: * Human body model (MIL-STD 883 Method 3015). | | | |

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for PE426525. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • Recommended Operating Condition for PE426525

| Parameter | Min | Typ | Max | Unit |
|--|------|------|---------------|------|
| Control high (V1, V2) | 2.7 | 3.0 | 3.3 | V |
| Control low (V1, V2) | –3.3 | –3.0 | –2.7 | V |
| Control current | | 390 | | nA |
| RF input power, CW (RFC–RFX) ⁽¹⁾ | | | Fig. 2 | dBm |
| RF input power, pulsed (RFC–RFX) ⁽²⁾ | | | Fig. 2 | dBm |
| Operating temperature range | –55 | +25 | +125 | °C |
| Notes: 1) 100% duty cycle, all bands, 50Ω. 2) Pulsed, 5% duty cycle of 4620 μs period, 50Ω. | | | | |

Electrical Specifications

Table 3 provides the PE426525 key electrical specifications @ +25 °C, V1 = +3.0V, V2 = –3.0V or V1 = –3.0V, V2 = +3.0V ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 3 • PE426525 Electrical Specifications

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|---------------------------|-----------|------------------|-------|-----|--------|----------|
| Operation frequency | | | 9 kHz | | 60 GHz | As shown |
| Insertion loss | RFC–RFX | 100 MHz | | 0.9 | 1.1 | dB |
| | | 100 MHz–26.5 GHz | | 1.3 | 1.6 | dB |
| | | 26.5–45 GHz | | 1.7 | 2.0 | dB |
| | | 45–50 GHz | | 1.9 | 2.3 | dB |
| | | 50–60 GHz | | 2.7 | 3.8 | dB |
| Isolation | All paths | 100 MHz | 74 | 80 | | dB |
| | | 100 MHz–26.5 GHz | 38 | 41 | | dB |
| | | 26.5–45 GHz | 33 | 38 | | dB |
| | | 45–50 GHz | 32 | 37 | | dB |
| | | 50–60 GHz | 29 | 36 | | dB |
| Return loss (active port) | RFC–RFX | 100 MHz | | 21 | | dB |
| | | 100 MHz–26.5 GHz | | 17 | | dB |
| | | 26.5–45 GHz | | 18 | | dB |
| | | 45–50 GHz | | 15 | | dB |
| | | 50–60 GHz | | 13 | | dB |

Table 3 • PE426525 Electrical Specifications (Cont.)

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|--|---------|---------------------------------|-----|--------|-----|------------------|
| Return loss (RFC port) | RFC–RFX | 100 MHz | | 21 | | dB |
| | | 100 MHz–26.5 GHz | | 20 | | dB |
| | | 26.5–45 GHz | | 18 | | dB |
| | | 45–50 GHz | | 16 | | dB |
| | | 50–60 GHz | | 14 | | dB |
| 2nd harmonic, 2fo | RFC–RFX | +25 dBm output power, 1 GHz | | 73 | | dBc |
| | | +25 dBm output power, 2 GHz | | 77 | | dBc |
| | | +25 dBm output power, 6.5 GHz | | 89 | | dBc |
| | | +25 dBm output power, 13.4 GHz | | 92 | | dBc |
| Input 1dB compression point ⁽¹⁾ | | | | Fig. 2 | | dBm |
| Input IP2 | | 1 GHz | | 93 | | dBm |
| | | 2 GHz | | 98 | | dBm |
| | | 6.5 GHz | | 109 | | dBm |
| | | 13.4 GHz | | 112 | | dBm |
| Input IP3 | | 1 GHz | | 49 | | dBm |
| | | 2 GHz | | 48 | | dBm |
| | | 6 GHz | | 46 | | dBm |
| | | 13.4 GHz | | 46 | | dBm |
| Video feed through ⁽²⁾ | | DC measurement | | 30 | | mV _{PP} |
| RF T _{RISE} / T _{FALL} | | 10%/90% RF | | 3 | | ns |
| Settling time | | 50% CTRL to 0.05 dB final value | | 48 | 60 | ns |
| Switching time | | 50% CTRL to 90% or 10% RF | | 8 | 12 | ns |

Notes:

- 1) The input 1dB compression point is a linearity figure of merit. Refer to **Table 2** for the RF input power (50Ω).
- 2) Measured with a 3.5 ns rise time, –3.0/+3.0V pulse and 100 MHz bandwidth.

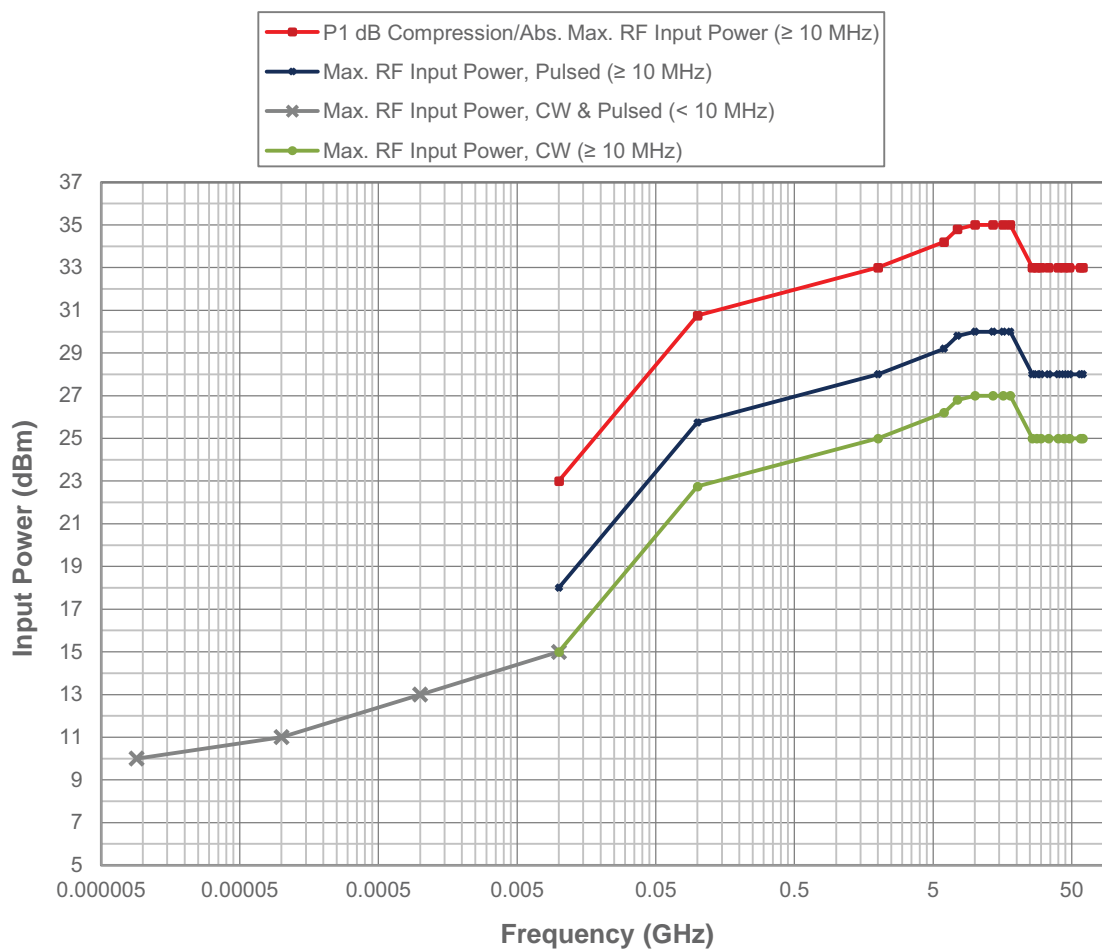
Control Logic

Table 4 provides the control logic truth table for the PE426525. States 2 and 3 are used in normal switching operations.

Table 4 • Truth Table for PE426525

| V1 | V2 | RF1 | RF2 | State |
|-------|-------|-----|-----|-------|
| –3.0V | –3.0V | OFF | OFF | 1 |
| –3.0V | +3.0V | OFF | ON | 2 |
| +3.0V | –3.0V | ON | OFF | 3 |
| +3.0V | +3.0V | ON | ON | 4 |

Figure 2 • Power De-rating Curve, 9 kHz–60 GHz, –55 °C to +125 °C Ambient, 50Ω



Typical Performance Data

Figure 3–Figure 12 show the typical performance data @ 25 °C, V1 = +3.0V, V2 = –3.0 or V1 = –3.0V, V2 = +3.0V ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Figure 3 • Insertion Loss vs Temperature (RFC–RFX)

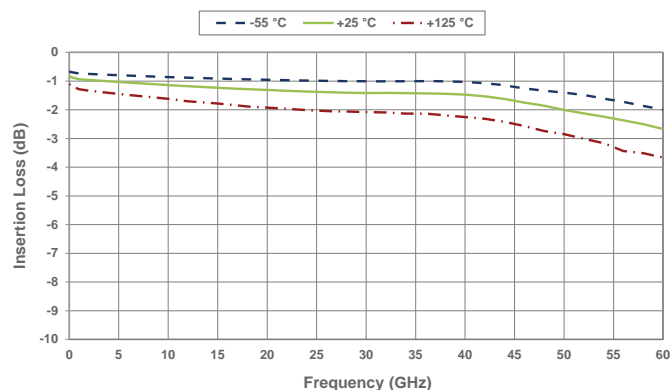


Figure 6 • Insertion Loss vs V1/V2 (RFC–RFX)

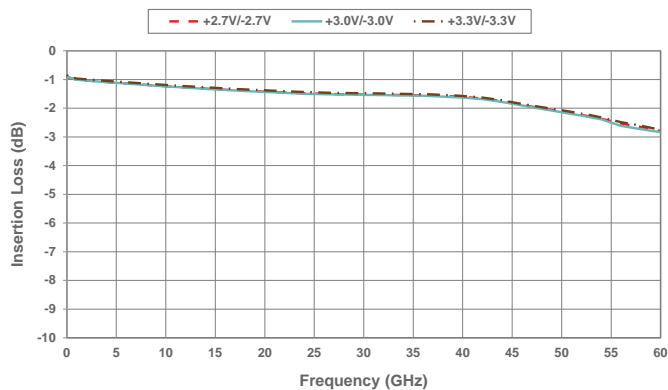


Figure 4 • RFC Port Return Loss vs Temperature

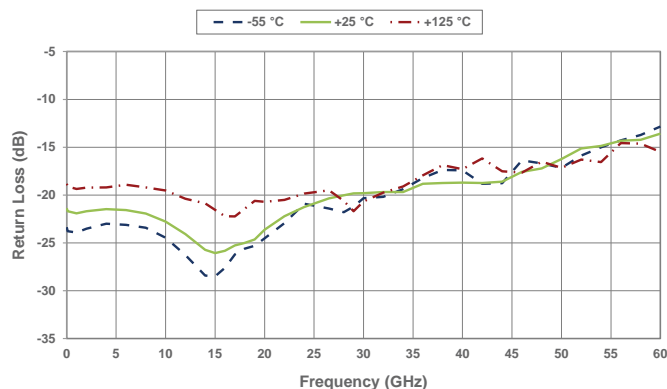


Figure 7 • RFC Port Return Loss vs V1/V2

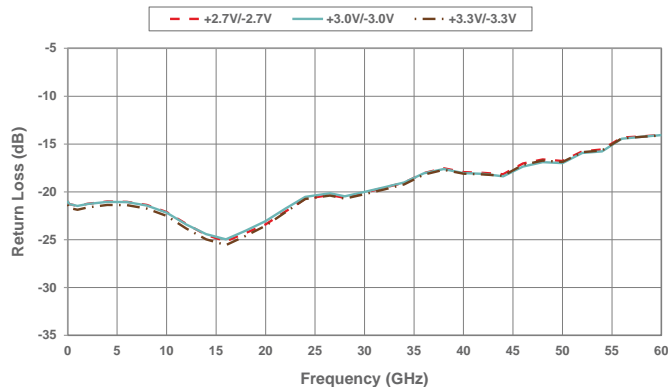


Figure 5 • Active Port Return Loss vs Temperature

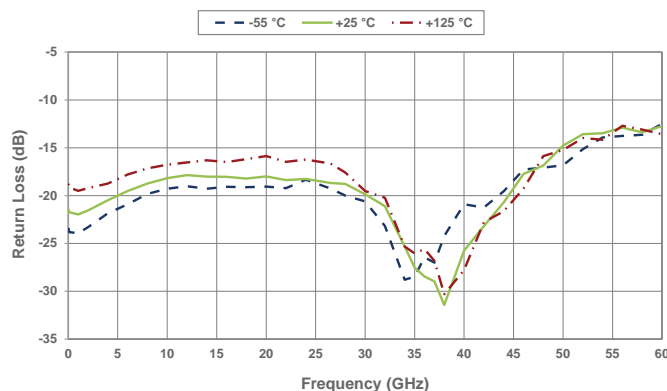


Figure 8 • Active Port Return Loss vs V1/V2

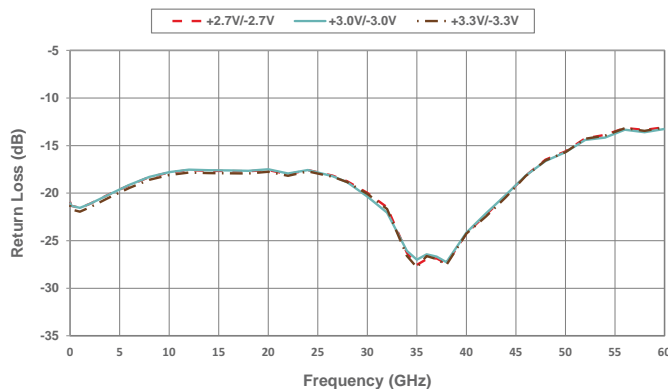


Figure 9 • Isolation vs Temperature (RFX–RFX)

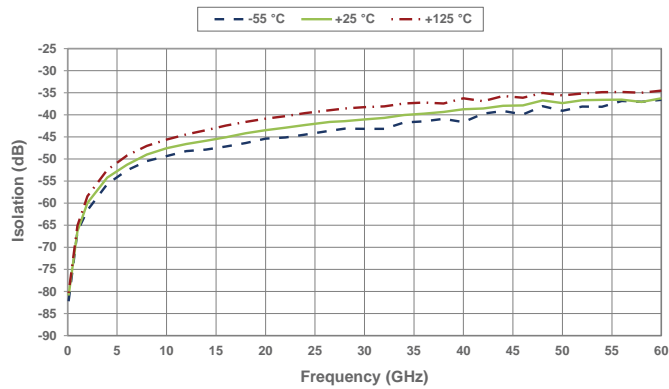


Figure 11 • Isolation vs V1/V2 (RFX–RFX)

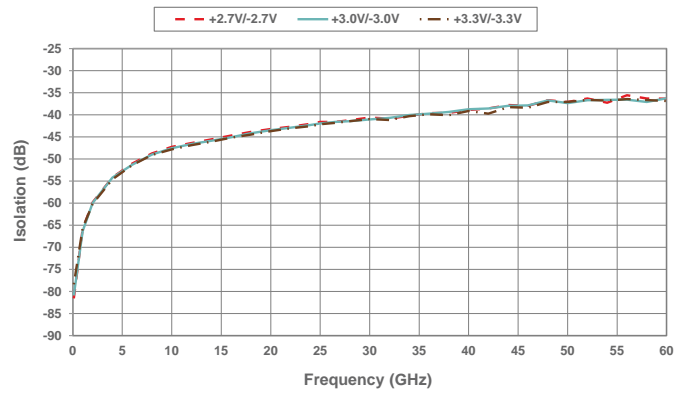


Figure 10 • Isolation vs Temperature (RFC–RFX)

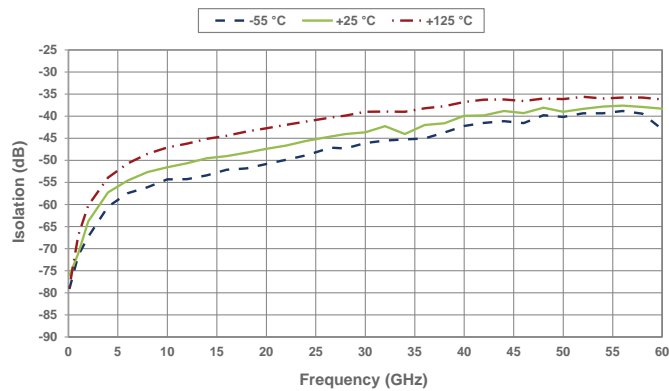
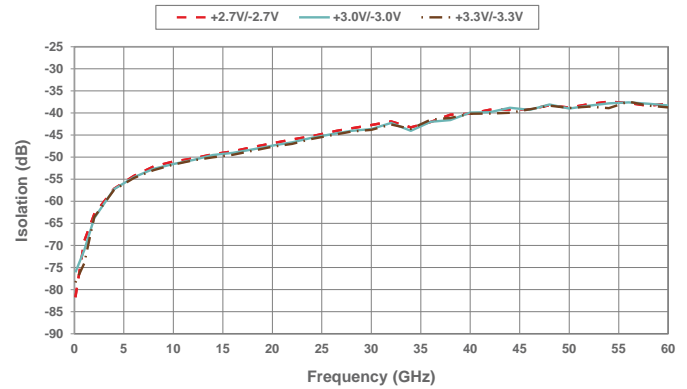


Figure 12 • Isolation vs V1/V2 (RFC–RFX)



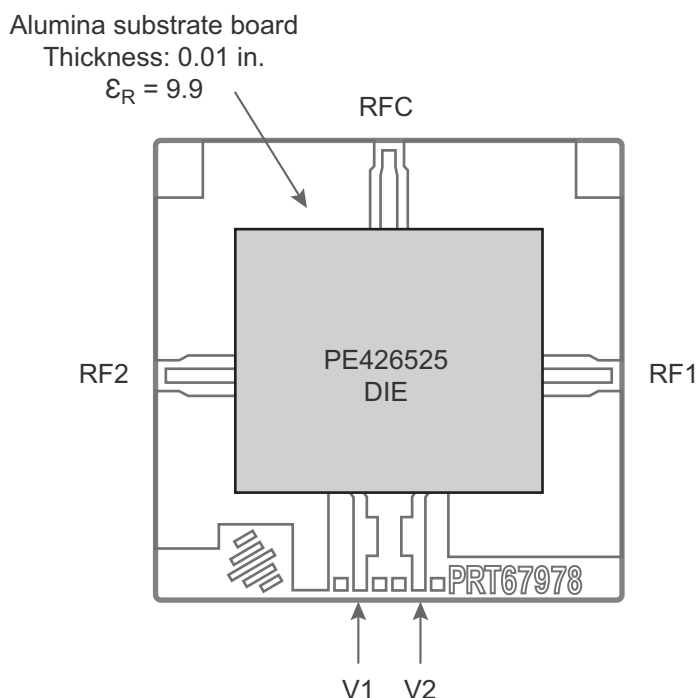
Evaluation Setup

The PE426525 s-parameter data and input 1dB compression point up to 60 GHz (**Table 3** and **Figure 3–Figure 12**) were taken using either co-planar waveguide with ground (CPWG) or grounded co-planar waveguide (GCPW) on an alumina substrate and RF probes.

The PE426525 2nd harmonic, input 1dB compression point below 18 GHz, input IP3 measurements, settling time and switching time (**Table 3**) were taken on a PCB using 2.92 mm connectors.

Bypass capacitors are not required.

Figure 13 • Alumina Substrate Board for PE426525



Pin Configuration

This section provides pin information for the PE426525. **Figure 14** shows the pin configuration of this device. **Table 5** provides a description for each pin.

Figure 14 • Pin Configuration (Bumps Up) for PE426525

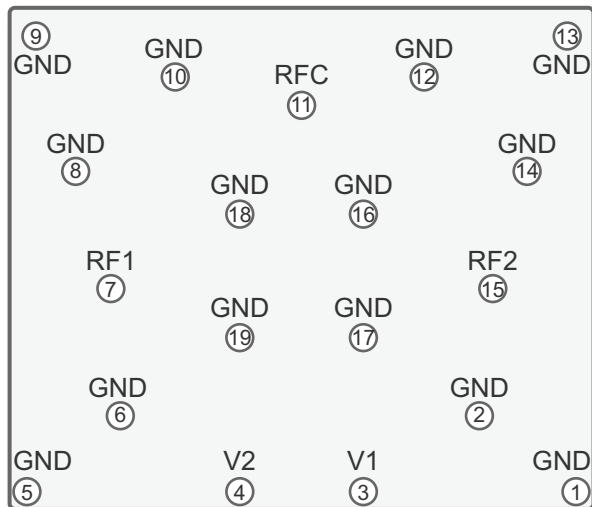


Table 5 • Pin Descriptions for PE426525

| Pin No. | Pin Name | Description |
|--------------------------------|----------|-----------------|
| 1, 2, 5, 6, 8–10, 12–14, 16–19 | GND | Ground |
| 3 | V1 | Control input 1 |
| 4 | V2 | Control input 2 |
| 7 | RF1 | RF port 1 |
| 11 | RFC | RF common port |
| 15 | RF2 | RF port 2 |

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE426525.

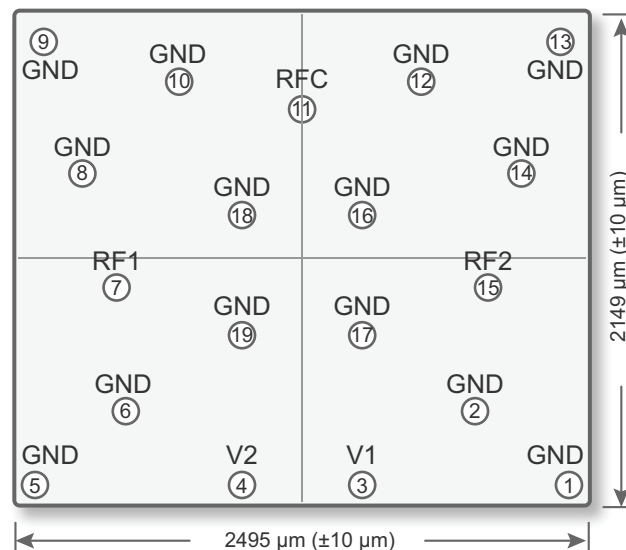
Table 6 • Mechanical Specifications for PE426525

| Parameter | Min | Typ | Max | Unit | Test Condition |
|-----------------------------|-------------|-------------|-------------|------|---|
| Die size, singulated (x, y) | 2485 × 2139 | 2495 × 2149 | 2505 × 2159 | μm | Including excess silicon, maximum tolerance = ±10 μm |
| Wafer thickness | 180 | 200 | 220 | μm | |
| Bump pitch | 500 | | | μm | |
| Bump height | 59.5 | 70 | 80.5 | μm | |
| Bump diameter | | 91 | | μm | |
| UBM diameter | 71 | 75 | 79 | μm | |

Table 7 • Pin Coordinates for PE426525^(*)

| Pin # | Pin Name | Pin Center (μm) | |
|-------|----------|-----------------|--------|
| | | X | Y |
| 1 | GND | 1128.5 | -958.5 |
| 2 | GND | 731.5 | -646.5 |
| 3 | V1 | 253.5 | -958.5 |
| 4 | V2 | -253.5 | -958.5 |
| 5 | GND | -1128.5 | -958.5 |
| 6 | GND | -731.5 | -646.5 |
| 7 | RF1 | -785.5 | -121.5 |
| 8 | GND | -931.5 | 363.5 |
| 9 | GND | -1091.5 | 913.5 |
| 10 | GND | -503.5 | 753.5 |
| 11 | RFC | 0 | 629 |
| 12 | GND | 503.5 | 753.5 |
| 13 | GND | 1091.5 | 913.5 |
| 14 | GND | 931.5 | 363.5 |
| 15 | RF2 | 785.5 | -121.5 |
| 16 | GND | 253.5 | 183.5 |
| 17 | GND | 253.5 | -326.5 |
| 18 | GND | -253.5 | 183.5 |
| 19 | GND | -253.5 | -326.5 |

Note: * All pin locations originate from the die center and refer to the center of the pin.

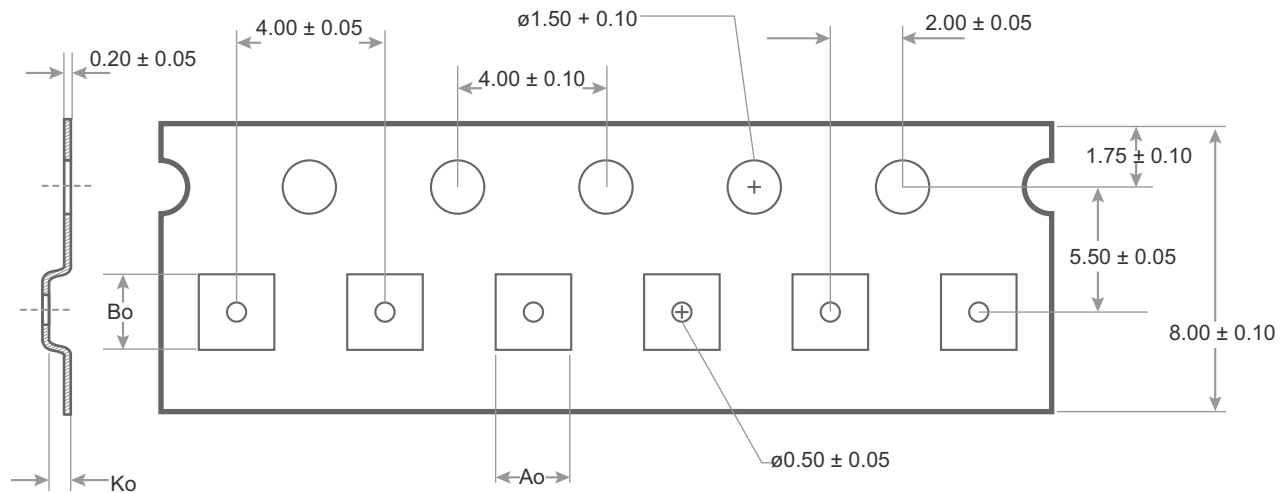
Figure 15 • Pin Layout for PE426525⁽¹⁾⁽²⁾

Notes:

- 1) Drawings are not drawn to scale.
- 2) Singulated die size shown, bump side up.

Tape and Reel Specification

This section provides the tape and reel specification for the PE426525.

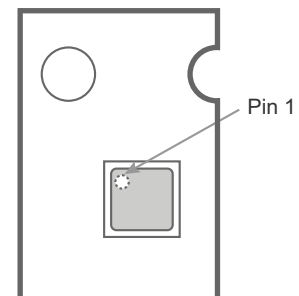
Figure 16 • Tape and Reel Specifications for PE426525



| Pocket | Nominal | Tolerance |
|--------|---------|-----------|
| Ao | 2.41 | ± 0.05 |
| Bo | 2.76 | ± 0.05 |
| Ko | 0.39 | ± 0.05 |

Notes:

Not Drawn to Scale
Dimensions are in millimeters
Maximum cavity angle 5 degrees
Bumped die are oriented active side down



Device Orientation in Tape

Ordering Information

Table 8 lists the available ordering code for the PE426525 as well as shipping method.

Table 8 • *Order Code for PE426525*

| Order Code | Description | Packaging | Shipping Method |
|-------------|-------------------------|----------------------|-----------------|
| PE426525A-X | PE426525 SPDT RF switch | Die on tape and reel | 500 die/T&R |

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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Product Brief

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Not Recommended for New Designs (NRND)

This product is in production but is not recommended for new designs.

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This product is currently going through the EOL process. It has a specific last-time buy date.

Obsolete

This product is discontinued. Orders are no longer accepted for this product.

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