

# Data Sheet



## SCC2130-D08

### Combined gyroscope and 3-axis accelerometer with digital SPI interface

#### Features

- $\pm 125^\circ/\text{s}$  X-axis angular rate measurement range
- $\pm 6\text{g}$  3-axis acceleration measurement (XYZ) range
- $-40^\circ\text{C} \dots +125^\circ\text{C}$  operating range
- 3.0V...3.6V supply voltage
- SPI digital interface
- Extensive self diagnostics features
- Size 15.0 x 8.5 x 4.3 mm (l x w x h)
- RoHS compliant robust SOIC plastic package suitable for lead free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology

#### Applications

SCC2130-D08 is targeted at applications demanding high stability with tough environmental requirements. Typical applications include:

- Inertial Measurement Units (IMUs) for highly demanding environments
- Platform stabilization and control
- Motion analysis and control
- Roll over detection
- Robotic control systems
- Machine control systems
- Navigation systems

#### Overview

The SCC2130-D08 is a combined high performance angular rate and accelerometer sensor component. It consists of X-axis angular rate sensor and three axis accelerometer sensor based on Murata's proven capacitive 3D-MEMS technology. Signal processing is done in one mixed signal ASIC that provides angular rate and acceleration output via flexible SPI digital interface. Sensor elements and ASIC are packaged to 24 pin premolded plastic housing that guarantees reliable operation over product's lifetime.

The SCC2130-D08 is designed, manufactured and tested for high stability, reliability and quality requirements. The component has extremely stable output over wide range of temperature, humidity and vibration. The component has several advanced self diagnostics features, is suitable for SMD mounting and is compatible with RoHS and ELV directives.

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## 1 Introduction

This document contains essential technical information about the SCC2130-D08 sensor including specifications, SPI interface descriptions, user accessible register details, electrical properties and application information. This document should be used as a reference when designing in SCC2130-D08 component.

## 2 Specifications

### 2.1 General Specifications

General specifications for SCC2130-D08 component are presented in Table 1. All analog voltages are related to the potential at AVSS and all digital voltages are related to the potential at DVSS.

Table 1. General specifications.

| Parameter                                                                  | Condition                             | Min | Typ  | Max  | Units |
|----------------------------------------------------------------------------|---------------------------------------|-----|------|------|-------|
| Analog supply voltage: AVDD                                                |                                       | 3.0 | 3.3  | 3.6  | V     |
| Analog supply current: I_AVDD                                              | Temperature range -40 ... +125 °C     |     | 15.2 |      | mA    |
| Digital supply voltage: DVDD                                               |                                       | 3.0 | 3.3  | 3.6  | V     |
| Digital supply current: I_DVDD                                             | Temperature range -40 ... +125 °C     |     | 3.3  |      | mA    |
| Boost supply current: I_L1<br>(current through inductor L1, see Figure 27) | Mean value                            |     | 6.7  | 11.5 | mA    |
|                                                                            | Peak value, T < 1µs                   |     |      | 110  | mA    |
|                                                                            | Max. value during startup (T ≤ 0.4ms) |     |      | 60   | mA    |
| Total current, I_TOTAL                                                     | I_AVDD + I_DVDD + I_L1                |     | 25.2 | 31.5 | mA    |
| Total current reset                                                        | Total average current during reset    |     |      | 5    | mA    |
| Rise/fall time: AVDD, DVDD, Vin_BOOST (see Figure 27)                      |                                       |     |      | 200  | ms    |

## 2.2 Performance Specifications for Gyroscope

Table 2. Gyro performance specifications (DVDD=AVDD=3.3V, ambient temperature and ODR=2.3kHz unless otherwise specified).

| Parameter                               | Condition                   | Min  | Typ   | Max | Units              |
|-----------------------------------------|-----------------------------|------|-------|-----|--------------------|
| Operating range                         | Measurement axis X          | -125 |       | 125 | °/s                |
| Offset (zero rate output)               |                             |      | 0     |     | LSB                |
| Offset error <sup>(A)</sup>             |                             | -1   |       | 1   | °/s                |
| Offset temperature drift <sup>(B)</sup> | -40°C ... +125°C            | -0.8 |       | 0.8 | °/s                |
| Offset short term bias stability        |                             |      | 1     |     | °/h                |
| Angular random walk                     |                             |      | 0.23  |     | °/√h               |
| Sensitivity                             |                             |      | 50    |     | LSB/(°/s)          |
| Sensitivity error <sup>(C)</sup>        | -40°C ... +125°C            | -2.5 |       | 2.5 | %                  |
| Linearity error <sup>(D)</sup>          |                             |      | ±0.5  |     | °/s                |
| Integrated noise (RMS)                  | 60Hz filter                 |      | 0.05  |     | °/s <sub>RMS</sub> |
| Noise density                           |                             |      | 0.005 |     | (°/s)/√Hz          |
| Cross axis sensitivity <sup>(E)</sup>   | per axis                    | -1.5 |       | 1.5 | %                  |
| G-sensitivity                           |                             | -0.1 |       | 0.1 | (°/s)/g            |
| Shock sensitivity                       | 50g, 6ms                    |      |       | 2.0 | °/s                |
| Shock recovery                          |                             |      |       | 50  | ms                 |
| Amplitude response                      | 10Hz filter, -3dB frequency |      | 10    |     | Hz                 |
|                                         | 60Hz filter, -3dB frequency |      | 60    |     | Hz                 |
| Power on start-up time                  | 10Hz filter                 |      |       | 750 | ms                 |
|                                         | 60Hz filter                 |      |       | 620 | ms                 |
| Recommended ODR <sup>(F)</sup>          |                             |      | 2300  |     | Hz                 |

Min/Max values are validation ±3 sigma variation limits from test population. Typical values are not guaranteed.

A) Includes offset calibration error and drift over lifetime.

B) Deviation from value at ambient temperature.

C) Includes calibration error, deviation from room temperature value and drift over lifetime.

D) Straight line through specified measurement range end points.

E) Cross axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction:

Cross axis for Y axis = Sensitivity Y / Sensitivity X

Cross axis for Z axis = Sensitivity Z / Sensitivity X

F) ODR = Output Data Rate, see section 5.1.7 for more details.

## 2.3 Performance Specifications for Accelerometer

Table 3. Accelerometer performance specifications (DVDD=AVDD=3.3V, ambient temperature and ODR=2.3kHz unless otherwise specified).

| Parameter                                    | Condition                                                  | Min  | Typ           | Max        | Unit              |
|----------------------------------------------|------------------------------------------------------------|------|---------------|------------|-------------------|
| Measurement range                            | Measurement axes XYZ                                       | -6   |               | 6          | g                 |
| Offset (zero acceleration output)            |                                                            |      | 0             |            | LSB               |
| Offset error <sup>(A)</sup>                  |                                                            | -20  |               | 20         | mg                |
| Offset temperature drift <sup>(B)</sup>      | -40°C ... +125°C                                           | -18  |               | 18         | mg                |
| Sensitivity                                  | Between ±3°                                                |      | 1962<br>0.029 |            | LSB/g<br>°/LSB    |
| Sensitivity error <sup>(A)</sup>             |                                                            | -1   |               | 1          | %                 |
| Sensitivity temperature drift <sup>(B)</sup> | -40°C ... +125°C                                           | -1   |               | 1          | %                 |
| Linearity error <sup>(C)</sup>               | -1g ... +1g range<br>-6g ... +6g range                     |      | ±5<br>±50     |            | mg<br>mg          |
| Integrated noise (RMS)                       | 60Hz filter                                                |      | 2.7           |            | mg <sub>RMS</sub> |
| Noise density                                |                                                            |      | 270           |            | µg/√Hz            |
| Cross axis sensitivity <sup>(D)</sup>        | per axis                                                   | -0.5 |               | 0.5        | %                 |
| Amplitude response                           | 10Hz filter, -3dB frequency<br>60Hz filter, -3dB frequency |      | 10<br>60      |            | Hz<br>Hz          |
| Power on start-up time                       | 10Hz filter<br>60Hz filter                                 |      |               | 450<br>320 | ms<br>ms          |
| Recommended ODR <sup>(E)</sup>               |                                                            |      | 2300          |            | Hz                |

Min/Max values are validation ±3 sigma variation limits from test population. Typical values are not guaranteed.

A) Includes calibration error and drift over lifetime.

B) Deviation from value at ambient temperature.

C) Straight line through specified measurement range end points.

D) Cross axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction. X-axis output cross axis sensitivity (cross axis for Y and Z-axis outputs are defined correspondingly):

Cross axis for Y axis = Sensitivity Y / Sensitivity X

Cross axis for Z axis = Sensitivity Z / Sensitivity X

E) ODR = Output Data Rate, see section 5.1.7 for more details.

## 2.4 Performance Specification for Temperature Sensor

Table 4. Temperature sensor performance specifications.

| Parameter                      | Condition                                          | Min. | Typ  | Max. | Unit   |
|--------------------------------|----------------------------------------------------|------|------|------|--------|
| Temperature signal range       |                                                    | -50  |      | +150 | °C     |
| Temperature signal sensitivity | Temperature sensor output in 2's complement format |      | 14.7 |      | LSB/°C |

Temperature is converted to °C with following equation:

$$\text{Temperature } [^{\circ}\text{C}] = 60 + (\text{TEMP} / 14.7),$$

where TEMP is temperature sensor output register content in decimal format.

## 2.5 Absolute Maximum Ratings

Within the maximum ratings (Table 5), no damage to the component shall occur. Parametric values may deviate from specification, yet no functional deviation shall occur. All analog voltages are related to the potential at AVSS, all digital voltages are related to DVSS.

Table 5. Absolute maximum ratings.

| Parameter      | Remark                                                | Min.                       | Typ | Max.     | Unit |
|----------------|-------------------------------------------------------|----------------------------|-----|----------|------|
| AVDD           | Supply voltage analog circuitry                       | -0.3                       |     | 4.3      | V    |
| DVDD           | Supply voltage digital circuitry                      | -0.3                       |     | 4.3      | V    |
| DIN/DOUT       | Maximum voltage at digital input and output pins      | -0.3                       |     | DVDD+0.3 | V    |
| VBoost, LBoost | Maximum voltage at high voltage input and output pins | -0.3                       |     | 40       | V    |
| Topr           | Operating temperature range                           | -40                        |     | 125      | °C   |
| Tstg           | Storage temperature range                             | -40                        |     | 150      | °C   |
| ESD_HBM        | ESD according Human Body Model (HBM), Q100-002        | ±2000                      |     |          | V    |
| ESD_MM         | ESD according Machine Model (MM), Q100-003            | ±200                       |     |          | V    |
| ESD_CDM        | ESD according Charged Device Model (CDM), Q100-011    | ±500<br>±750 (corner pins) |     |          | V    |
| US             | Ultrasonic agitation (cleaning, welding, etc)         | Prohibited                 |     |          |      |

## 2.6 Pin Description

The pinout for SCC2130-D08 is presented in Figure 1, while the pin descriptions can be found in Table 6.

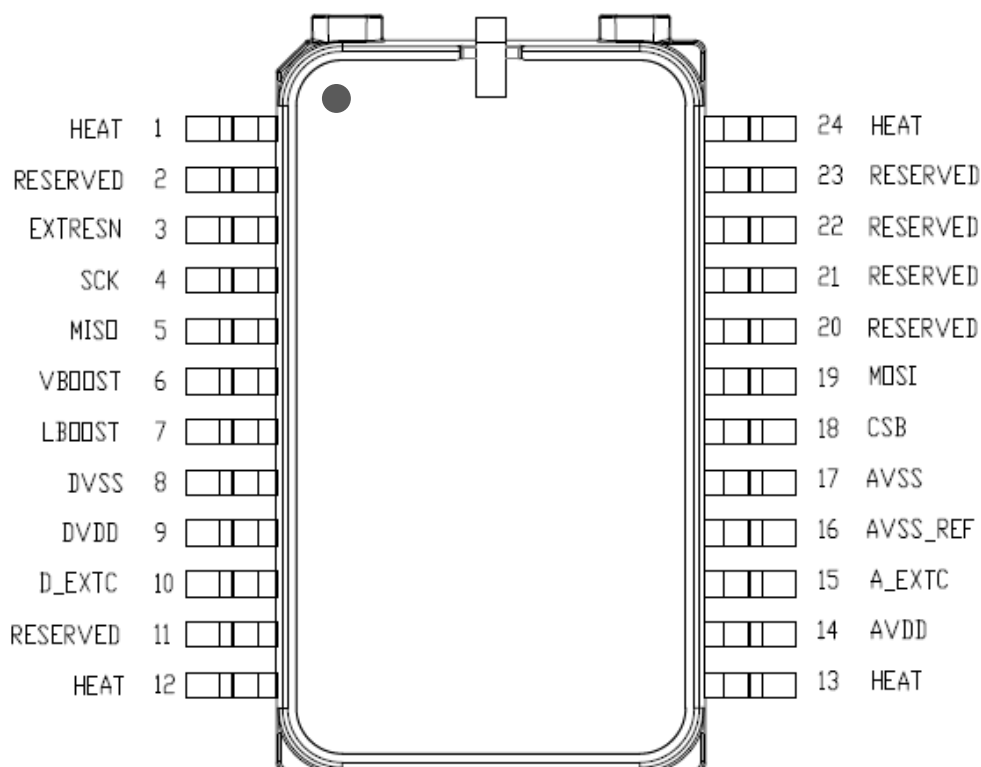


Figure 1. Pinout for SCC2130-D08.



Table 6. SCC2130-D08 pin descriptions.

| Pin#          | Name     | Type    | Description                                                                                                                                          |
|---------------|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 12, 13, 24 | HEAT     | -       | Heat sink connection, connect externally to AVSS                                                                                                     |
| 2, 11         | RESERVED | -       | Factory use only, leave floating                                                                                                                     |
| 3             | EXTRESN  | DIN     | External Reset, 3.3V logic compatible Schmitt-trigger input with internal pull-up, LOW-HIGH transition causes system restart. Minimum low time 100us |
| 4             | SCK      | DIN     | CLK signal of SPI Interface                                                                                                                          |
| 5             | MISO     | DOUT    | Data Out of SPI Interface                                                                                                                            |
| 6             | VBOOST   | AOUT_HV | External capacitor connection for high voltage analog supply, high voltage pad $\approx 30V$                                                         |
| 7             | LBOOST   | AIN_HV  | Connection for inductor for high voltage generation, high voltage pad $\approx 30V$                                                                  |
| 8             | DVSS     | GND     | Digital Supply Return, connect externally to AVSS                                                                                                    |
| 9             | DVDD     | SUPPLY  | Digital Supply Voltage                                                                                                                               |
| 10            | D_EXTC   | AOUT    | External capacitor connection for digital core ( typ. 1.8V)                                                                                          |
| 11            | RESERVED | -       | Factory use only, leave floating                                                                                                                     |
| 14            | AVDD     | SUPPLY  | Analog Supply voltage                                                                                                                                |
| 15            | A_EXTC   | AOUT    | External capacitor connection for positive reference voltage                                                                                         |
| 16            | AVSS_REF | GND     | Analog reference ground, connect externally to AVSS                                                                                                  |
| 17            | AVSS     | GND     | Analog Supply Return, connect externally to DVSS                                                                                                     |
| 18            | CSB      | DIN     | Chip Select of SPI Interface, 3.3V logic compatible Schmitt-trigger input                                                                            |
| 19            | MOSI     | DIN     | Data In of SPI Interface, 3.3V logic compatible Schmitt-trigger input                                                                                |
| 20            | RESERVED | -       | Factory use only, leave floating or connect to GND                                                                                                   |
| 21            | RESERVED | -       | Factory use only, leave floating or connect to GND                                                                                                   |
| 22            | RESERVED | -       | Factory use only, leave floating                                                                                                                     |
| 23            | RESERVED | -       | Factory use only, leave floating                                                                                                                     |

## 2.7 Typical performance characteristics

### 2.7.1 Gyro typical performance characteristics

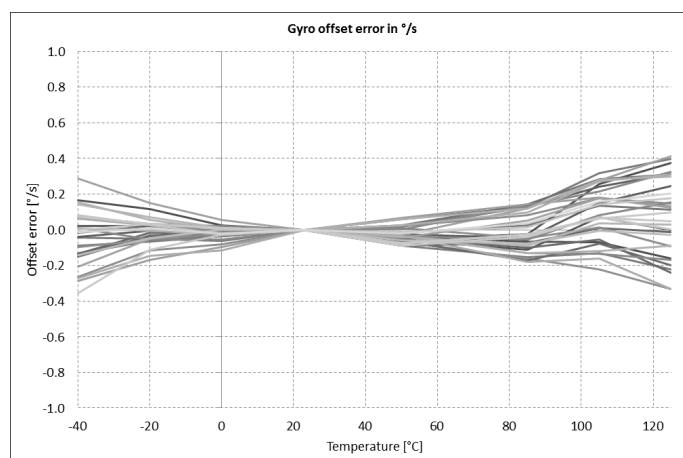


Figure 2. SCC2130-D08 gyro typical output temperature drift in °/s.

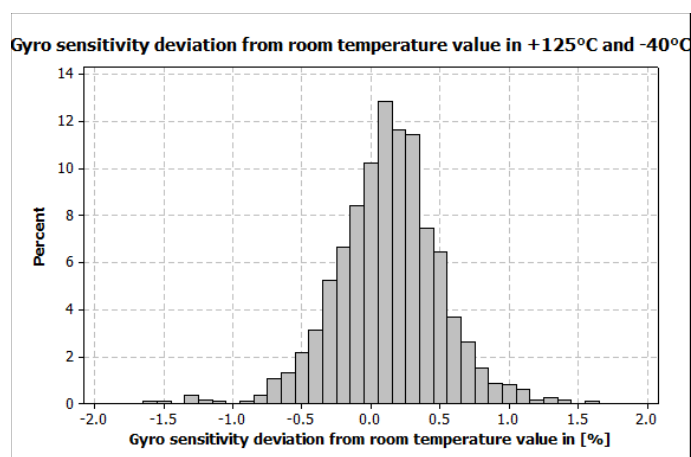


Figure 3. SCC2130-D08 gyro typical sensitivity deviation from room temperature value in %.

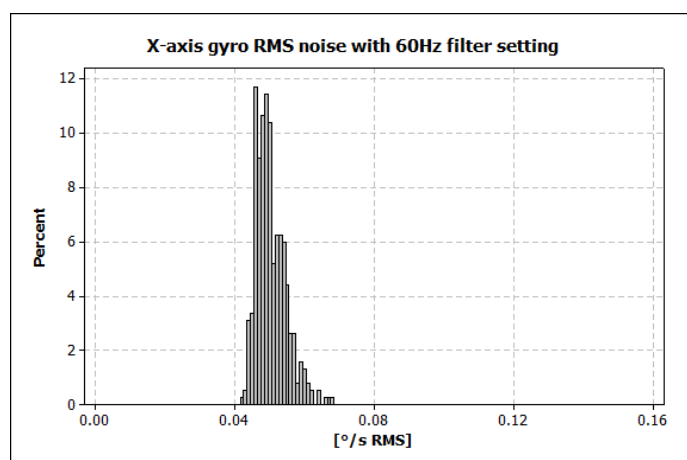


Figure 4. SCC2130-D08 gyro typical RMS noise in °/s<sub>RMS</sub>.

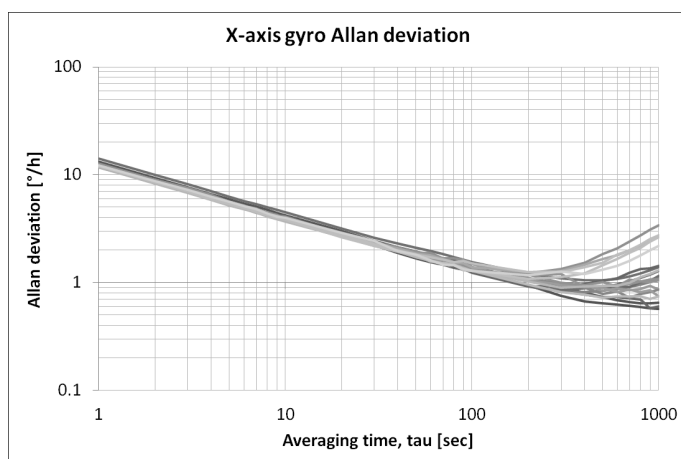


Figure 5. SCC2130-D08 gyro Allan deviation in °/h.

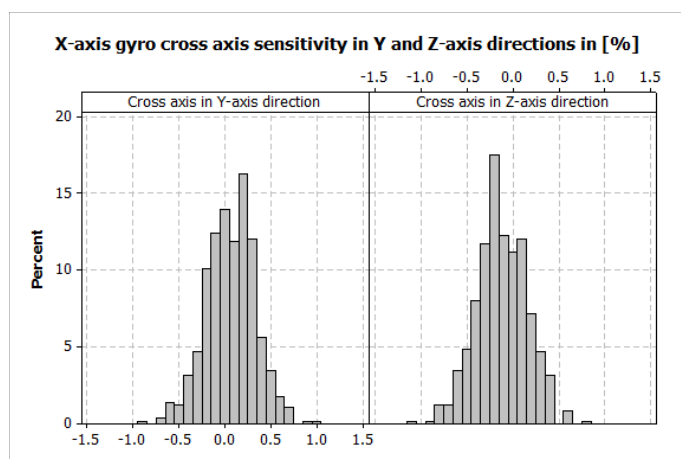


Figure 6. SCC2130-D08 gyro typical cross axis sensitivity in %.

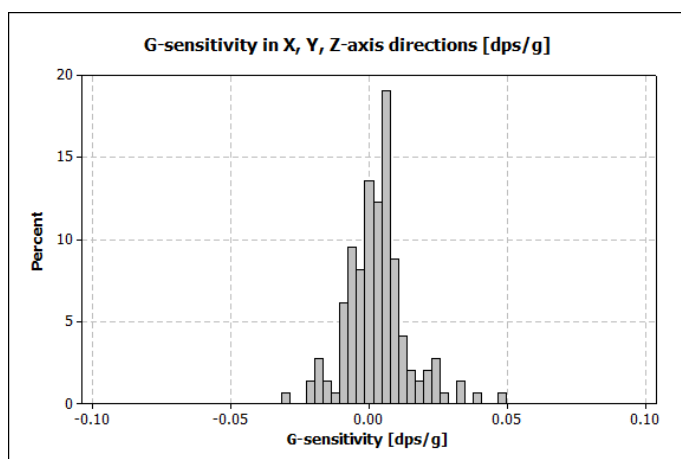


Figure 7. SCC2130-D08 gyro typical G-sensitivity in (°/s)/g.

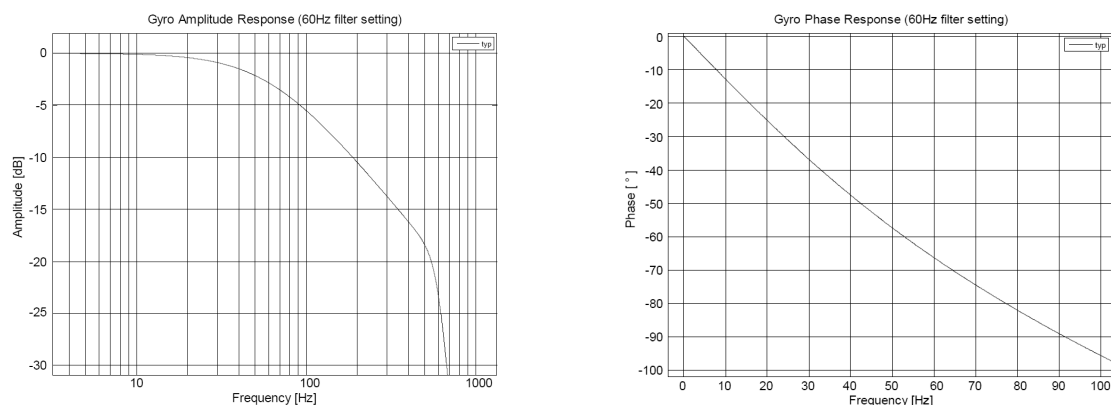


Figure 8. SCC2130-D08 gyro amplitude and phase response with 60Hz filter setting.

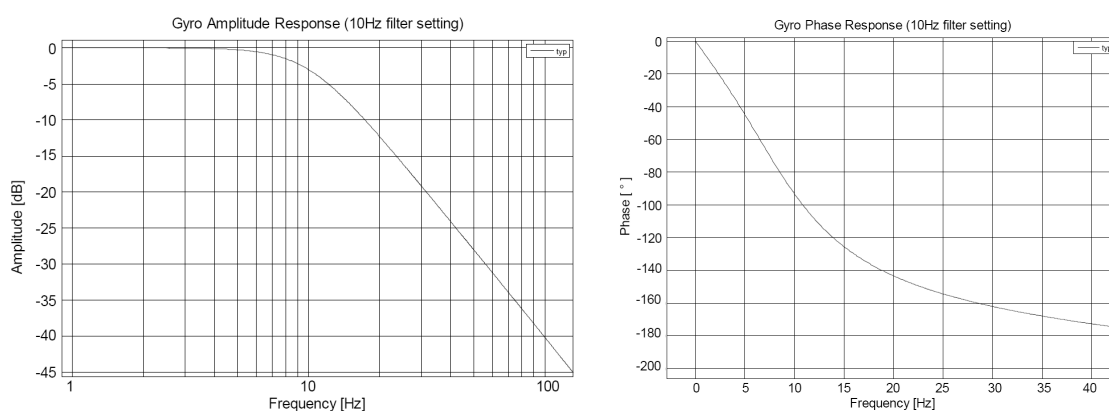


Figure 9. SCC2130-D08 gyro amplitude and phase response with 10Hz filter setting.

## 2.7.2 Accelerometer typical performance characteristics

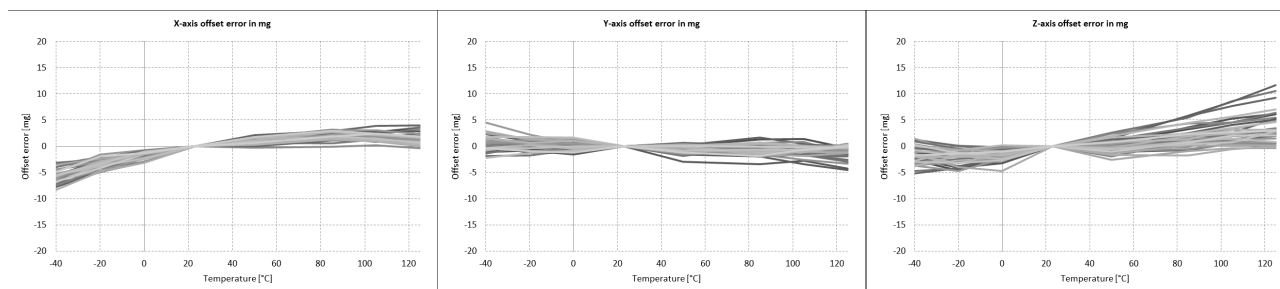


Figure 10. SCC2130-D08 accelerometer typical offset temperature drift mg (X-axis in +1g orientation).

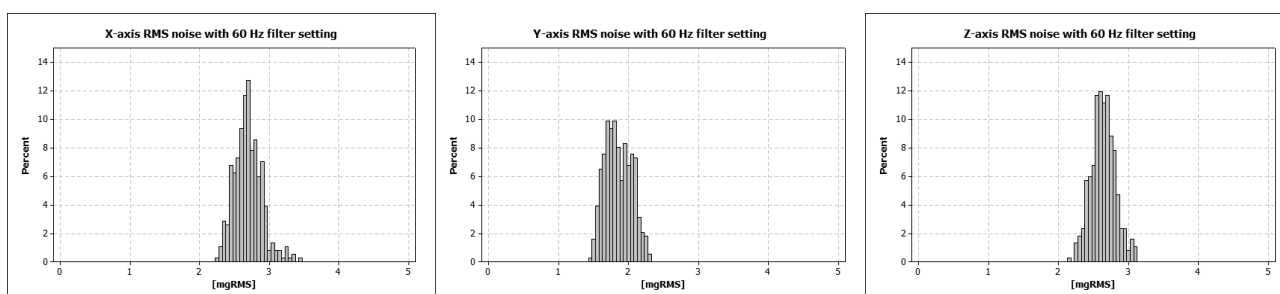


Figure 11. SCC2130-D08 accelerometer typical RMS noise in  $mg_{RMS}$ .

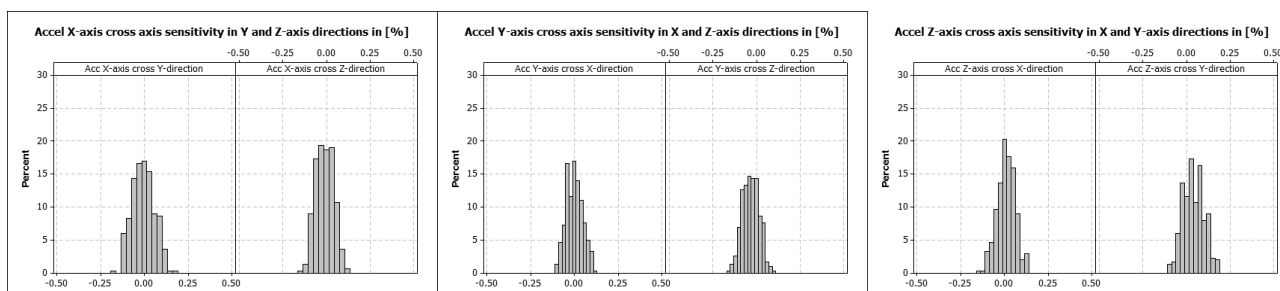


Figure 12. SCC2130-D08 accelerometer typical cross axis sensitivity in %.

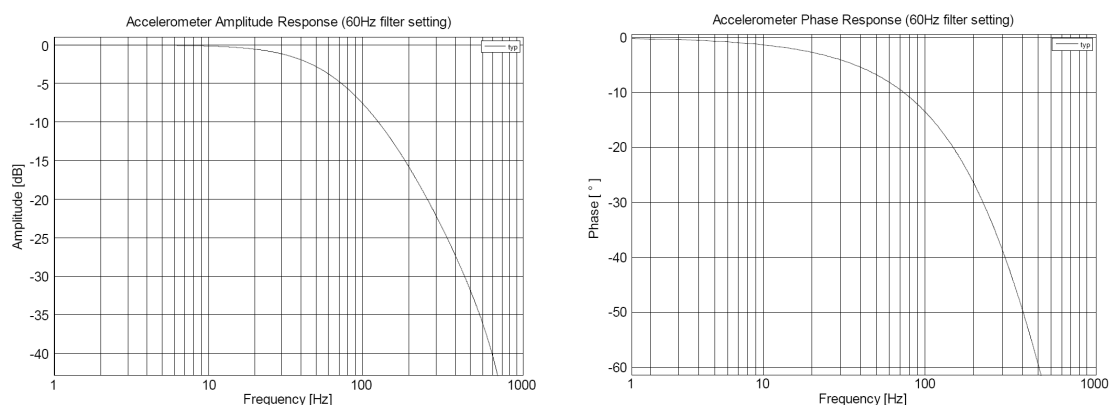


Figure 13. SCC2130-D08 accelerometer amplitude and phase response with 60Hz filter setting.

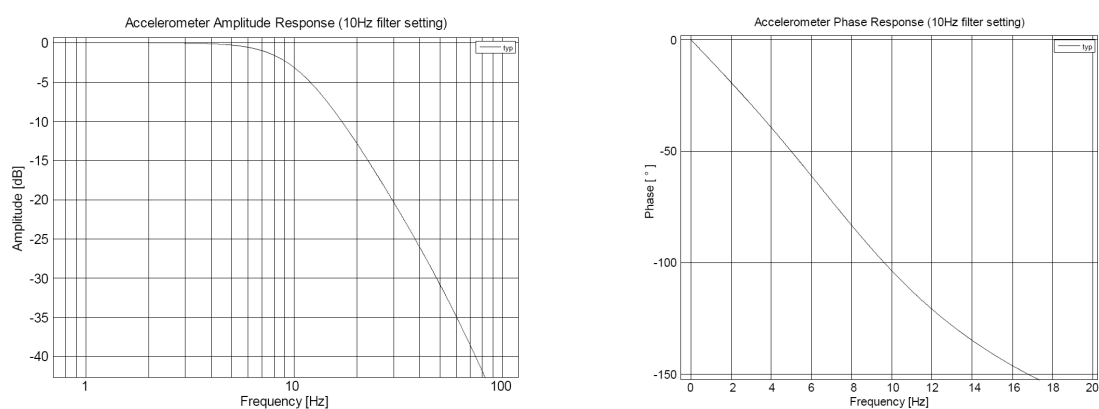


Figure 14. SCC2130-D08 accelerometer amplitude and phase response with 10Hz filter setting.

## 2.8 Digital I/O Specification

Table 7 describes the DC characteristics of SCC2130-D08 sensor SPI I/O pins. Supply voltage is 3.3 V unless otherwise specified. Current flowing into the circuit has a positive value.

Table 7. SPI DC characteristics.

| Symbol                                       | Description                                                                                                                              | Min.     | Nom. | Max.     | Unit |
|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|----------|------|----------|------|
| <b>Serial Clock SCLK</b>                     |                                                                                                                                          |          |      |          |      |
| V <sub>inHigh</sub>                          | Input high voltage                                                                                                                       | 2        |      | DVDD+0.3 | V    |
| V <sub>inLow</sub>                           | Input low voltage                                                                                                                        | -0.3     |      | 0.8      | V    |
| V <sub>hy</sub>                              | Input hysteresis                                                                                                                         | 0.3      |      |          | V    |
| I <sub>leak</sub>                            | Input leakage current, 0V ≤ V <sub>in</sub> ≤ DVDD                                                                                       | -1       |      | 1        | uA   |
| C <sub>in</sub>                              | Input capacitance                                                                                                                        |          |      | 15       | pF   |
| <b>Chip select CSB (Pull Up), low active</b> |                                                                                                                                          |          |      |          |      |
| V <sub>inHigh</sub>                          | Input high voltage                                                                                                                       | 2        |      | DVDD+0.3 | V    |
| V <sub>inLow</sub>                           | Input low voltage                                                                                                                        | -0.3     |      | 0.8      | V    |
| V <sub>hy</sub>                              | Input hysteresis                                                                                                                         | 0.3      |      |          | V    |
| I <sub>source</sub>                          | Input current source (Pull Up), V <sub>in</sub> = 0V                                                                                     | 10       |      | 50       | uA   |
| C <sub>in</sub>                              | Input capacitance                                                                                                                        |          |      | 15       | pF   |
| V <sub>in_open</sub>                         | Open circuit output voltage                                                                                                              | 2        |      |          | V    |
| <b>Serial data input MOSI (Pull Down)</b>    |                                                                                                                                          |          |      |          |      |
| V <sub>inHigh</sub>                          | Input high voltage                                                                                                                       | 2        |      | DVDD+0.3 | V    |
| V <sub>inLow</sub>                           | Input low voltage                                                                                                                        | -0.3     |      | 0.8      | V    |
| V <sub>hy</sub>                              | Input hysteresis                                                                                                                         | 0.3      |      |          | V    |
| I <sub>source</sub>                          | Input current source (Pull Up), V <sub>in</sub> = DVDD                                                                                   | 10       |      | 50       | uA   |
| C <sub>in</sub>                              | Input capacitance                                                                                                                        |          |      | 15       | pF   |
| V <sub>in_open</sub>                         | Open circuit output voltage                                                                                                              |          |      | 0.3      | V    |
| <b>Serial data output MISO (Tri state)</b>   |                                                                                                                                          |          |      |          |      |
| V <sub>outHigh</sub> _ -1mA                  | Output high voltage, I <sub>out</sub> = -1mA                                                                                             | DVDD-0.5 |      |          | V    |
| V <sub>outHigh</sub> _ -50μA                 | Output high voltage, I <sub>out</sub> = -50μA                                                                                            | DVDD-0.2 |      |          | V    |
| V <sub>inHigh</sub> _ 1mA                    | Output low voltage, I <sub>out</sub> = +1mA                                                                                              |          |      | 0.5      | V    |
| V <sub>inHigh</sub> _ 50μA                   | Output low voltage, I <sub>out</sub> = +50μA                                                                                             |          |      | 0.3      | V    |
| I <sub>out_Hz</sub>                          | High impedance output current, 0V < V <sub>MISO</sub> < DVDD                                                                             | -1       |      | 1        | uA   |
| C <sub>ld_miso</sub>                         | Capacitive load. The slope of the MISO output signal may need to be controlled to meet EMI requirements under specified load conditions. |          |      | 200      | pF   |

## 2.9 SPI AC Characteristics

The AC characteristics of SCC2130-D08 are defined in Figure 15 and Table 8.

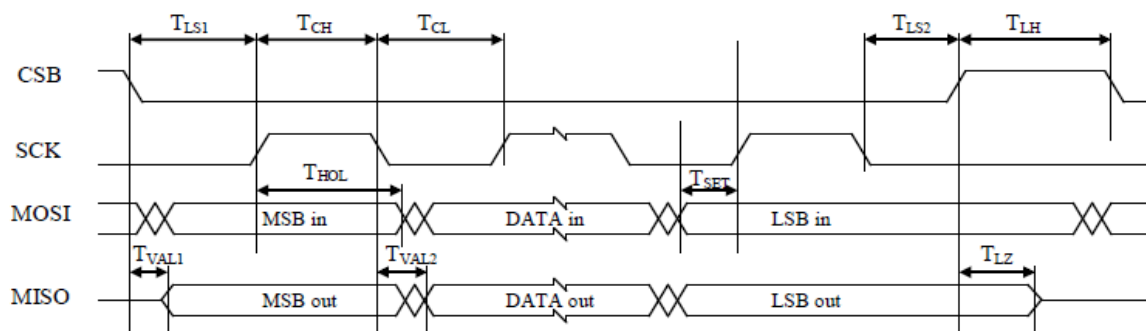


Figure 15. Timing diagram of SPI communication.

Table 8. SPI AC electrical characteristics.

| Symbol     | Description                                                                         | Min. | Nom.        | Max. | Unit |
|------------|-------------------------------------------------------------------------------------|------|-------------|------|------|
| $F_{SPI}$  | It is recommended to use maximum SCK frequency, see section 5.1.7 for more details. | 0.1  |             | 8    | MHz  |
| $T_{SPI}$  |                                                                                     |      | $1/F_{SPI}$ |      |      |
| $T_{CH}$   | High time: duration of logical high level at SCLK                                   | 45   | $T_{SPI}/2$ |      | ns   |
| $T_{CL}$   | Low time: duration of logical low level at SCLK                                     | 45   | $T_{SPI}/2$ |      | ns   |
| $T_{LS1}$  | Setup time CSB: time between the falling edge of CSB and the rising edge of SCLK    | 45   | $T_{SPI}/2$ |      | ns   |
| $T_{VAL1}$ | Delay time: time delay from the falling edge of CSB to data valid at MISO           |      |             | 30   | ns   |
| $T_{SET}$  | Setup time at MOSI: setup time of MOSI before the rising edge of SCLK               | 15   |             |      | ns   |
| $T_{HOL}$  | MOSI data hold time                                                                 | 8    |             |      | ns   |
| $T_{VAL2}$ | Delay time: time delay from falling edge of SCLK to data valid at MISO              |      |             | 30   | ns   |
| $T_{LS2}$  | Hold time of CSB: time between the falling edge of SCLK and the rising edge of CSB  | 45   | $T_{SPI}/2$ |      | ns   |
| $T_{LZ}$   | Tri-state delay time: time between the rising edge of CSB to MISO in Tri-state      |      |             | 15   | ns   |
| $T_{LH}$   | Time between SPI cycles: minimum high time of CSB between two consecutive transfers | 250  |             |      | ns   |



## 2.10 Measurement Axis and Directions

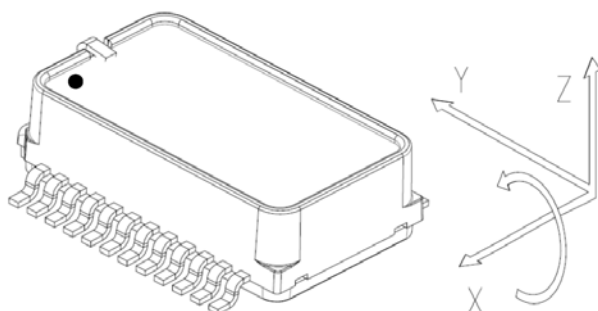


Figure 16. SCC2130-D08 measurement directions.

Table 9. SCC2130-D08 accelerometer measurement directions.

|                                   |                                   |                                   |
|-----------------------------------|-----------------------------------|-----------------------------------|
| <p>x: 0g<br/>y: 0g<br/>z: +1g</p> | <p>x: +1g<br/>y: 0g<br/>z: 0g</p> | <p>x: 0g<br/>y: 0g<br/>z: -1g</p> |
| <p>x: 0g<br/>y: -1g<br/>z: 0g</p> | <p>x: -1g<br/>y: 0g<br/>z: 0g</p> | <p>x: 0g<br/>y: +1g<br/>z: 0g</p> |

## 2.11 Package Characteristics

### 2.11.1 Package Outline Drawing

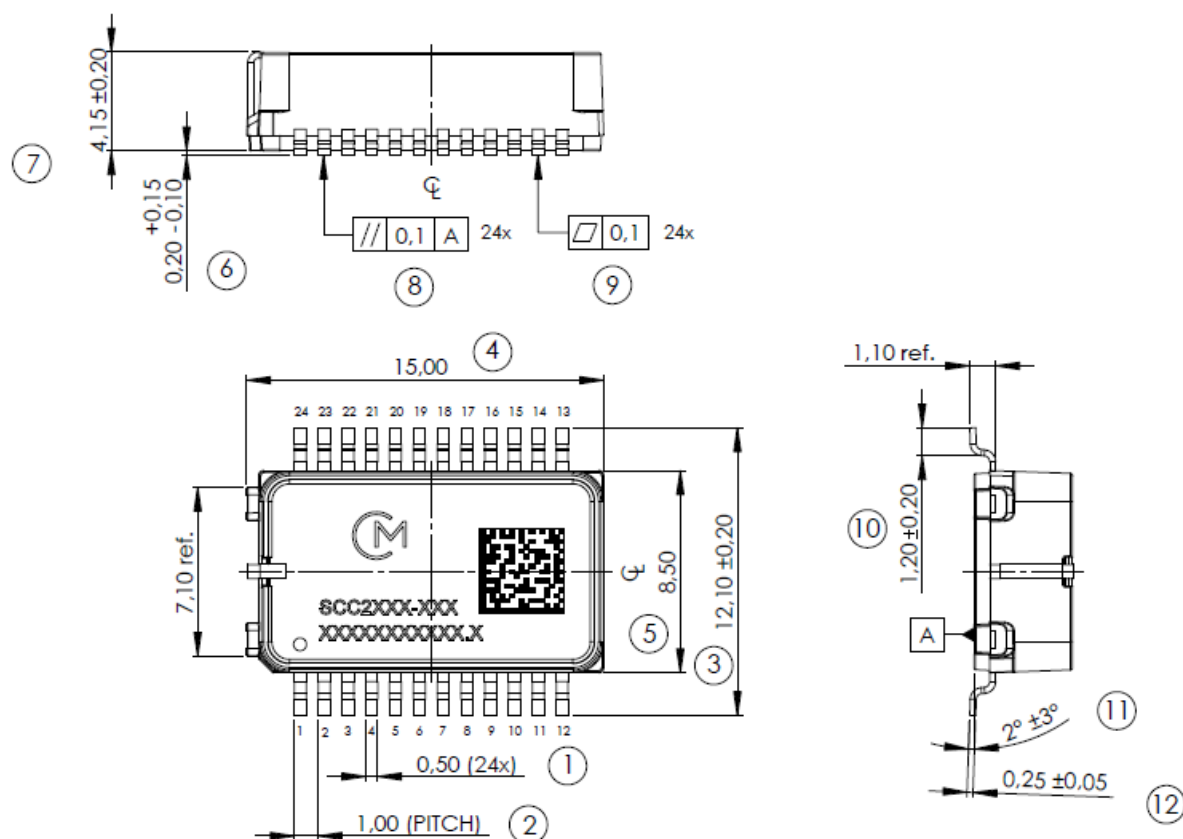


Figure 17. Package outline. The tolerances are according to ISO2768-f (see Table 10).

Table 10. Limits for linear measures (ISO2768-f).

| Tolerance class | Limits in mm for nominal size in mm |              |               |                 |
|-----------------|-------------------------------------|--------------|---------------|-----------------|
|                 | 0.5 to 3                            | Above 3 to 6 | Above 6 to 30 | Above 30 to 120 |
| f (fine)        | ±0.05                               | ±0.05        | ±0.1          | ±0.15           |

## 2.12 PCB Footprint

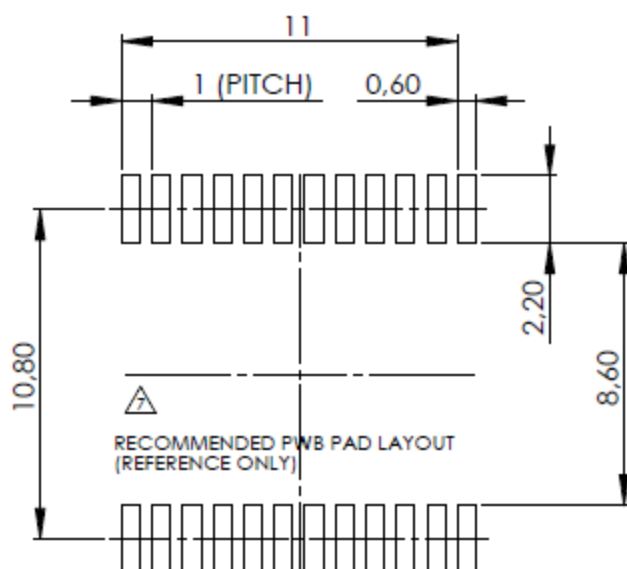


Figure 18. Recommended PWB pad layout for SCC2130-D08. The tolerances are according to ISO2768-f (see Table 10).

## 2.13 Abbreviations

|      |                                         |
|------|-----------------------------------------|
| ASIC | Application Specific Integrated Circuit |
| SPI  | Serial Peripheral Interface             |
| RT   | Room Temperature                        |
| DPS  | Degrees per second                      |
| FS   | Full scale                              |
| CSB  | Chip Select                             |
| SCK  | Serial Clock                            |
| MOSI | Master Out Slave In                     |
| MISO | Master In Slave Out                     |
| MCU  | Microcontroller                         |

### 3 General Product Description

The SCC2130-D08 sensor consists of independent acceleration and angular rate sensing elements, and single Application-Specific Integrated Circuit (ASIC) used to sense and control those elements. Figure 19 contains an upper level block diagram of the component. The ASIC provides one common SPI interface used to control and read the accelerometer and the gyroscope.

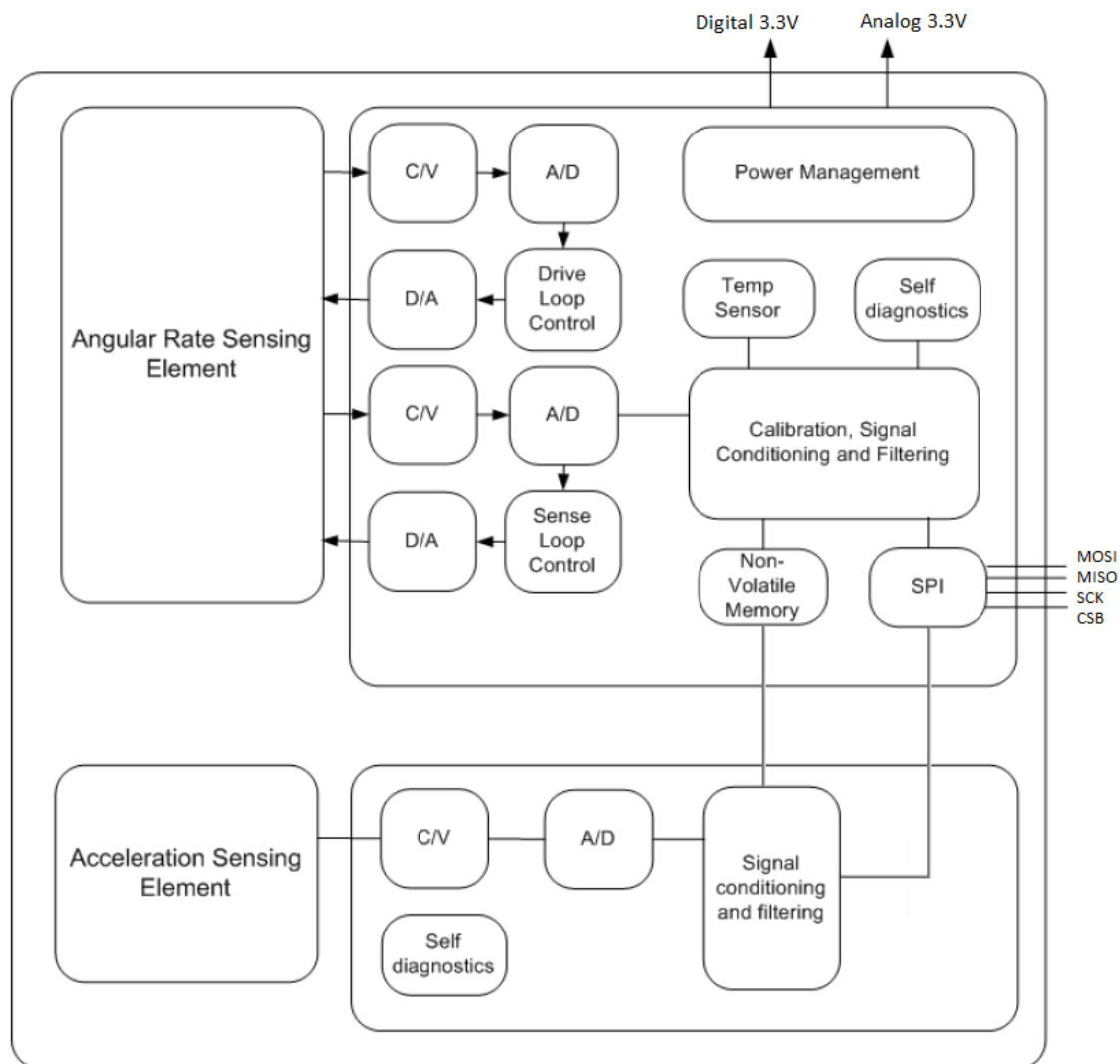


Figure 19. SCC2130-D08 component block diagram.

The angular rate and acceleration sensing elements are manufactured using Murata proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables making robust, extremely stable and low noise capacitive sensors.

The acceleration sensing element consists of four acceleration sensitive masses. Acceleration causes capacitance change that is converted into a voltage change in the signal conditioning ASIC.

The angular rate sensing element consists of moving masses that are purposely excited to in-plane drive motion. Rotation in sensitive direction causes out of plane movement that can be measured as capacitance change with the signal conditioning ASIC.

### 3.1 Factory Calibration

SCC2130-D08 sensors are factory calibrated. No separate calibration is required in the application. Parameters that are trimmed during production include sensitivities, offsets and frequency responses. Calibration parameters are stored to non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during the start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

## 4 Component Operation, Reset and Power Up

### 4.1 Component Operation

Simplified sensor power up sequence is shown in Figure 20 below. The SCC2130-D08 component has internal power-on reset circuit. It releases the internal reset-signal once the power supplies are within the specified range. After the reset, the sensor performs an internal startup sequence. During the startup sequence SCC2130-D08 reads configuration and calibration data from the non-volatile memory to volatile registers. 620ms after the power on or reset, sensor shall be able to provide valid acceleration and angular rate data, separate measurement mode activation is not needed.

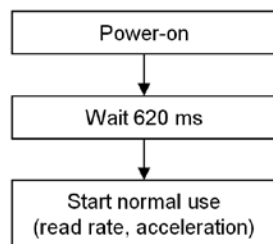


Figure 20. Simplified reset and power up sequence.

Sensor uses 60Hz low pass filter setting by default. In case the optional 10Hz low pass filter is used the filter setting can be set by writing the FLT bits to 01b in Status Summary register. See section 6.2.8 for more information on Status Summary register. Section 5.1.4 shows full SPI write frames for filter settings

SCC2130-D08 component has extensive internal failsafe diagnostics to detect over range and possible internal failures. If the internal failsafe diagnostics are used they should be enabled by clearing the status registers during component power up by following the sequence shown in section 4.2 (Figure 21).

## 4.2 Reset and Power Up Sequence For Enabling Internal Failsafe Diagnostics

Reset and power up sequence for enabling component internal failsafe diagnostics is shown below in Figure 21. After the reset, the sensor performs an internal startup sequence. 20 ms after the reset the SPI bus becomes accessible and the output filter can be set to a desired value. If the filter is not set to a valid value (60Hz or 10Hz setting), the default setting (00b = 60Hz) is used and the S\_OK\_C flag in Status Summary Register will indicate a failure. In 750ms (10Hz filter setting) or in 620ms (60Hz filter selection) the accelerometer and the gyro shall be able to deliver valid data.

During the startup sequence the sensor performs a series of internal tests that will set various error flags in the sensor status registers and to clear them it is necessary to read all status registers after the startup sequence is complete.

Once startup sequence is completed, the SPI frame Return Status bits (RS bits) indicate sensor operation status. Normal operation is indicated with RS bit content of 01b. In case the LOOPF\_OK bit in Common Status register is failing, the sensor should be reset and re-started.

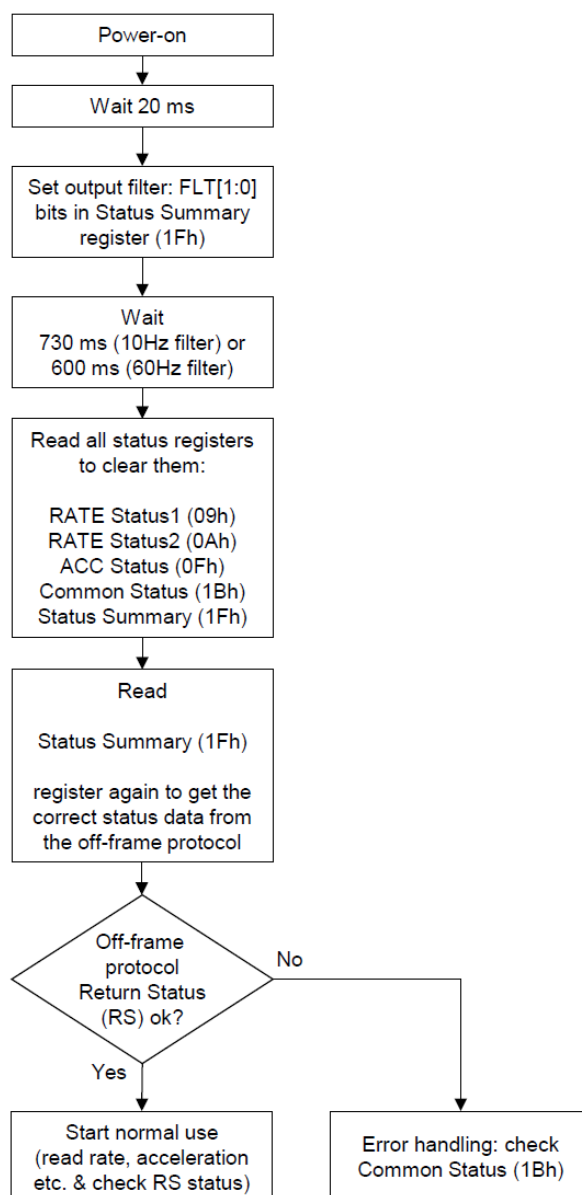


Figure 21. Reset and power up sequence for enabling internal failsafe diagnostics.

## 5 Component Interfacing

### 5.1 SPI Interface

#### 5.1.1 General

The SCC2130-D08 has one common SPI interface for the accelerometer and the angular rate sensor. SPI communication transfers data between the SPI master and registers of the SCC2130-D08 ASIC. The SCC2130-D08 always operates as a slave device in master-slave operation mode. 3-wire SPI connection cannot be used.

**SPI interface pins:**

|      |                          |            |
|------|--------------------------|------------|
| CSB  | Chip Select (active low) | MCU → ASIC |
| SCK  | Serial Clock             | MCU → ASIC |
| MOSI | Master Out Slave In      | MCU → ASIC |
| MISO | Master In Slave Out      | ASIC → MCU |

#### 5.1.2 Protocol

SPI communication uses off-frame protocol so each transfer has two phases.

The first phase contains the SPI command (Request) and the data (Response) of the previous command. The second phase contains the next Request and the Response to the Request of the first phase, see Figure 22.

Data word length is 32 bits, the data is transferred MSB first. The first response after reset is undefined and shall be discarded.

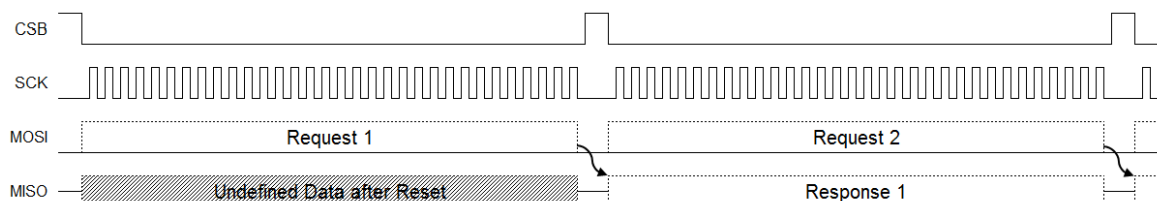


Figure 22. SPI protocol example.

The interleaved Request - Response cycle then continues as shown in Figure 23.

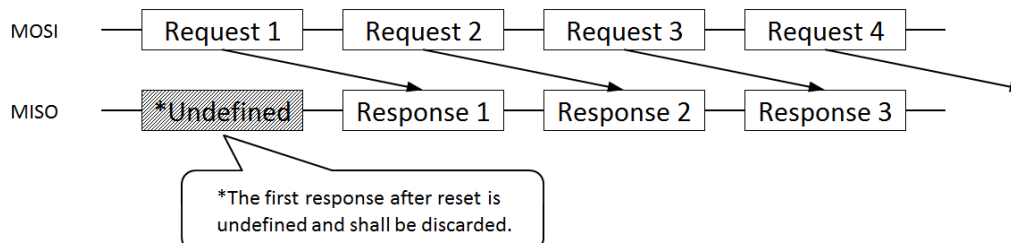


Figure 23. Request – Response frame relationship.



The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge. The data is captured on the SCK's rising edge (MOSI line) and it is propagated on the SCK's falling edge (MISO line). This equals to SPI Mode 0 (CPOL = 0 and CPHA = 0), see Figure 24.

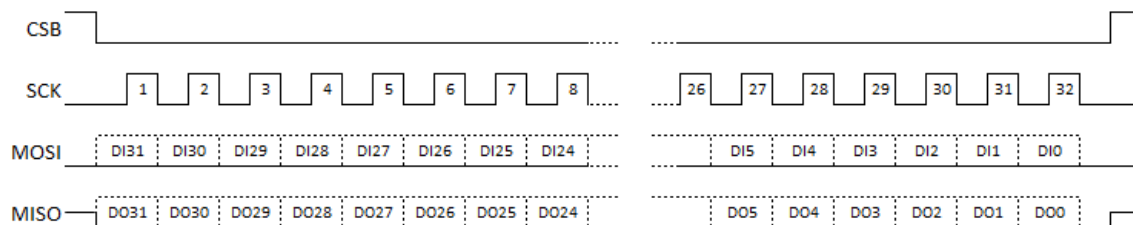


Figure 24. SPI Frame Format.

### 5.1.3 General Instruction format

The SPI frame is divided into four parts (See Figure 25 and Table 11):

1. Operation Code (OP)
2. Return status (RS, in MISO)
3. Data (DI, DO)
4. Checksum (CRC)

Unused bits shall be set to 0, this is important for the checksum calculation.

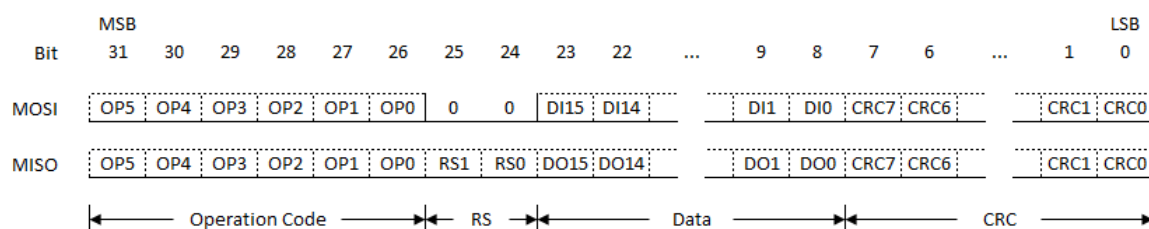


Figure 25. SPI instruction format.

Table 11. SPI bit definitions.

| Bits    | Name           | MOSI                                                                                | MISO                                                                                |
|---------|----------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| OP[5:0] | Operation code | Requested operation:<br>• OP5: Write = 1 / Read = 0<br>• OP[4:0] = Register address | Performed operation:<br>• OP5: Write = 1 / Read = 0<br>• OP[4:0] = Register address |
| RS[1:0] | Return status  | n.a.                                                                                | Sensor status                                                                       |
| D[15:0] | Data           | Data to be written                                                                  | Return data                                                                         |
| CR[7:0] | Checksum       | Checksum of MOSI bits [31:8]                                                        | Checksum of MISO bits [31:8]                                                        |

## 5.1.4 Operations

Table 12. Operations and their equivalent SPI frames.

| Operation                                   | Register             | SPI Frame Binary (OP, RS, Data, CRC) | SPI Frame Hex |
|---------------------------------------------|----------------------|--------------------------------------|---------------|
| Read RATE                                   | RATE (01h)           | 000001 00 0000000000000000 11110111  | 040000F7h     |
| Read ACC_X                                  | ACC_X (04h)          | 000100 00 0000000000000000 11110101  | 100000E9h     |
| Read ACC_Y                                  | ACC_Y (05h)          | 000101 00 0000000000000000 11110111  | 140000EFh     |
| Read ACC_Z                                  | ACC_Z (06h)          | 000110 00 0000000000000000 11110101  | 180000E5h     |
| Read TEMP                                   | TEMP (07h)           | 000111 00 0000000000000000 11110011  | 1C0000E3h     |
| Read RATE Status 1                          | RATE Status 1 (09h)  | 001001 00 0000000000000000 11100111  | 240000C7h     |
| Read RATE Status 2                          | RATE Status 2 (0Ah)  | 001010 00 0000000000000000 11101101  | 280000CDh     |
| Read ACC Status                             | ACC Status (15h)     | 001111 00 0000000000000000 11101011  | 3C0000D3h     |
| Write ResetControl HardReset                | ResetControl (16h)   | 110110 00 0000000000000100 00110001  | D8000431h     |
| Write ResetControl MonitorST                | ResetControl (16h)   | 110110 00 0000000000001000 10101101  | D80008ADh     |
| Read Serial ID0                             | Serial ID0 (18h)     | 011000 00 0000000000000000 10100001  | 600000A1h     |
| Read Serial ID1                             | Serial ID0 (19h)     | 011001 00 0000000000000000 10100111  | 640000A7h     |
| Read Common Status                          | Common Status (1Bh)  | 011011 00 0000000000000000 10101011  | 6C0000ABh     |
| Read Status Summary                         | Status Summary (1Fh) | 011111 00 0000000000000000 10110011  | 7C0000B3h     |
| Write Flt[1:0] =10b: set 60Hz filter active | Status Summary (1Fh) | 111111 00 0010000000000000 00000110  | FC200006h     |
| Write Flt[1:0] =01b: set 10Hz filter active | Status Summary (1Fh) | 111111 00 0001000000000000 11000111  | FC1000C7h     |

## 5.1.5 Return Status

SPI frame Return Status bits (RS bits) indicate the functional status of the sensor, see Return Status definitions in Table 13.

Table 13. Return Status definitions.

| RS[1] | RS[0] | Description                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | 0     | Initialization running                                                                                                                                                                                                                                                                                                                                     |
| 0     | 1     | Normal operation of selected channel                                                                                                                                                                                                                                                                                                                       |
| 1     | 0     | Selftest of selected channel                                                                                                                                                                                                                                                                                                                               |
| 1     | 1     | Reserved or not existing register addressed, error of selected channel or common failure (see Status Summary Register bits S_OK_C, S_OK_R, S_OK_A) <ul style="list-style-type: none"> <li>S_OK_C is the summary of Common Status</li> <li>S_OK_R is the summary of RATE Status 1 and RATE Status 2</li> <li>S_OK_A is the summary of ACC Status</li> </ul> |

The priority of the return status states is from high to low: 10 → 00 → 11 → 01.

## 5.1.6 Checksum (CRC)

For SPI transmission error detection a Cyclic Redundancy Check (CRC) is implemented, for details see Table 14.

Table 14. SPI CRC definition.

| Parameter | Value                                         |
|-----------|-----------------------------------------------|
| Name      | CRC-8                                         |
| Width     | 8 bit                                         |
| Poly      | 1Dh (generator polynom: $X^8+X^4+X^3+X^2+1$ ) |
| Init      | FFh (initialization value)                    |
| XOR out   | FFh (inversion of CRC result)                 |

The CRC register has to be initialized with FFh to ensure a CRC failure in case of stuck-at-0 and stuck-at-1 error on the SPI bus. C-programming language example for CRC calculation is presented in Figure 26. It can be used as is in an appropriate programming context.

```
// Calculate CRC for 24 MSB's of the 32 bit dword
// (8 LSB's are the CRC field and are not included in CRC calculation)
uint8_t CalculateCRC(uint32_t Data)
{
    uint8_t BitIndex;
    uint8_t BitValue;
    uint8_t CRC;

    CRC = 0xFF;
    for (BitIndex = 31; BitIndex > 7; BitIndex--)
    {
        BitValue = (uint8_t)((Data >> BitIndex) & 0x01);
        CRC = CRC8(BitValue, CRC);
    }
    CRC = (uint8_t)~CRC;
    return CRC;
}

static uint8_t CRC8(uint8_t BitValue, uint8_t CRC)
{
    uint8_t Temp;

    Temp = (uint8_t)(CRC & 0x80);
    if (BitValue == 0x01)
    {
        Temp ^= 0x80;
    }
    CRC <<= 1;
    if (Temp > 0)
    {
        CRC ^= 0x1D;
    }
    return CRC;
}
```

Figure 26. C-programming language example for CRC calculation.

### CRC calculation example:

Read RATE register (01h) -> SPI[31:8] = 040000h -> CRC [7:0] -> F7h.  
 Further examples can be found in Table 12.

### **5.1.7 Recommendation for the SPI interface implementation**

SPI communication may interfere with the measured angular rate signal due to sensor internal capacitive coupling. If the harmonic overtones of the SPI communication activity are close to gyro operational frequency, the SPI cross talk can be seen as increased noise level in angular rate signal.

Cross talk can be eliminated by choosing the output data rate (sample rate) in a suitable way, i.e. avoiding the overtones on the gyro operation frequency. For optimum performance it is recommended that 2.3kHz or 3.2kHz output data rate is used with maximum serial clock (SCK) frequency (8MHz). The design performance should be verified carefully.

## 6 Register Definition

### 6.1 Sensor Data Block

Table 15. Sensor data block.

| Addr<br>OP[4:0] | Bits   | Register Name | No. of<br>Bits | Read/<br>Write | Description                                                                                              |
|-----------------|--------|---------------|----------------|----------------|----------------------------------------------------------------------------------------------------------|
| 01h             | [15:0] | RATE          | 16             | R              | Rate output in 2's complement format                                                                     |
| 04h             | [15:0] | ACC_X         | 16             | R              | X-axis acceleration output in 2's complement format                                                      |
| 05h             | [15:0] | ACC_Y         | 16             | R              | Y-axis acceleration output in 2's complement format                                                      |
| 06h             | [15:0] | ACC_Z         | 16             | R              | Z-axis acceleration output in 2's complement format                                                      |
| 07h             | [16:0] | TEMP          | 16             | R              | Temperature sensor output in 2's complement format. See section 2.4 for temperature conversion equation. |

SPI read frames with CRC content for these registers are shown in Table 12.

#### 6.1.1 Example of Angular Rate Data Conversion

For example, if RATE register read results: RATE = **05FFE08Bh**, the register content is converted to angular rate as follows:

- 05h = 000001 01b
  - o 000001b = operation code = Read RATE
  - o 01b = return status (RS bits) = no error
- FFE0h = 1111 1111 1110 0000b = RATE register content
  - o FFE0h in 2's complement format = -32d
  - o Angular rate = -32LSB / sensitivity = -32LSB / (50LSB/(°/s)) = -0.64°/s
- 8Bh = CRC of 05FFE0h

#### 6.1.2 Example of Acceleration Data Conversion

For example, if ACC\_X register read results: ACC\_X = **1100DC02h**, the register content is converted to acceleration rate as follows:

- 11h = 000100 01b
  - o 000100b = operation code = Read ACC\_X
  - o 01b = return status (RS bits) = no error
- 00DCh = bin 0000 0000 1101 1100b = ACC\_X register content
  - o 00DCh in 2's complement format = 220d
  - o Acceleration = 220LSB / sensitivity = 220LSB / (1962LSB/g) = 0.112g
- 02h = CRC of 1100DCh

#### 6.1.3 Example of Temperature Data Conversion

For example, if TEMP register read results: TEMP = **1DFE6F4Eh**, the register content is converted to temperature as follows:

- 1Dh = bin 000111 01b
  - o bin 000111b = operation code = Read TEMP
  - o 01 = return status (RS bits) = no error
- FE6Fh = bin 1111 1110 0110 1111 = TEMP register content
  - o FE6Fh in 2's complement format = -401d
  - o Temperature =  $60 + (\text{TEMP} / 14.7) = 60 + [-401/14.7] = +32.7^{\circ}\text{C}$
  - o See section 2.4 for temperature conversion equation
- 4Eh = CRC of 1DFE6Fh

## 6.2 Sensor Status Block

Table 16. Sensor status block.

| Addr<br>OP[4:0] | Bits   | Register Name  | No. of<br>Bits | Read/<br>Write | Description                                    |
|-----------------|--------|----------------|----------------|----------------|------------------------------------------------|
| 09h             | [15:0] | RATE Status 1  | 16             | R              | Gyro sensor status                             |
| 0Ah             | [15:0] | RATE Status 2  | 16             | R              | Gyro sensor status                             |
| 0Fh             | [15:0] | ACC Status     | 16             | R              | Accelerometer status                           |
| 15h             | [15:0] | Test           | 16             | R/W            | R/W register for SPI communication checking    |
| 16h             | [15:0] | ResetControl   | 16             | R/W            | Reset status and trigger bits                  |
| 18h             | [15:0] | Serial ID0     | 16             | R              | Component serial number least significant bits |
| 19h             | [15:0] | Serial ID1     | 16             | R              | Component serial number most significant bits  |
| 1Bh             | [15:0] | Common Status  | 16             | R              | Status of common blocks                        |
| 1Dh             | [15:0] | Identification | 16             | R              | Product type Identification                    |
| 1Fh             | [15:0] | Status Summary | 16             | R/W            | Status overview                                |

Note:

R/W for the register means, that the content of the register can be read, and that it is also possible to over write the content of the register in normal mode operation. The following signal blocks will then operate with the value written to the register. After a write cycle to the register, the register will keep its value until another write cycle or reset occurs.

SPI read and write frames with CRC content for these registers are shown in Table 12.

## 6.2.1 RATE Status 1 Register (09h)

Table 17. RATE Status 1 register.

| D15     | D14       | D13           | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5       | D4        | D3         | D2           | D1            | D0      | Bit   |
|---------|-----------|---------------|-----|-----|-----|----|----|----|----|----------|-----------|------------|--------------|---------------|---------|-------|
| -       | -         | -             |     |     |     |    |    |    |    | -        | -         | -          | -            | -             | -       | Write |
| VCMF_OK | Vboost_OK | Reserved[7:0] |     |     |     |    |    |    |    | SDM_D_OK | dQ_Amp_OK | dDR_Amp_OK | Q_AmpCtrl_OK | DR_AmpCtrl_OK | OF_R_OK | Read  |

RATE Status 1 register indicates saturation or failure in gyroscope. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 18. RATE Status 1 register bit description.

| Register Bit  | Description                                                       |
|---------------|-------------------------------------------------------------------|
| OF_R_OK       | This bit indicates signal path saturation and overflow conditions |
| DR_AmpCtrl_OK | Status of drive amplitude control                                 |
| Q_AmpCtrl_OK  | Status of compensation signal amplitude control                   |
| dDR_Amp_OK    | Status of drive amplitude                                         |
| dQ_Amp_OK     | Status of compensation signal amplitude                           |
| SDM_D_OK      | Status of drive path stability                                    |
| VBoost_OK     | Status of VBoost voltage                                          |
| VCMF_OK       | Status of biasing voltage                                         |

## 6.2.2 RATE Status 2 Register (0Ah)

Table 19. RATE Status 2 register.

| D15           | D14 | D13 | D12 | D11 | D10 | D9 | D8        | D7     | D6     | D5     | D4     | D3      | D2      | D1      | D0      | Bit   |
|---------------|-----|-----|-----|-----|-----|----|-----------|--------|--------|--------|--------|---------|---------|---------|---------|-------|
| -             |     |     |     |     |     |    | -         | -      | -      | -      | -      | -       | -       | -       | -       | Write |
| Reserved[6:0] |     |     |     |     |     |    | S_P_Pk_OK | S_N_OK | S_P_OK | D_N_OK | D_P_OK | SI_N_OK | SI_P_OK | DI_N_OK | DI_P_OK | Read  |

RATE Status 2 register indicates saturation or failure in gyroscope. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 20. RATE Status 2 register bit description.

| Register Bit | Description                               |
|--------------|-------------------------------------------|
| DI_P_OK      | Indicates saturation or failure condition |
| DI_N_OK      | Indicates saturation or failure condition |
| SI_P_OK      | Indicates saturation or failure condition |
| SI_N_OK      | Indicates saturation or failure condition |
| D_P_OK       | Indicates saturation or failure condition |
| D_N_OK       | Indicates saturation or failure condition |
| S_P_OK       | Indicates saturation or failure condition |
| S_N_OK       | Indicates saturation or failure condition |
| S_P_Pk_OK    | Indicates saturation or failure condition |

### 6.2.3 ACC Status Register (0Fh)

Table 21. ACC Status register.

| D15           | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6          | D5            | D4        | D3         | D2     | D1     | D0 | Bit   |
|---------------|-----|-----|-----|-----|-----|----|----|----|-------------|---------------|-----------|------------|--------|--------|----|-------|
| -             |     |     |     |     |     |    |    |    | -           | -             | -         | -          | -      | -      | -  | Write |
| Reserved[8:0] |     |     |     |     |     |    |    |    | C2V_VREF_OK | Reserved[2:0] | OF_ACC_OK | ADC_SAT_OK | SAT_OK | STC_OK |    | Read  |

ACC Status register indicates saturation or failure in accelerometer. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 22. ACC Status register bit description.

| Register Bit | Description                               |
|--------------|-------------------------------------------|
| STC_OK       | Indicates saturation or failure condition |
| SAT_OK       | Indicates saturation or failure condition |
| ADC_SAT_OK   | Indicates saturation or failure condition |
| OF_ACC_OK    | Indicates saturation or failure condition |
| C2V_VREF_OK  | Status of reference voltage               |



## 6.2.4 Reset Control Register (16h)

Table 23. Reset Control register.

| D15            | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3        | D2        | D1            | D0 | Bit   |
|----------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----------|-----------|---------------|----|-------|
| Reserved[11:0] |     |     |     |     |     |    |    |    |    |    |    | MonitorST | HardReset | Reserved[1:0] |    | Write |
|                |     |     |     |     |     |    |    |    |    |    |    | -         | -         |               |    | Read  |

Table 24. Reset Control register bit description.

| Register Bit | Description                                                                                                                    |
|--------------|--------------------------------------------------------------------------------------------------------------------------------|
| HardReset    | Writing this bit to 1 generates an EXTRESN compatible signal. Thus it is possible to generate hardware reset via SPI interface |
| MonitorST    | Writing this bit to 1 initiates self test of internal monitoring circuit                                                       |

## 6.2.5 Serial ID0 and Serial ID1 Registers (18h and 19h)

SCC2130-D08 serial number is laser marked on top of component lid and stored in to Serial ID0 and Serial ID1 registers. Serial number is in 32bit unsigned integer format. Serial number register bit descriptions are shown below in Table 25 and Table 26.

Table 25. Serial ID0 (18h) register (serial number LSB word).

| D15       | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Bit   |
|-----------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-------|
| -         | -   | -   | -   | -   | -   | -  | -  | -  | -  | -  | -  | -  | -  | -  | -  | Write |
| ID0[15:0] |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    | Read  |

Table 26. Serial ID1 (19h) register (serial number MSB word).

| D15       | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Bit   |
|-----------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-------|
| -         | -   | -   | -   | -   | -   | -  | -  | -  | -  | -  | -  | -  | -  | -  | -  | Write |
| ID1[15:0] |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    | Read  |

Example serial number conversion shown below:

- Serial ID0 register content: 8612h = bin 1000 0110 0001 0010
- Serial ID1 register content: 8FB9h = bin 1000 0110 0001 0010
- Full serial number: 8FB9 8612h = 2411300370
- Serial number laser marked on lid is 2411300370SCC

## 6.2.6 Common Status Register (1Bh)

Table 27. Common Status register.

| D15      | D14         | D13        | D12        | D11     | D10           | D9 | D8 | D7 | D6       | D5          | D4           | D3       | D2      | D1           | D0      | Bit   |
|----------|-------------|------------|------------|---------|---------------|----|----|----|----------|-------------|--------------|----------|---------|--------------|---------|-------|
| -        | -           | -          | -          | -       | -             | -  | -  | -  | -        | -           | -            | -        | -       | -            | -       | Write |
| NMode_OK | MonCheck_OK | CRC_OTP_OK | CRC_SPI_OK | OF_C_OK | StateMon[3:0] |    |    |    | LOOPF_OK | TEMP_Mon_OK | VBG2_0P9V_OK | Reserved | VDDD_OK | VBG1_0P9V_OK | DVDD_OK | Read  |

Common Status register indicates failure in common signals/blocks. Failure is indicated by setting OK flag to 0, the condition will be latched until a read cycle on the register.

Table 28. Common Status register bit description.

| Register Bit  | Description                                                                                        |
|---------------|----------------------------------------------------------------------------------------------------|
| DVDD_OK       | Status of DVDD digital 3.3V supply voltage                                                         |
| VBG1_0P9V_OK  | Status of internal reference voltage                                                               |
| VDDD_OK       | Status of digital core supply voltage                                                              |
| VBG2_0P9V_OK  | Status of internal reference voltage                                                               |
| TEMP_Mon_OK   | Status of temperature sensor signal                                                                |
| LOOPF_OK      | Status of loop filter                                                                              |
| StateMon[3:0] | Status of state machine for self test of monitoring circuit.                                       |
| OF_C_OK       | This bit indicates signal path saturation and overflow conditions related to common signals/blocks |
| CRC_SPI_OK    | This bit indicates CRC failure in SPI communication                                                |
| CRC_OTP_OK    | This bit indicates CRC failure in OTP memory                                                       |
| MonCheck_OK   | Result of the monitoring circuit self test                                                         |
| NMode_OK      | Bit = 0 : ASIC test mode activated<br>Bit = 1 : ASIC is in normal mode                             |

## 6.2.7 Identification Register (1Dh)

Table 29. Identification register.

| D15                  | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Bit   |
|----------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|-------|
| -                    | -   | -   | -   | -   | -   | -  | -  | -  | -  | -  | -  | -  | -  | -  | -  | Write |
| Identification[15:0] |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    | Read  |

Table 30. Identification register bit description.

| Register Bit   | Description                                                    |
|----------------|----------------------------------------------------------------|
| Identification | Default value: 001Dh (bin 0000 0000 0001 1101) for SCC2130-D08 |

## 6.2.8 Status Summary Register (1Fh)

Table 31. Status Summary register.

| D15    | D14         | D13      | D12 | D11           | D10 | D9 | D8 | D7     | D6            | D5     | D4            | D3     | D2 | D1 | D0 | Bit   |
|--------|-------------|----------|-----|---------------|-----|----|----|--------|---------------|--------|---------------|--------|----|----|----|-------|
| -      | -           | Flt[1:0] |     | -             |     |    |    | -      | -             | -      | -             | -      | -  | -  | -  | Write |
| STC_EN | SelfTestDis |          |     | Reserved[5:0] |     |    |    | S_OK_C | Reserved[1:0] | S_OK_A | Reserved[1:0] | S_OK_R |    |    |    | Read  |

Table 32. Identification register bit description.

| Register Bit | Description                                                                                                                                                                                                                                                               |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S_OK_R       | Sensor status summary flag for gyro                                                                                                                                                                                                                                       |
| S_OK_A       | Sensor status summary flag for accelerometer                                                                                                                                                                                                                              |
| S_OK_C       | Status summary flag for common blocks and functionalities                                                                                                                                                                                                                 |
| Flt[1:0]     | Output Filter Selection:<br>00b: 60Hz filter active for ACC and GYRO signal (default after reset),<br>with Flt default setting S_OK_C is set to 0<br>01b: 10Hz filter active for ACC and GYRO signals<br>10b: 60Hz filter active for ACC and GYRO signal<br>11b: Reserved |
| SelfTestDis  | SelfTestDis='1' indicates that the self test of the monitoring circuit is disabled.                                                                                                                                                                                       |
| STC_EN       | STC_EN='1' indicates that the accelerometer self test is enabled.                                                                                                                                                                                                         |

## 7 Application information

### 7.1 Application Circuitry and External Component Characteristics

See Figure 27 and Table 33 for specification of the external components. The PCB layout example is shown in Figure 28.

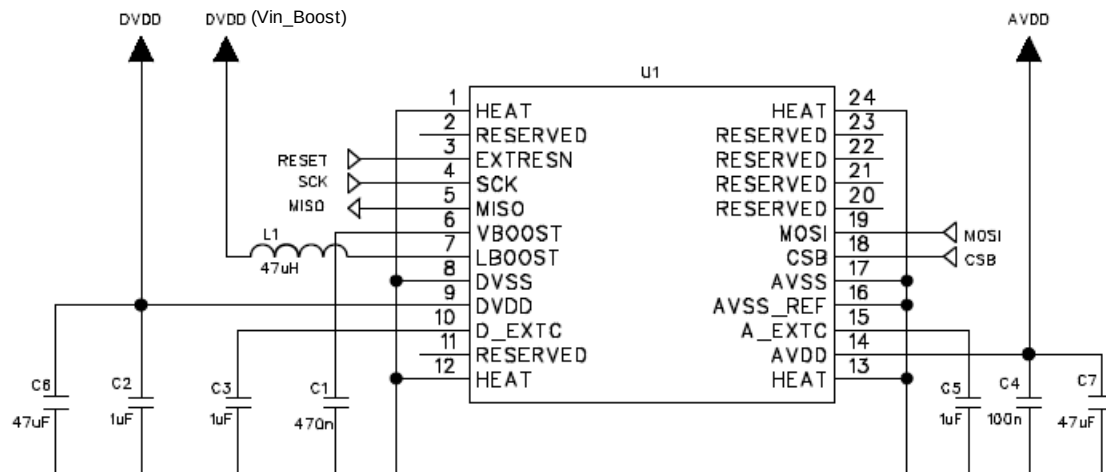


Figure 27. Application schematic.

Table 33. External component description for SCC2130-D08.

| Symbol | Description                                                                                                                   | Min.      | Nom. | Max.        | Unit          |
|--------|-------------------------------------------------------------------------------------------------------------------------------|-----------|------|-------------|---------------|
| C1     | High voltage capacitor.<br>Voltage rating<br>ESR<br>Recommended component:<br>Murata GCM21BR71H474KA55, 0805, 470N, 50V, X7R  | 376<br>30 | 470  | 564<br>100  | nF<br>V<br>mΩ |
| C2     | Decoupling capacitor between DVDD and DVSS<br>ESR<br>Recommended component:<br>Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R   | 700       | 1000 | 1300<br>100 | nF<br>mΩ      |
| C3     | Decoupling capacitor between D_EXTC and DVSS<br>ESR<br>Recommended component:<br>Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R | 700       | 1000 | 1300<br>100 | nF<br>mΩ      |
| C4     | Decoupling capacitor between AVDD and AVSS<br>ESR<br>Recommended component:<br>Murata GCM188R71C104KA37, 0603, 100N, 16V, X7R | 70        | 100  | 130<br>100  | nF<br>mΩ      |
| C5     | Decoupling capacitor between A_EXTC and AVSS<br>ESR<br>Recommended component:<br>Murata GCM21BR71C105KA58, 0805, 1U, 16V, X7R | 700       | 1000 | 1300<br>100 | nF<br>mΩ      |
| C6, C7 | Optional decoupling capacitor<br>ESR<br>Recommended component:<br>Murata GRM32ER71A476KE15L, 1210, 47U, 10V, X7R              | 22        | 47   | 100         | μF<br>mΩ      |
| L1     | Inductance for high voltage generation from Vin_Boost<br>ESR<br>Recommended component:<br>Bourns CM322522-470KL               | 37        | 47   | 57<br>5     | μH<br>Ω       |

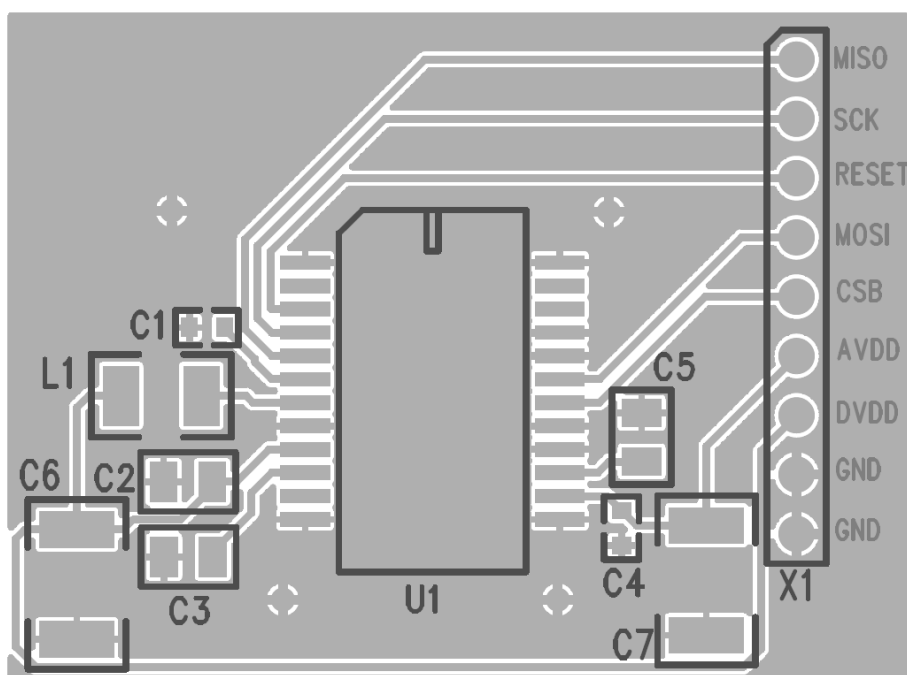


Figure 28. Application PCB layout.

General circuit diagram and PCB layout recommendations for SCC2130-D08 (refer to Figure 27 and Figure 28):

1. Connect decoupling SMD capacitors (C1 - C5) right next to respective component pins.
2. Locate ground plane under component.
3. Do not route signals or power supplies under the component on top layer.
4. Minimize the trace length between the L1 inductor and LBOOST pin (pin 7).
5. Ensure good ground connection of DVSS, AVSS\_REF and AVSS pins (pins 8, 15, 16).
6. For optimum performance the use of decoupling capacitors C6 and C7 is recommended. Capacitor C6 should be located close to C2 and C7 close to C4.

## 7.2 Assembly Instructions

Usage of PCB coating materials may effect component performance. The coating material and coating process used should be validated. For additional assembly related details please refer to "Technical Note 96" for assembly instructions:

TN96\_Assembly\_Instructions\_for\_SCC2000\_Series

## 8 Order information

Table 34. SCC2130-D08 order codes with packing quantity.

| Order code      | Description                                                                       | Packing | Qty    |
|-----------------|-----------------------------------------------------------------------------------|---------|--------|
| SCC2130-D08-004 | Gyro (X-axis $\pm 125$ dps) accelerometer ( $\pm 6$ g) combo with digital SPI i/f | Bulk    | 4pcs   |
| SCC2130-D08-05  | Gyro (X-axis $\pm 125$ dps) accelerometer ( $\pm 6$ g) combo with digital SPI i/f | T&R     | 50pcs  |
| SCC2130-D08-6   | Gyro (X-axis $\pm 125$ dps) accelerometer ( $\pm 6$ g) combo with digital SPI i/f | T&R     | 600pcs |

# Mouser Electronics

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