W-LAN+Bluetooth Combo Module Data Sheet

NXP Chipset 88W8997
for 802.11a/b/g/n/ac 2x2 MU-MIMO
+ Bluetooth 5.1

Tentative P/N : LBEE5XV1YM-TEMP

This Datasheet is preliminary version, and subject to change without notice.

Revision History

Revision Code	Date	Changed Item	Comments
-	2020.01.15	First version	
A	2020.02.17	8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS 10. REFERENCE PERIPHERAL CIRCUIT	Added label design information. Added Reference Circuit
B	2020.06.15	Part Number Pin name 11. Pin States	Changed part number to LBEE5XV1YM Changed pin name RXP/RXN/TXP/TXN to PCIE_RXP/PCIE_RXN/PCIE_TXP/PCIE_TXN. Added pin state table
C	2020.06.20	4. Dimensions	Added Solder bump and defined T1 dimension

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Table of Contents

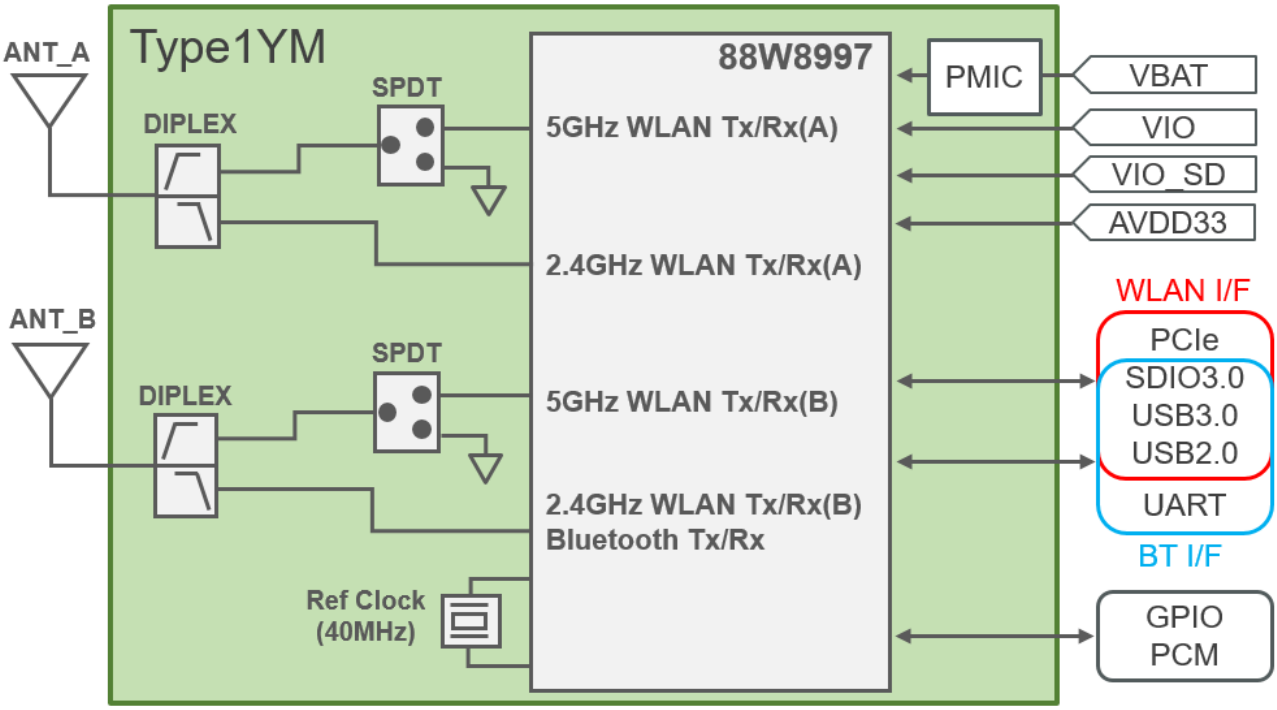
1. SCOPE

This specification is applied to the IEEE802.11a/b/g/n/ac WLAN 2x2 MU-MIMO + Bluetooth 5.1 combo module.

2. KEY FEATURE

- NXP 88W8997 inside
- Compliant with IEEE802.11a/b/g/n/ac, MU-MIMO
- Compliant with Bluetooth specification v5.1
- Supports standard PCI Express / SDIO3.0 / USB2.0&3.0 Interface for WLAN
- UART / SDIO3.0 / USB2.0&3.0 interfaces support for Bluetooth is Host Controller Interface (HCI)
- Surface mount type 11.8 x 8.4 mm(Typical), H = 1.3 mm(Max.)
- Weight : (TBD)
- MSL : 3
- RoHS compliant

3. BLOCK DIAGRAM



4. SAMPLE ORDERING INFORMATION

Ordering Part Number	Description
LBEE5XV1YM-TEMP	In case of sample order
LBEE5fXV1YM-TEMP-D	EVB

5. ABSOLUTE MAXIMUM RATINGS

Parameter		Min	Max	Unit
Storage Temperature		-30	+85	deg.C
Supply Voltage	VBAT	--	6.0	V
	VIO	--	2.2	V
		--	3.0	V
		--	4.0	V
	VIO_SD	--	2.2	V
		--	4.0	V
	AVDD33	--	4.0	

Note) Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

6. OPERATING CONDITION

Parameter		Min	Typ	Max	Unit
Operating Temperature		-30	--	+85	deg.C
Operating Voltage	VBAT	2.7	--	5.5	V
	VIO	1.62	1.8	1.98	V
		2.25	2.5	2.75	V
		2.97	3.3	3.47	V
	VIO_SD	1.62	1.8	1.98	V
		2.97	3.3	3.47	V
	AVDD33	2.97	3.3	3.63	V

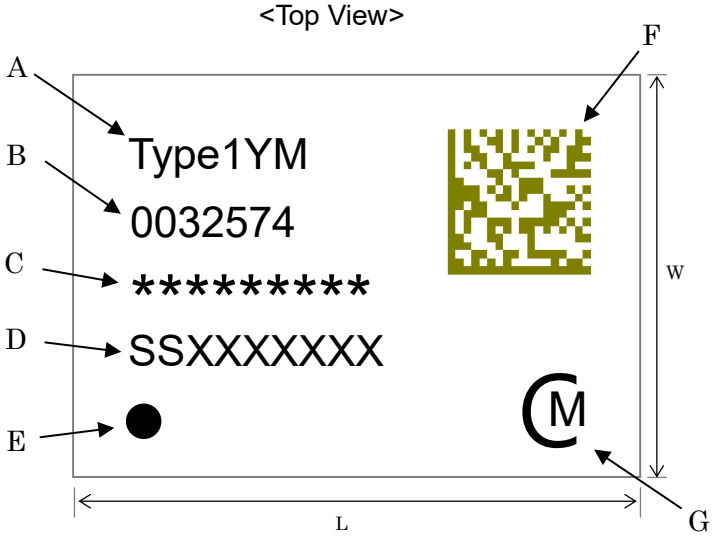
Note) Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

7. EXTERNAL Sleep Clock Timing

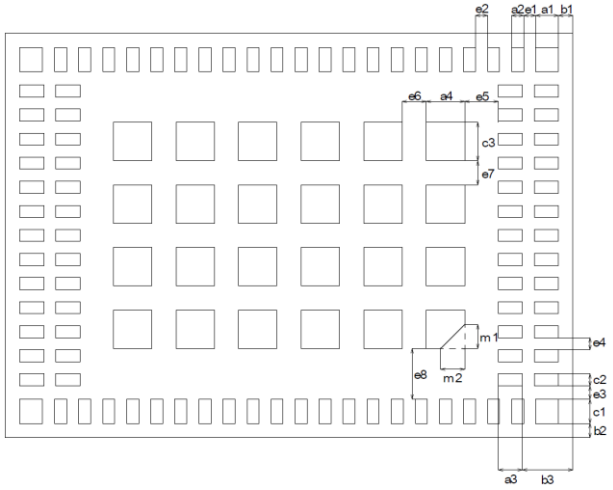
Symbol	Parameter	Min	Typ	Max	Unit
CLK	Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	--	32.768	--	kHz
V_{IH}	Input levels, where VIO = 1.8, 2.5, 3.3 V	0.7*VIO	--	VIO+0.4	V
V_{IL}		-0.4	--	0.3*VIO	V
PN	Phase noise requirement (@100kHz)	--	-125	--	dBc/Hz
Jc	Cycle jitter	--	1.5	--	ns(RMS)
SR	Slew rate limit (10-90%)	--	--	100	ns
DC	Duty cycle tolerance	20	--	80	%

8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS

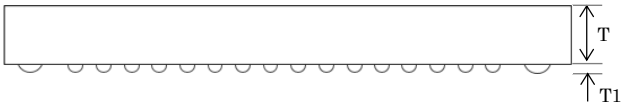
<Top View>



<Bottom View>



<Side View>



Marking	Meaning
A	Module Type
B	Production Process Number
C	Serial Number
D	Inspection Number
E	Pin 1 Marking
F	2D code
G	Murata Logo

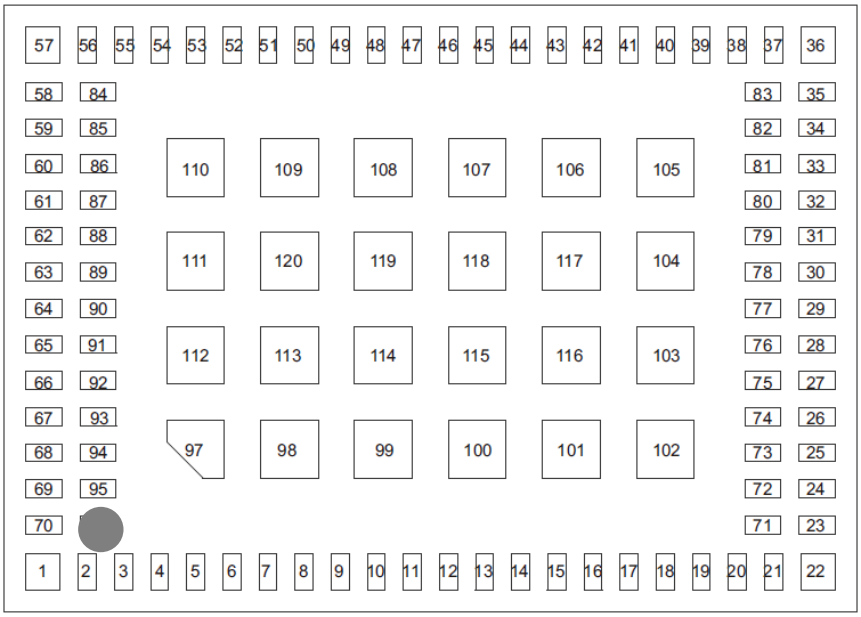
Mark	Dimensions	Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	11.8 ± 0.2	W	8.4 ± 0.2	T	1.3 max.	a1	0.475 ± 0.1
a2	0.25 ± 0.1	a3	0.5 ± 0.2	a4	0.8 ± 0.1	b1	0.3 ± 0.2
b2	0.3 ± 0.2	b3	1.05 ± 0.2	c1	0.5 ± 0.1	c2	0.25 ± 0.1
c3	0.8 ± 0.1	e1	0.25 ± 0.1	e2	0.25 ± 0.1	e3	0.25 ± 0.1
e4	0.25 ± 0.1	e5	0.7 ± 0.1	e6	0.5 ± 0.1	e7	0.5 ± 0.1
e8	1.05 ± 0.1	m1	0.5 ± 0.2	m2	0.5 ± 0.2	T1	0.045 typ.

(unit : mm)

9. MODULE PIN DESCRIPTIONS

9.1. Pin Assignment

<TOP VIEW>



No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	29	GND	57	GND
2	GPIO[24]	30	PMIC_EN	58	GND
3	GPIO[3]	31	GPIO[21]	59	WLAN_RF_A
4	GPIO[2]	32	PCIE_WAKE_N	60	GND
5	GPIO[17]	33	GPIO[5]	61	GPIO[6]
6	GPIO[16]	34	DNC	62	GPIO[9]
7	GPIO[15]	35	DNC	63	GPIO[8]
8	GPIO[14]	36	GND	64	GPIO[13]
9	VIO	37	GND	65	GPIO[10]
10	GPIO[20]	38	GND	66	GPIO[11]
11	GPIO[25]	39	PCIE_RXP	67	GPIO[12]
12	GND	40	PCIE_RXN	68	GND
13	DM	41	PCIE_TXP	69	WLAN_RF_B
14	DP	42	PCIE_TXN	70	GND
15	GND	43	PCIE_CLKP	71	GPIO[26]
16	VIO_SD	44	PCIE_CLKN	72	GPIO[27]
17	AVDD33	45	GND	73	GPIO[18]
18	SD_D1	46	GPIO[4]	74	GND
19	SD_D0	47	GPIO[0]	75	VBAT
20	SD_CLK	48	DNC	76	VBAT
21	SD_CMD	49	DNC	77	GND
22	GND	50	AVDD18	78	GPIO[1]
23	SD_D3	51	DNC	79	GPIO[23]
24	SD_D2	52	CONFIG_HOST_3	80	GPIO[22]
25	GPIO[19]	53	CONFIG_HOST_2	81	GPIO[7]
26	GND	54	CONFIG_HOST_1	82	PCIE_CLKREQ_N
27	VBAT	55	CONFIG_HOST_0	83	DNC
28	VBAT	56	SLP_CLK	84-120	GND

9.2. Pin Description

No.	Pin name	Type	Connection to IC pin name	Description
1	GND	Ground	-	Ground
2	GPIO[24]	I/O	GPIO[24]	Programmable GPIO
3	GPIO[3]	I/O	GPIO[3]	Programmable GPIO
4	GPIO[2]	I/O	GPIO[2]	Programmable GPIO
5	GPIO[17]	I/O	GPIO[17]	Programmable GPIO
6	GPIO[16]	I/O	GPIO[16]	Programmable GPIO
7	GPIO[15]	I/O	GPIO[15]	Programmable GPIO
8	GPIO[14]	I/O	GPIO[14]	Programmable GPIO
9	VIO	Power	VIO	Power Supply
10	GPIO[20]	I/O	GPIO[20]	Programmable GPIO
11	GPIO[25]	I/O	GPIO[25]	Programmable GPIO
12	GND	Ground	-	Ground
13	DM	I/O	USB_DMNS	USB Serial Differential Data-Negative
14	DP	I/O	USB_DPLS	USB Serial Differential Data-Positive
15	GND	Ground	-	Ground
16	VIO_SD	Power	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply
17	AVDD33	Power	AVDD33	3.3V Analog Power Supply
18	SD_D1	I/O	SD_DAT[1]	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
19	SD_D0	I/O	SD_DAT[0]	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line
20	SD_CLK	I/O	SD_CLK	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
21	SD_CMD	I/O	SD_CMD	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
22	GND	Ground	-	Ground
23	SD_D3	I/O	SD_DAT[3]	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
24	SD_D2	I/O	SD_DAT[2]	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Interrupt (optional)
25	GPIO[19]	I/O	GPIO[19]	Programmable GPIO
26	GND	Ground	-	Ground
27	VBAT	Power	PVIN(PMIC)	Power Supply
28	VBAT	Power	PVIN(PMIC)	Power Supply
29	GND	Ground	-	Ground
30	PMIC_EN	I	EN(PMIC)	Enable Input for All Regulators
31	GPIO[21]	I/O	GPIO[21]	Programmable GPIO
			PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)
32	PCIE_WAKE_N	I/O	PCIE_WAKEn	PCIe wake signal (active low)
33	GPIO[5]	I/O	GPIO[5]	Programmable GPIO
34	NC	-	-	No Connect
35	NC	-	-	No Connect

36	GND	Ground	-	Ground
37	GND	Ground	-	Ground
38	GND	Ground	-	Ground
39	PCIE_RXP	I	PCIE_RX_P	PCI Express Lane 0, Receive Pair, Positive Signal 2.5GHz serial low-voltage interface
			USB3_RX_P	USB 3.0 receive data – positive
40	PCIE_RXN	I	PCIE_RX_N	PCI Express Lane 0, Receive Pair, Negative Signal 2.5GHz serial low-voltage interface
			USB3_RX_N	USB 3.0 receive data - negative
41	PCIE_TXP	O	PCIE_TX_P	PCI Express Lane 0, Transmit Pair, Positive Signal 2.5GHz serial low-voltage interface
			USB3_TX_P	USB3.0 transmit data - positive
42	PCIE_TXN	O	PCIE_TX_N	PCI Express Lane 0, Transmit Pair, Negative Signal 2.5GHz serial low-voltage interface
			USB3_TX_N	USB3.0 transmit data - negative
43	PCIE_CLKP	I	PCIE_RCLK_P	PCI Express Platform Reference Clock Positive signal of differential pair 100 MHz low-voltage interface
44	PCIE_CLKN	I	PCIE_RCLK_N	PCI Express Platform Reference Clock Negative signal of differential pair 100 MHz low-voltage interface
45	GND	Ground	-	Ground
46	GPIO[4]	I/O	GPIO[4]	Programmable GPIO
47	GPIO[0]	I/O	GPIO[0]	Programmable GPIO Oscillator Mode : XOSC_EN/CLK_REQ(output)(active high) 0 = disable external oscillator 1 = enable external oscillator
48	DNC	-	DNC	Do Not Connect
49	DNC	-	DNC	Do Not Connect
50	AVDD18	O	VLDO(PMIC)	LDO Output
51	DNC	DNC	DNC	Do Not Connect
52	CONFIG_HOST_3		CONFIG_HOST[3]	Configuration interface[3] See 9.3Configuration Pins
53	CONFIG_HOST_2		CONFIG_HOST[2]	Configuration interface[2] See 9.3Configuration Pins
54	CONFIG_HOST_1		CONFIG_HOST[1]	Configuration interface[1] See 9.3Configuration Pins
55	CONFIG_HOST_0		CONFIG_HOST[0]	Configuration interface[0] See 9.3Configuration Pins
56	SLP_CLK	I	SLP_CLK_IN	Sleep Clock Input Used for WLAN and Bluetooth low power modes. If no sleep clock input is provided, an internal sleep clock (derived from reference clock) will be used. if SLP_CLK is not connected, the internal circuit will detect no signal, and firmware will initialize the sleep clock based on the reference clock.
57	GND	Ground	-	Ground
58	GND	Ground	-	Ground
59	WLAN_RF_A	I/O	RF_TR_2_A RF_TR_5_A	RF Transmit / Receive (2.4G/5 GHz) – PathA
60	GND	Ground	-	Ground
61	GPIO[6]	I/O	GPIO[6]	Programmable GPIO
62	GPIO[9]	I/O	GPIO[9]	Programmable GPIO
63	GPIO[8]	I/O	GPIO[8]	Programmable GPIO
64	GPIO[13]	I/O	GPIO[13]	Programmable GPIO

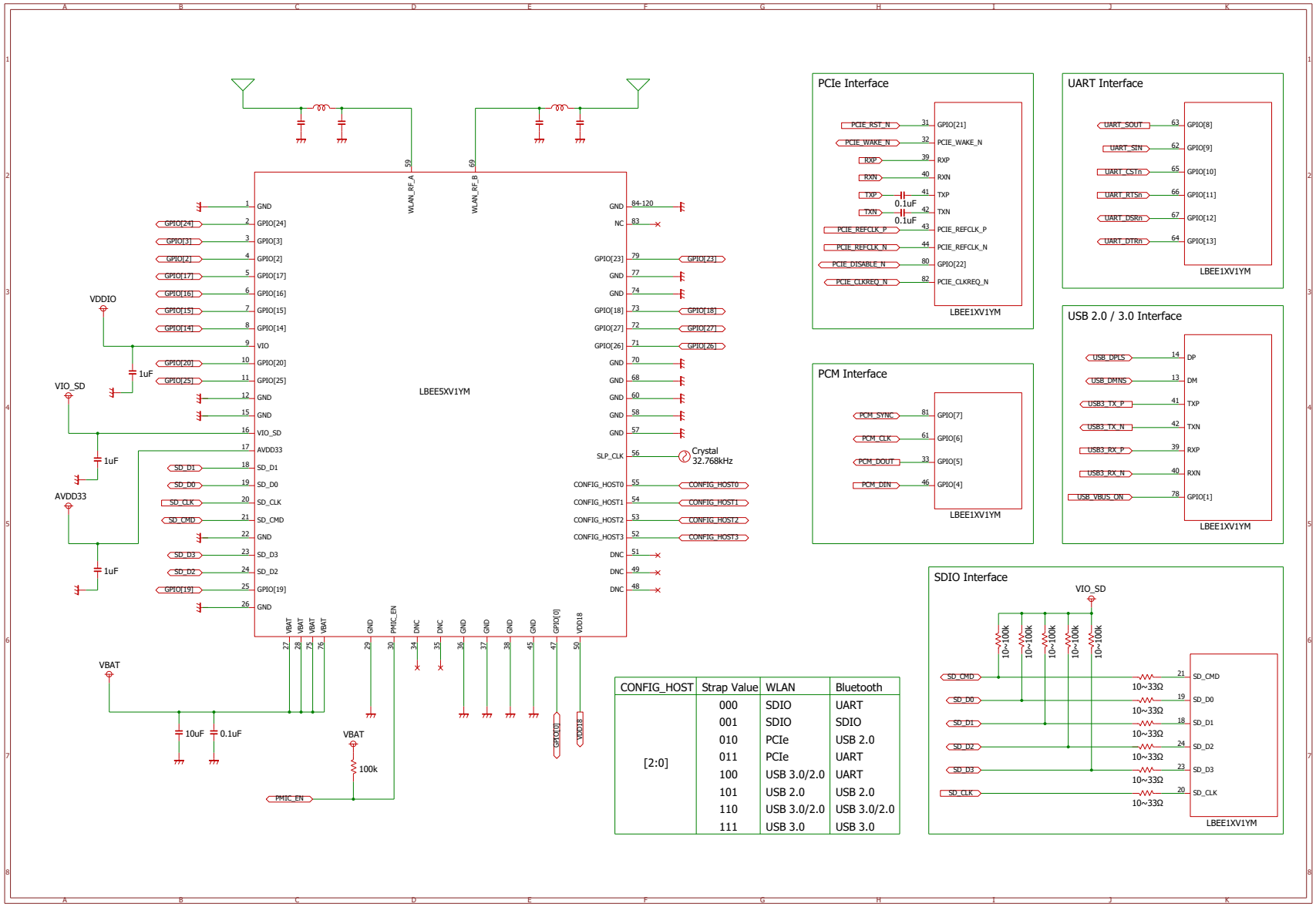
65	GPIO[10]	I/O	GPIO[10]	Programmable GPIO
66	GPIO[11]	I/O	GPIO[11]	Programmable GPIO
67	GPIO[12]	I/O	GPIO[12]	Programmable GPIO
68	GND	Ground	-	Ground
69	WLAN_RF_B	I/O	RF_TR_2_A RF_TR_5_A	RF Transmit / Receive (2.4G/5 GHz) – PathB
70	GND	Ground	-	Ground
71	GPIO[26]	I/O	GPIO[26]	Programmable GPIO
72	GPIO[27]	I/O	GPIO[27]	Programmable GPIO
73	GPIO[18]	I/O	GPIO[18]	Programmable GPIO
74	GND	Ground	-	Ground
75	VBAT	Power	PVIN(PMIC)	Power Supply
76	VBAT	Power	PVIN(PMIC)	Power Supply
77	GND	Ground	-	Ground
78	GPIO[1]	I/O	GPIO[1]	Programmable GPIO
79	GPIO[23]	I/O	GPIO[23]	Programmable GPIO
80	GPIO[22]	I/O	GPIO[22]	Programmable GPIO
			PCIE_W_DISABLEn	PCIe host indication to disable the WLAN function of the device (input) (active low)
81	GPIO[7]	I/O	GPIO[7]	Programmable GPIO
82	PCIE_CLKREQ_N	I/O	PCIE_CLKRQn	PCI Express Wake Signal
83	NC	-	-	No Connect
84-120	GND	Ground	-	Ground

9.3. Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[2]	CONFIG_HOST[2]	Firmware Boot Options No hardware impact. Software reads and boots accordingly. See table below.
CON[1]	CONFIG_HOST[1]	
CON[0]	CONFIG_HOST[0]	

Strap Value	WLAN	Bluetooth/ BLE	ROM Notes	Firmware Download Mode	Number of SDIO Functions
000	SDIO	UART	--	Parallel	1 (WLAN)
001	SDIO	SDIO	--	Parallel	2 (WLAN, Bluetooth)
010	PCIe	USB 2.0	Initialize USB 2.0 PHY and COM PHY PCIe portion	Parallel	
011	PCIe	UART	Initialize only COM PHY PCIe portion	Parallel	
100	USB 3.0/2.0	UART	Initialize both COM PHY USB 3.0 and USB 2.0 PHY	Parallel	
101	USB 2.0	USB 2.0	Initialize only USB 2.0 PHY	Parallel	
110	USB 3.0/2.0	USB 3.0/2.0	Initialize both COM PHY USB 3.0 and USB 2.0 PHY	Parallel	
111	USB3.0	USB 3.0	Initialize only COM PHY USB 3.0 portion	Parallel	

10. REFERENCE PERIPHERAL CIRCUIT



CONFIG_HOST	Strap Value	WLAN	Bluetooth
[2:0]	000	SDIO	UART
	001	SDIO	SDIO
	010	PCIe	USB 2.0
	011	PCIe	UART
	100	USB 3.0/2.0	UART
	101	USB 2.0	USB 2.0
	110	USB 3.0/2.0	USB 3.0/2.0
	111	USB 3.0	USB 3.0

11. Pin States

Pin states information for the tables below include:

- After firmware is downloaded, the pads (GPIO, Serial interface, RF control) are programmed in functional mode per the functionality of the pins.
- For SDIO, once the command is received from the host, the pads are configured accordingly.
- Pull-up and pull-down are only effective when the pad is in input mode.
- The power-down state shown is the default configuration. Many pads have programmable power-down values, which can be set by firmware.

I/O State Table

Pin Name	Supply	No Pad Power State	Reset State	HW State[1]	PD State[2]	PD Prog[3]	Internal PU/PD
GPIO[0]	VIO	tristate	output	output	drive low	yes	nominal PU
GPIO[1]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[2]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[3]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[4]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[5]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[6]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[7]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[8]	VIO	tristate	input	input	drive low	yes	weak PU
GPIO[9]	VIO	tristate	input	input	tristate	yes	weak PU
GPIO[10]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[11]	VIO	tristate	input	input	drive high	yes	weak PU
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PD
GPIO[13]	VIO	tristate	input	input	drive high	yes	nominal PU
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[15]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[16]	VIO	tristate	input	input	tristate	yes	nominal PD
GPIO[17]	VIO	tristate	input	input	tristate	yes	nominal PD
GPIO[18]	VIO	tristate	input	input	tristate	yes	nominal PD
GPIO[19]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[20]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[21]	VIO	tristate	input	input	tristate	yes	nominal PU

[1] Hardware default state after reset
[2] Power-down state
[3] Power-down state programmable

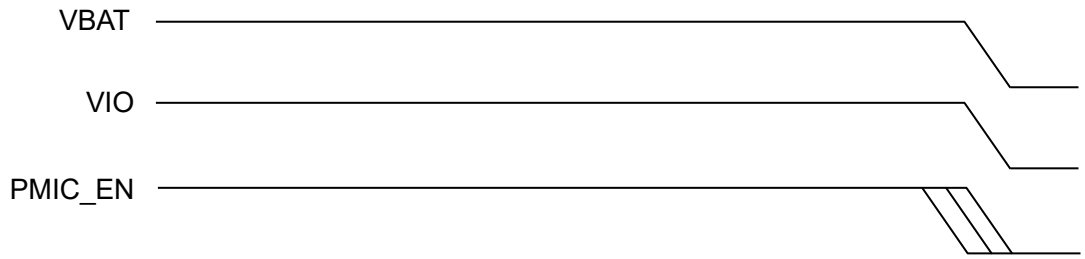
GPIO[22]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[23]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[24]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[25]	VIO	tristate	input	input	drive high	yes	nominal PU
GPIO[26]	VIO	tristate	input	input	tristate	yes	nominal PU
GPIO[27]	VIO	tristate	input	input	tristate	yes	nominal PU
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU
SD_D0	VIO_SD	tristate	input	input	tristate	no	nominal PU
SD_D1	VIO_SD	tristate	input	input	tristate	no	nominal PU
SD_D2	VIO_SD	tristate	input	input	tristate	no	nominal PU
SD_D3	VIO_SD	tristate	input	input	tristate	no	nominal PU
PCIE_CLKP	VDD18	-	-	-	-	-	-
PCIE_CLKN	VDD18	-	-	-	-	-	-
PCIE_TXP	VDD18	-	-	-	-	-	-
PCIE_TXN	VDD18	-	-	-	-	-	-
PCIE_RXP	VDD18	-	-	-	-	-	-
PCIE_RXN	VDD18	-	-	-	-	-	-
PCIE_WAKE_N	VIO	tristate	input	output	N/A	N/A	N/A
PCIE_CLKREQ_N	VIO	tristate	input	output	N/A	N/A	N/A
CONFIG_HOST_0	VDD18	tristate	input	input	tristate	no	weak PU
CONFIG_HOST_1	VDD18	tristate	input	input	tristate	no	weak PU
CONFIG_HOST_2	VDD18	tristate	input	input	tristate	no	weak PU
CONFIG_HOST_3	VDD18	tristate	input	input	tristate	no	weak PU

12. POWER SEQUENCE

12.1. POWER ON SEQUENCE

A minimum time of 100ms is required after PMIC_EN is deasserted (=0) and before it is asserted (=1).

12.2. POWER OFF SEQUENCE



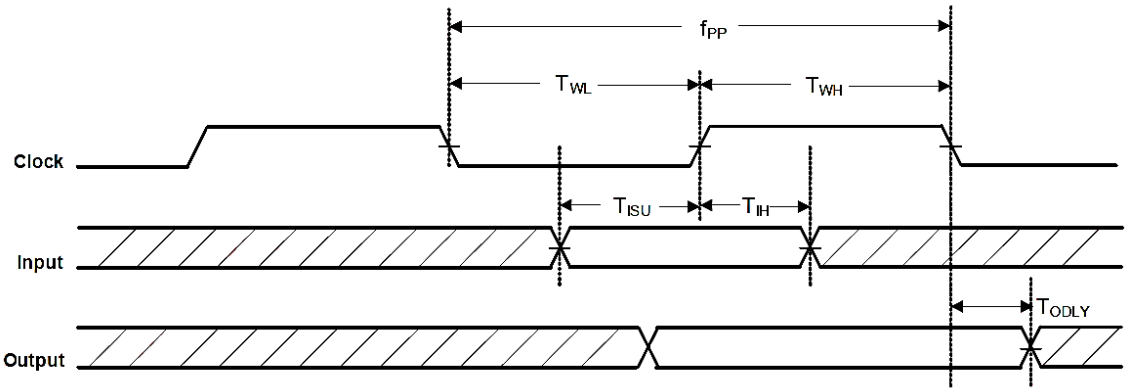
13. Host Interface Specification

13.1. SDIO Specifications

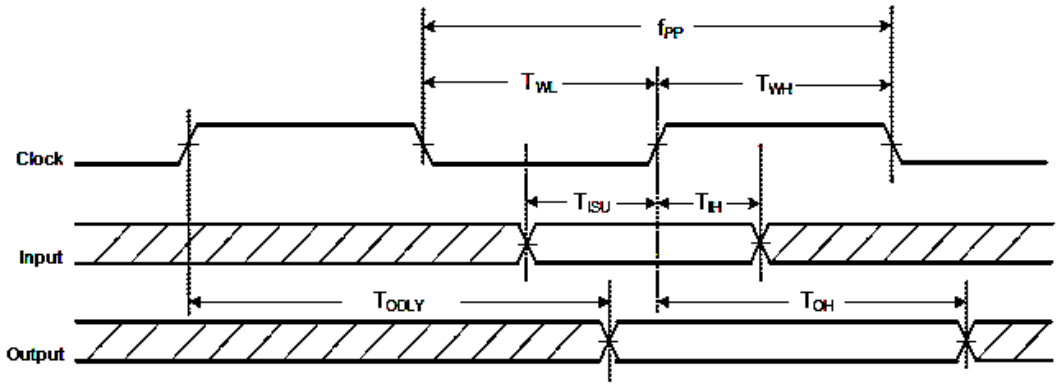
The SDIO host interface pins are powered from the VIO_SD voltage supply.
The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO transfer modes.

13.1.1. Default Speed, High-Speed Modes

SDIO Protocol Timing Diagram—Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram—High Speed Mode (3.3V)



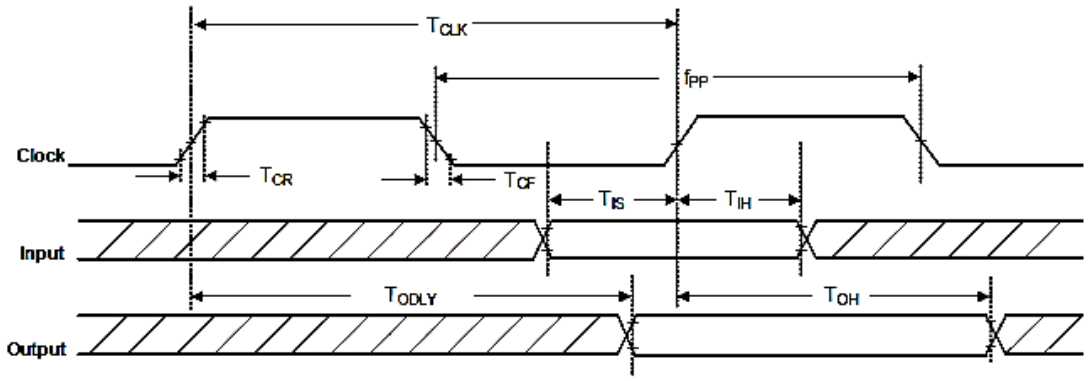
SDIO Timing Data—Default Speed, High-Speed Modes (3.3V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	Normal	0	-	25	MHz
		High-speed	0	-	50	MHz
T_{WL}	Clock low time	Normal	10	-	-	ns
		High-speed	7	-	-	ns
T_{WH}	Clock high time	Normal	10	-	-	ns
		High-speed	7	-	-	ns
T_{ISU}	Input setup time	Normal	5	-	-	ns
		High-speed	6	-	-	ns
T_{IH}	Input hold time	Normal	5	-	-	ns
		High-speed	2	-	-	ns
T_{ODLY}	Output delay time	Normal	-	-	14	ns
	CL ≤ 40 pF (1 card)	High-speed	-	-	14	ns
T_{OH}	Output hold time	High-speed	2.5	-	-	ns

13.1.2. SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8 V)

SDIO protocol Timing Diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8 V)



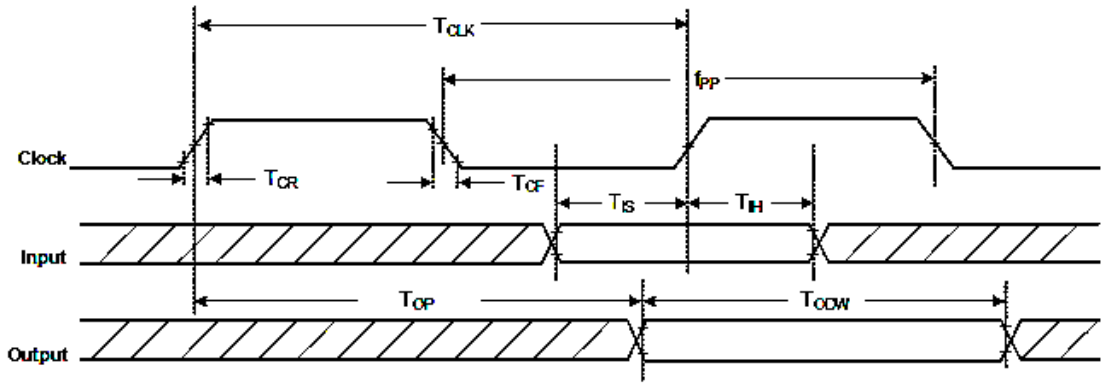
SDIO Timing Data—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8 V)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	-	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	-	-	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	-	-	ns
T_{CLK}	Clock time	SDR12/25/50	10	-	40	ns
T_{CR}, T_{CF}	Rise time, fall time TCR, TCF< 2ns(max) at 100 MHz CCARD=10 pF	SDR12/25/50	-	-	0.2*T_{CLK}	ns
T_{ODLY}	Output dekay time CL ≤ 30pF	SDR12/25/50	-	-	7.5	ns
T_{OH}	Output hold time CL=15 pF	SDR12/25/50	1.5	-	-	ns

13.1.3. SDR104 Mode (208 MHz) (1.8 V)

SDIO Protocol Timing Diagram—SDR104 Mode (208 MHz)



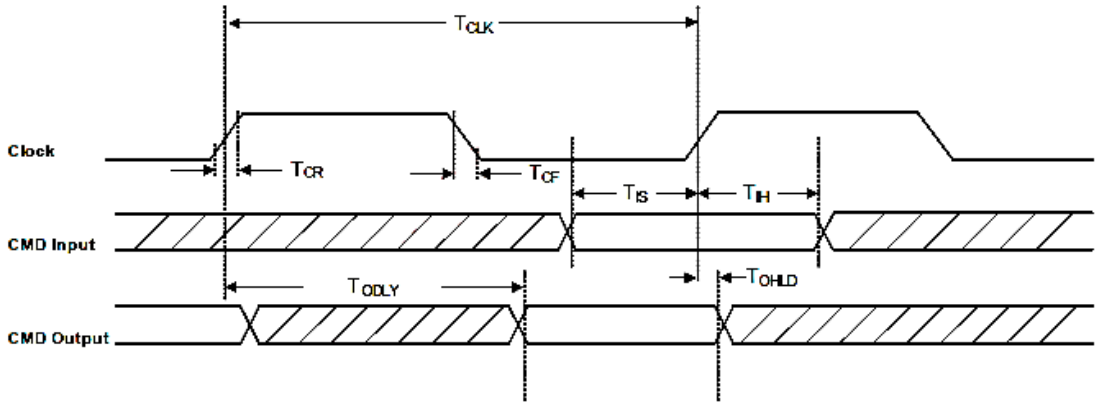
SDIO Timing Data—SDR104 Mode (208 MHz)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

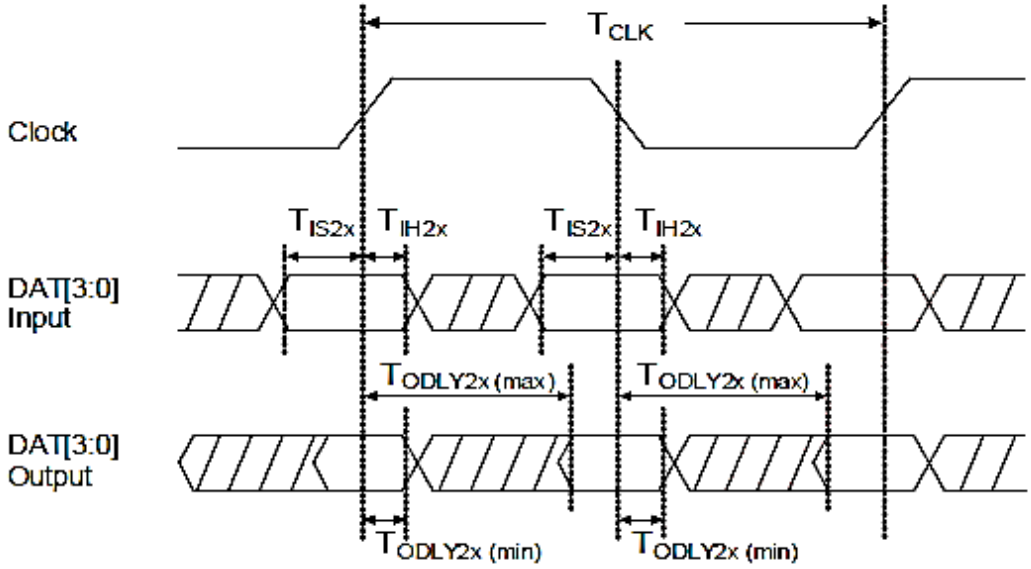
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	-	208	MHz
T_{IS}	Input setup time	SDR104	1.4	-	-	ns
T_{IH}	Input hold time	SDR104	0.8	-	-	ns
T_{CLK}	Clock time	SDR104	4.8	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time TCR, TCF< 0.96 ns(max) at 208 MHz CCARD=10 pF	SDR104	-	-	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	-	10	ns
T_{ODW}	Output timimg of variable data window	SDR104	2.88	-	-	ns

13.1.4. DDR50 Mode (50 MHz) (1.8 V)

SDIO CMD Timing Diagram—DDR50 Mode (50 MHz)



SDIO DAT[3:0] Timing Diagram—DDR50 Mode (50 MHz)



SDIO Timing Data—DDR50 Mode (50 MHz)

Note: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	-	-	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF}< 4.00 ns(max) at 50 MHz C_{CARD}=10 pF	DDR50	-	-	0.2*T_{CLK}	ns
Clock Duty	-	DDR50	45	-	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	-	-	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	-	-	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	-	-	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	-	-	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
T_{ODLY2x} (max)	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	-	-	7.0	ns
T_{ODLY2x} (min)	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	-	-	ns

13.2. PCI Express Specifications

The PCI Express host interface pins are powered from the AVDD18 voltage supply.

13.2.1. Differential Tx Output Electricals

PCI Express Tx Output Specifications Data—2.5 GT/s

Note: In accordance with PCI Express Base Specification, Revision 2.1 March 4. 2009.

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	399.88	--	400.12	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{TX-DFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.8	--	1.2	V
$V_{TX-DIFF-PP-LOW}$	Low power differential peak-to-peak tTx voltage swing $V_{TX-DFFpp} = 2*\|VT_{XD+} - V_{TXD-}$	0.4	--	1.2	V
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	--	4.0	dB
T_{TX-EYE}	Tx eye including all jitter sources	0.75	--	--	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
$T_{TX-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.125	--	--	UI
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	10	--	--	dB
RL_{TX-CM}	Tx package plus Si common mode return loss	6	--	--	dB
$V_{TX-CM-AC-P}$	Tx AC common mode voltage	--	20	--	mV
$I_{TX-SHORT}$	Tx short circuit current limit	--	--	90	mA
$V_{TX-DC-CM}$	Tx DC common mode voltage	0	--	3.6	V
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	--	100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20	--	--	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle	--	--	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	--	--	1.0	ms
C_{TX}	AC coupling capacitor	75	--	200	nF

PCI Express Tx Output Specifications Data—5 GT/s

Note: In accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	199.94	--	200.06	ps
$V_{TX-DIFFpp}$	Differential peak-to-peak Tx voltage swing $V_{TX-DFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.8	--	1.2	V
$V_{TX-DIFFpp-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{TX-DFFpp} = 2*\|VT_{XD+} - V_{TXD-}\|$	0.4	--	1.2	V
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0	--	4.0	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio (6 dB)	5.5	--	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width Measured relative to rising/falling pulse.	0.9	--	--	UI
T_{TX-EYE}	Tx eye including all jitter sources	0.75	--	--	UI
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz Deterministic jitter only.	--	--	0.15	UI
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5 MHz Total energy measured over a 10 kHz—1.5 MHz range.	--	3.0	--	Ps RMS
$T_{TX-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing.	0.15	--	--	UI
$RL_{TX-DIFF}$	Tx package plus Si differential return loss (1.25-2.5 GHz)	10	--	--	dB
	Tx package plus Si differential return loss (0.05-1.25 GHz)	8	--	--	
RL_{TX-CM}	Tx package plus Si common mode return loss	6	--	--	dB
$V_{TX-CM-AC-PP}$	Tx AC common mode voltage	--	--	100	mVPP
$I_{TX-SHORT}$	Tx short circuit current limit	--	--	90	mA
$V_{TX-DC-CM}$	Tx DC common mode voltage	0	--	3.6	V
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0	--	100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage $V_{TX-IDLE-DIFF-DC} = \|V_{TX-Idle-D+} - V_{TX-Idle-D-}\| \leq 20$ mV	0	--	20	mV
$V_{TX-IDLE-DIFF-DC}$	DC Electrical idle differential peak output voltage $V_{TX-IDLE-DIFF-DC} = \|V_{TX-Idle-D+} - V_{TX-Idle-D-}\| \leq 5$ mV	0	--	5	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20	--	--	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid differential signaling after leaving electrical idle	--	--	8	ns
$T_{CROSSLINK}$	Crosslink random timeout	--	--	1.0	ms
C_{TX}	AC coupling capacitor	75	--	200	nF

13.2.2. Differential Rx Input Electricals

PCI Express Rx Input Specifications Data—2.5 GT/s

Note: In accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	399.88	--	400.12	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture	0.175	--	1.2	V
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.175	--	1.2	V
T_{RX-EYE}	Rx eye time opening Minimum eye time at Rx pins to yield a 10^{-12} BER.	0.40	--	--	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between median and deviation from median	--	--	0.3	UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage	--	--	150	mV
$RL_{RX-DIFF}$	Differential return loss	15	--	--	dB
RL_{RX-CM}	Common mode return loss	0	--	3.6	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{RX-DC}	DC input impedance	40	50	60	W
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200	--	--	kΩ
$V_{RX-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65	--	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
$L_{RX-SKEW}$	Total skew	--	--	20	ns

PCI Express Rx Input Specifications Data—5 GT/s

Note: In accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit Interval (UI) UI does not account for SSC induced variations.	199.94	--	200.06	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture	0.120	--	1.2	V
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.100	--	1.2	V
$T_{RX-TJ-CC}$	Maximum Rx inherent total timing error for common Refclk Rx architecture	--	--	0.40	UI
$T_{RX-TJ-DC}$	Maximum Rx inherent total timing error for data clocked Rx architecture	--	--	0.34	UI
$T_{RX-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error for common Refclk Rx architecture		--	0.30	UI
$T_{RX-DJ-DD-DC}$	Maxximum Rx inherent deterministic timing error for data clocked Rx architeuture		--	0.24	UI
$T_{RX-MIN-PLISE}$	Minimum width pulse at Rx Measured to account for worst Tj at 10^{-12} BER.	0.6	--	--	UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage	--	--	150	mV
$RL_{RX-DIFF}$	Differential return loss	15	--	--	dB
RL_{RX-CM}	Common mode return loss	0	--	3.6	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{RX-DC}	DC input impedance	40	50	60	W
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200	--	--	kΩ
$V_{RX-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65	--	175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
$L_{RX-SKEW}$	Total skew	--	--	20	ns

13.3. USB Specifications

The USB 3.0 device interface pins are powered from the AVDD33 voltage supply.

13.3.1. USB LS Driver and Receiver Parameters

USB LS Driver and Receiver Specifications Data

Note: In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.

Note: The load is 100Ω differential for these parameters, unless other specified.

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	--	1.5	--	Gbps
BR_{PPM}	Baud rate tolerance	-15000.0	--	15000.0	ppm
Driver Specifications					
V_{OH}	Output signal ended high Defined with 1.425 kΩ pull-up resister to 3.6V.	2.8	--	3.6	V
V_{OL}	Output signal ended low Defined with 1.425 kΩ pull-down register to ground.	0.0	--	0.3	V
V_{CRS}	Output signal crossover voltage See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162.	1.3	--	2.0	V
T_{LR}	Data fall time ・See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162. ・Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	--	300.0	ns
T_{LF}	Data rise time ・See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162. ・Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	--	300.0	ns
T_{LRFM}	Rise and fall time matching	80.0	--	125.0	%
T_{UDJ1}	Source jitter total: to next transition ・Including frequency tolerance. Timing difference between the differential data signals. ・Defined at crossover point of differential data signals.	-95.0	--	95.0	ns
T_{UDJ2}	Source jitter total: for paired transitions ・Including frequency tolerance. Timing difference between the differential data signals. ・Defined at crossover point of differential data signals.	-150.0	--	150.0	ns
Receiver Specifications					
V_{IH}	Input signal ended high	2.0	--	--	V
V_{IL}	Input signal ended low	--	--	0.8	V
V_{DI}	Differential input sensitivity	0.2	--	--	V

13.3.2. USB FS Driver and Receiver Parameters

USB FS Driver and Receiver Specifications Data

Note: In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.

Note: The load is 100Ω differential for these parameters, unless other specified.

Symbol	Parameter	Min	Typ	Max	Units
BR	Baud rate	--	12.0	--	Mbps
BR_{PPM}	Baud rate tolerance	-2500.0	--	2500.0	ppm
Driver Specifications					
V_{OH}	Output signal ended high Defined with 1.425 kΩ pull-up resister to 3.6V.	2.8	--	3.6	V
V_{OL}	Output signal ended low Defined with 1.425 kΩ pull-down register to ground.	0.0	--	0.3	V
V_{CRS}	Output signal crossover voltage See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162.	1.3	--	2.0	V
T_{FR}	Output rise time ・See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162. ・Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	--	20.0	ns
T_{FL}	Output fall time ・See figure 42, USB LS/FS Data Rise and Fall Time Diagram, on page 162. ・Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	--	20.0	ns
T_{DJ1}	Source jitter total: to next transition ・Including frequency tolerance. Timing difference between the differential data signals. ・Defined at crossover point of differential data signals.	-3.5	--	3.5	ns
T_{DJ2}	Source jitter total: for paired transitions ・Including frequency tolerance. Timing difference between the differential data signals. ・Defined at crossover point of differential data signals.	-4.0	--	4.0	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2.0	--	5.0	ns
Receiver Specifications					
V_{IH}	Input signal ended high	2.0	--	--	V
V_{IL}	Input signal ended low	--	--	0.8	V
V_{DI}	Differential input sensitivity	0.2	--	--	V
T_{JR1}	Receiver jitter: to next transition Defined at crossover point of differential data signals.	-18.5	--	18.5	ns

14. ELECTORICAL CHARACTERISTICS

14.1. DC/RF Characteristics for IEEE802.11b - 2.4G

Conditions : 25deg.C, VBAT =3.6V.
11Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11b-2.4GHz			
Mode	DSSS / CCK			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	1, 2, 5.5,11Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	17(TBD)	TBD	dBm
Spectrum Mask				
(a) 1st side lobes	-	-	-30	dBr
(b) 2nd side lobes	-	-	-50	dBr
Power-on/off ramp	-	-	2.0	usec
RF Carrier Suppression	15	-	-	dB
Modulation Accuracy	-	-	35	%
Frequency tolerance	-20	-	20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (FER≦ 8%)	-	-	-76	dBm
Maximum Input Level (FER ≦ 8%)	-10	-	-	dBm
Adjacent Channel Rejection (FER ≦ 8%)	35	-	-	dB

14.2. DC/RF Characteristics for IEEE802.11g - 2.4G

Conditions : 25deg.C, VBAT =3.6V.
54Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11g-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	TBD	13(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-25	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Minimum Input Level (PER ≤ 10%)	-	-	-65	dBm
Maximum Input Level (PER ≤ 10%)	-20	-	-	dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1	-	-	dB

14.3. DC/RF Characteristics for IEEE802.11n - 2.4GHz

Conditions : 25deg.C, VBAT =3.6V.
65Mbps (MCS7 – HT 20MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-2.4GHz			
Mode	OFDM			
Channel frequency (spacing)	2412 to 2472 MHz (5MHz)			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**unit**
Power Levels	TBD	12(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≧ +/-30MHz	-	-	-45	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20	-	20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Minimum Input Level (PER ≦ 10%)	-	-	-64	dBm
Maximum Input Level (PER ≦ 10%)	-20	-	-	dBm
Adjacent Channel Rejection (PER ≦ 10%)	-2	-	-	dB

14.4. DC/RF Characteristics for IEEE802.11a - 5GHz

Conditions : 25deg.C, VBAT =3.6V.
54Mbps mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11a-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	13(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error	-	-	-25	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-65	dBm
Maximum Input Level (PER ≦ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

14.5. DC/RF Characteristics for IEEE802.11n(HT 20MHz) - 5GHz

Conditions : 25deg.C, VBAT =3.6V.
65Mbps (MCS7 – HT 20MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	-	mA
(b) Rx mode	-	TBD	-	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	12(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 11MHz	-	-	-20	dBr
(b) at fc +/- 20MHz	-	-	-28	dBr
(c) at fc ≥ +/-30MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-64	dBm
Maximum Input Level (PER ≦ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	16	-	-	dB

14.6. DC/RF Characteristics for IEEE802.11n(HT 40MHz) - 5GHz

Conditions : 25deg.C, VBAT =3.6V.
135Mbps (MCS7 – HT 40MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11n-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5180 - 5825MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	-	mA
(b) Rx mode	-	TBD	-	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	12(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc ≥ +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-61	dBm
Maximum Input Level (PER ≦ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-2			dB

14.7. DC/RF Characteristics for IEEE802.11ac(HT 40MHz) - 5GHz

Conditions : 25deg.C, VBAT =3.6V.
180Mbps (MCS9 – HT 40MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11ac-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5190 - 5795MHz			
Data rate	13.5,27,40.5,54,81,108,121.5,135,162,180Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	10(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 21MHz	-	-	-20	dBr
(b) at fc +/- 40MHz	-	-	-28	dBr
(c) at fc ≥ +/-60MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b) 1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≤ 10%)	-	-	-54	dBm
Maximum Input Level (PER ≦ 10%)	-30	-	-	dBm

14.8. DC/RF Characteristics for IEEE802.11ac(HT 80MHz) - 5GHz

Conditions : 25deg.C, VBAT =3.6V.
390Mbps (MCS9 – HT 80MHz) mode unless otherwise specified.

Items	**Contents**			
Specification	IEEE802.11ac-5GHz			
Mode	OFDM			
Channel frequency (spacing)	5210 - 5775MHz			
Data rate	29.3,58.5,87.8,117,175.5,234,263.3,292.5,351,390 Mbps			
Current Consumption	**Min.**	**Typ.**	**Max.**	**Unit**
(a) Tx mode (99% Tx mode)	-	TBD	TBD	mA
(b) Rx mode	-	TBD	TBD	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Power Levels	TBD	10(TBD)	TBD	dBm
Spectrum Mask				
(a) at fc +/- 41MHz	-	-	-20	dBr
(b) at fc +/- 80MHz	-	-	-28	dBr
(c) at fc ≧ +/-120MHz	-	-	-40	dBr
Constellation Error (measured at enhanced mode)	-	-	-32	dB
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<26000MHz	-	-	-30	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**Unit**
Minimum Input Level (PER ≦ 10%)	-	-	-51	dBm
Maximum Input Level (PER ≦ 10%)	-30	-	-	dBm
Adjacent Channel Rejection (PER < 10%)	-9			dB

14.9. DC/RF Characteristics for Bluetooth

Conditions : 25 deg.C, VBAT = 3.6V, 2-Antenna mode

Items	Contents			
Bluetooth specification (power class)	Version 4.2 (Class2)			
Channel frequency (spacing)	2402 to 2480 MHz (1MHz)			
Current Consumption	**Min.**	**Typ.**	**Max.**	**unit**
(a) DH5 Packet 50% Rx/Tx slot duty cycle	-	TBD	-	mA
(b) 2DH5 Packet 50% Rx/Tx slot duty cycle	-	TBD	-	mA
(c) 3DH5 Packet 50% Rx/Tx slot duty cycle	-	TBD	-	mA
Transmitter	**Min.**	**Typ.**	**Max.**	**Unit**
Output Power (at 1DH5)	TBD	TBD	TBD	dBm
Frequency range	2402	-	2480	MHz
20dB bandwidth	-		1	MHz
Adjacent Channel Power *1				
(a) [M-N] =2	-	-	-20	dBm
(b) [M-N] ≥3	-	-	-40	dBm
Modulation characteristics				
(a) Modulation Δf1avg	140	-	175	kHz
(b) Modulation Δf2max	115		-	kHz
(c) Modulation Δf2avg / Δf1avg	0.8	-	-	
Carrier Frequency Drift				
(a) 1slot	-25	-	+25	kHz
(b) 3slot / 5slot	-40	-	+40	kHz
(c) Maximum drift rate	-20	-	+20	kHz/50us
EDR Relative Power	-4	-	+1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
(a) ωi	-75	-	+75	kHz
(b) ωi+ωo	-75	-	+75	kHz
(c) ωo	-10	-	+10	kHz
(d) RMS DEVM (DQPSK)	-	-	20	%
(e) Peak DEVM (DQPSK)	-	-	35	%
(f) 99% DEVM (DQPSK)	-	-	30	%
(g) RMS DEVM (8DPSK)	-	-	13	%
(h) Peak DEVM (8DPSK)	-	-	25	%
(i) 99% DEVM (8DPSK)	-	-	20	%
Spurious Emissions (BW=100kHz)				
(a) 30Hz≦f<1000MHz	-	-	-36	dBm
(b)1000MHz≦f<12750MHz	-	-	-30	dBm
(c) 1800MHz<f≦1900MHz	-	-	-47	dBm
(d) 5150MHz<f≦5300MHz	-	-	-47	dBm
Receiver	**Min.**	**Typ.**	**Max.**	**unit**
Sensitivity (BER≤0.1%)	-	-	-80	dBm
Maximum Input Level (BER≤0.1%)	-20	-	-	dBm
EDR Sensitivity (BER≤0.007%)				
(a) 8DPSK	-	-	-70	dBm

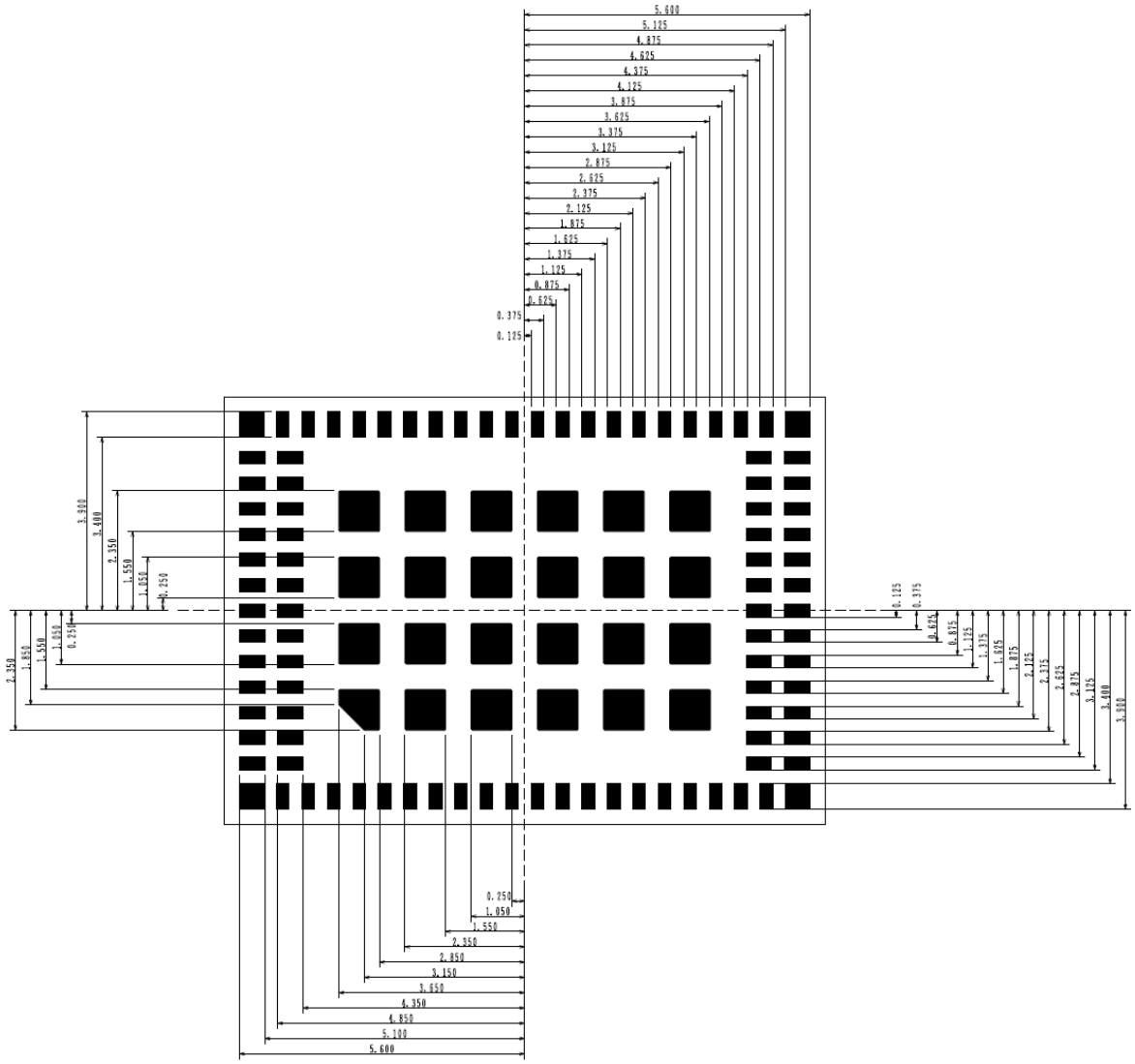
*1: Up to three spurious responses within Bluetooth limits are allowed.

14.10. DC/RF Characteristics for Bluetooth (LE)

Conditions : 25 deg.C, VBAT = 3.6V, 2-Antenna mode

Items	Contents			
Bluetooth specification (power class)	Version 4.2(LE)			
Channel frequency (spacing)	2402 to 2480 MHz (2MHz)			
Number of RF Channel	40			
Item / Condition	**Min.**	**Typ.**	**Max.**	**Unit**
Center Frequency	2402	-	2480	MHz
Channel Spacing	-	2	-	MHz
Number of RF channel	-	40	-	-
Output power	TBD	TBD	TBD	dBm
Modulation Characteristics				
1) $\Delta f1_{avg}$	225	-	275	kHz
2) $\Delta f2_{max}$ (at 99.9%)	185	-	-	kHz
3) $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8	-	-	-
Carrier frequency offset and drift				
1) Frequency offset	-	-	150	kHz
2) Frequency drift	-	-	50	kHz
3) Drift rate	-	-	20	kHz
Receiver sensitivity (PER < 30.8%)	-	-	-70	dBm
Maximum input signal level (PER < 30.8%)	-10	-	-	dBm
PER Report Integrity (-30dBm input)	50	-	65.4	%

15. Land Pattern



Top View. Unit : mm

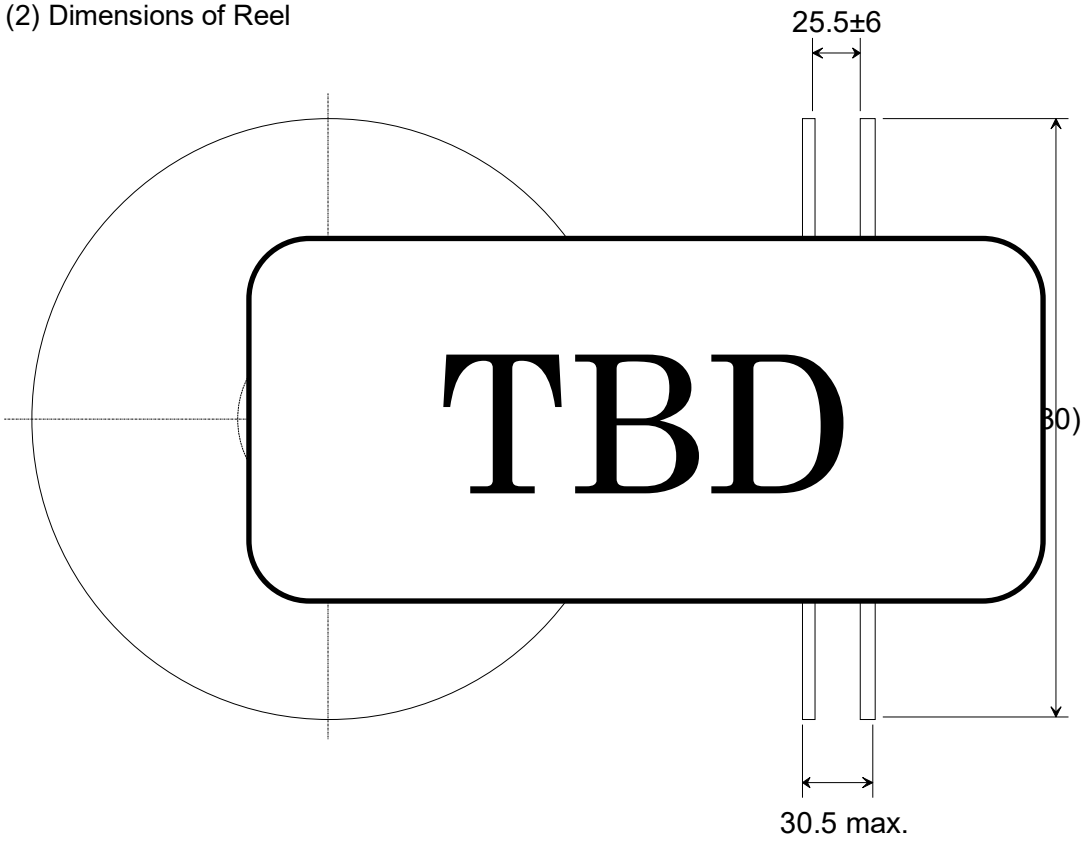
16. TAPE AND REEL PACKING

(1) Dimensions of Tape (Plastic tape)

TBD

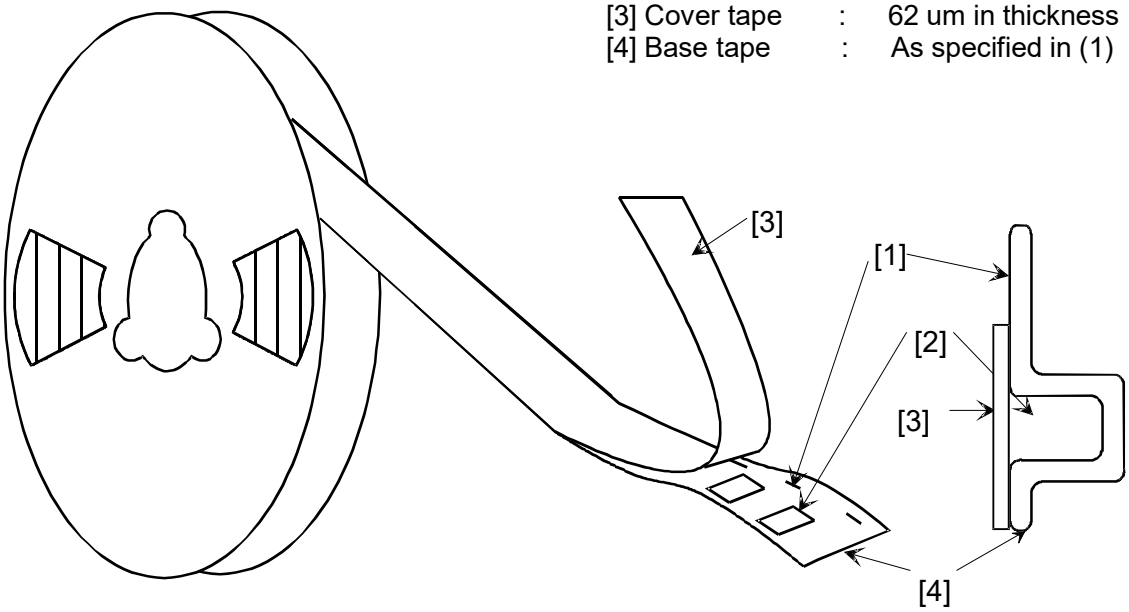
1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
2) Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.15mm
3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

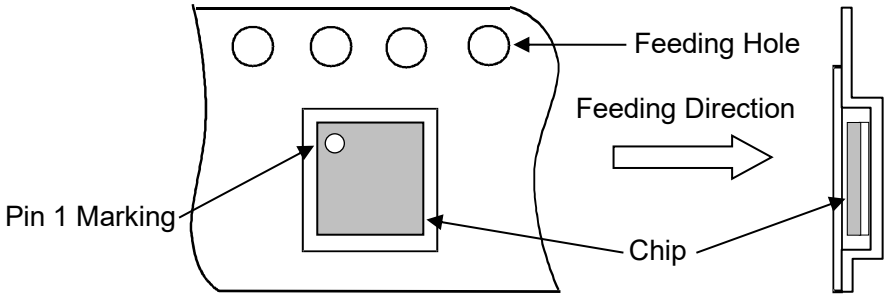
(2) Dimensions of Reel



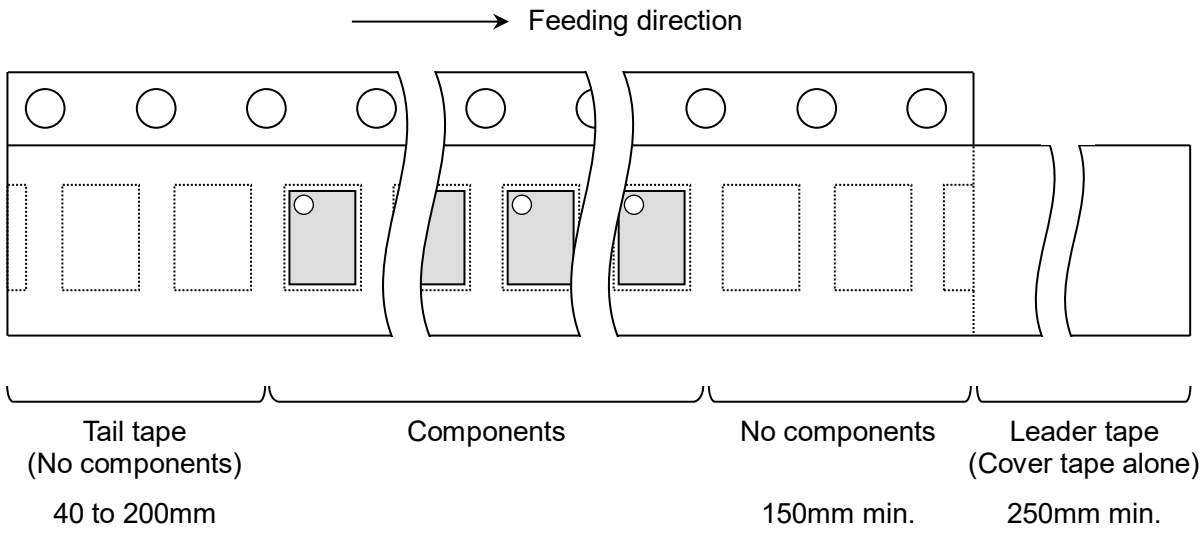
(3) Taping Diagrams

[1] Feeding Hole : As specified in (1)
[2] Hole for chip : As specified in (1)
[3] Cover tape : 62 um in thickness
[4] Base tape : As specified in (1)





(4) Leader and Tail tape



(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

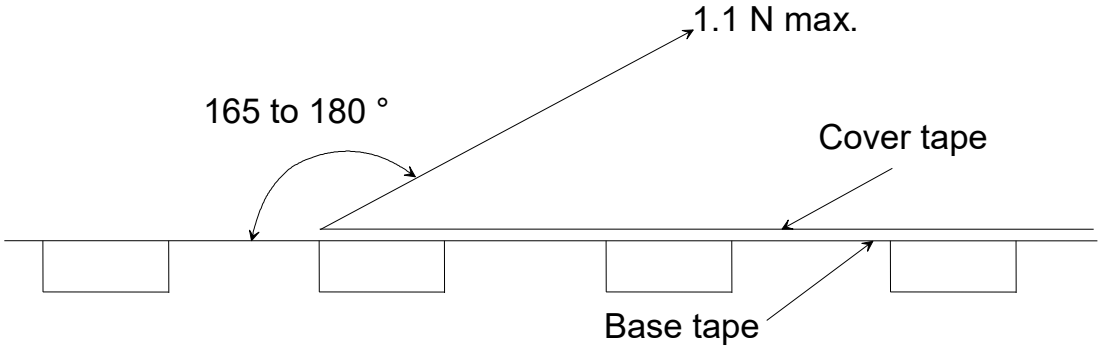
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape: 5N min.

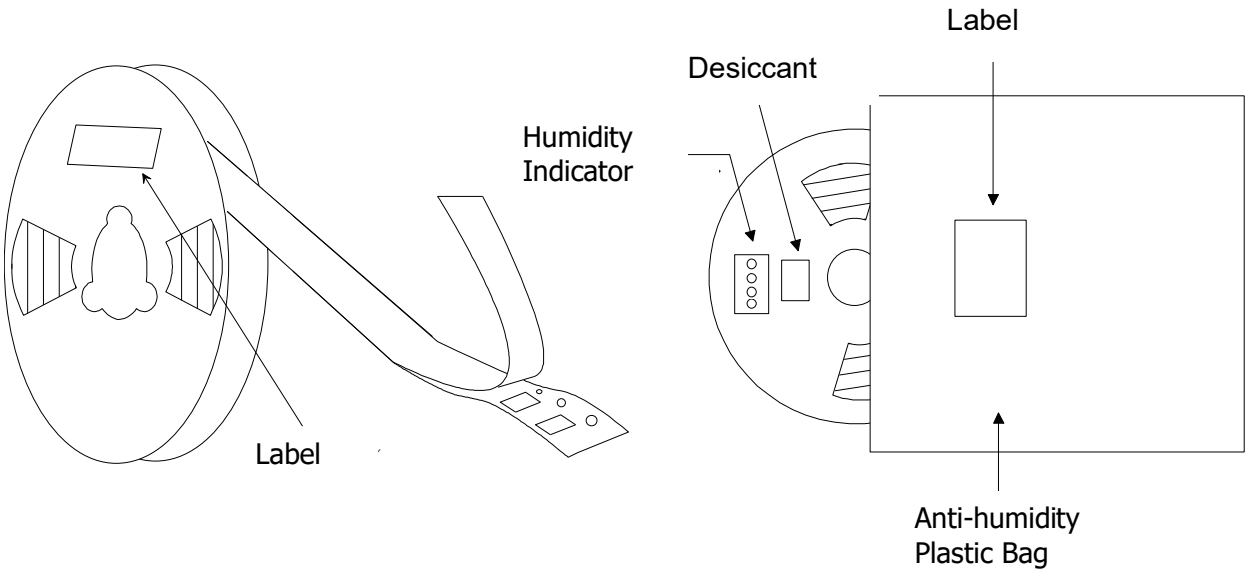
(8) Packaging unit : 1000pcs./ reel

(9) material - Base tape : Plastic
Reel : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force: 1.1N max. in the direction of peeling as shown below.



(11) PACKAGE (Humidity proof packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

17. NOTICE

17.1. Storage Conditions:

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time
The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

17.2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

17.3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

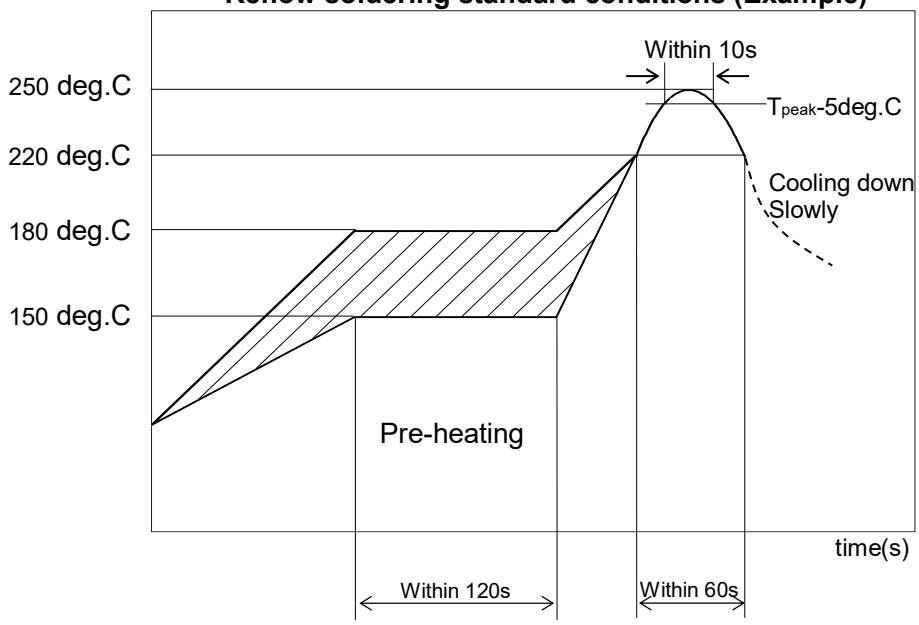
17.4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

17.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.
Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Reflow soldering standard conditions (Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

17.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

17.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

17.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

18. PRECONDITION TO USE OUR PRODUCTS

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.
All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.
Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.
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- Aerospace equipment
- Undersea equipment.
- Power plant control equipment
- Medical equipment.
- Traffic signal equipment.
- Burning / explosion control equipment
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

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Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.
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