

## DESCRIPTION

The MPQ6411 is a windowed watchdog timer. It is used to reset and monitor the microcontroller. In normal operation, the MCU sends a trigger signal to the MPQ6411 in a defined time window cyclically. A missing or fault trigger signal causes the watchdog to reset the MCU.

The MPQ6411 provides a reset signal (low-level voltage) to the MCU during power-up or under voltage. Its power supply (VCC) has 5V and 3.3V options.

By setting MODE to high or low, the watchdog operates in long window mode or short window mode; the window is programmable.

The MPQ6411 is available in SOIC8 package.

## FEATURES

- Windowed Watchdog
- Power-On Reset during Power-Up and Under Voltage
- Programmable Short Window Mode or Long Window Mode
- Watchdog Disable Function
- Low Shutdown Mode Current
- SOIC8 Package
- Available in AEC-Q100 Grade 1

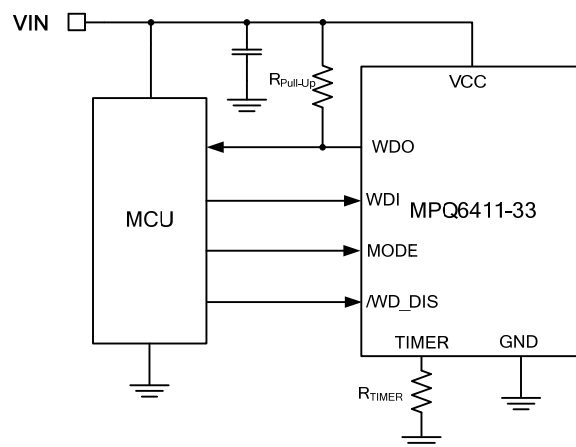
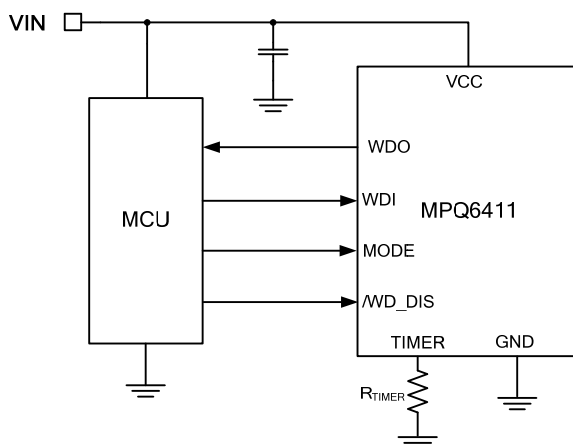
## APPLICATIONS

- Automotive Systems
- Industrial Systems

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## TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ6411GS	SOIC-8	<i>See Below</i>
MPQ6411GS-AEC1	SOIC-8	
MPQ6411GS-33**	SOIC-8	
MPQ6411GS-33-AEC1**	SOIC-8	

\* For Tape & Reel, add suffix –Z (e.g. MPQ6411GS–Z);

\*\* Pre-release

## TOP MARKING

**MP6411**  
**LLLLLLLL**  
**MPSYWW**

MP6411: Product code of MPQ6411GS and MPQ6411GS-AEC1

LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

## TOP MARKING

**M6411-33**  
**LLLLLLLL**  
**MPSYWW**

M6411-33: Product code of MPQ6411GS-33 and MPQ6411GS-33-AEC1

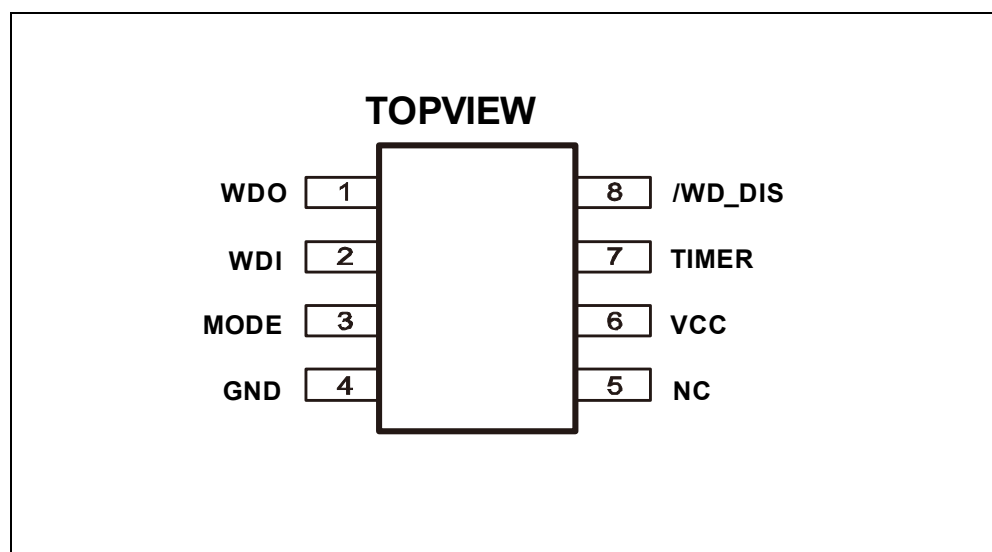
LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

# PACKAGE REFERENCE



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

All pins .....-0.3V to +6V  
Continuous power dissipation ( $T_A = +25^{\circ}\text{C}$ ) <sup>(2)</sup>  
SOIC8.....1.3W  
Junction temperature.....150°C  
Lead temperature .....260°C  
Storage temperature..... -65°C to +150°C

## Recommended Operating Conditions

Supply voltage (VCC)  
MPQ6411..... 5V  
MPQ6411-33.....3.3V  
Operating junction temp. ( $T_J$ )..... -40°C to 125°C

**Thermal Resistance** <sup>(3)</sup>       $\theta_{JA}$        $\theta_{JC}$   
SOIC-8.....96.....45...°C/W

### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX)- $T_A$ )/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) Measured on JESD51-7, 4-layer PCB.

# ELECTRICAL CHARACTERISTICS

VCC = 5V for MPQ6411, VCC = 3.3V for MPQ6411-33, T<sub>J</sub> = - 40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Timer voltage		R <sub>TIMER</sub> = 51k		0.3		V
Quiescent current	I <sub>Q</sub>	MPQ6411, R <sub>TIMER</sub> = 100k		16	19	μA
		MPQ6411-33, R <sub>TIMER</sub> = 100k		10	14	
		MPQ6411, R <sub>TIMER</sub> = 51k		25	32	μA
		MPQ6411-33, R <sub>TIMER</sub> = 51k		14	18	
Power on reset threshold	V <sub>POR-HIGH</sub>	MPQ6411, WDO goes high with rising VCC	4.4	4.6	4.8	V
		MPQ6411-33, WDO goes high with rising VCC	2.9	3	3.1	
	V <sub>POR-LOW</sub>	MPQ6411, WDO goes low with falling VCC	4.3	4.5	4.7	V
		MPQ6411-33, WDO goes low with falling VCC	2.8	2.9	3	
Timing						
Single period	T	R <sub>TIMER</sub> = 51k	-10%	880	+10%	μs
Power on delay <sup>(4)</sup>	t <sub>0</sub>	R <sub>TIMER</sub> = 51k		10		cycle
Sync signal monitoring time <sup>(4)</sup>	t <sub>1</sub>	R <sub>TIMER</sub> = 51k		450		cycle
Watchdog window close time (short mode) <sup>(4)</sup>	t <sub>2</sub>	R <sub>TIMER</sub> = 51k, MODE = low		15		cycle
Watchdog window open time (short mode) <sup>(4)</sup>	t <sub>3</sub>	R <sub>TIMER</sub> = 51k, MODE = low		10		cycle
Watchdog window close time (long mode) <sup>(4)</sup>	t <sub>4</sub>	R <sub>TIMER</sub> = 51k, MODE = high		1500		cycle
Watchdog window open time (long mode) <sup>(4)</sup>	t <sub>5</sub>	R <sub>TIMER</sub> = 51k, MODE = high		1000		cycle
WDO reset pulse width <sup>(4)</sup>	t <sub>6</sub>	R <sub>TIMER</sub> = 51k		4		cycle
WDI_OK pulse width			10		5000	μs
Input and Output						
WDI logic high		MPQ6411	3.2			V
		MPQ6411-33	2.1			
WDI logic low		MPQ6411			0.8	V
		MPQ6411-33			0.6	
MODE logic high		MPQ6411	3.2			V
		MPQ6411-33	2.1			
MODE logic low		MPQ6411			0.8	V
		MPQ6411-33			0.6	

# ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 5V for MPQ6411, VCC = 3.3V for MPQ6411-33, T<sub>J</sub> = - 40°C to +125°C, unless otherwise noted.

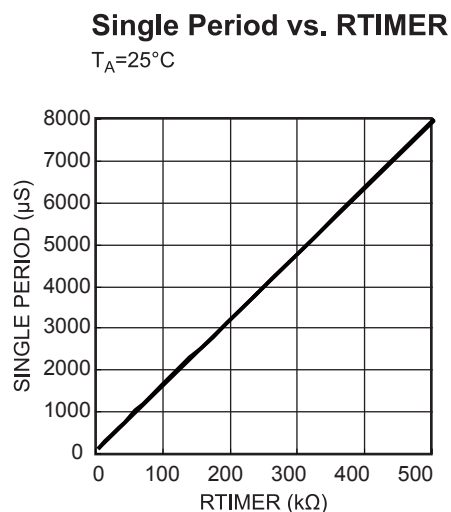
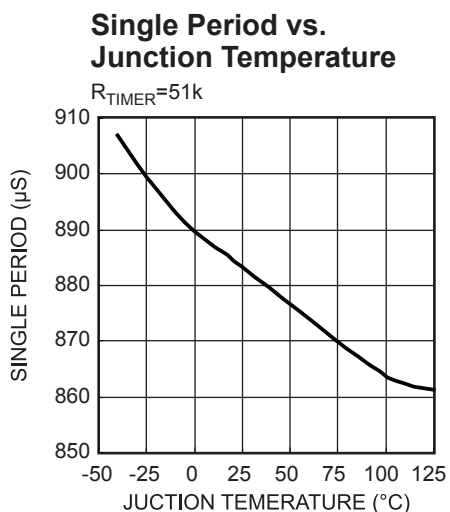
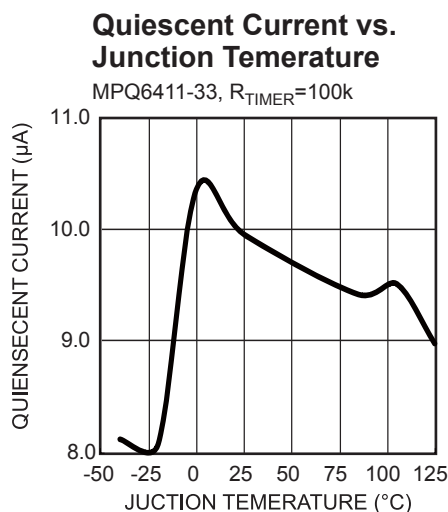
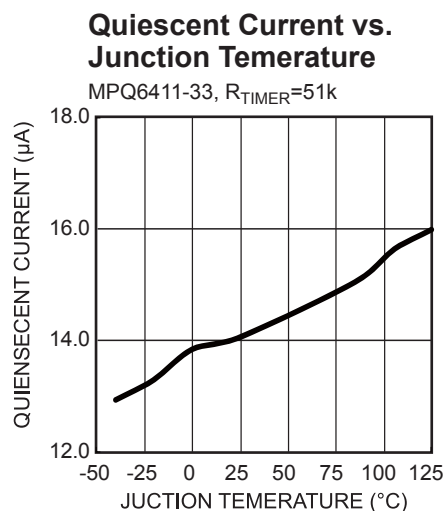
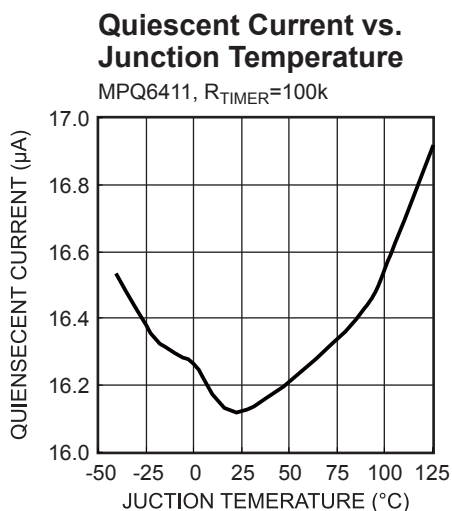
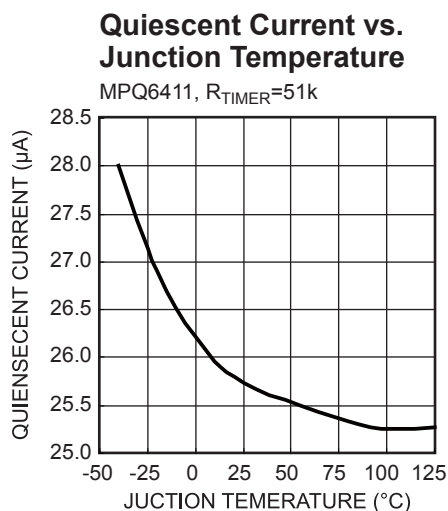
Parameter	Symbol	Condition	Min	Typ	Max	Units
MODE input Current		MPQ6411, MODE = 5V		0.1	1	μA
		MPQ6411-33, MODE = 3.3V				
		MPQ6411, MODE = 0V		5	8	μA
		MPQ6411-33, MODE = 0V				
/WD_DIS logic high		MPQ6411	3.2			V
		MPQ6411-33	2.1			
/WD_DIS logic low		MPQ6411			0.8	V
		MPQ6411-33			0.6	
/WD_DIS input Current		MPQ6411, WD_DIS = 5V		0.1	1	μA
		MPQ6411-33, WD_DIS = 3.3V				
		MPQ6411, WD_DIS = 0V		5	8	μA
		MPQ6411-33, WD_DIS = 0V				
WDO high		MPQ6411, VCC = 5V, I <sub>WDO</sub> = 1mA	V <sub>CC</sub> -0.2			V
		MPQ6411-33, VCC=3.3V, R <sub>Pull-Up</sub> =100KΩ	3.29			
WDO low		MPQ6411, VCC = 5V, I <sub>WDO</sub> = 1mA			0.2	V
		MPQ6411, VCC = 1V, I <sub>WDO</sub> = 300μA			0.1	
		MPQ6411-33, Sink 1mA Current			0.1	

## Notes:

4) Derived from bench characterization. Not tested in production.

## TYPICAL CHARACTERISTICS

VCC=5V for MPQ6411, VCC=3.3V for MPQ6411-33, unless otherwise noted.



## PIN FUNCTION

Pin #	Name	Description
1	WDO	Watchdog output. WDO outputs a reset signal to the MCU. MPQ6411 WDO is the output of a inverter, it is not must to connect WDO to VCC or another voltage source through a resistor. MPQ6411-33 WDO is the open drain of a MOSFET and should be connected to VCC or another voltage source through a resistor (e.g.100kΩ).
2	WDI	Watchdog input. WDI receives the trigger signal from the MCU.
3	MODE	Mode switching pin. Pull MODE high to make the watchdog operate in long window mode; pull MODE low to make it work in short window mode. MODE has a weak internal pull-up.
4	GND	Ground.
5	NC	Not connected.
6	VCC	Power input.
7	TIMER	Watchdog timer pin. TIMER sets the time-out with an external resistor
8	/WD_DIS	Watchdog disable pin. Pull /WD_DIS low to disable the watchdog; pull /WD_DIS high to enable the watchdog. It has a weak internal pull-up.

## FUNCTIONAL BLOCK DIAGRAM

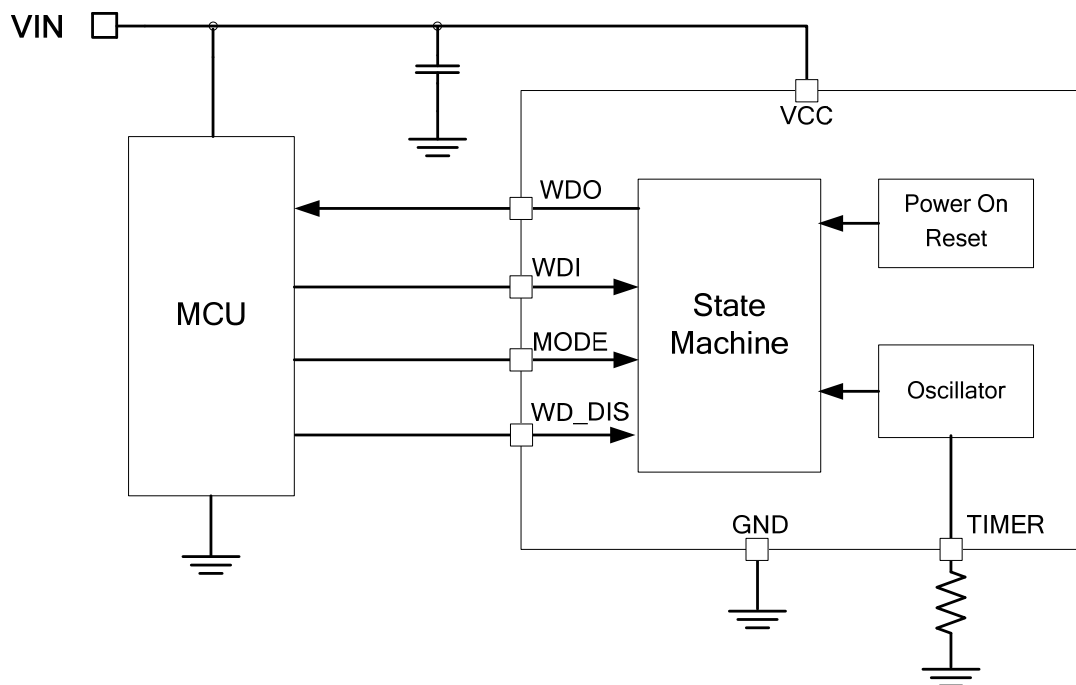
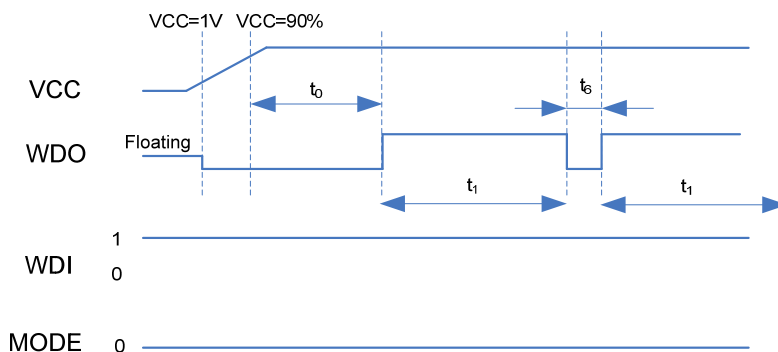


Figure 1: Functional Block Diagram

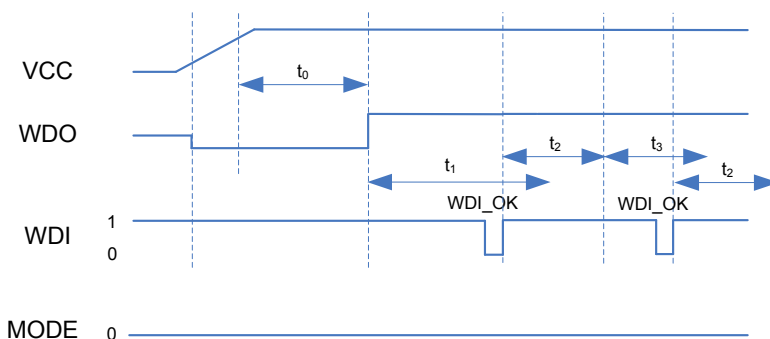


# TIMING DIAGRAM

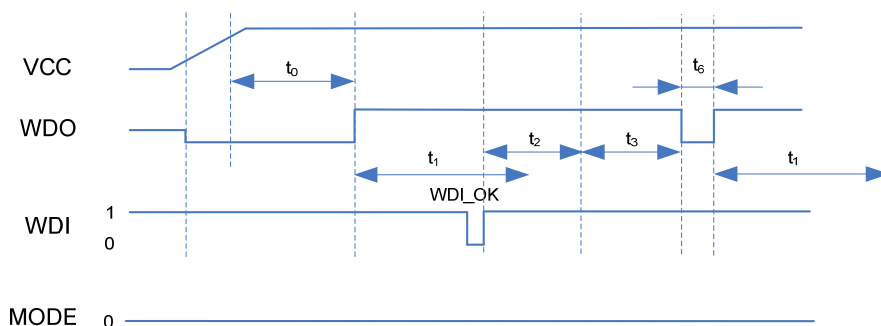
## Power-on reset and no sync signal



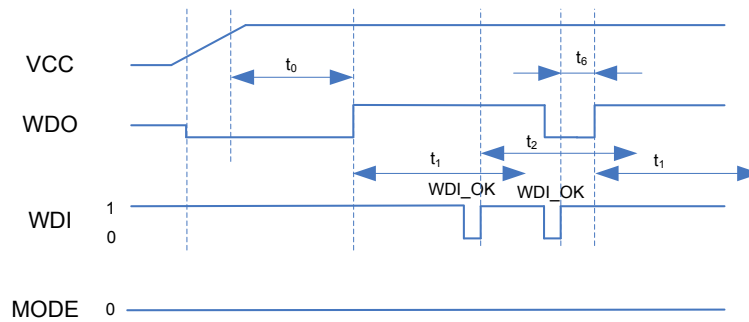
## Synchronized by WDI and triggered in open window (MODE=0, short window mode)



## Synchronized by WDI and no trigger signal (MODE=0, short window mode)

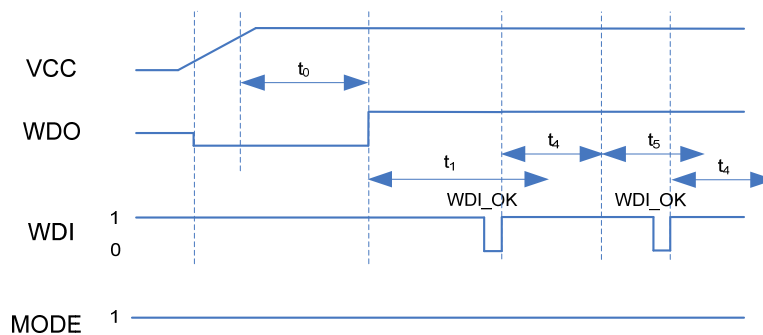


**Synchronized by WDI and triggered in closed window (MODE=0, short window mode)**

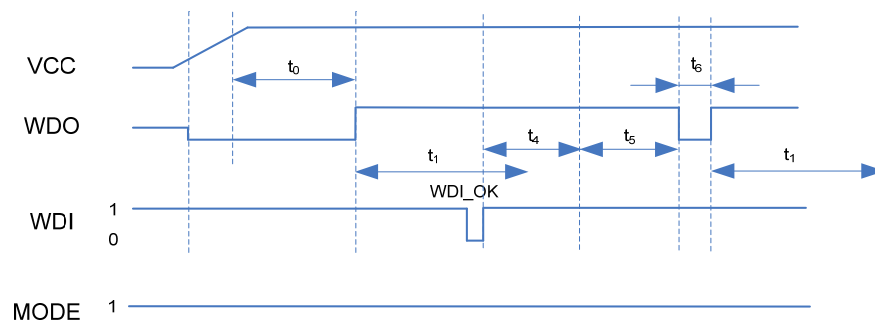


Note: When the WDI\_OK rising edge that comes at WDO is low, the  $t_6$  timer will be reset. Therefore, in the situation above, the WDO reset signal maintains a  $t_6 + \text{WDI\_OK}$  time.

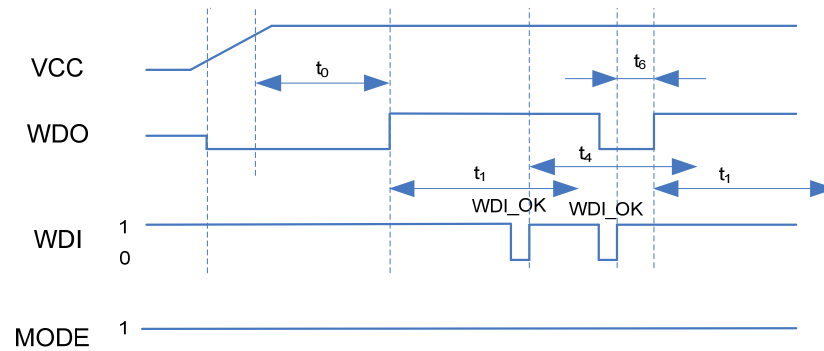
**Synchronized by WDI and triggered in open window (MODE=1, long window mode)**



**Synchronized by WDI and no trigger signal (MODE=1, long window mode)**

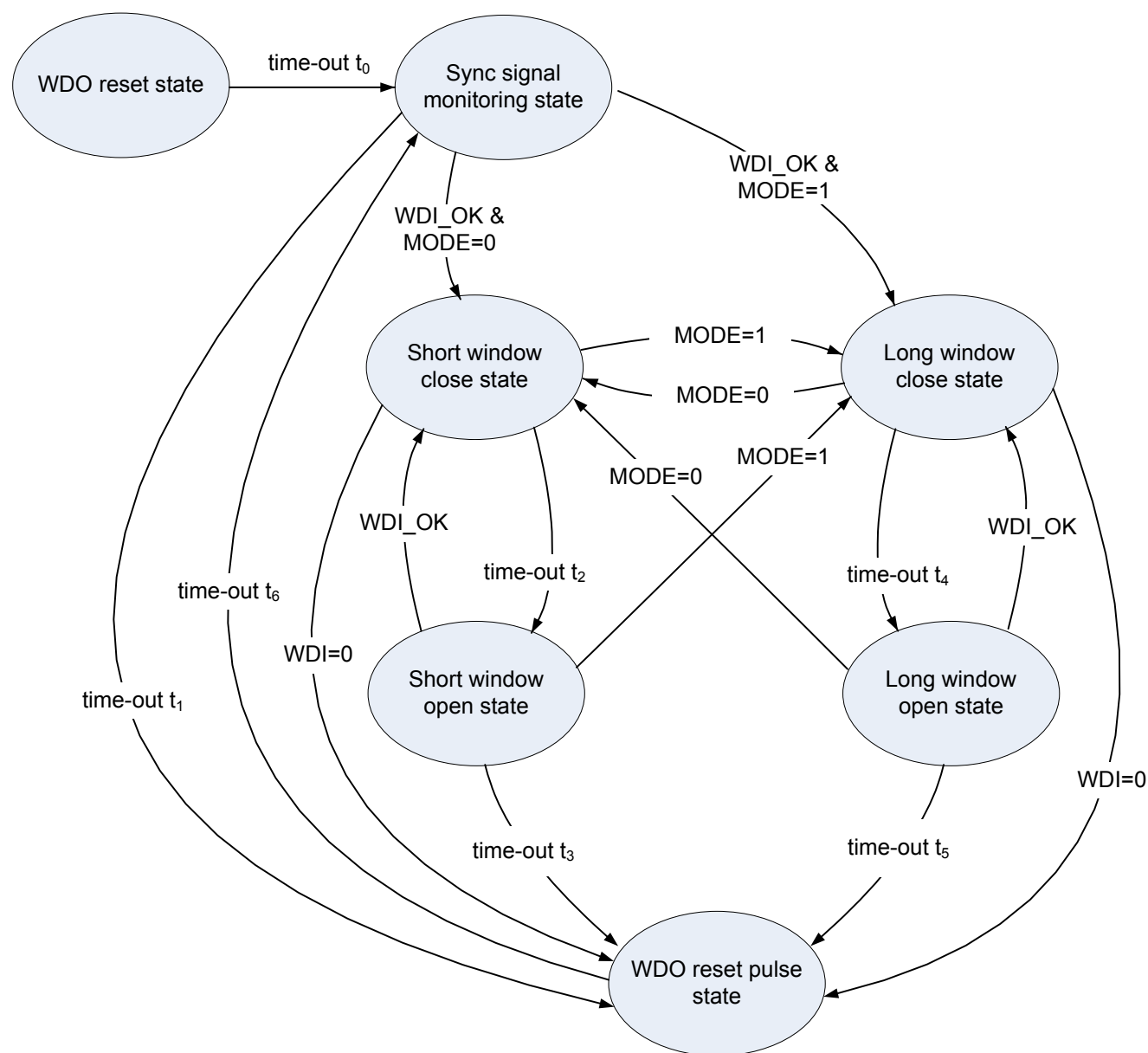


**Synchronized by WDI and triggered in closed window (MODE=1, long window mode)**



Note: When the WDI\_OK rising edge that comes at WDO is low, the  $t_6$  timer will be reset. Therefore, in the situation above, the WDO reset signal maintains a  $t_6 + \text{WDI\_OK}$  time.

# STATE DIAGRAM



**Note:** The state diagram above does not include if a WDI error occurs.

## OPERATION

### Supply Voltage

VCC= 5V±10% is recommended for MPQ6411 /MPQ6411-AEC1 normal operation; while VCC= 3.3V±10% is recommended for MPQ6411-33/MPQ6411-33-AEC1 normal operation. WDO is pulled low when VCC rises to 1V or above. After VCC rises to 90% (typically), WDO will remain at a low level for  $t_0$  to reset the MCU.

### TIMER

Period T (μs):

$$T(\mu s) = 15.75 \times R_{\text{TIMER}}(k\Omega) + 73.5$$

$R_{\text{TIMER}}(k\Omega)$ :

$$R_{\text{TIMER}}(k\Omega) = 0.063 \times T(\mu s) - 4.67$$

For example:  $R_{\text{TIMER}}=51k\Omega$ ,  $T \approx 0.88ms$

### Monitor MCU Synchronization Signal

When the watchdog is in a “sync signal monitoring state,” the following will occur:

- ◆ If the watchdog IC receives a WDI\_OK signal from the MCU within  $t_1$  (WDI remains low for 10μs to 5ms), the timer will be reset, and the watchdog works in normal operation.
- ◆ If the watchdog does not receive the WDI\_OK signal from the MCU during  $t_1$ , it will generate a reset signal and go into “sync signal monitor state” again.

### Short Window Mode

If the MCU and watchdog are synchronized correctly and MODE is low, the watchdog will work in short window mode:

- ◆ If WDI\_OK is received in a window close state ( $t_2$ ), the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- ◆ If WDI\_OK is received in a window open state ( $t_3$ ), the watchdog goes into a window

close state. The MCU works in normal operation in this situation.

- ◆ If no WDI\_OK signal is received in  $t_2+t_3$ , the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- ◆ If MODE is pulled high during short window mode, the watchdog will go into long window mode.

### Long Window Mode

If the MCU and watchdog are synchronized correctly and MODE is high, the watchdog will operate in long window mode, and the following will occur:

- ◆ If WDI\_OK is received in a window close state ( $t_4$ ), the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- ◆ If WDI\_OK is received in a window open state ( $t_5$ ), the watchdog goes into a window close state. The MCU works in normal operation in this situation.
- ◆ If no WDI\_OK signal is received in  $t_4+t_5$ , the watchdog outputs a reset signal and goes into a sync signal monitoring state.
- ◆ If MODE is pulled low during a long window mode, the watchdog will go into a short window mode.

### Watchdog Disable

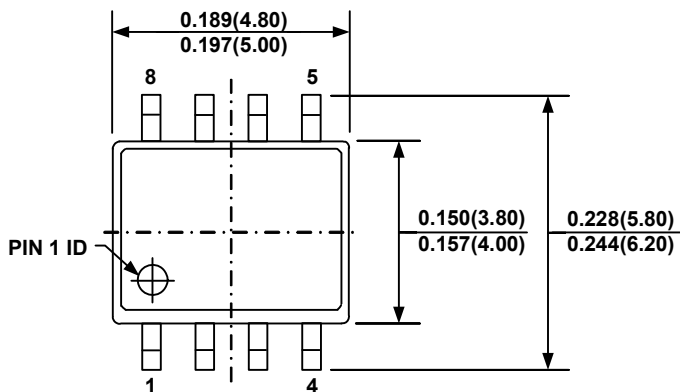
Pull /WD\_DIS low to disable the watchdog; pull it high to enable the watchdog. /WD\_DIS has a weak internal pull-up, so the watchdog is enabled if /WD\_DIS is left open.

### WDI Error

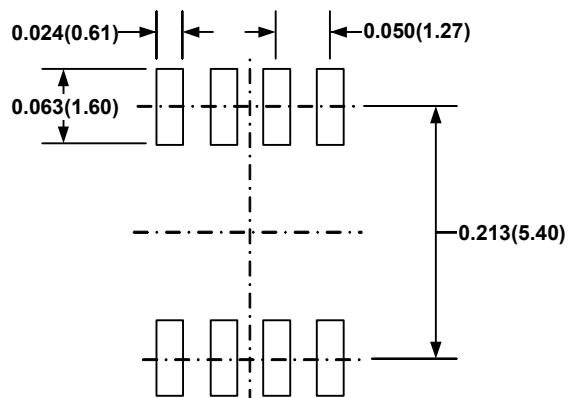
If a WDI signal remains at a low level for longer than the maximum WDI\_OK pulse width, it is regarded as an error. When this error occurs, WDO is pulled down until WDI returns to a high level.

# PACKAGE INFORMATION

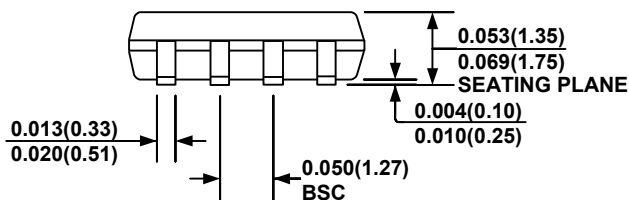
## SOIC-8



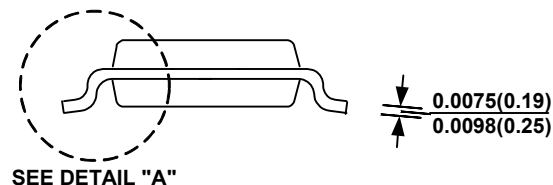
**TOP VIEW**



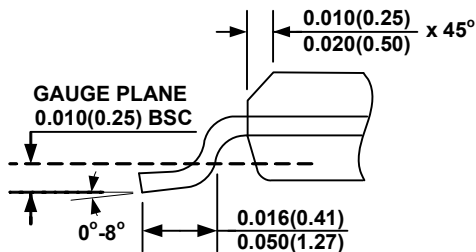
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

## NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

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