



MPQ4590

640V Non-Isolated Regulator, Up to 400mA Output Current AEC-Q100 Qualified

DESCRIPTION

The MPQ4590 is a primary-side regulator that provides accurate constant voltage (CV) regulation without an optocoupler. The MPQ4590 supports buck, buck-boost, boost, and flyback topologies and has an integrated 640V MOSFET to simplify structure and reduce costs. These features make the MPQ4590 an ideal regulator for low-power applications, such as home appliances and standby power.

The MPQ4590 is a green-mode operation regulator. Both the peak current and switching frequency decrease as the load decreases. This feature provides excellent efficiency at light load and improves the overall average efficiency.

Full protection features include thermal shutdown (OTP), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open-loop protection.

The MPQ4590 is available in a SOIC-8 package.

FEATURES

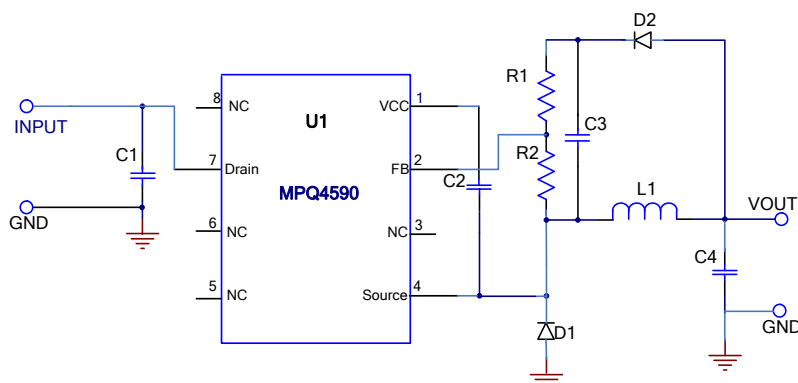
- Guaranteed Industrial/Automotive Temp Range Limits
- Primary-Side CV Control Supporting Buck, Buck-Boost, Boost, and Flyback Topologies
- Integrated 640V/13.5Ω MOSFET and Current Source
- <30mW No-Load Power Consumption
- Up to 5W Output Power
- Maximum DCM Output Current Less than 250mA
- Maximum CCM Output Current Less than 400mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak-Current Compression
- Internally Biased VCC
- OTP, UVLO, OLP, SCP, Open-Loop Protection
- Available in a SOIC-8 Package
- Available in AEC-Q100 Qualified Grade

APPLICATIONS

- Automotive PTC Heater
- Electric or Hybrid Cars
- Industrial Controls
- Standby Power

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ4590GS*	SOIC-8	See Below
MPQ4590GS-AEC1**		See Below

* For Tape & Reel, add suffix -Z (e.g.: MPQ4590GS-Z).

** For Tape & Reel, add suffix -Z (e.g.: MPQ4590GS-AEC1-Z).

TOP MARKING (MPQ4590GS & MPQ4590GS-AEC1)

MP4590
LLLLLLLL
MPSYWW

MP4590: Part number

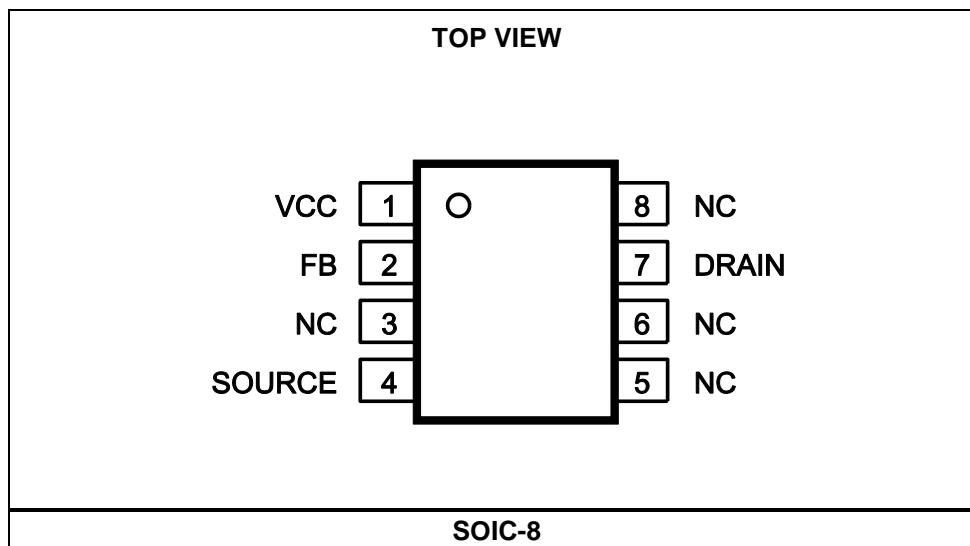
LLLLLLLL: Lot number

MPS: MPS prefix

Y: Year code

WW: Week code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin # SOIC-8	Name	Description
1	VCC	Control circuit power supply.
2	FB	Regulator feedback.
3, 5, 6, 8	NC	No connection.
4	SOURCE	Internal power MOSFET source. SOURCE is the ground reference for VCC and FB.
7	DRAIN	Internal power MOSFET drain. DRAIN is the high-voltage current source input.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Drain to source -0.3V to 640V
 All other pins -0.3V to 6.5V
 Continuous power dissipation ($T_A = +25^{\circ}\text{C}$) ⁽²⁾
 SOIC-8 1W
 Junction temperature 150°C
 Lead temperature 260°C
 Storage temperature -60°C to $+150^{\circ}\text{C}$
 ESD capability human body model 2.0kV
 ESD charged device model
 SOIC-8 2.0kV

Recommended Operating Conditions

Operating junction temp. (T_J) .. -40°C to $+125^{\circ}\text{C}$
 Operating VCC range 5.3V to 5.6V

Thermal Resistance ⁽³⁾ θ_{JA} θ_{JC}
 SOIC-8 96 45 ... $^{\circ}\text{C/W}$

NOTES:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(\text{MAX})$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowance continuous power dissipation at any ambient temperature is calculated by $PD(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$. Exceeding the maximum allowance power dissipation produces an excessive die temperature, causing the device to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VCC = 5.5V, T_J = -40°C~125°C, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Start-Up Current Source and Internal MOSFET (DRAIN)						
Internal regulator supply current	I _{regulator}	V _{CC} = 4V, V _{DRAIN} = 100V	2	4.1	6	mA
Drain pin leakage current	I _{Leak}	V _{CC} = 5.8V, V _{DRAIN} = 400V, T _J = 25°C		10	17	μA
		V _{CC} = 5.8V, V _{DRAIN} = 400V, T _J = -40°C - 125°C			20	
Breakdown voltage	V _{(BR)DSS}	T _J = 25°C	700			V
On resistance	R _{on}	T _J = 25°C		13.5	17	Ω
		T _J = 125°C		23	28	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator stops	VCC _{OFF}	T _J = 25°C	5.4	5.6	6	V
		T _J = -40°C - 125°C	5.2		6.2	
VCC level (decreasing) where the internal regulator turns on	VCC _{ON}	T _J = 25°C	5.1	5.3	5.7	V
		T _J = -40°C - 125°C	4.9		5.9	
VCC regulator on and off hysteresis			130	250		mV
VCC level (decreasing) where the IC stops	VCC _{stop}		3	3.4	3.6	V
VCC level (decreasing) where the protection phase ends	VCC _{pro}			2.5	2.8	V
Internal IC consumption	I _{CC}	f _s = 28kHz, T _J = 25°C			720	μA
		f _s = 28kHz, T _J = -40°C - 125°C			750	
Internal IC consumption (no switching)	I _{CC}				200	μA
Internal IC consumption, latch-off phase	I _{CC} LATCH	V _{CC} = 5.3V, T _J = 25°C		16	24	μA
		V _{CC} = 5.3V, T _J = -40°C - 125°C			26	
Internal Current Sense						
Peak current limit	I _{Limit}	T _J = 25°C	600	660	720	mA
		T _J = -40°C - 125°C	480		840	
Leading-edge blanking	τ _{LEB1}			350		ns
SCP threshold	I _{SCP}	T _J = 25°C	750	900		mA
		T _J = -40°C - 125°C	540			
Leading-edge blanking for SCP ⁽⁴⁾	τ _{LEB2}			180		ns
Feedback Input (FB)						
Minimum off time	τ _{minoff}		9.5	12	15	μs
Maximum on time	τ _{manon}	T _J = 25°C	19	24	31	μs
		T _J = -40°C - 125°C	18		32	
Primary MOSFET feedback turn-on threshold	V _{FB}		2.45	2.55	2.65	V

ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 5.5V, T_J = -40°C~125°C, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

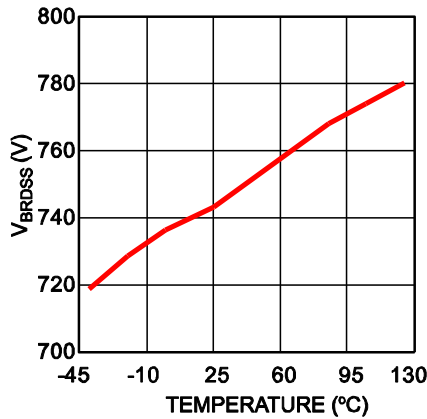
Parameter	Symbol	Condition	Min	Typ	Max	Units
OLP feedback trigger threshold	V _{FB_OLP}	T _J = 25°C	1.6	1.7	1.8	V
		T _J = -40°C - 125°C			1.85	
OLP delay time	T _{OLP}	f _s = 28kHz		220		ms
Open-loop detection	V _{OLD}		0.4	0.5	0.6	V
Thermal Shutdown						
Thermal shutdown threshold ⁽⁴⁾				150		°C
Thermal shutdown recovery hysteresis ⁽⁴⁾				30		°C

NOTE:

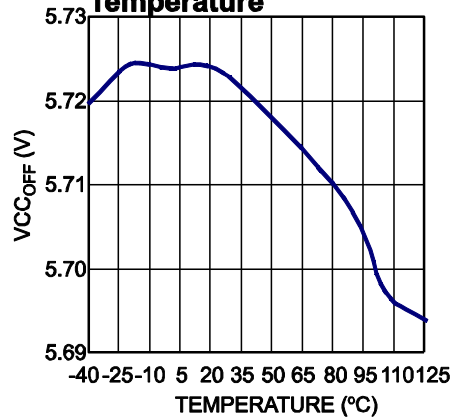
4) This parameter is guaranteed by design.

TYPICAL CHARACTERISTICS

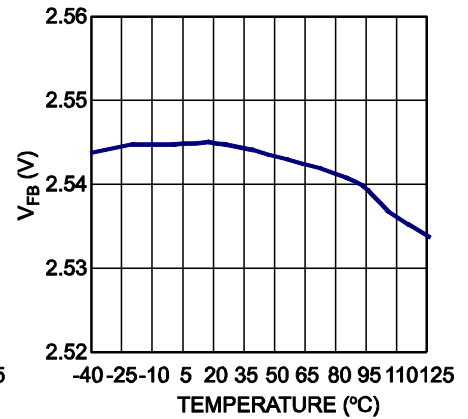
Breakdown Voltage vs. Temperature



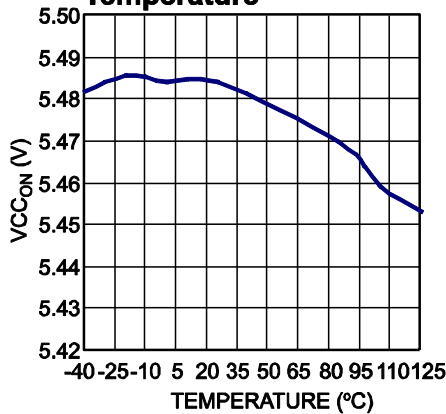
VCC Increasing Level at which the Internal Regulator Stops vs. Temperature



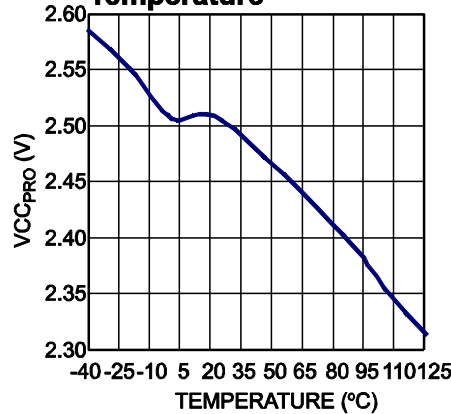
Feedback Voltage vs. Temperature



VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature



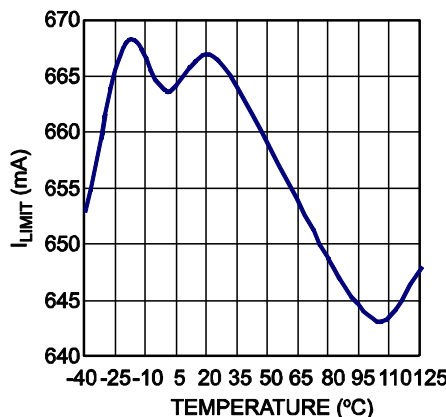
VCC Decreasing Level at which the Protection Phase Ends vs. Temperature



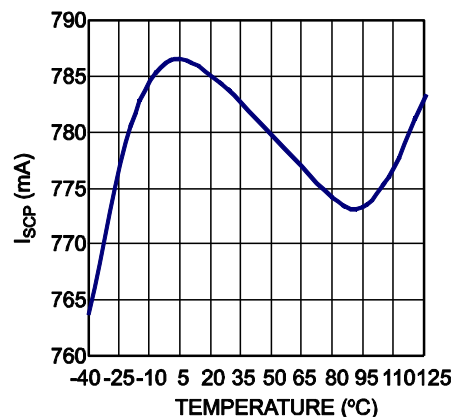
On State Resistance vs. Temperature



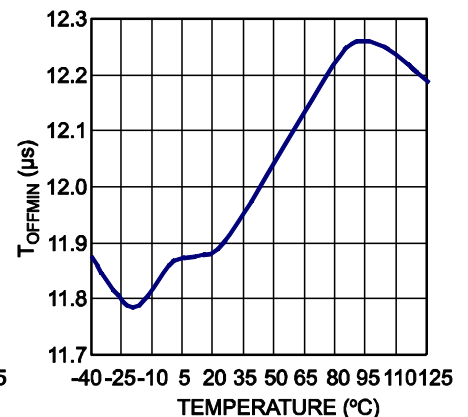
Peak Current Limit vs. Temperature



SCP Point vs. Temperature

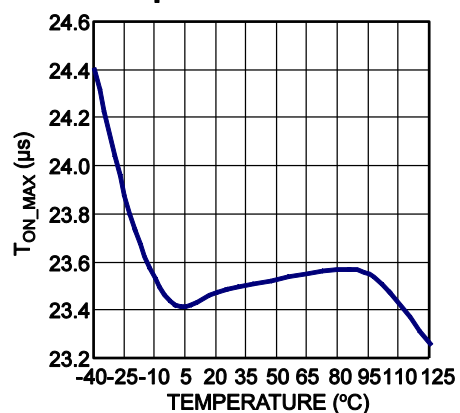


Minimum Off Time vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

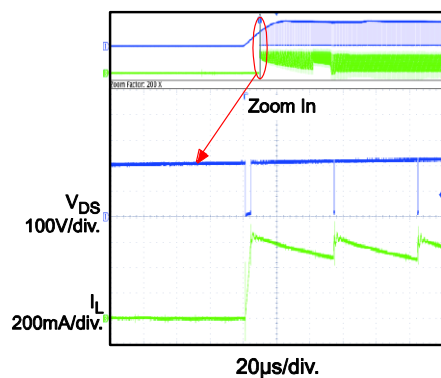
Maximum On Time vs. Temperature



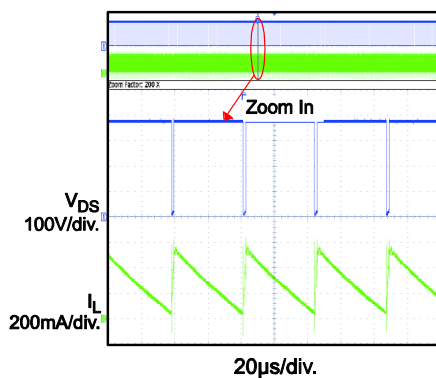
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 370V$, $V_{OUT} = 12V$, $I_{OUT} = 300mA$, $L = 1.2mH$, $C_{OUT} = 100\mu F$, $T_A = +25^{\circ}C$, unless otherwise noted.

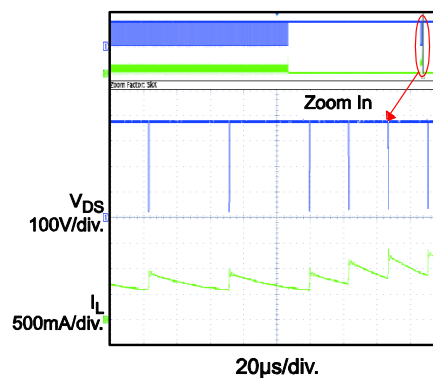
Start-Up



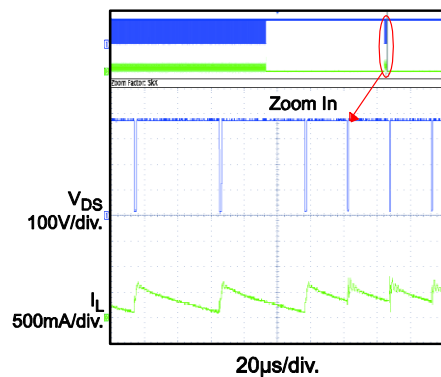
Normal Operation



SCP



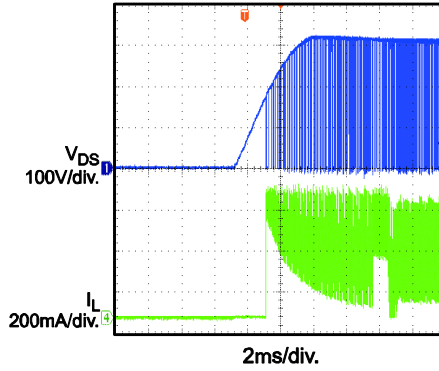
Open-Loop Detection



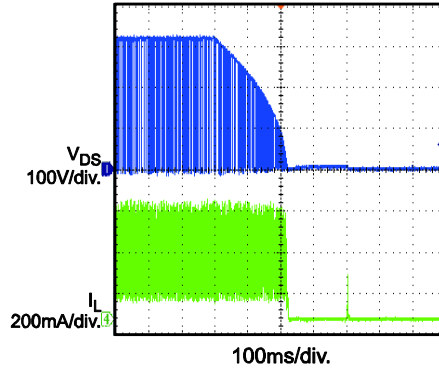
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 370V$, $V_{OUT} = 12V$, $I_{OUT} = 300mA$, $L = 1.2mH$, $C_{OUT} = 100\mu F$, $T_A = +25^{\circ}C$, unless otherwise noted.

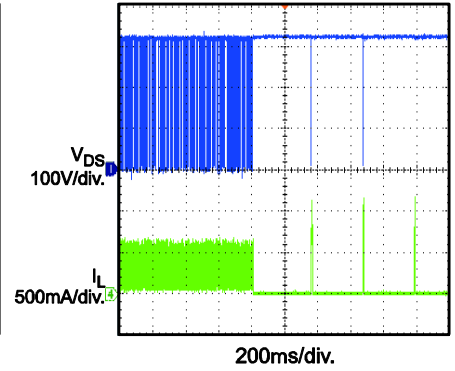
Input Power Start-Up



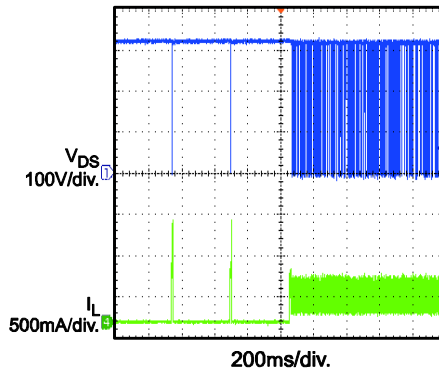
Input Power Shutdown



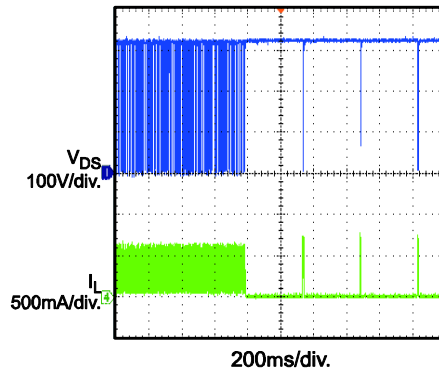
SCP Entry



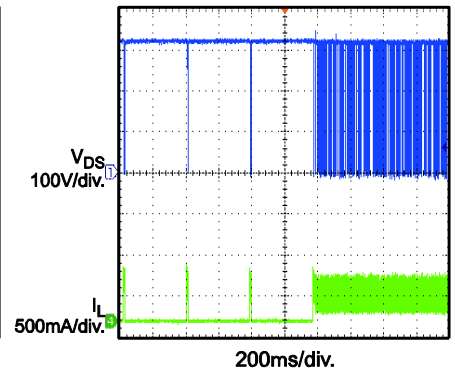
SCP Recovery



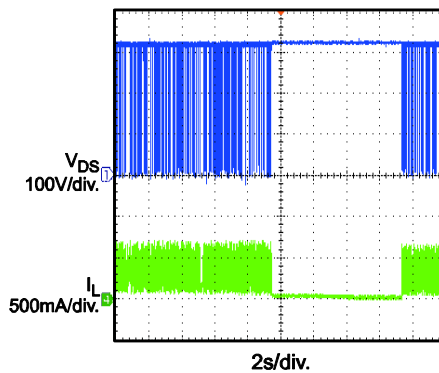
Open-Loop Detection Entry



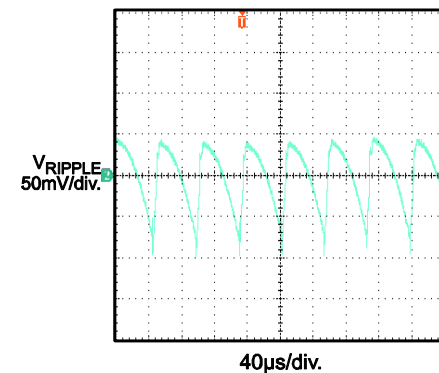
Open-Loop Detection Recovery



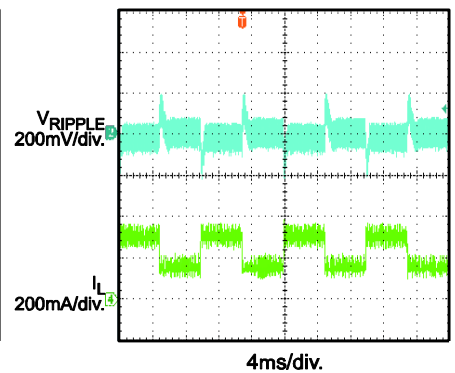
OTP



Output Ripple



Load Transient



The diagram illustrates the internal architecture of a power MOSFET driver. It features several interconnected functional blocks:

- Vcc**: The main power supply input, connected to the **Power Management** block.
- Drain**: The MOSFET drain terminal, connected to the **Start up unit** and the **Peak current Limitation** block.
- Source**: The MOSFET source terminal, connected to the **Protection Unit** and the **Peak current Limitation** block.
- Power Management**: Receives **Vcc** and provides control signals to the **Start up unit** and the **Driving Signal Management** block.
- Start up unit**: Interacts with **Power Management** and provides a signal to the **Driving Signal Management** block.
- Driving Signal Management**: The central control block that drives the MOSFET gate and receives feedback from the **Feedback control** and **Peak current Limitation** blocks.
- Feedback control**: Receives the **FB** (feedback) signal and provides input to the **Driving Signal Management** block.
- Protection Unit**: Monitors the **Source** terminal and provides input to the **Driving Signal Management** block.
- Peak current Limitation**: Monitors the **Drain** and **Source** terminals to prevent overcurrent and provides input to the **Driving Signal Management** block.

 The MOSFET symbol is shown with its gate connected to the **Driving Signal Management** block, its drain to **Drain**, and its source to **Source**.

Figure 1: Functional Block Diagram

OPERATION

The MPQ4590 is a green-mode-operation regulator. The peak current and the switching frequency both decrease as the load decreases. As a result, the MPQ4590 offers excellent light-load efficiency and improves average efficiency. The regulator operates with a minimal number of external components (see Figure 10).

Start-Up and Under-Voltage Lockout (UVLO)

The internal high-voltage regulator self-supplies the IC from DRAIN. When VCC reaches 5.6V, the IC begins switching, and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below 5.3V. A small capacitor (in the low μF range) can maintain VCC, lowering the capacitor cost.

The IC stops switching when VCC drops below 3.4V.

Under fault conditions (such as overload protection (OLP), short-circuit protection (SCP), and over-temperature protection (OTP)), the IC stops switching, and an internal current source ($\sim 16\mu\text{A}$) discharges the VCC capacitor. The internal high-voltage regulator will not charge the VCC capacitor until VCC drops below 2.4V. The restart time can be estimated using Equation (1):

$$\tau_{\text{restart}} = C_{\text{VCC}} \times \frac{V_{\text{CC}} - 2.4\text{V}}{16\mu\text{A}} + C_{\text{VCC}} \times \frac{5.6\text{V} - 2.4\text{V}}{4.1\text{mA}} \quad (1)$$

Soft Start (SS)

The IC stops operation when VCC drops below 3.4V. The IC begins operation when VCC charges to 5.6V. Whenever the chip starts operation, there is a soft-start period. Soft start prevents the inductor current from overshooting by limiting the minimum off time.

The MPQ4590 adopts a 2-phase minimum off-time limit soft start. Each soft-start phase retains 128 switching cycles. During soft-start, the off time limit shortens gradually from 48 μs to 24 μs to the 12 μs normal operation off time limit (see Figure 2).

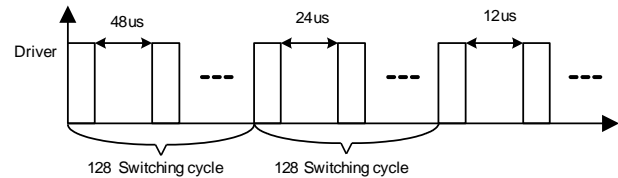


Figure 2: τ_{minoff} at Start-Up

Constant Voltage Operation

The MPQ4590 acts as a fully integrated regulator when used in the buck topology. The MPQ4590 regulates the output voltage by monitoring the sampling capacitor.

At the beginning of each cycle, the integrated MOSFET turns on while the feedback voltage drops below the 2.55V reference voltage, which indicates an insufficient output voltage. The peak current limitation determines the on period. After the on period elapses, the integrated MOSFET turns off. The sampling capacitor (C3) voltage is charged to the output voltage when the freewheeling diode (D1) turns on. In this way, the sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation under continuous conduction mode (CCM).

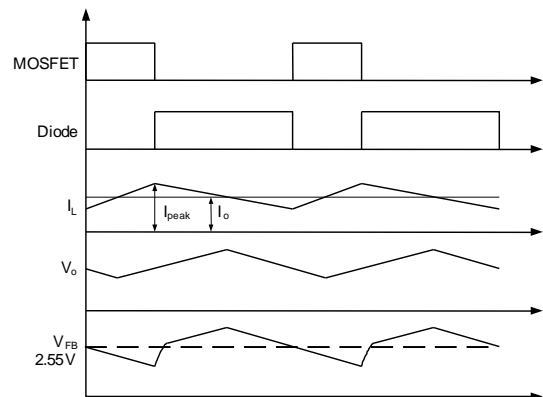


Figure 3: V_{FB} vs. V_{O}

The output voltage can be determined with Equation (2):

$$V_{\text{O}} = 2.55\text{V} \times \frac{R1 + R2}{R2} \quad (2)$$

Frequency Foldback and Peak Current Compression

The MPQ4590 remains highly efficient in light-load conditions by reducing the switching frequency automatically.

Under light-load or no-load conditions, the output voltage drops very slowly, which increases the MOSFET off time. This decreases the frequency as the load decreases.

Determine the switching frequency with Equation (3) for CCM and Equation (4) for discontinuous conduction mode (DCM):

$$f_s = \frac{(V_{in} - V_o)}{2L(I_{peak} - I_o)} \cdot \frac{V_o}{V_{in}} \quad (3)$$

$$f_s = \frac{2(V_{in} - V_o)}{LI_{peak}^2} \cdot \frac{I_o V_o}{V_{in}} \quad (4)$$

Simultaneously, the peak current limit decreases from 660mA as the off-time increases. In standby mode, the frequency and the peak current are both minimized, allowing for a smaller dummy load. Peak-current compression helps further reduce no-load consumption. The peak current limit can be estimated with Equation (5):

$$I_{Peak} = 660\text{mA} - (2.4\text{mA}/\mu\text{s}) \times (\tau_{off} - 12\mu\text{s}) \quad (5)$$

Where τ_{off} is the power module's off time.

Error Amplifier (EA) Compensation

The MPQ4590 has an internal error amplifier (EA) compensation loop that samples the feedback voltage 6 μ s after the MOSFET turns off and regulates the output based on the 2.55V reference voltage (see Figure 4).

Ramp Compensation

An internal ramp compensation circuit is used to improve the load regulation. An exponential voltage signal is added to pull down the reference voltage of the feedback comparator (see Figure 4). The ramp compensation is a function of the load conditions: the compensation is about 1mV/ μ s under full-load conditions, and the compensation increases exponentially as the peak current decreases.

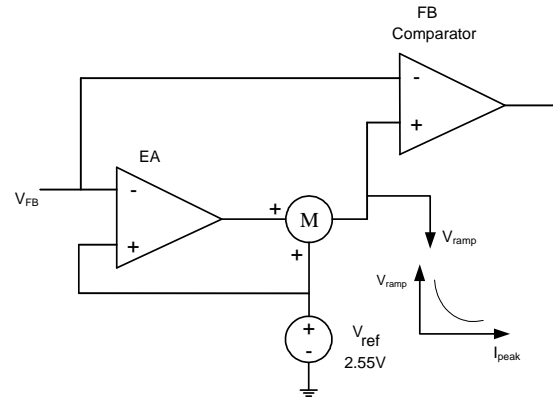


Figure 4: EA and Ramp Compensation

Overload Protection (OLP)

The maximum output power of the MPQ4590 is limited by the maximum switching frequency and peak current limit. If the load current is too large, the output voltage drops, making the FB voltage drop.

When the FB voltage drops below 1.7V, this is considered to be an error flag, and the timer starts up. If the timer reaches 220ms ($f_s = 28\text{kHz}$), OLP occurs. This timer duration prevents an OLP trigger when the power supply starts up or the load transitions. The power supply should start up in less than 220ms ($f_s = 28\text{kHz}$). The OLP delay time can be calculated with Equation (6):

$$\tau_{Delay} \approx 220\text{ms} \times \frac{28\text{kHz}}{f_s} \quad (6)$$

Short-Circuit Protection (SCP)

The MPQ4590 monitors the peak current and shuts down when the peak current rises above the SCP threshold. The power supply resumes operation once the fault is removed.

Thermal Shutdown (OTP)

To prevent any thermal-induced damage, the MPQ4590 stops switching when the junction temperature exceeds 150°C. During thermal shutdown (OTP), the VCC capacitor is discharged to 2.4V, and then the internal high voltage regulator recharges. The MPQ4590 recovers when the junction temperature drops below 120°C.

Open-Loop Detection

If the FB voltage is lower than 0.5V, the IC stops switching, and a restart cycle begins. During soft start, open-loop detection is blanked.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit prevents a premature switching pulse termination due to the turn-on spike (see Figure 5). Turn-on spikes are caused by parasitic capacitance and a reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET.

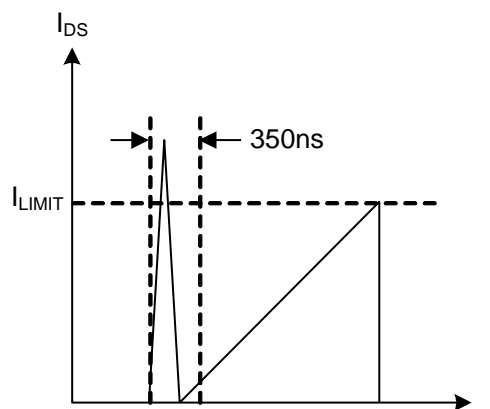
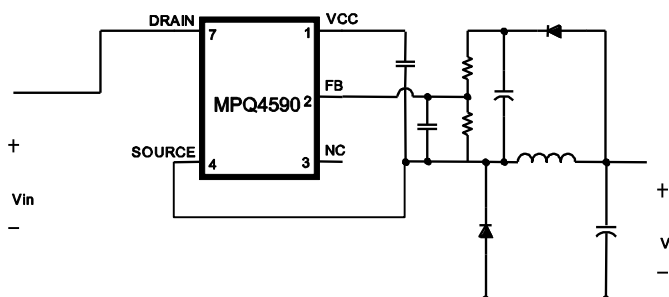
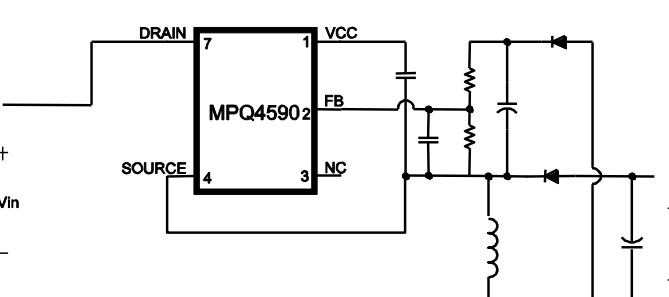
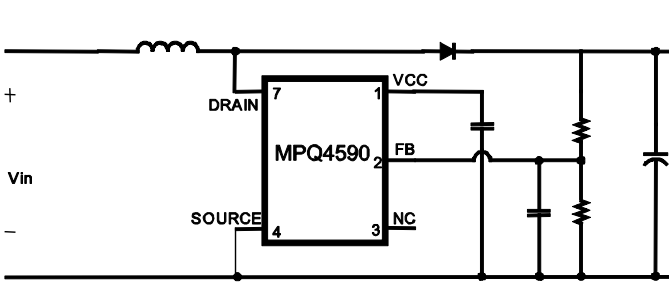
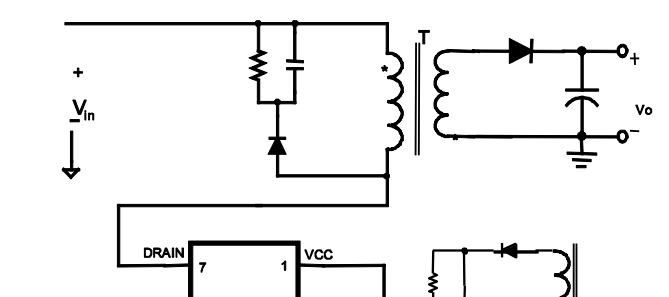


Figure 5: Leading-Edge Blanking

APPLICATION INFORMATION

Table 1: Common Topologies Using MPQ4590

Topology	Circuit Schematic	Features
High-Side Buck		<ol style="list-style-type: none"> 1. No isolation 2. Positive output 3. Low cost 4. Direct feedback
High-Side Buck-Boost		<ol style="list-style-type: none"> 1. No isolation 2. Negative output 3. Low cost 4. Direct feedback
Boost		<ol style="list-style-type: none"> 1. No isolation 2. Positive output 3. Low cost 4. Direct feedback
Flyback		<ol style="list-style-type: none"> 1. Isolation 2. Positive output 3. Low cost 4. Indirect feedback

Topology Options

The MPQ4590 can be used in common topologies, such as buck, buck-boost, boost, and flyback.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with a low equivalent series resistance (ESR) for the best performance. Ceramic capacitors are recommended, but tantalum or low ESR electrolytic capacitors may also suffice.

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be approximated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Inductor

The MPQ4590 has a minimum off time limit that determines the maximum power output. The maximum power increases as the inductor increases. Using a very small inductor may cause failure at full load, but a larger inductor results in a higher OLP load. It is recommended to select an inductor with a minimum value that can supply the rated power. Estimate the maximum power with Equation (8) for CCM and Equation (9) for DCM:

$$P_{Omax} = V_o \left(I_{peak} - \frac{V_o \tau_{minoff}}{2L} \right) \quad (8)$$

$$P_{Omax} = \frac{1}{2} L I_{peak}^2 \cdot \frac{1}{\tau_{minoff}} \quad (9)$$

For mass production, tolerance on the parameters, such as peak current limitation and minimal off time, should be taken into consideration.

Figure 6 shows an example of a P_{min} curve with a 12V output. $I_{peak} = 0.6A$ and $T_{minoff} = 15\mu s$ is used as the worst-case scenario for P_{MIN} calculation.

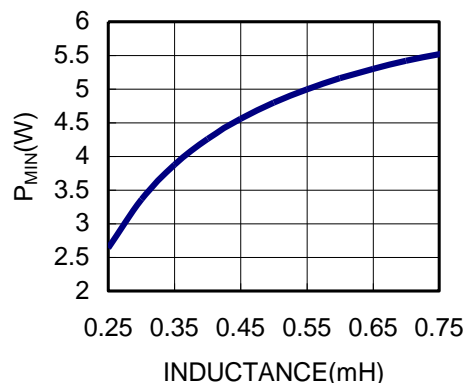


Figure 6: P_{min} vs. L at 12V

For a 3.6W output converter (12V, 0.3A), the minimum inductor value is about 0.36mH. However, using a 0.36mH inductor makes the switching frequency is too high, which causes poor efficiency. Usually, it is recommended to use an inductor that make the switching frequency higher than 20kHz, but not too high in large output current applications.

To reduce costs, use a standard off-the-shelf inductor no less than the calculated value.

Freewheeling Diode

The diode should be selected based on the maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation for CCM condition. It is recommended to use an ultra-fast diode such as the EGC10JH.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Estimate the output voltage ripple with Equation (10) for CCM and Equation (11) for DCM:

$$V_{\text{CCM_ripple}} = \frac{\Delta i}{8f_s C_o} + \Delta i \cdot R_{\text{ESR}} \quad (10)$$

$$V_{\text{DCM_ripple}} = \frac{I_o}{f_s C_o} \cdot \left(\frac{I_{\text{pk}} - I_o}{I_{\text{pk}}} \right)^2 + I_{\text{pk}} \cdot R_{\text{ESR}} \quad (11)$$

It is recommended to use ceramic, tantalum, or low ESR electrolytic capacitors to reduce the output voltage ripple.

Feedback Resistors

A resistor divider determines the output voltage. Appropriate R1 and R2 values should be chosen to maintain V_{FB} at 2.55V. Avoid using an R2 value that is too large. R2 is recommended to be 5 - 10kΩ.

Feedback Capacitor

The feedback capacitor provides a sample-and-hold function. Small capacitors result in poor regulation at light loads, and large capacitors affect circuit operation. Roughly estimate an optimal capacitor value using Equation (12):

$$\frac{1}{2} \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \leq C_{\text{FB}} \leq \frac{V_o}{R_1 + R_2} \cdot \frac{C_o}{I_o} \quad (12)$$

Dummy Load

A dummy load is required to maintain load regulation. This ensures sufficient inductor energy to charge the sample-and-hold capacitor to detect the output voltage. Normally, a 3mA dummy load is needed and can be adjusted according to the regulated voltage. Selecting the dummy load is a compromise between small no-load consumption and good no-load regulation, especially for applications that require 30mW of no load consumption. Use a Zener diode to reduce no-load consumption if no-load regulation is not a concern.

Auxiliary VCC Supply

For applications with an output voltage above 7V, the MPQ4590 can achieve the 30mW no-load power requirement by using an external VCC supply to reduce overall power consumption.

This auxiliary VCC supply is derived from the resistor connected between C3 and C4 (see Figure 7).

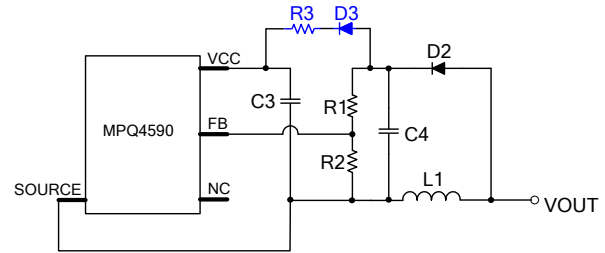


Figure 7: Auxiliary VCC Supply Circuit

C4 should be set larger than the recommendation above. D3 is used in case VCC interferes with FB, and R3 is determined with Equation (13):

$$R \approx \frac{V_o - 5.8V}{I_s} \quad (13)$$

Where I_s is the VCC consumption under no-load condition. R should be adjusted to meet the actual I_s value since it varies in different applications. In a particular configuration, I_s can be measured at about 250μA.

Surge Performance

An appropriate input capacitor value should be chosen to obtain a good surge performance. Figure 8 shows the half-wave rectifier. Table 2 shows the capacitance required under normal conditions for different surge voltages. FR1 is a 20Ω/2W fused resistor and L1 is 1mH for this recommendation.

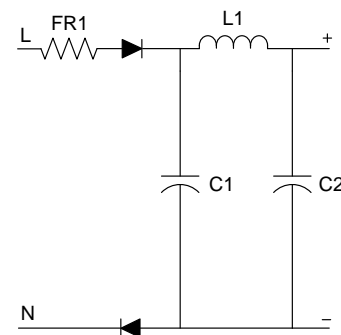


Figure 8: Half-Wave Rectifier

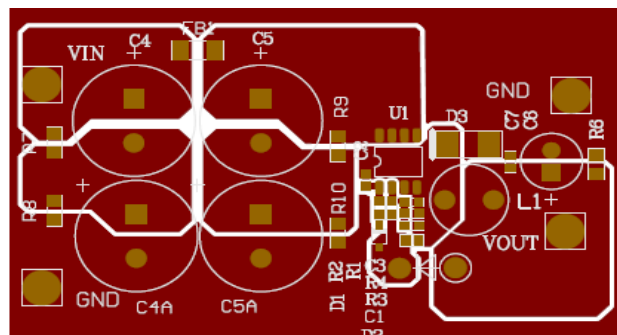
Table 2: Recommended Capacitance

Surge Voltage	500V	1000V
C1	1 μ F	2.2 μ F
C2	1 μ F	2.2 μ F

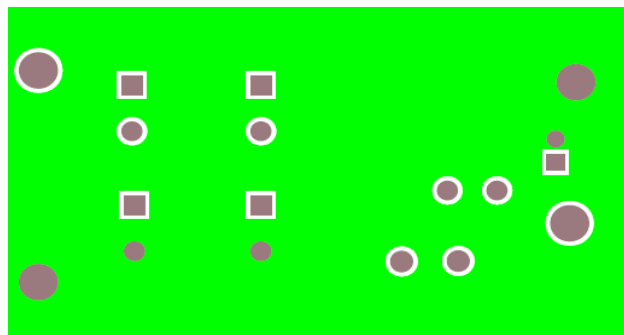
PCB Layout Guidelines

Efficient PCB layout is critical for reliable operation and good EMI and thermal performance. For best results, refer to Figure 9 and follow the guidelines below.

- 1) Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
- 2) Place the power inductor far away from the input filter while keeping the loop area to the inductor to a minimum.
- 3) Place a capacitor (valued at several hundred pF) between the FB pin and the source as close the IC as possible.
- 4) Connect the exposed pads or large copper area with the DRAIN pin to improve thermal performance.



Top Layer



Bottom Layer

Figure 9: Recommended Layout

Design Example

Table 3 shows a design example following the application guidelines for the specifications below.

Table 3: Design Example

V_{IN}	120V to 600V
V_{OUT}	12V
I_{OUT}	300mA

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUIT

Figure 10 shows a typical application example of a 12V, 300mA, non-isolated power supply using the MPQ4590.

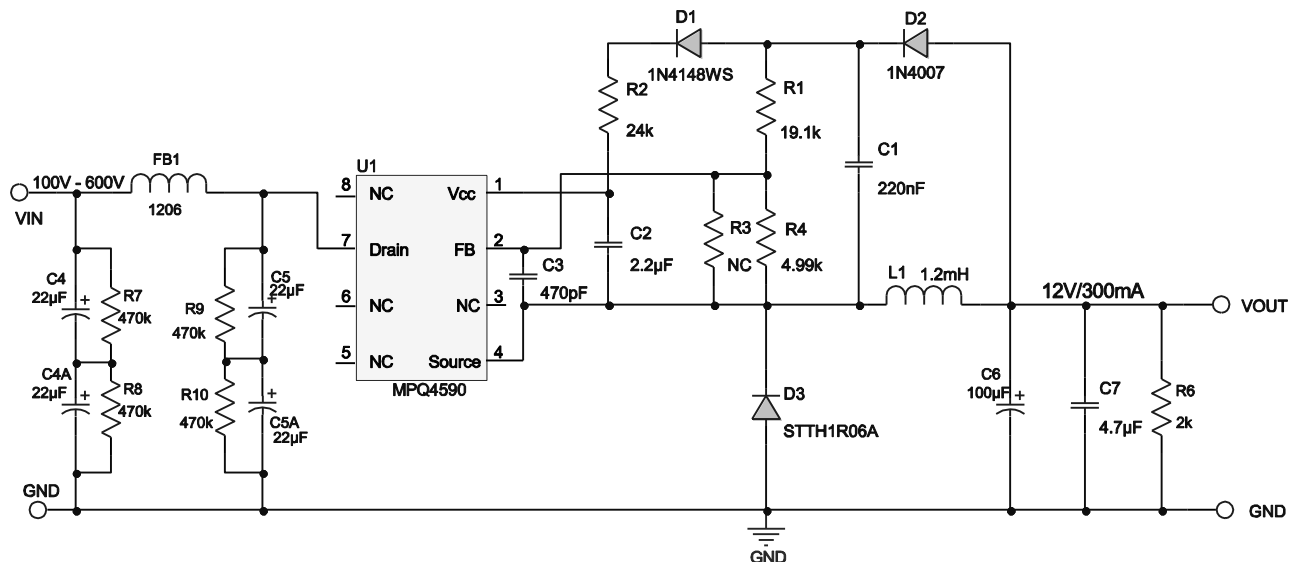
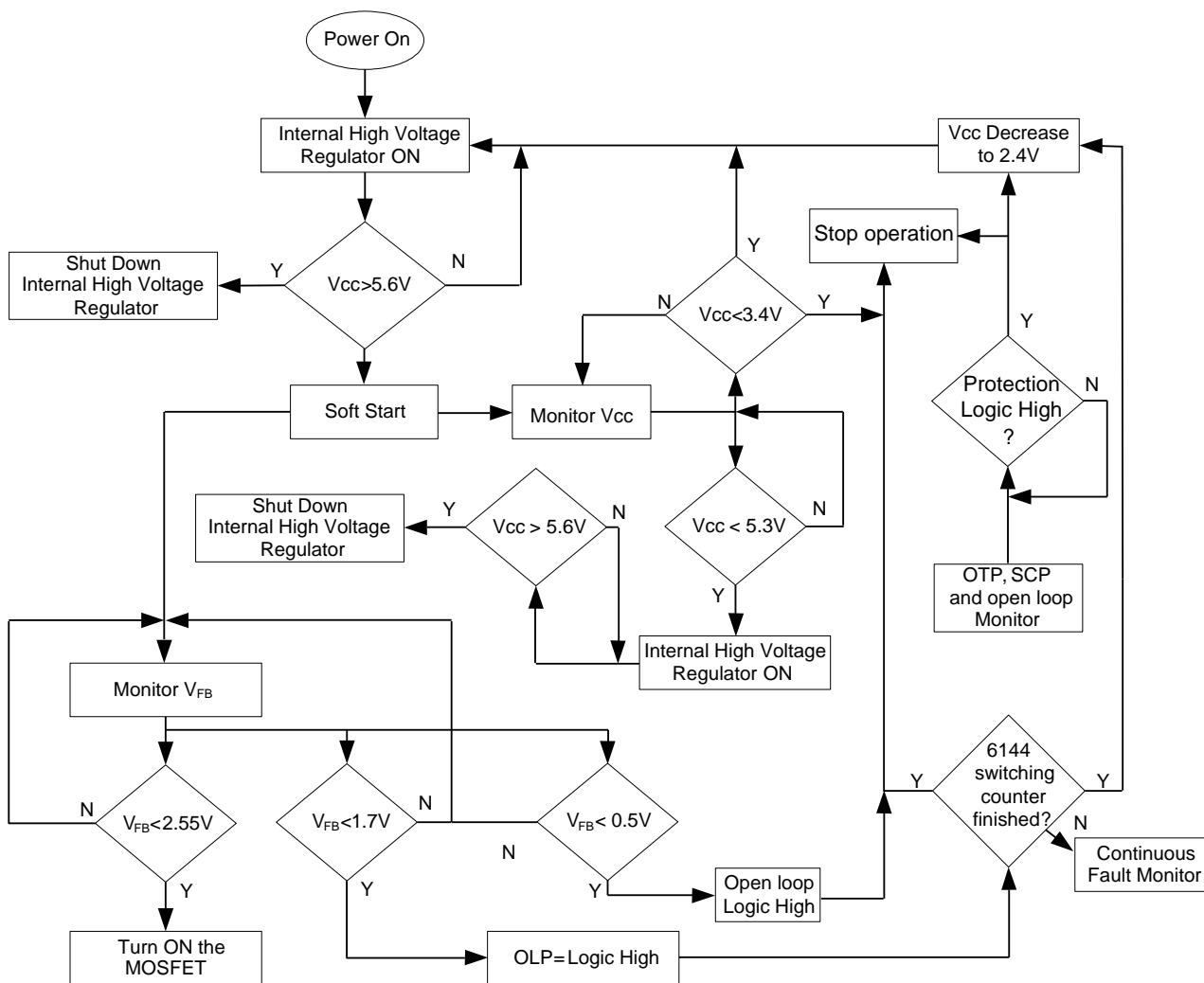


Figure 9: Typical Application at 12V, 300mA

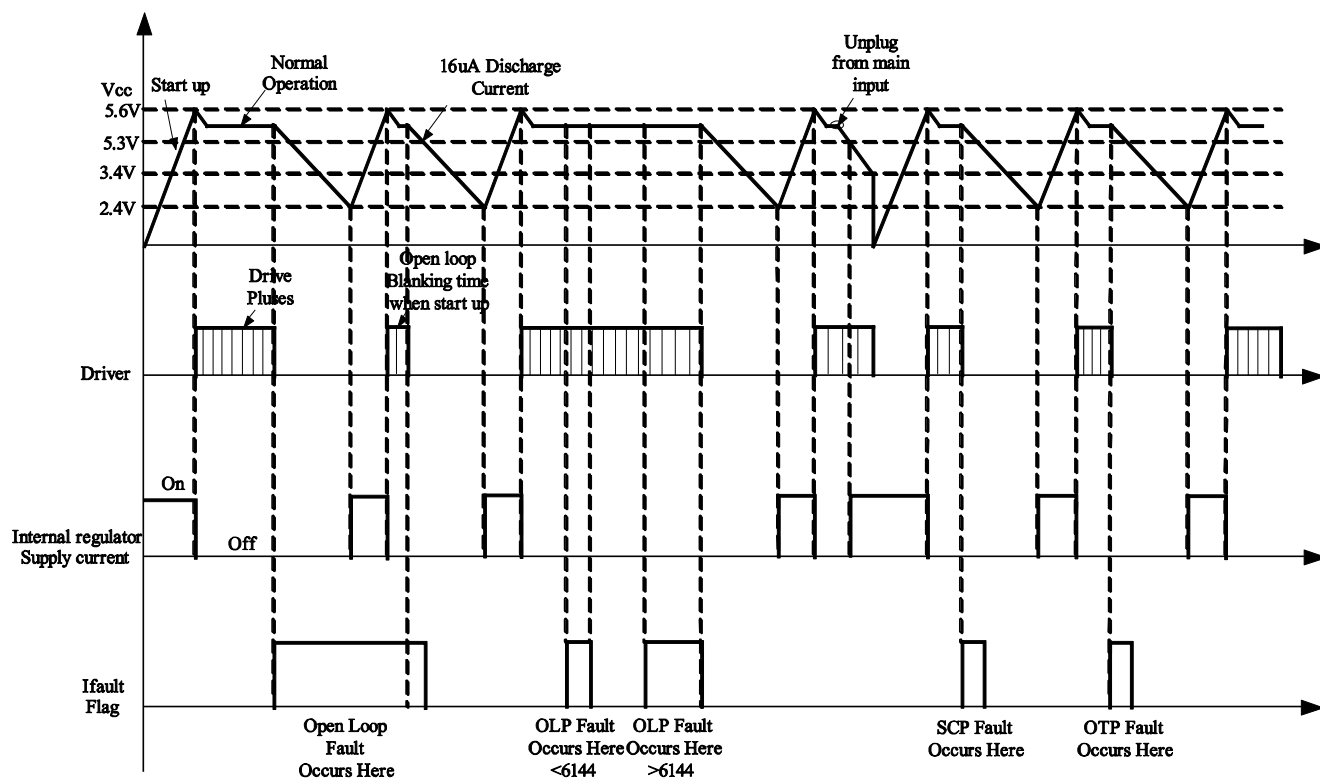
FLOW CHART



UVLO, SCP, OLP, OTP and Open loop protections are auto restart

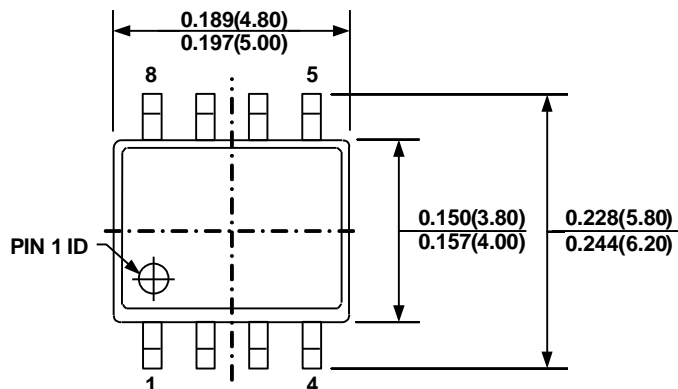
Figure 11: Control Flow Chart

SIGNAL EVOLUTION

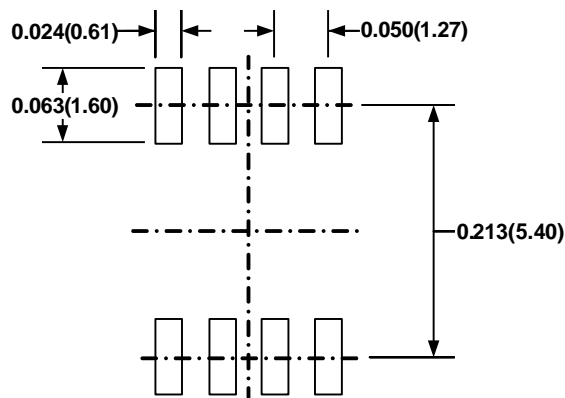


PACKAGE INFORMATION

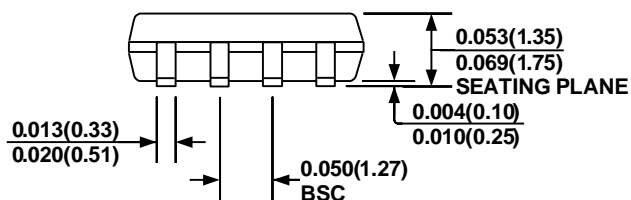
SOIC-8



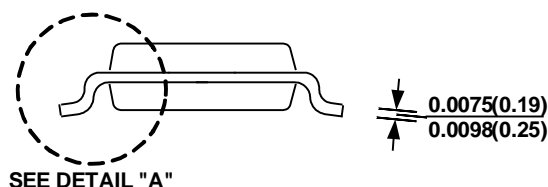
TOP VIEW



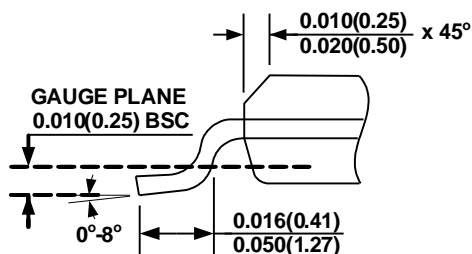
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) CONTROL DIMENSION IS IN INCHES DIMENSION IN BRACKET IS IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS012, VARIATION AA
- 6) DRAWING IS NOT TO SCALE

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