MPQ4315

45V, 5A, Low I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4315 is a synchronous step-down switching converter with a configurable frequency and integrated internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It provides up to 5A of highly efficient output, with current mode control for fast loop response.

The wide 3.3V to 45V input range accommodates a variety of step-down applications in automotive input environments. Its low 1.7μA shutdown mode quiescent current makes the MPQ4315 ideal for use in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency under light-load conditions to reduce the switching and gate driver losses. An open-drain power good signal indicates whether the output is within 93% to 106% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High-duty cycle and low-dropout mode are provided for the automotive cold crank conditions.

The MPQ4315 is available in a QFN-20 (4mmx4mm) wettable flank package, and is AEC-Q100 Grade 1 qualified.

MPQ4315 FAMILY VERSIONS

Part Number	Output Current	Package Options
MPQ4312	2A	QFN-20 (4mmx4mm) WF (1)
MPQ4313	3A	
MPQ4314	4A	
MPQ4315	5A	
MPQ4316	6A	
MPQ4317	7A	

Note:

1) WF means wettable flank.

FEATURES

- Wide 3.3V to 45V Operating Voltage Range
- 5A Continuous Output Current
- 1.7μA Low Shutdown Supply Current
- 18μA Sleep Mode Quiescent Current
- Internal 48mΩ High-Side MOSFET and 20mΩ Low-Side MOSFET
- 350kHz to 1000kHz Configurable Switching Frequency for Car Battery Applications
- Can Be Synchronized to an External Clock
- Out-of-Phase Synchronized Clock Output
- Frequency Spread Spectrum (FSS) for Low EMI
- Symmetric V_{IN} for Low EMI
- Power Good Output
- External Soft Start
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout Mode
- Hiccup Over-Current Protection
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems
- Industrial Power Systems

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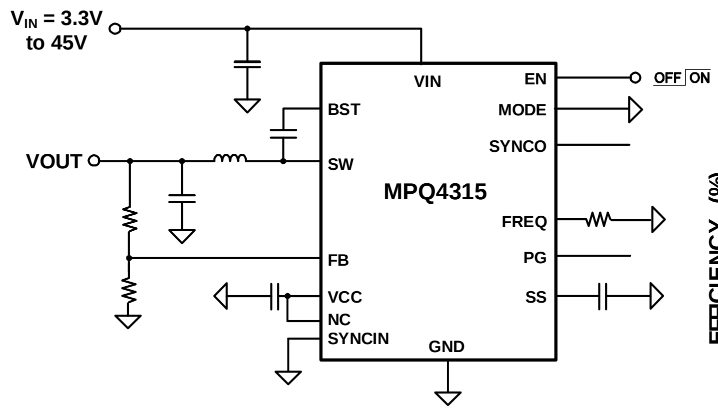
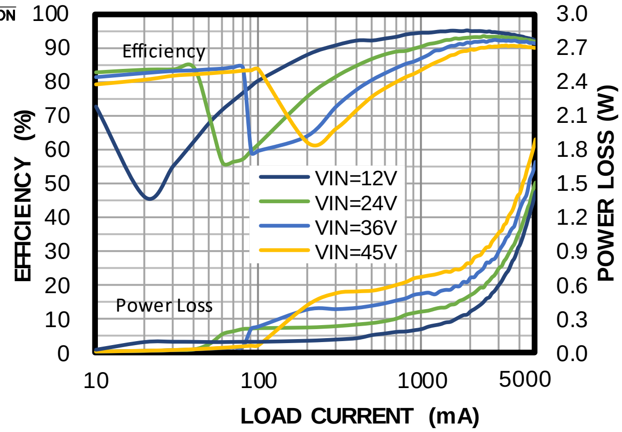
TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 3.3V, f_{SW} = 470kHz, L = 4.7µH, AAM



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4315GRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ4315GRE-AEC1–Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

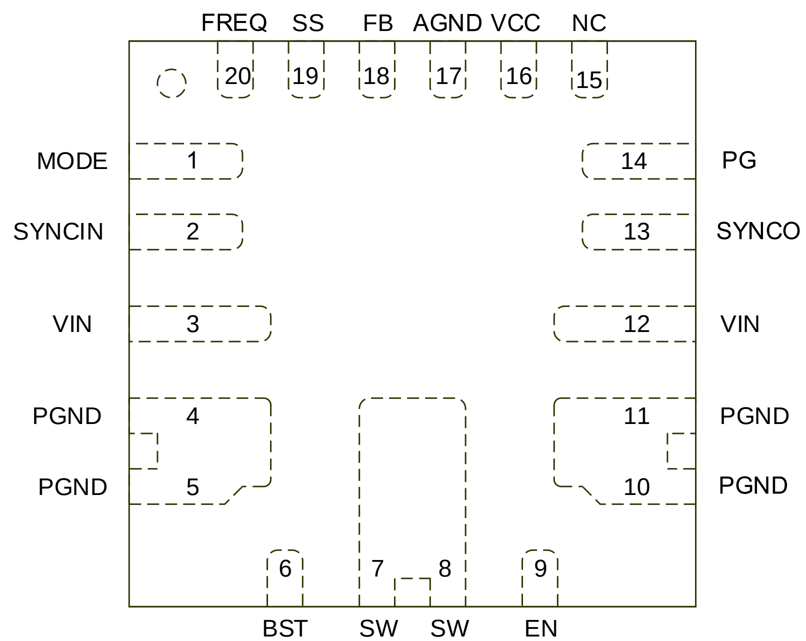
TOP MARKING (MPQ4315GRE-AEC1)

MPSYWW
MP4315
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4315: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-20 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM select pin.** Pull the MODE pin high for the MPQ4315 to operate in forced continuous conduction mode (FCCM) under light loads. Pull it low for it to operate in advanced asynchronous mode (AAM) under light loads. Do not float this pin.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. This pin is also used for multi-phase operation. The pin is internally high impedance. Do not float this pin under any circumstances. Connect this pin to GND if not used. If used, ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a ≤51kΩ resistor between the pin and GND in case the external sync clock pull-down capability is not strong enough or the pin enters a high-impedance state.
3, 12	VIN	**Input supply.** VIN supplies power to all the internal control circuitry and the power switch connected to SW. It is recommended to place a decoupling capacitor connected to ground and close to VIN in order to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between this BST and SW. See the Application Information section on page 28 to calculate the size of this capacitor.
7, 8	SW	**Switch node.** SW is the output of the internal power switch.
9	EN	**Enable.** Pull this pin below the specified threshold (0.85V) to shut down the MPQ4315. Pull it above the specified threshold (1V) to enable the MPQ4315.
13	SYNCO	**SYNC output.** This pin outputs a clock signal that is 180° out of phase with the internal oscillator signal, or the opposite of the clock signal applied at the SYNCIN pin. Float this pin if not used.
14	PG	**Power good indicator.** The output of PG is an open drain. If this pin is used, a pull-up resistor to the power source is required. PG goes high if the output voltage (V_{OUT}) is within 93% to 106% of the nominal voltage. It goes low if V_{OUT} is above 107.5% or below 91% of the nominal voltage.
15	NC	**Not connected.** Connect NC to the VCC pin or V_{OUT} (≥3V). Do not float this pin.
16	VCC	**Bias supply.** The VCC pin supplies 5V to the internal control circuit and gate drivers. Place a decoupling capacitor connected to ground close to this pin. See the Application Information section on page 28 to calculate the size of this capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.815V.
19	SS	**Soft-start input.** Place a capacitor from SS to GND to set the soft-start time. The MPQ4315 sources 6μA from the SS pin to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency configuration.** Connect a resistor from this pin to ground to set the switching frequency (f_{SW}). Follow the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 13 to set the frequency.

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ABSOLUTE MAXIMUM RATINGS [2]

VIN, EN ....-0.3V to +50V
SW ....-0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST .... V_{SW} + 5.5V
All other pins ....-0.3V to 5.5V
Continuous power dissipation (T_A = 25°C) [3] [5]
QFN-20 (4mmx4mm)................................ 5.4W
Operating junction temperature ....150°C
Lead temperature ....260°C
Storage temperature................ -65°C to +150°C

ESD Ratings

HBM (Human body model) ....±2kV
CDM (Charged device model) .... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ....3.3V to 45V
Output voltage (V_{OUT})..........0.815V to 0.95 x V_{IN}
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)
JESD51-7 [4]............................44.........9....°C/W
EVQ4315-R-00A [5]..................23........2.5..°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
5) Measured on a 9cmx9cm, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	IN_{UVLO_RISING}		2.8	3.0	3.2	V
V_{IN} UVLO falling threshold	$IN_{UVLO\_FALLING}$		2.45	2.65	2.85	V
V_{IN} UVLO hysteresis	IN_{UVLO_HYS}			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
V_{IN} quiescent current	I_Q	V_{FB} = 0.85V, no load, sleep mode		18	26	μA
V_{IN} quiescent current (switching) (6)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 316kΩ		20		μA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
V_{IN} shutdown current	I_{SHDN}	EN = 0V		1.7	3.5	μA
FB voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		V_{IN} = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (6)	t_{ON_MIN}			100		ns
Minimum off time (6)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		530	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		deg
High-side current limit	I_{LIMIT}	Duty cycle = 30%	6.4	8	9.6	A
Low-side valley current limit	I_{LIMIT_VALLEY}		4.8	6	7.2	A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Zero-current detection (ZCD) threshold	I_{ZCD}	AAM	-0.15	0.1	+0.35	A
Low-side reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
HS-FET on resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		48	80	mΩ
LS-FET on resistance	R_{ON_LS}	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	4	6	8	µA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	88.5%	93%	97.5%	V_{REF}
		V_{FB} falling	101.5%	106%	110.5%	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	86.5%	91%	95.5%	
		V_{FB} rising	103%	107.5%	112%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown [(6)]	T_{SD}			170		°C
Thermal shutdown hysteresis [(6)]	T_{SD_HYS}			20		°C

Note:

6) Guaranteed by characterization. Not tested in production.

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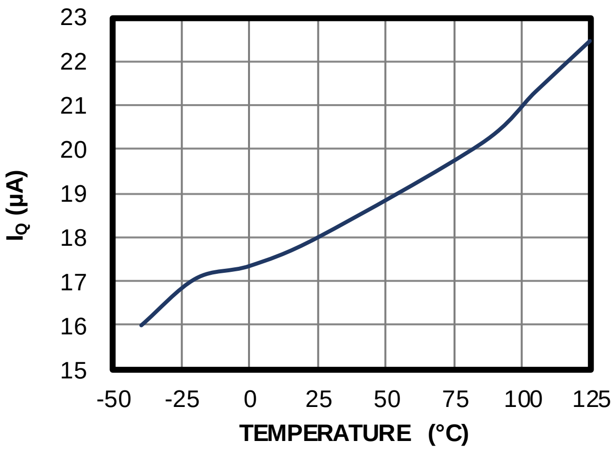
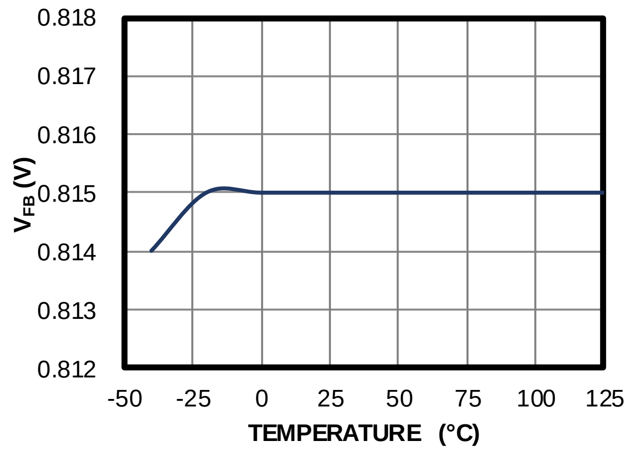
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

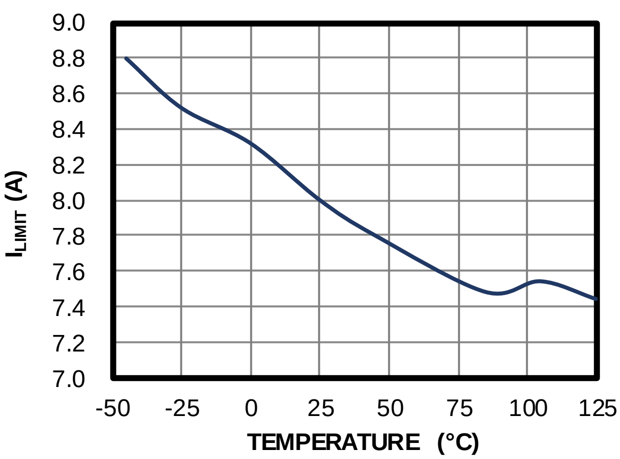
Quiescent Current vs. Temperature



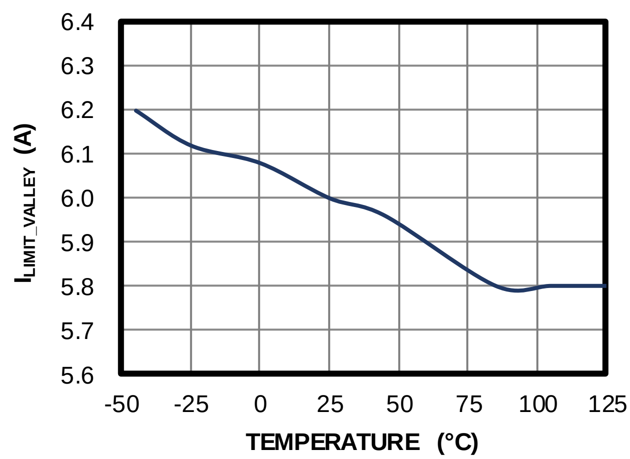
Feedback Voltage vs. Temperature



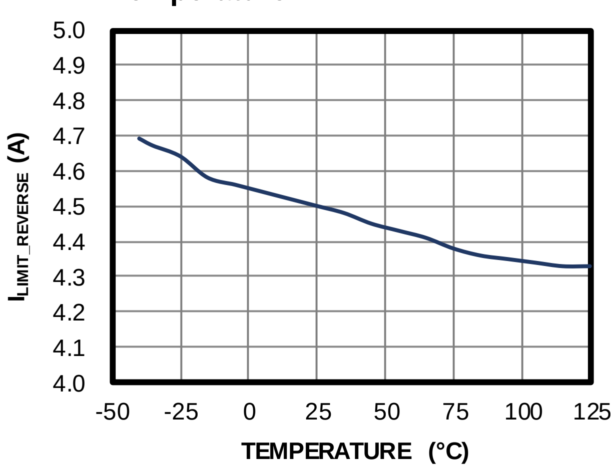
Current Limit vs. Temperature



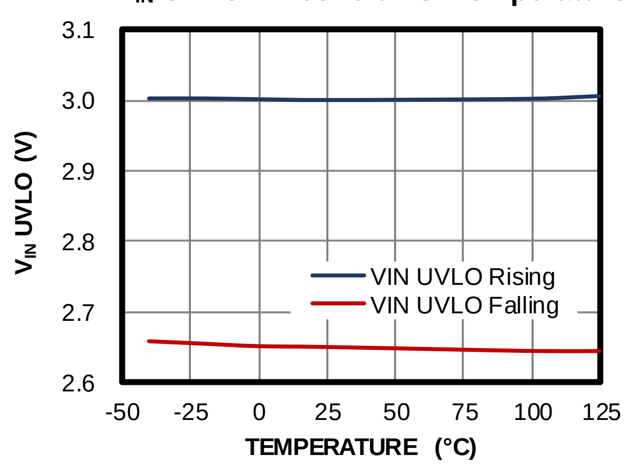
Valley Current Limit vs. Temperature



Reverse Current Limit vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



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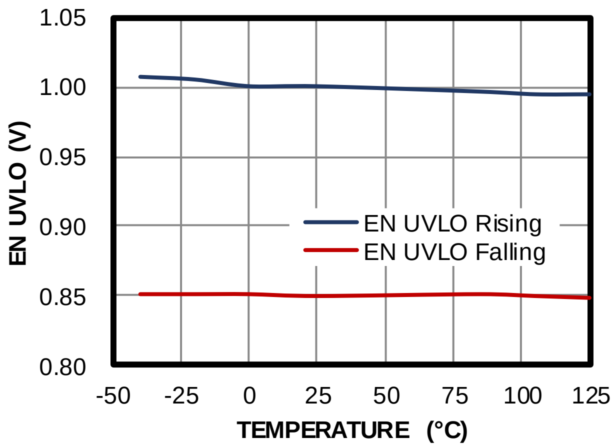
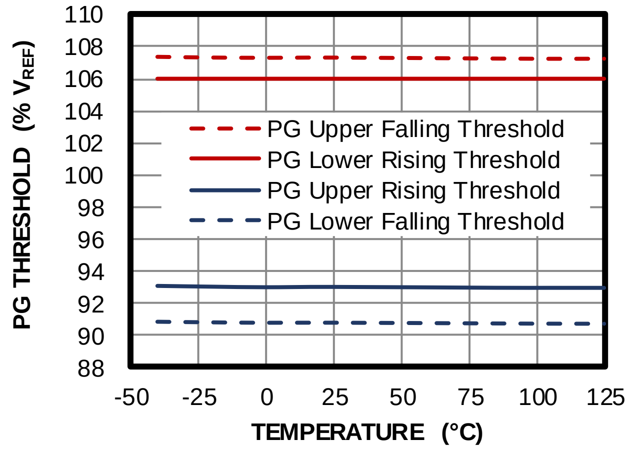
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

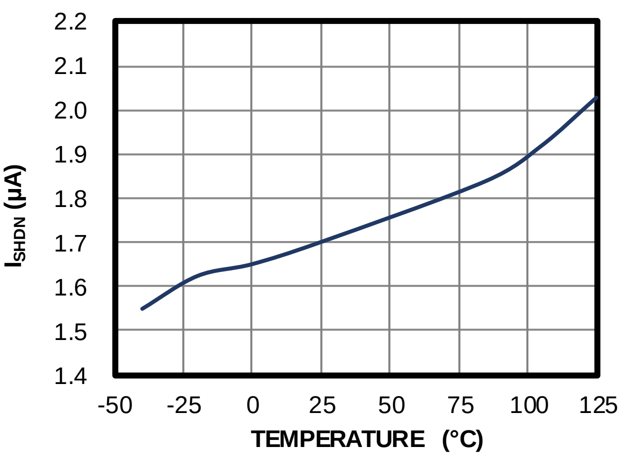
EN UVLO Threshold vs. Temperature



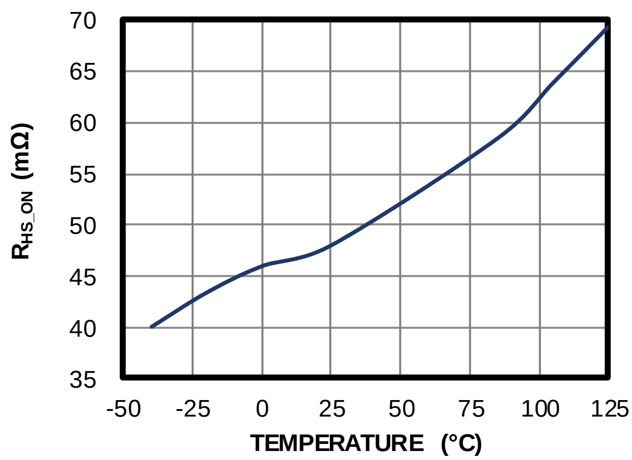
PG Rising/Falling Threshold vs. Temperature



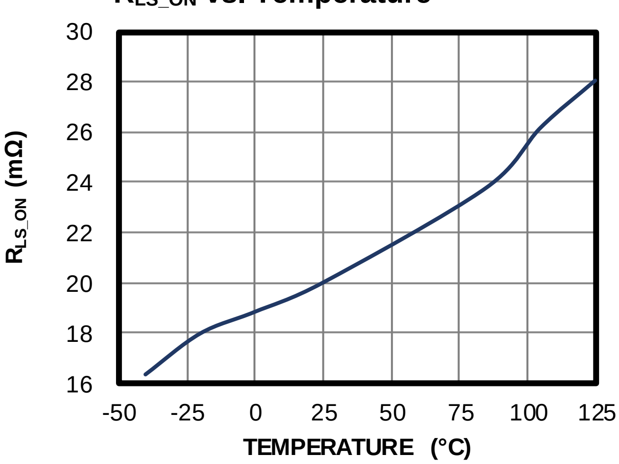
V_{IN} Shutdown Current vs. Temperature



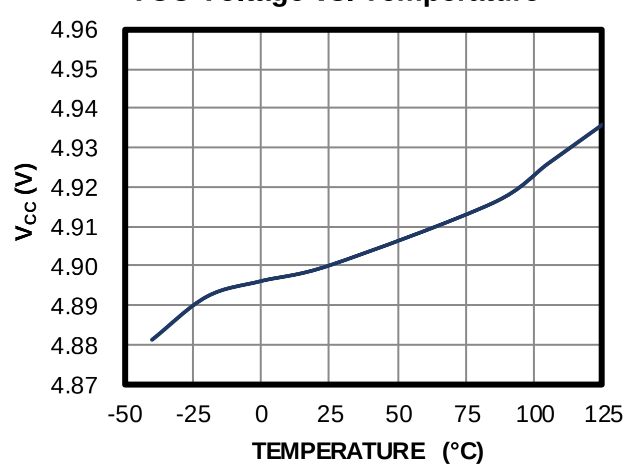
R_{HS_ON} vs. Temperature



R_{LS_ON} vs. Temperature



VCC Voltage vs. Temperature



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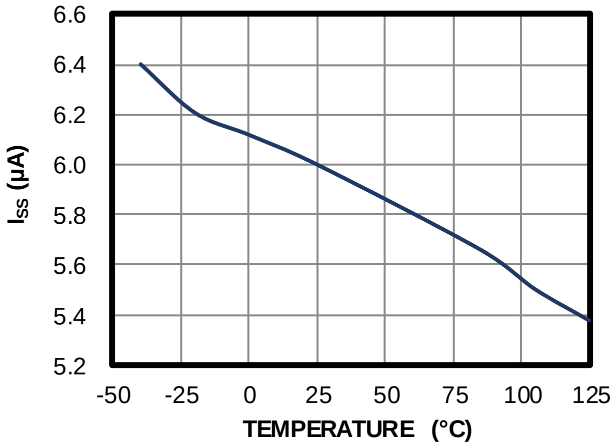
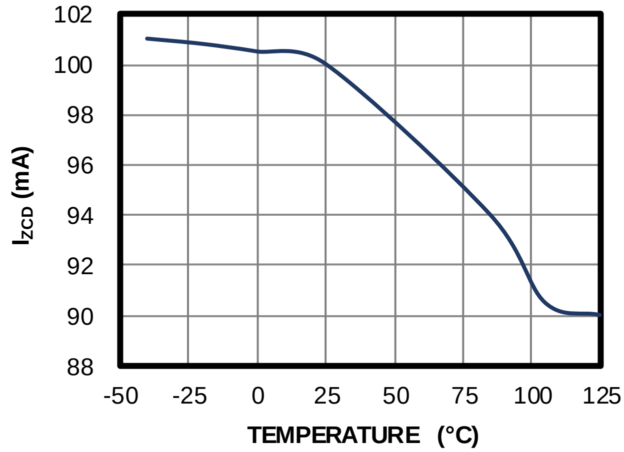
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft Start Current vs. Temperature

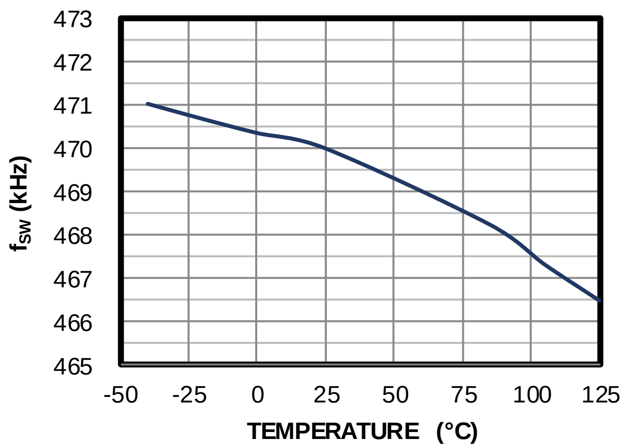


Zero-Current Detection Threshold vs. Temperature



Switching Frequency vs. Temperature

R_{FREQ} = 62kΩ



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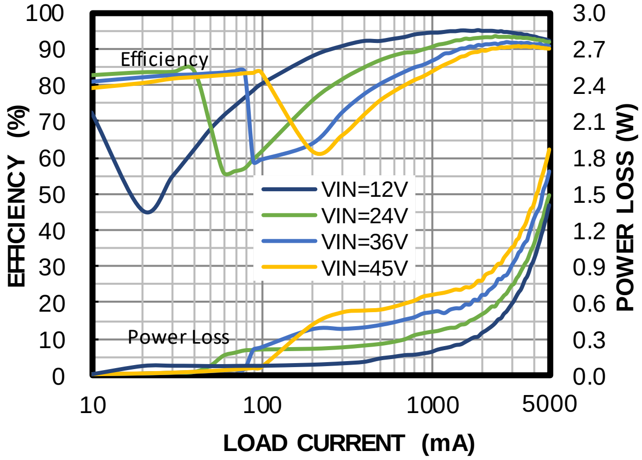
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

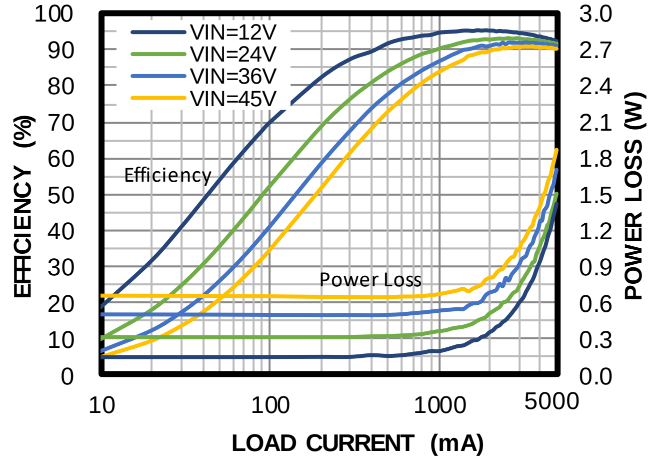
Efficiency vs. Load Current vs. Power Loss

AAM, V_{OUT} = 3.3V, L = 4.7µH (7)



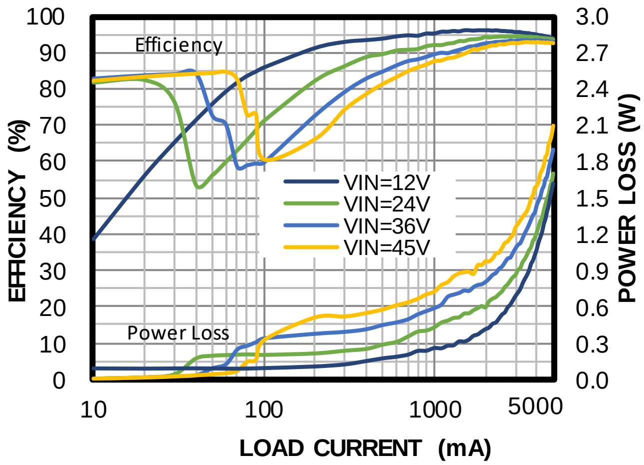
Efficiency vs. Load Current vs. Power Loss

FCCM, V_{OUT} = 3.3V, L = 4.7µH (7)



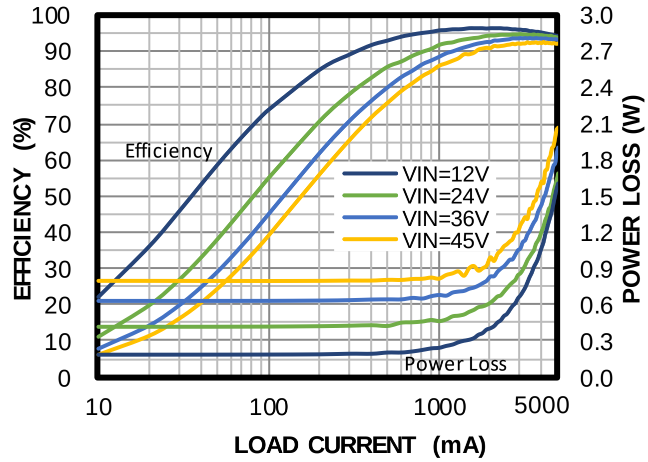
Efficiency vs. Load Current vs. Power Loss

AAM, V_{OUT} = 5V, L = 4.7µH (7)



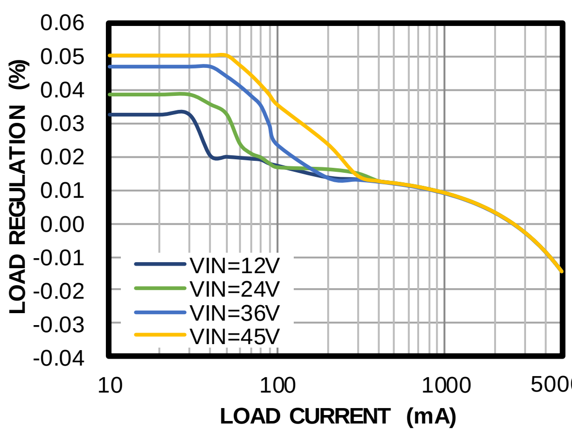
Efficiency vs. Load Current vs. Power Loss

FCCM, V_{OUT} = 5V, L = 4.7µH (7)



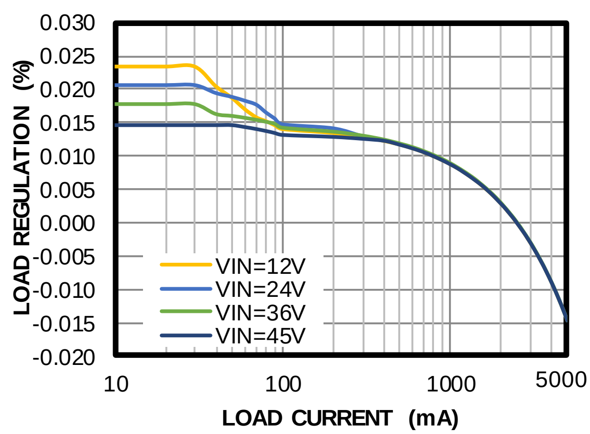
Load Regulation

AAM



Load Regulation

FCCM



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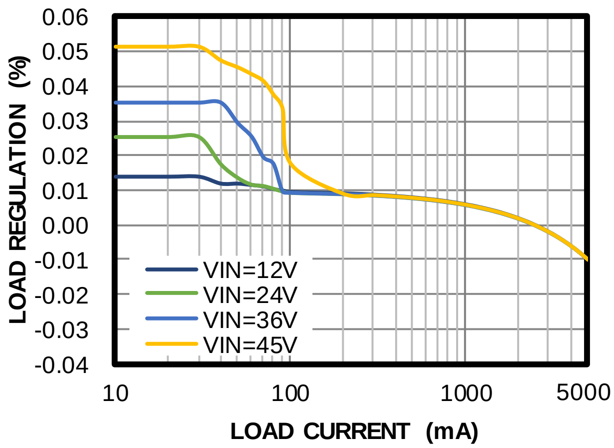
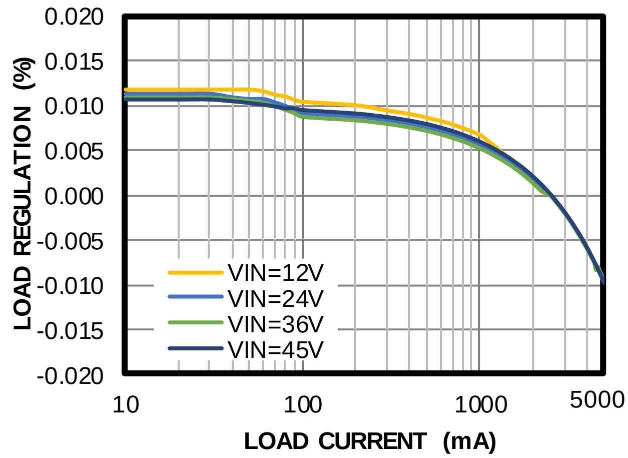
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

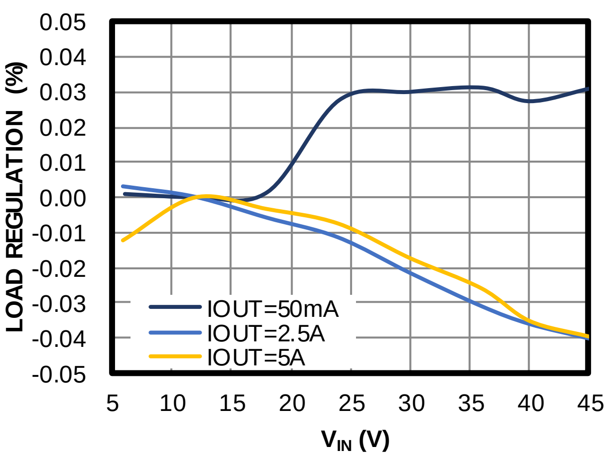
Load Regulation
AAM, V_{OUT} = 5V



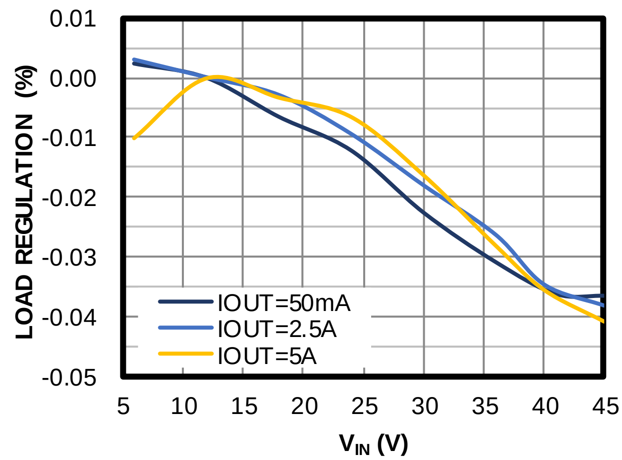
Load Regulation
FCCM, V_{OUT} = 5V



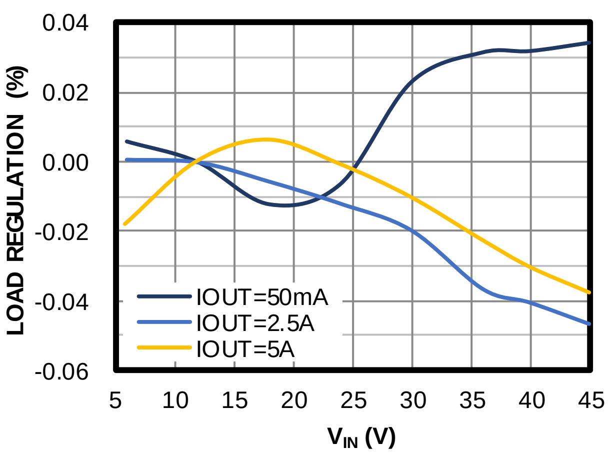
Line Regulation
AAM



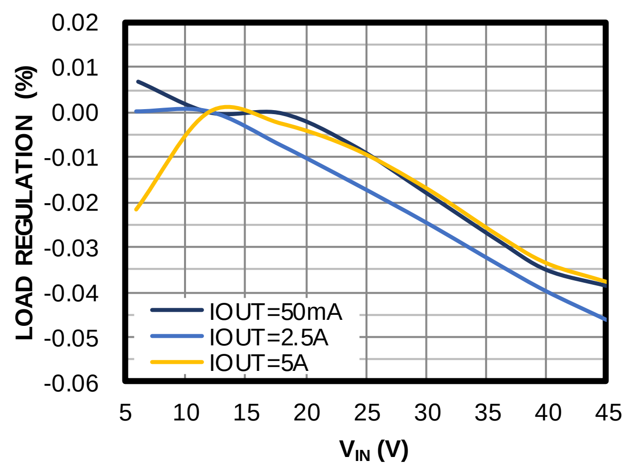
Line Regulation
FCCM



Line Regulation
AAM, V_{OUT} = 5V



Line Regulation
FCCM, V_{OUT} = 5V



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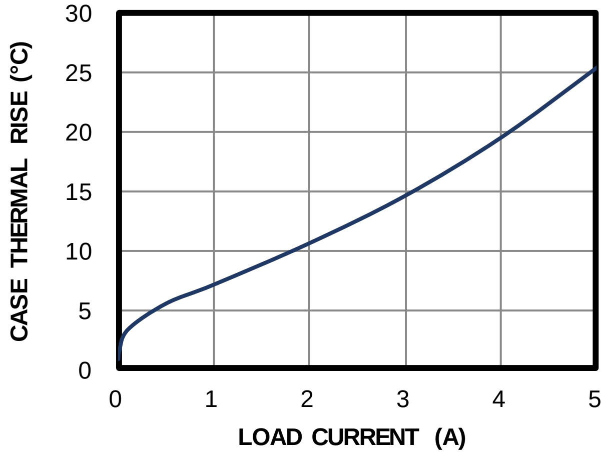
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

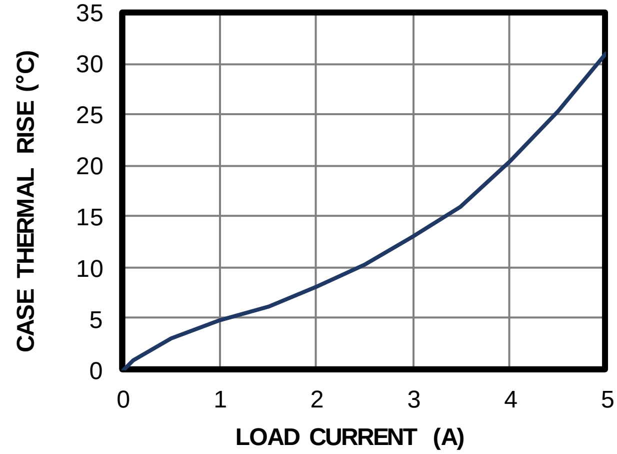
Case Thermal Rise

V_{OUT} = 3.3V

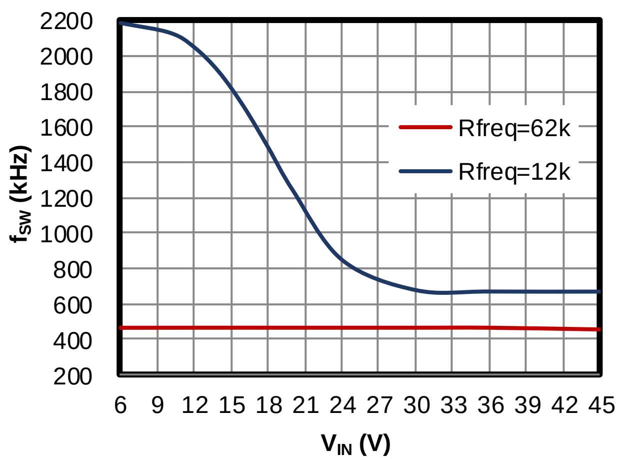


Case Thermal Rise

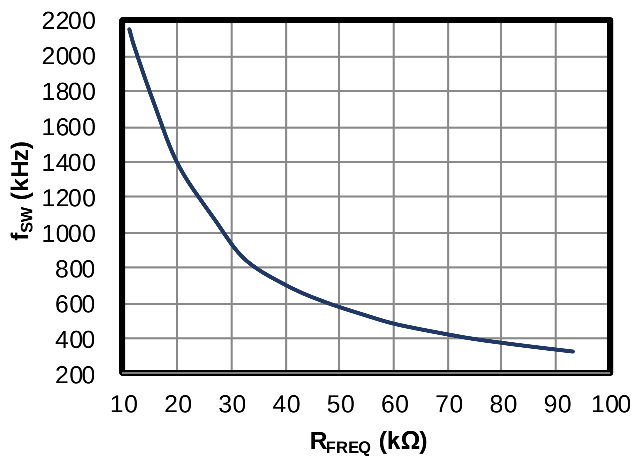
V_{OUT} = 5V



f_{SW} vs. V_{IN}

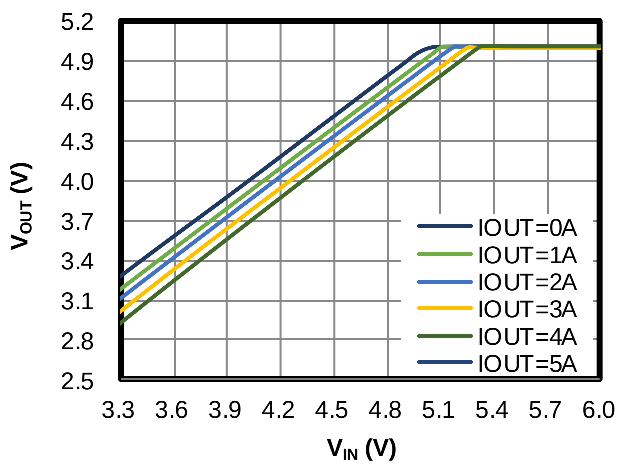


f_{SW} vs. R_{FREQ}



Low-Dropout Mode

V_{OUT} = 5V



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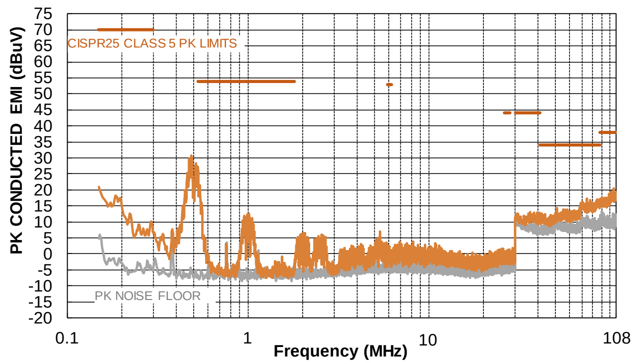
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, L = 4.7µH, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. (8)

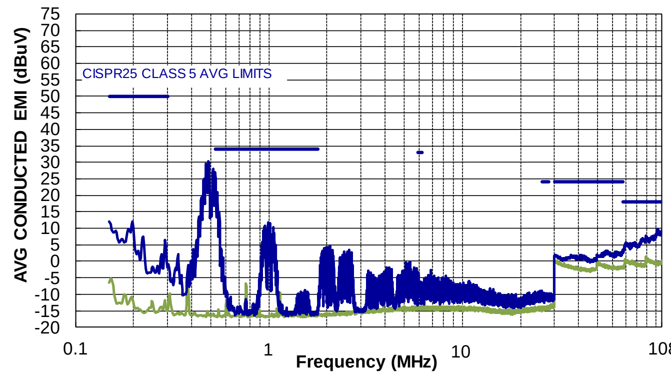
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



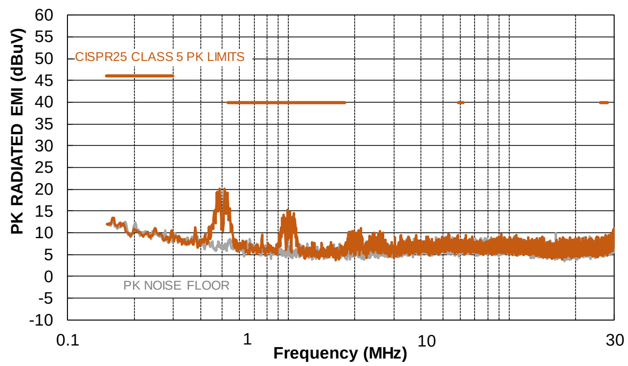
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



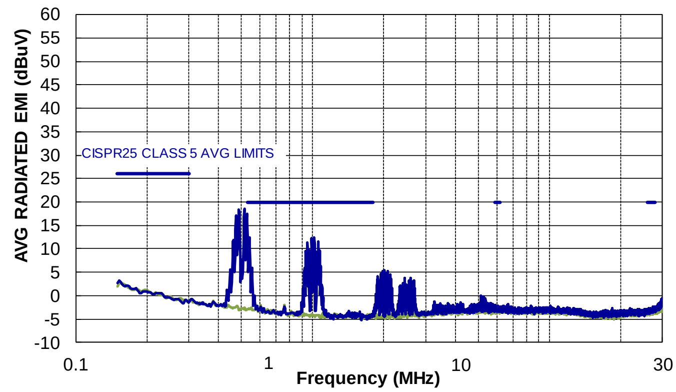
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



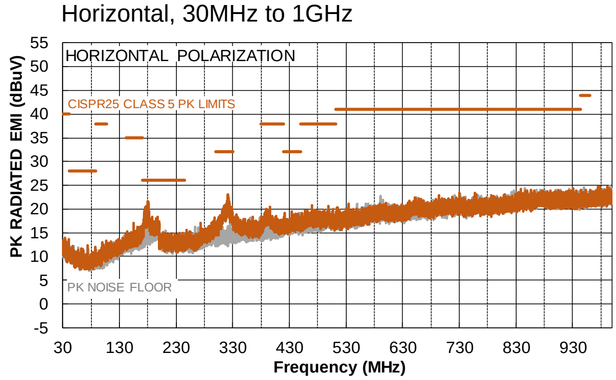
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



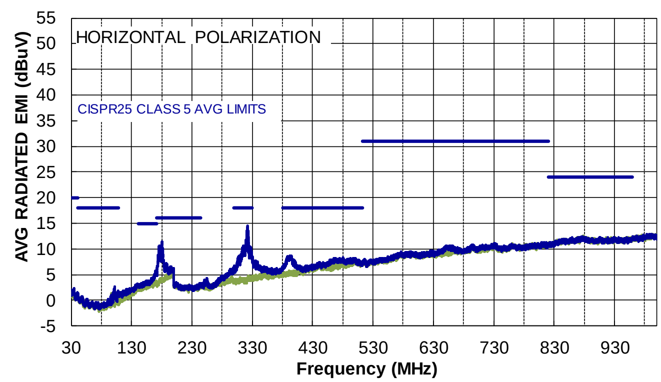
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



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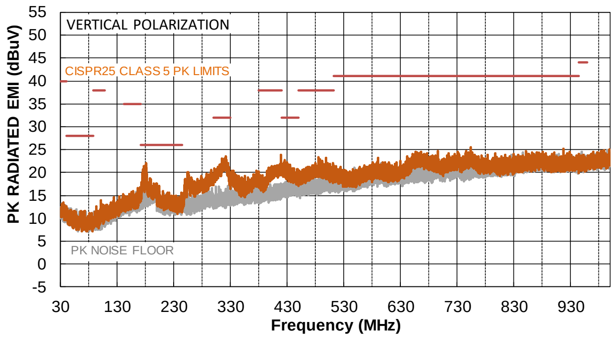
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 5A, L = 4.7µH, f_{SW} = 470kHz, T_A = 25°C, unless otherwise noted. (8)

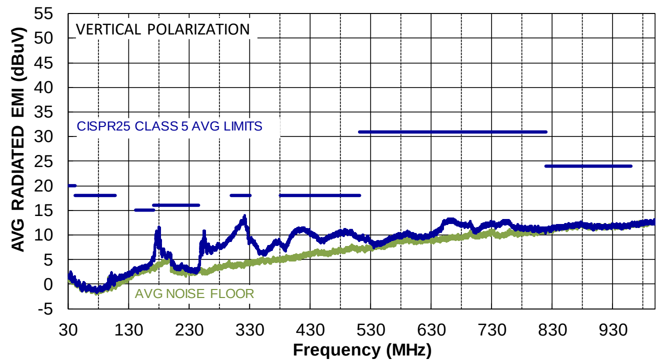
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

7) Inductor part number: XAL6060-472MEC. DCR = 15.02mΩ.
8) EMC test results are based on the application circuit with EMI filters (see Figure 12 in the Typical Application Circuits section on page 31).

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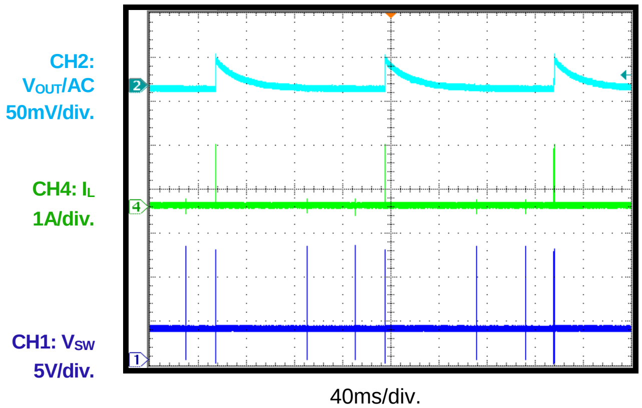
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

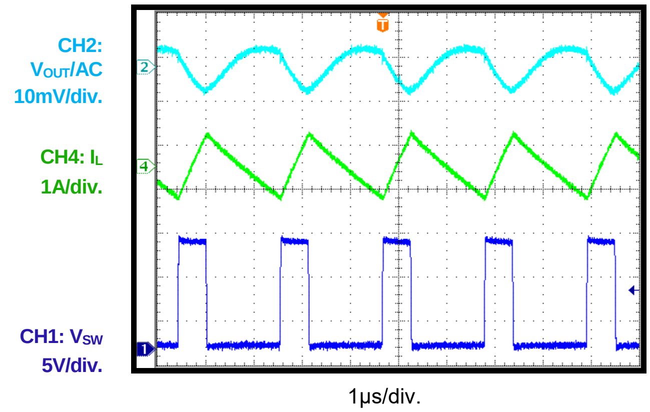
Steady State

I_{OUT} = 0A, AAM



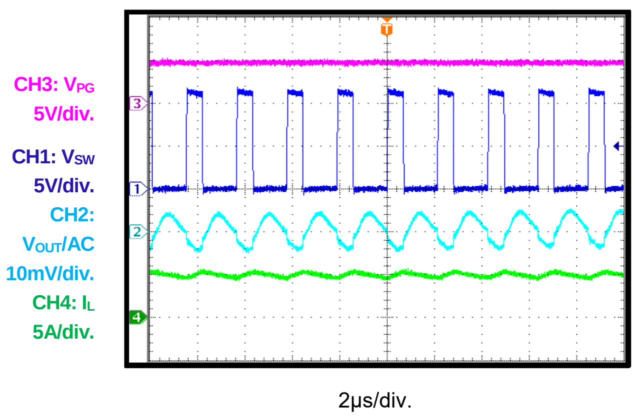
Steady State

I_{OUT} = 0A, FCCM



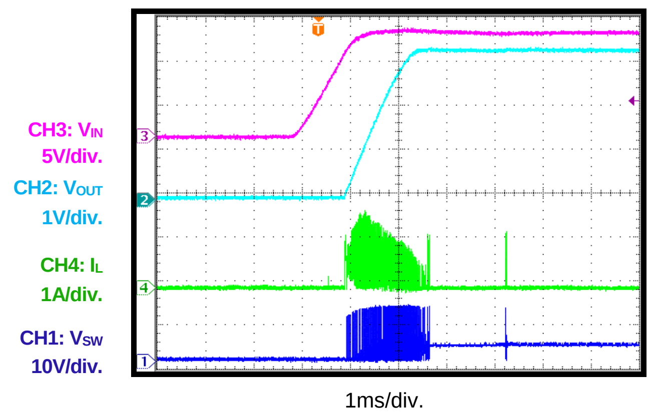
Steady State

I_{OUT} = 5A



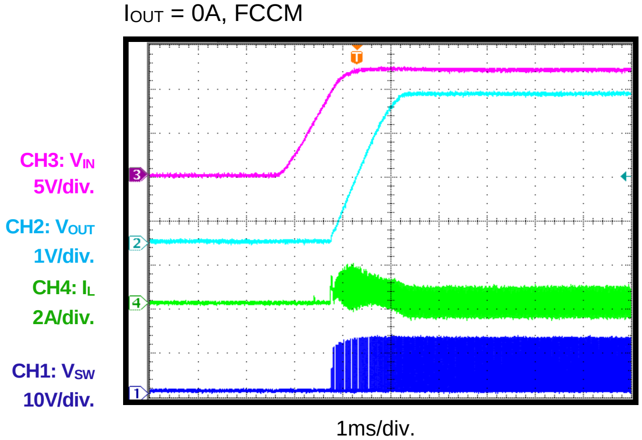
Start-Up through VIN

I_{OUT} = 0A, AAM



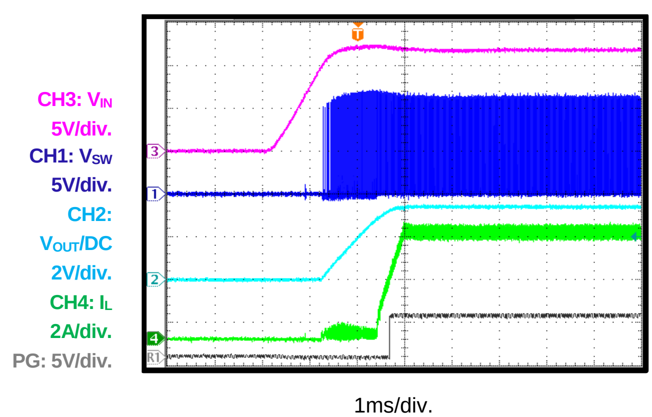
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 5A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

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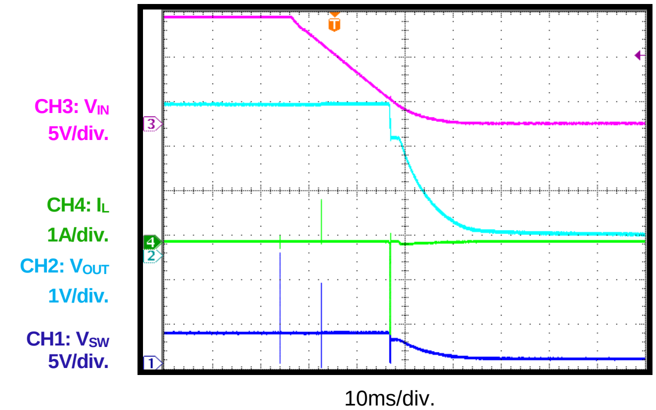
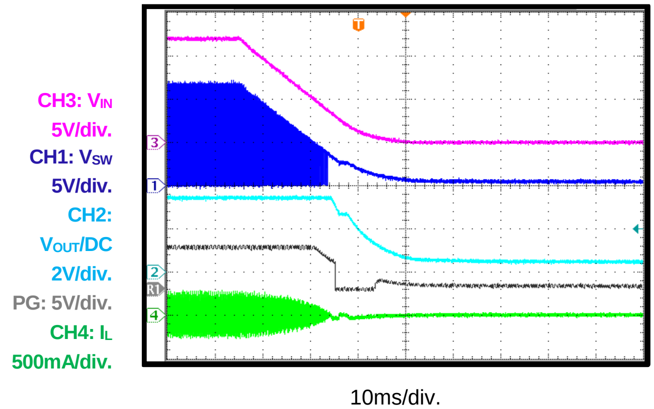
Shutdown through VIN

I_{OUT} = 0A, AAM



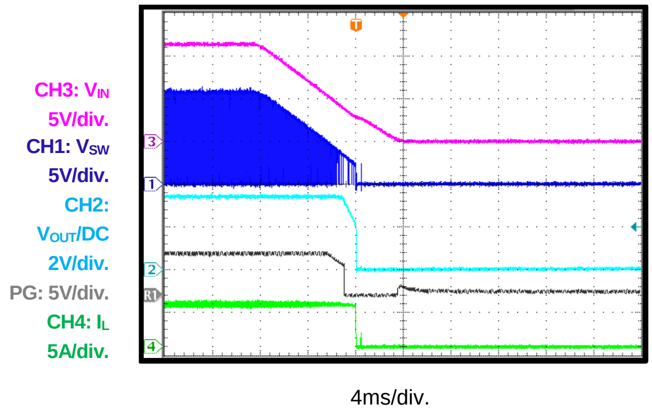
Shutdown through VIN

I_{OUT} = 0A, FCCM



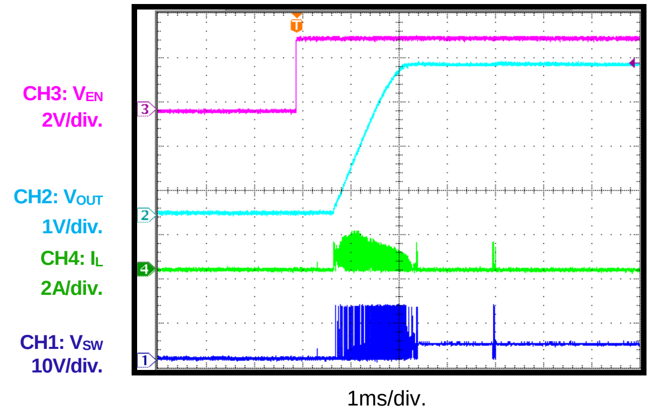
Shutdown through VIN

I_{OUT} = 5A



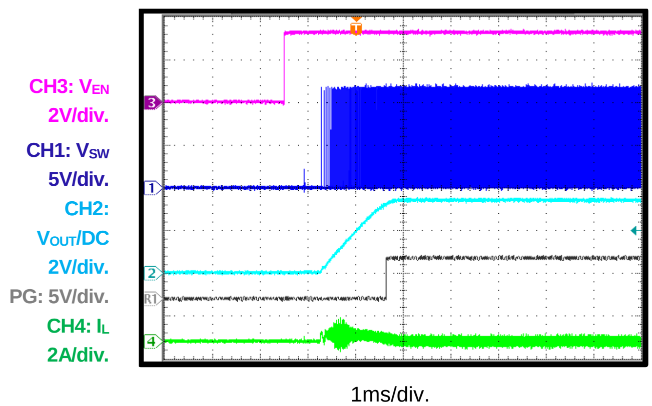
Start-Up through EN

I_{OUT} = 0A, AAM



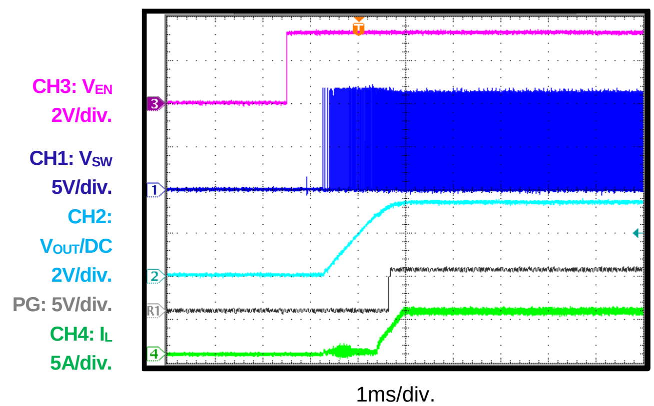
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 5A



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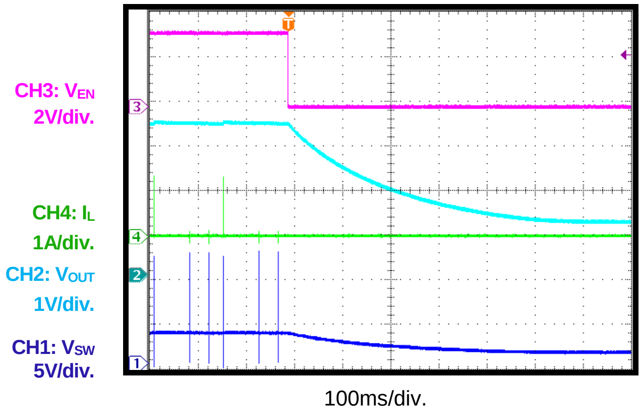
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

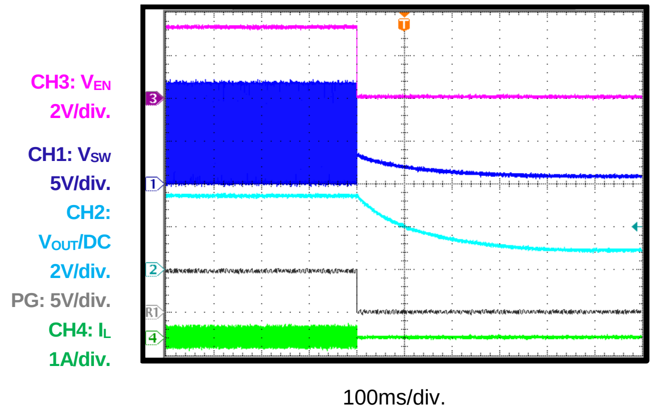
Shutdown through EN

I_{OUT} = 0A, AAM



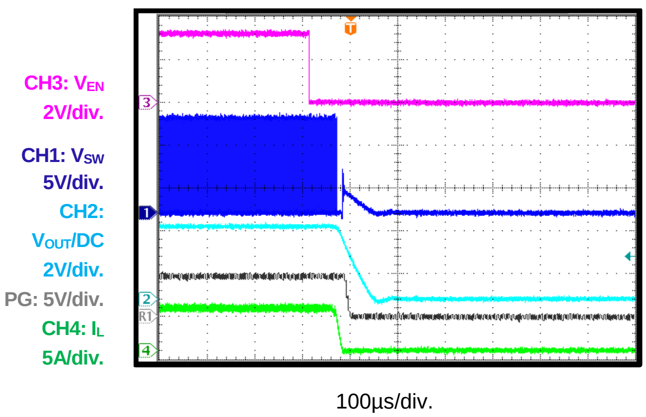
Shutdown through EN

I_{OUT} = 0A, FCCM



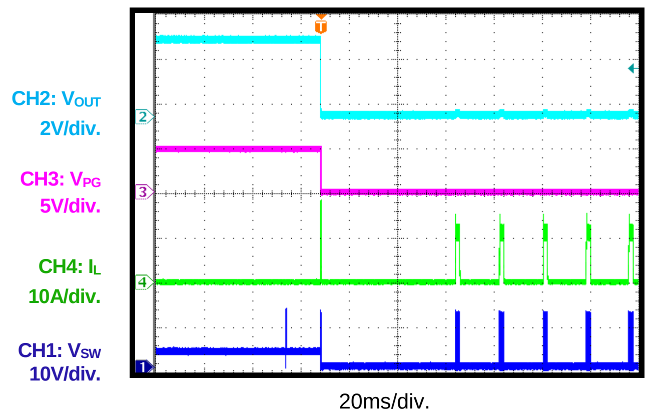
Shutdown through EN

I_{OUT} = 5A



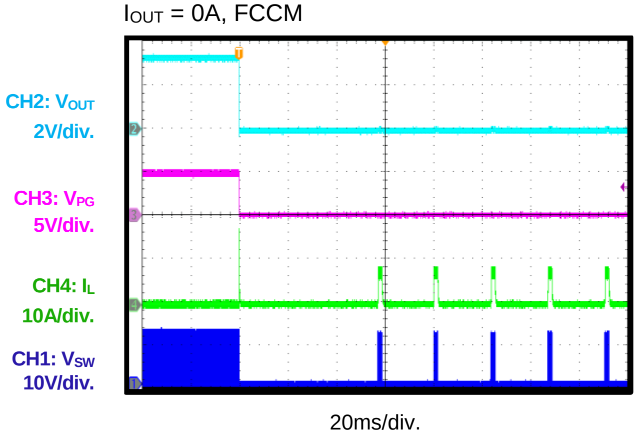
SCP Entry

I_{OUT} = 0A, AAM



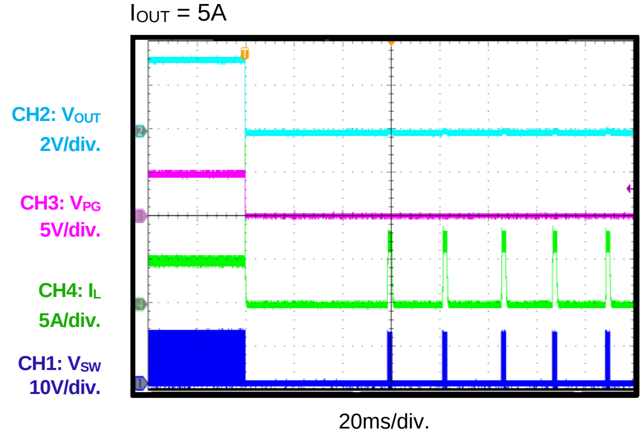
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 5A



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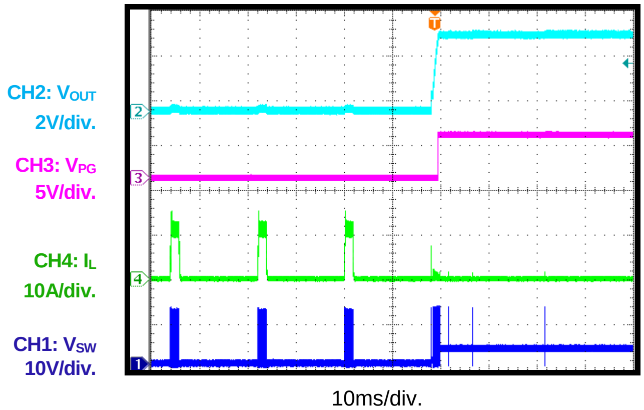
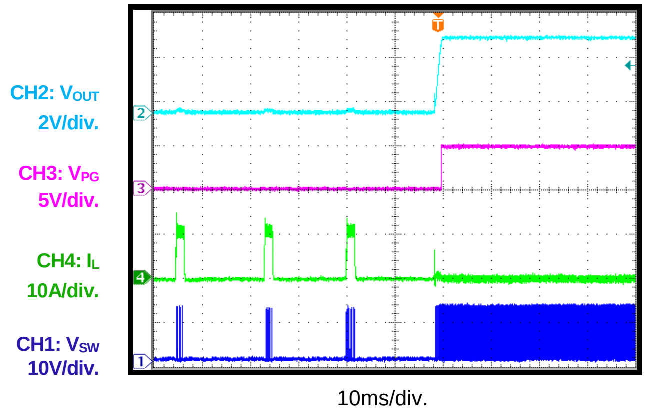
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

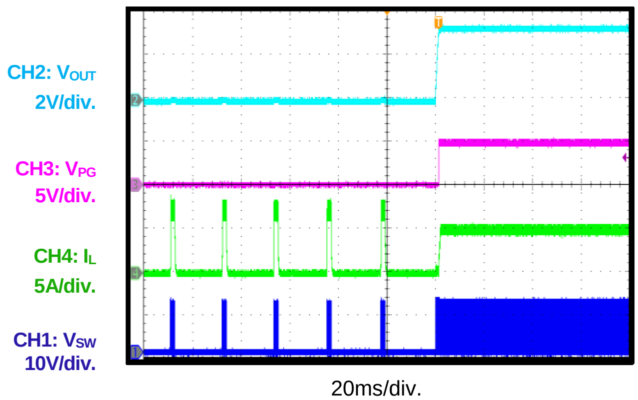
SCP Recovery
I_{OUT} = 0A, AAM



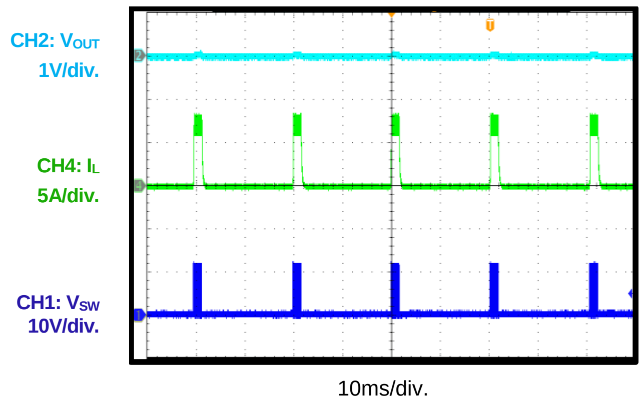
SCP Recovery
I_{OUT} = 0A, FCCM



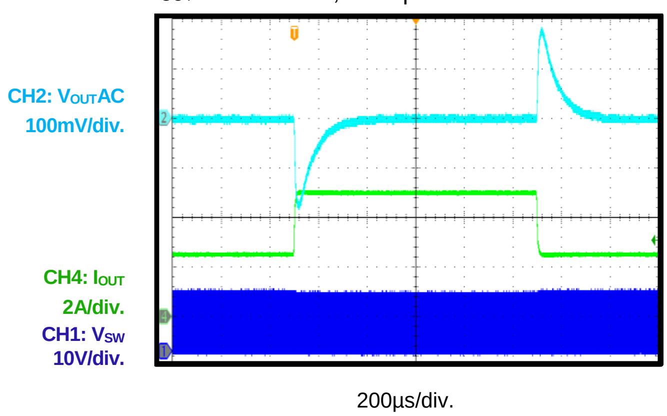
SCP Recovery
I_{OUT} = 5A



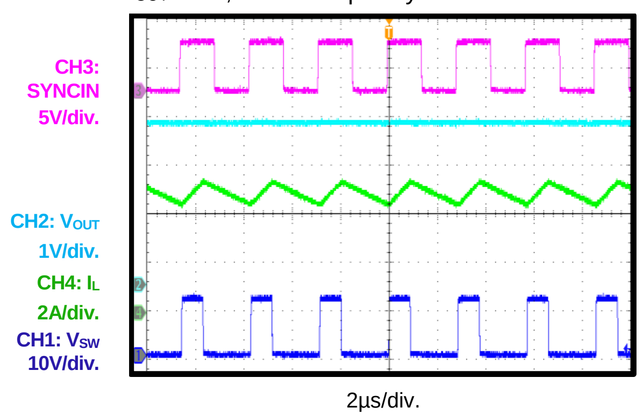
SCP Steady State



Load Transient
I_{OUT} = 2.5A to 5A, 1.6A/µs



SYNC Operation
I_{OUT} = 5A, SYNC frequency = 350kHz



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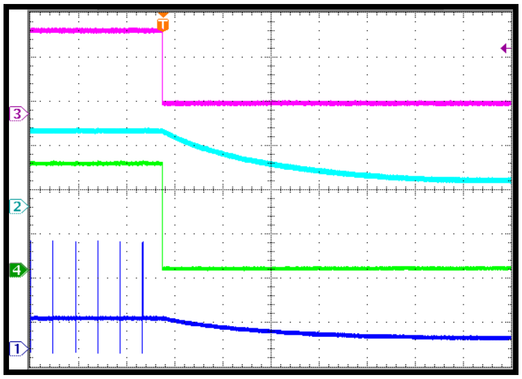
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

PG in Shutdown through EN

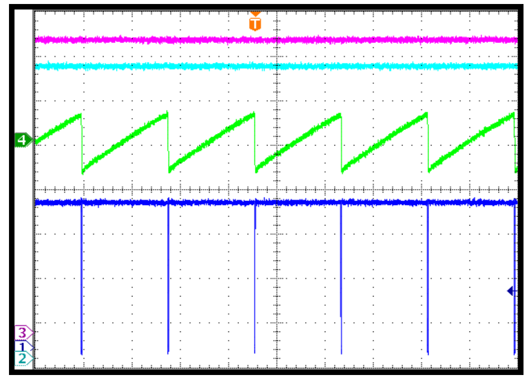
I_{OUT} = 0A, AAM



100ms/div.

Low-Dropout Mode

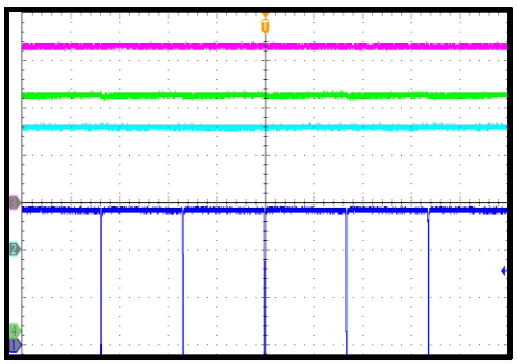
V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



4µs/div.

Low-Dropout Mode

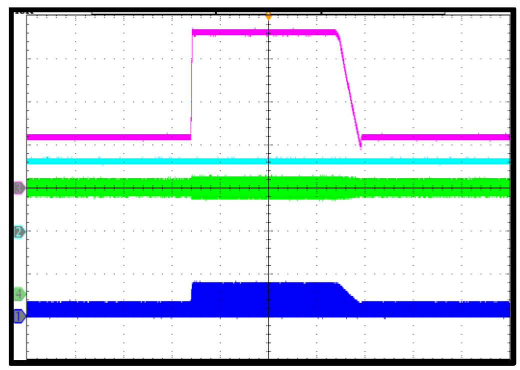
V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 5A



4µs/div.

Load Dump

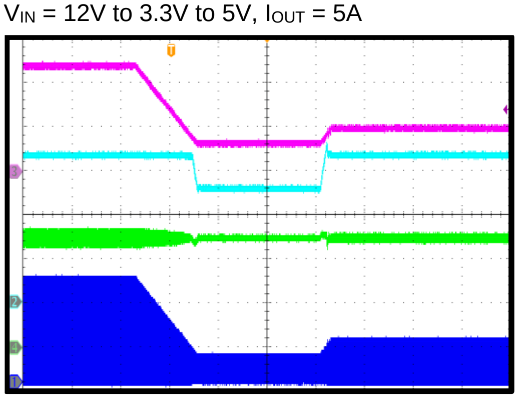
V_{IN} = 12V to 36V, I_{OUT} = 5A



1ms/div.

Cold Crank

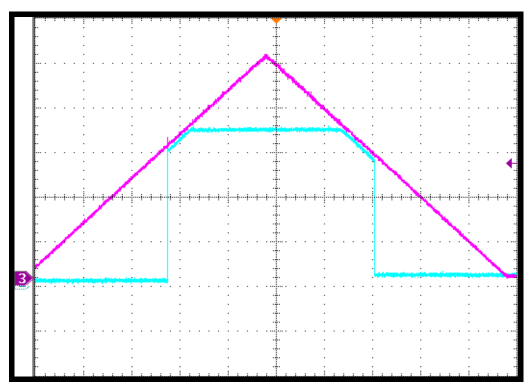
V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 5A



4ms/div.

V_{IN} Ramp Up and Down

I_{OUT} = 0.1A



1s/div.

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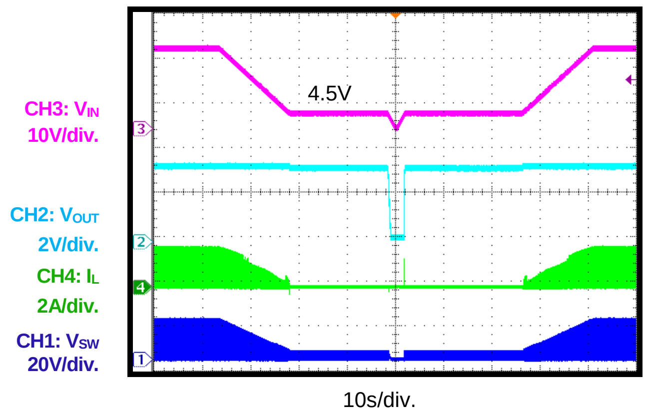
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM, T_A = 25°C, unless otherwise noted.

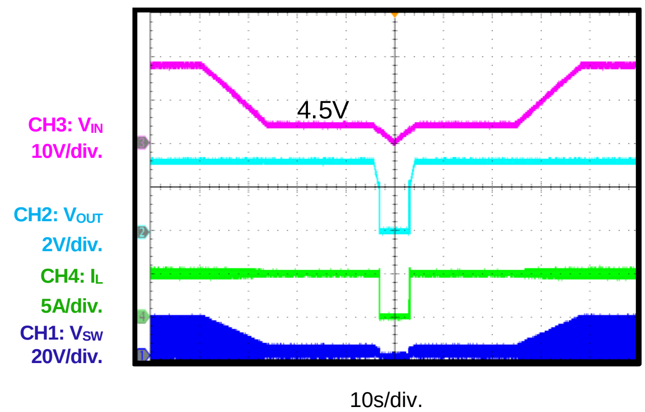
V_{IN} Ramp Down and Up

I_{OUT} = 1mA



V_{IN} Ramp Down and Up

I_{OUT} = 5A



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FUNCTIONAL BLOCK DIAGRAM

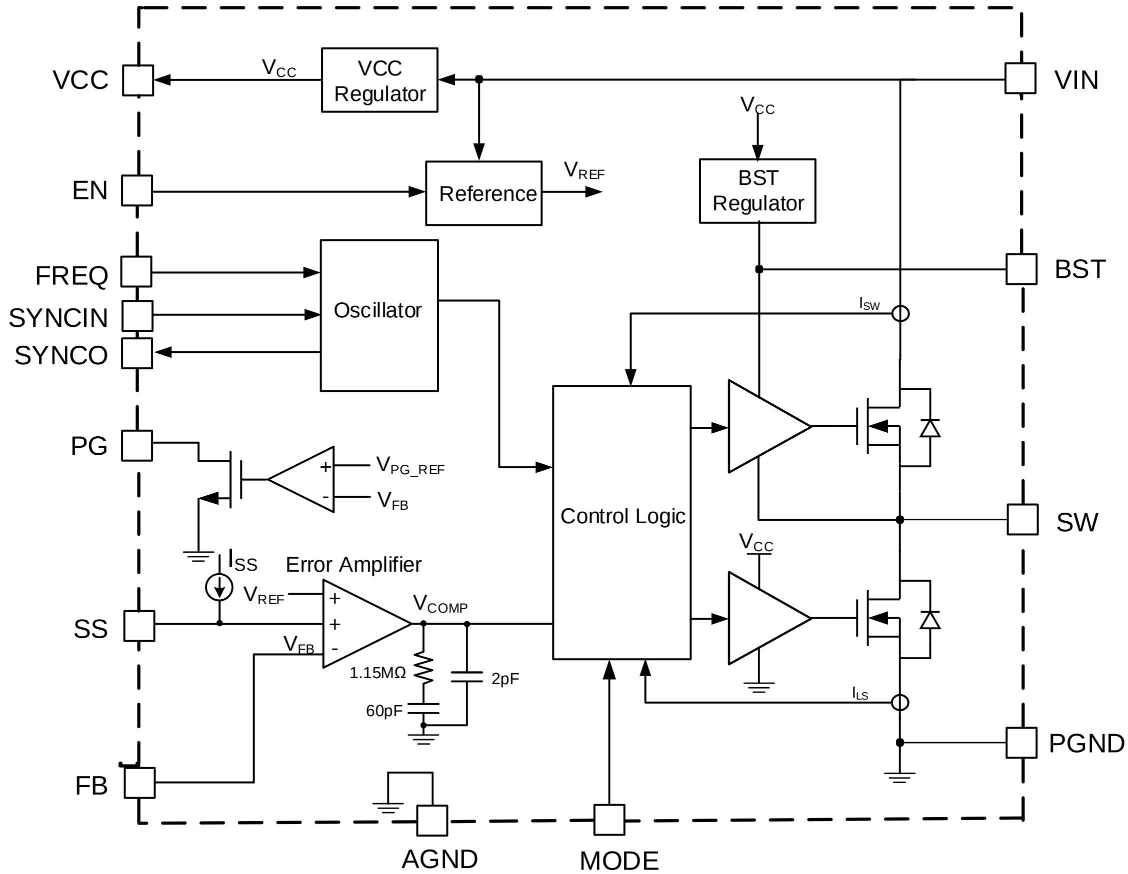

Figure 1: Functional Block Diagram

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Timing Sequence

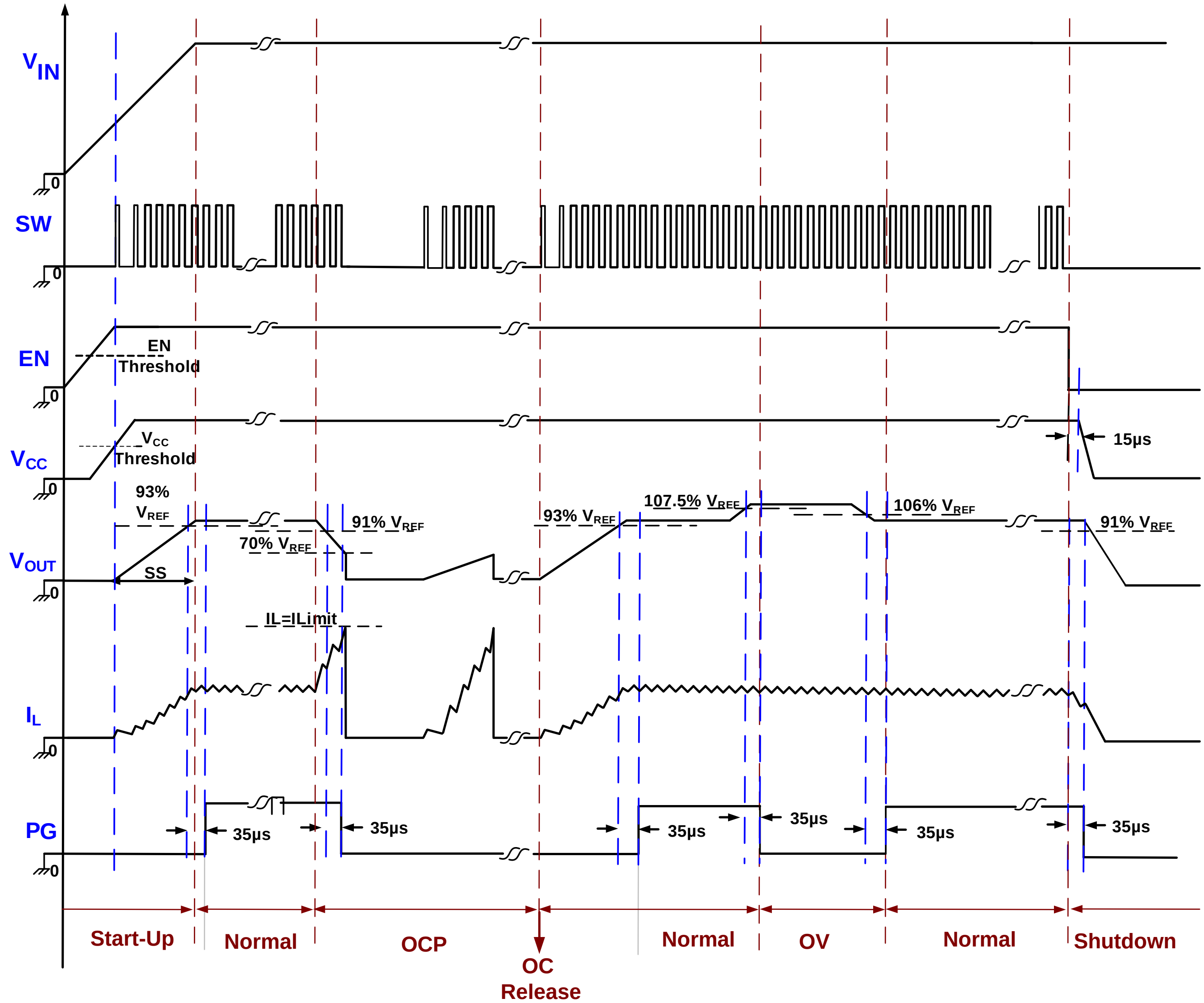

Figure 2: Timing Sequence

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OPERATION

The MPQ4315 is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides 5A of highly efficient output with current mode control.

The device features a wide input voltage range, configurable switching frequency, external soft start, and precision current limiting. Its very low operational quiescent current makes it ideal for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4315 operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until its current reaches the value set by internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the HS-FET turns off, the LS-FET turns on immediately and remains on until the next cycle starts. Once LS-FET is on, it remains on for at least 80ns before the next cycle starts.

If the HS-FET current does not reach the current value set by COMP within one PWM period, then the HS-FET remains on, saving a turn-off operation. If the on time lasts longer than 10µs even though the COMP current is not reached, the HS-FET is forced off.

Light-Load Operation

Under light-load conditions, the MPQ4315 can operate in two different modes by setting the MODE pin to a different status (see Figure 3).

When the CCM pin is pulled above 1.8, the MPQ4315 works in forced continuous conduction mode (FCCM). The device works with a fixed frequency across the no-load to full-load range in this mode. FCCM offers the advantages of a controllable frequency and lower output ripple at light loads.

When the MODE pin is below than 0.4V, the MPQ4315 works in asynchronous advanced mode (AAM). AAM optimizes efficiency during light-load and no-load conditions.

When AAM is enabled, the MPQ4315 first enters non-synchronous operation as long as the inductor current (I_L) approaches zero at light loads. If the load is further decreased or there is no load, V_{COMP} decreases to the set value, and the MPQ4315 enters AAM. In AAM, the internal clock is reset every time V_{COMP} crosses the set value. The crossover time is taken as benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the MPQ4315 operates in discontinuous conduction mode (DCM) or FCCM, which both have a constant switching frequency.

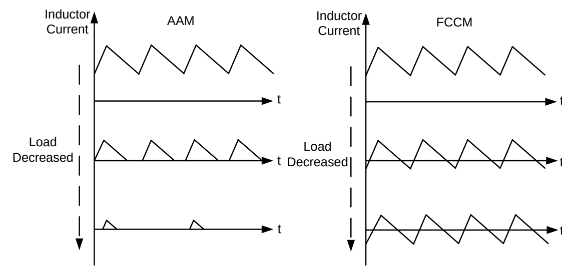

Figure 3: AAM vs. FCCM

Error Amplifier (EA)

The error amplifier (EA) compares the voltage on the FB pin (V_{FB}) with the internal reference voltage (V_{REF}, about 0.815V) and outputs a current proportional to the difference between the two. This output current is then used to charge the compensation network to form V_{COMP}, which controls the power MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V and its maximum is clamped to 2.0V. COMP is internally pulled down to GND when the device shuts down.

Internal VCC Regulator

Most of the internal circuitry is powered by the internal, 4.9V VCC regulator. This regulator uses V_{IN} as input and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the VCC voltage (V_{CC}) is in full regulation. When V_{IN} is below 4.9V, the V_{CC} output drops.

Bootstrap Charging

The bootstrap capacitor (C_{BST}) is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is lower than its regulation, a PMOS pass transistor connected

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from VCC to BST turns on to charge C_{BST}. Any external circuitry should provide enough voltage headroom to facilitate charging. When the HS-FET is on, the bootstrap voltage (V_{BST}) is above V_{CC}, so C_{BST} cannot be charged.

At higher duty cycles, the time period available to the bootstrap charging is shorter so C_{BST} may not charge sufficiently. If the external circuit does not have sufficient voltage and time to charge C_{BST}, extra external circuitry can be used to ensure that V_{BST} is within the normal operation range.

Low-Dropout Mode and BST Refresh

To improve dropout, the MPQ4315 is designed to operate at close to 100% duty cycle as long as the voltage from BST to SW is above 2.5V. When the BST-to-SW voltage drops below 2.5V, the HS-FET turns off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is mainly influenced by the voltage drop across the power MOSFET, the inductor resistance, the low-side diode, and the PCB resistance.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. The MPQ4315 can be enabled two ways:

1. Enable the IC with the external logic H/L signal. When EN is pulled below its falling threshold voltage (0.85V), the chip goes into the lowest shutdown current mode. Force this pin above the EN rising threshold voltage (1V) to turn on the part.
2. Enable the IC with the programmable V_{IN} under-voltage lockout (UVLO) threshold. With high enough input voltage (V_{IN}), the chip can be enabled and disabled by the EN pin. With the internal current source, this circuit can generate a programmable V_{IN} UVLO and hysteresis (see Figure 4).

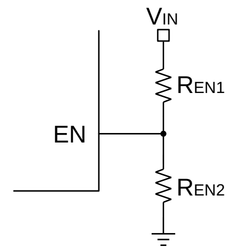

Figure 4: EN Divider Circuit

Frequency Programmable and Foldback

The MPQ4315 oscillating frequency can be programmed by an external resistor (R_{FREQ}) from the FREQ pin to ground, or by a logic-level SYNC signal.

To set the switching frequency f_{SW}, select the RFREQ value following the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 13. Note that f_{SW} will fold back at a high V_{IN} when set at high values to avoid the minimum on time being triggered and output going out of regulation. The f_{SW} vs. V_{IN} curve in Typical Performance Characteristics section on page 13 shows an example of R_{FREQ} is 12kΩ. The corresponding f_{SW} is about 2.1MHz at V_{IN} = 12V, and drops to below 1.5MHz when V_{IN} > 18V. f_{SW} then drops into the AM band (<1.8MHz), which should be avoided for car battery applications due to EMC requirements. The recommended f_{SW} range for car battery applications is 350kHz to 1000kHz. Table 1 lists recommended R_{FREQ} values for common frequencies. Higher frequencies may be supported for applications that do not have a critical f_{SW} limit or have a relatively low, stable V_{IN}.

Table 1: Resistor Selection for Frequency

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

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Frequency Spread Spectrum (FSS)

The MPQ4315 uses a 12kHz modulation frequency with a 128-step triangular profile to spread the internal oscillator frequency over a 20% (±10%) window. The steps are fixed and independent of the setting oscillator frequency to optimize the frequency spread spectrum (FSS) performance.

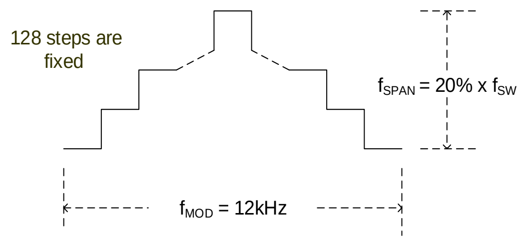

Figure 5: Spread Spectrum Scheme

Side bands are created by modulating the switching frequency with the triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics is distributed into smaller pieces. Thus, the peak EMI noise is significantly reduced.

Soft Start (SS)

Soft start (SS) is implemented to prevent V_{OUT} from overshooting during start-up. When soft start begins, an internal current source begins charging the external soft-start capacitor (C_{SS}). When the soft-start voltage (V_{SS}) is below V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF)=\frac{t_{SS}(ms)\times I_{SS}(\mu A)}{V_{REF}(V)}=6.25\times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Biased Start-Up

if V_{FB} > V_{SS} - 150mV at start-up, the output has a pre-biased voltage, and neither the HS-FET nor LS-FET turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown (TSD)

Thermal shutdown (TSD) is implemented to protect the MPQ4315 from thermal runaway. When the silicon die temperature exceeds its upper threshold, the power MOSFETs shut down. When the temperature falls back below this threshold, the MPQ4315 starts up and resumes normal operation.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET, then fed to the high-speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs. When the HS-FET is on, the comparator is blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the MOSFET current with V_{COMP}. When the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET. The internal power MOSFET's maximum current is internally limited cycle by cycle.

Hiccup Protection

When the output is shorted to ground, causing V_{OUT} to drop below 70% of its nominal output, the IC shuts down momentarily and discharges C_{SS}. Once the soft-start capacitor is fully discharged, the IC restart with a full soft start. This hiccup process repeats until the fault is removed.

Start-Up and Shutdown

If V_{IN} and EN exceeds their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents; then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer keeps the power MOSFET off for about 50µs to blank the startup glitches. When the soft start block is enabled, the SS output is held low to ensure the rest circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN low, V_{IN} low, and TSD. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4315 includes an open-drain power good (PG) output that whether V_{OUT} is within its normal range. Connect this pin to a high-voltage source, such as VCC, when used. PG goes high if V_{OUT} is within 93% to 106% of the nominal voltage, and goes low when V_{OUT} is above

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107.5% or below 91% of the nominal voltage.

SYNCIN and SYNCO

f_{SW} can be synced to the rising edge of the clock signal applied at the SYNCIN pin. The recommended SYNCIN frequency range is 350kHz to 1000kHz. SYNCIN off time should be shorter than the internal oscillator period, or the internal clock could turn on the HS-FET before SYNCIN's rising edge. There are no other limits on the pulse width of SYNCIN; however, there is always parasitic capacitance of the pad there, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.

When applying SYNCIN in AAM, drive SYNCIN below its specified threshold (0.4V) or leave SYNCIN floating before the MPQ4315 starts up to enter AAM. Then add the external SYNCIN clock. To avoid SYNCIN floating when using this function through an external clock, connect a resistor to GND. Given SYNCIN's drive capability, the resistor is recommended to be between 10kΩ and 51kΩ.

The SYNCO pin provides a default 180° phase-shifted clock from the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a 180° phase shift clock compared with the internal clock. If there is an external SYNCIN clock, SYNCO provides a 180° phase shift clock compared with the external SYNCIN clock. This enables the user to easily implement a dual-phase interleaved configuration.

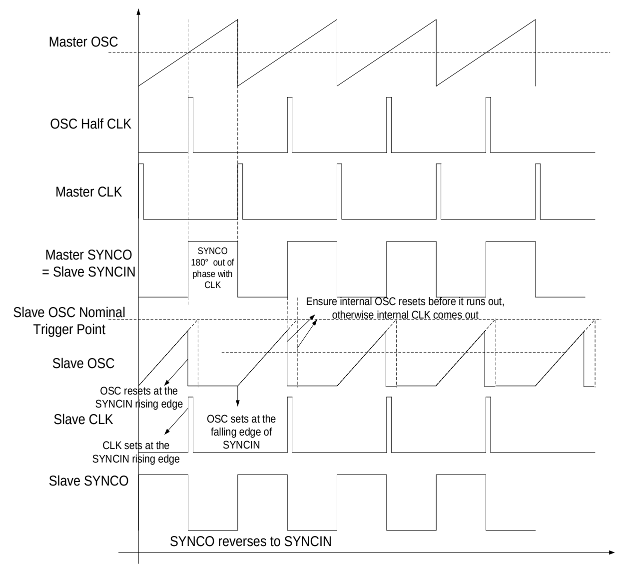

Figure 6: SYNCIN/SYNCO Scheme

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 7).

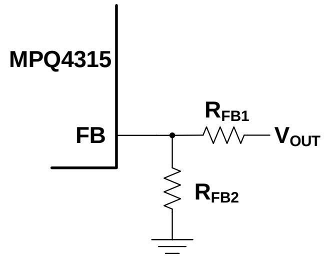

Figure 7: Feedback Network

Calculate R_{FB2} with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Recommended Resistors for Output Voltages

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor

The converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. Estimate the RMS current in C_{IN} with Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

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For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4315 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can then be calculated with Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I_{LP}) can be calculated with Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

VIN UVLO Setting

The MPQ4315 has an internal fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, and the falling threshold is about 2.65V. For applications that require a higher UVLO point, an external resistor divider can be placed between VIN and EN to achieve a higher equivalent UVLO threshold (see Figure 8).

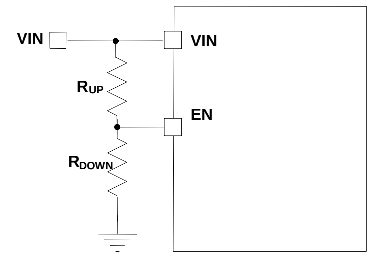

Figure 8: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (11)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

External BST Diode and Resistor

An External BST Diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. It is recommended for V_{CC} or V_{OUT} to be this power supply in the circuit (see Figure 9).

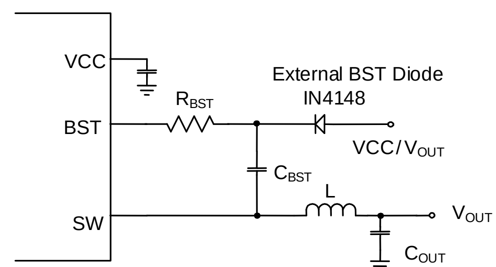

Figure 9: Optional External Bootstrap Diode to Enhance Efficiency

The recommended External BST Diode is IN4148, and the recommended BST capacitance is 0.1µF to 1µF. Place a resistor (R_{BST}) in series with the C_{BST} to reduce the SW rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction, but compromises efficiency. To make an appropriate tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

Setting the VCC Capacitor

The VCC capacitor should be 10 times greater than the boost capacitor. A VCC capacitor above 68µF is not recommended.

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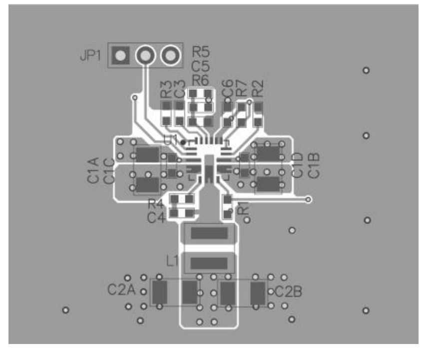
PCB Layout Guidelines [9]

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

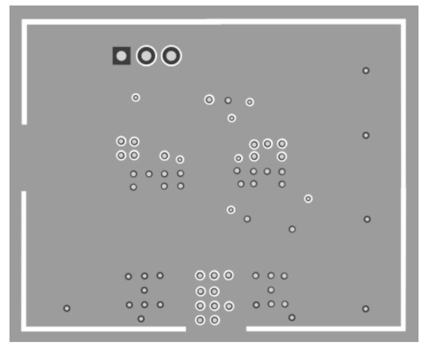
1. Place symmetric input capacitors as close as possible to the VIN and GND pins.
2. Connect a large copper ground plane directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to as possible the VCC and GND pins.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the IC to keep the trace that connects to FB as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

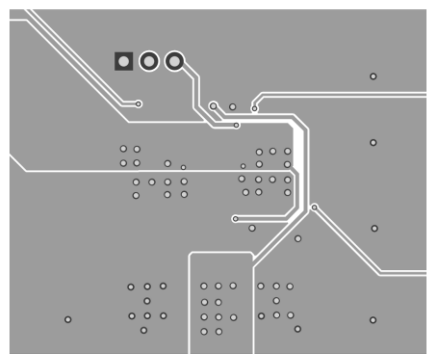
9) The recommended PCB layout is based on Figure 11.



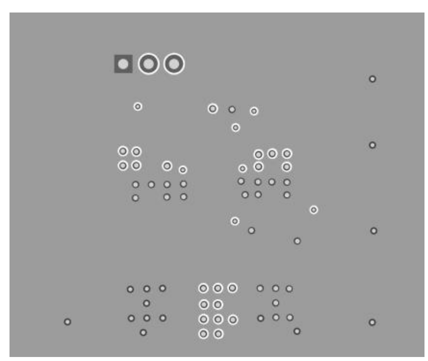
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 10: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

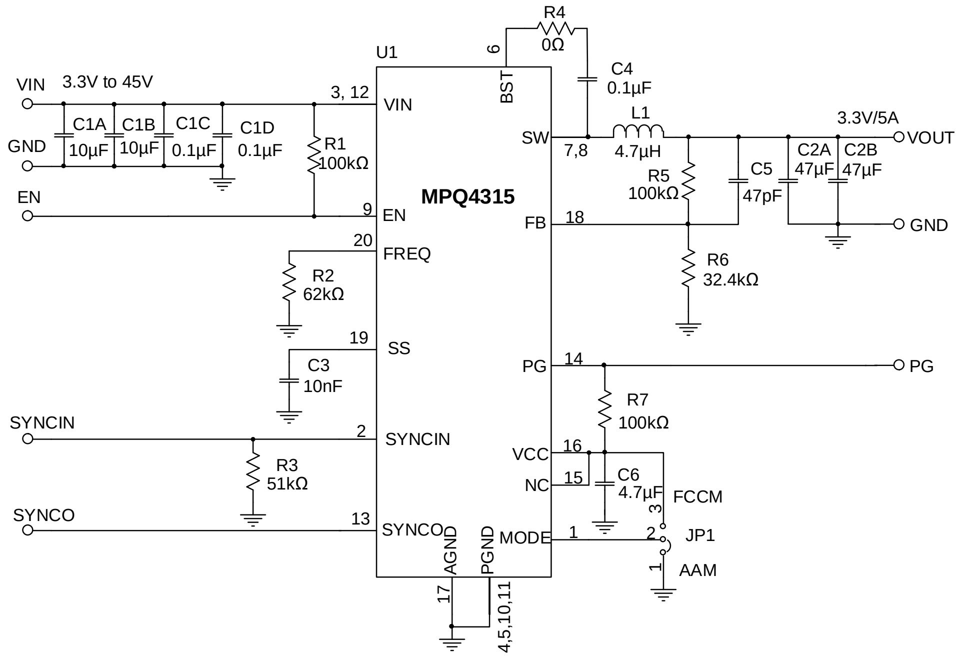

Figure 11: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 470kHz)

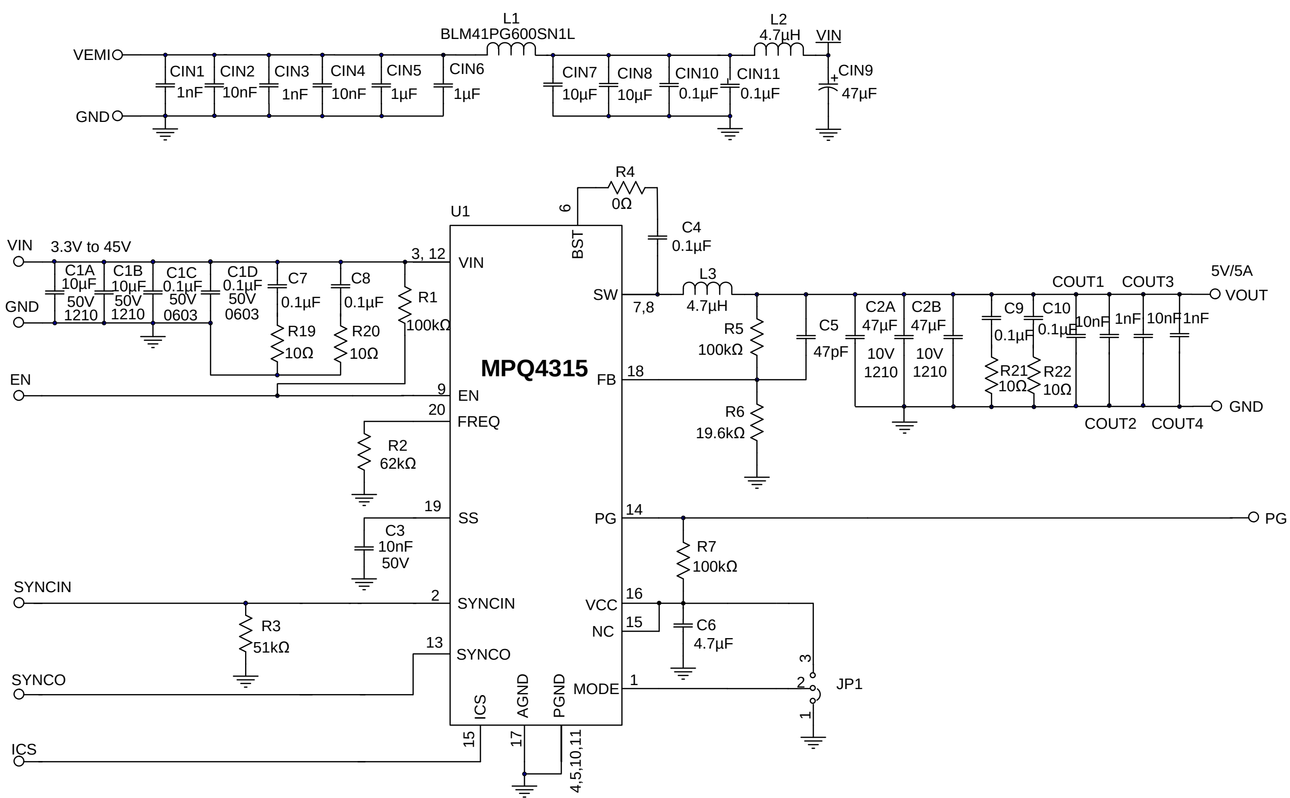

Figure 12: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 470kHz with EMI Filters)

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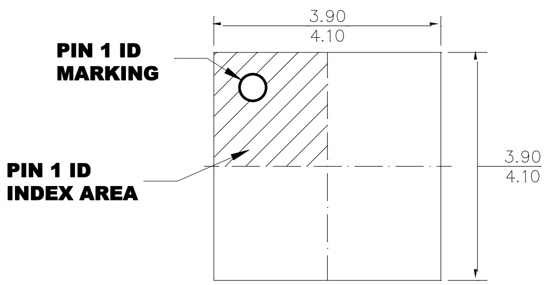
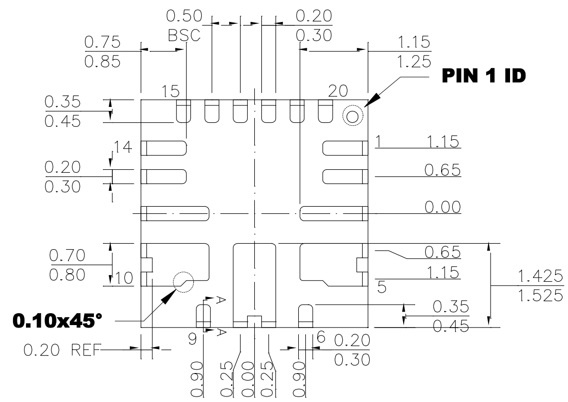
PACKAGE INFORMATION

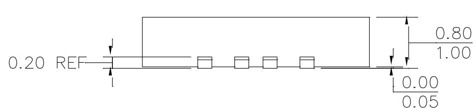
QFN-20 (4mmx4mm)
Wettable Flank



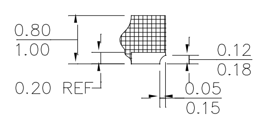
TOP VIEW



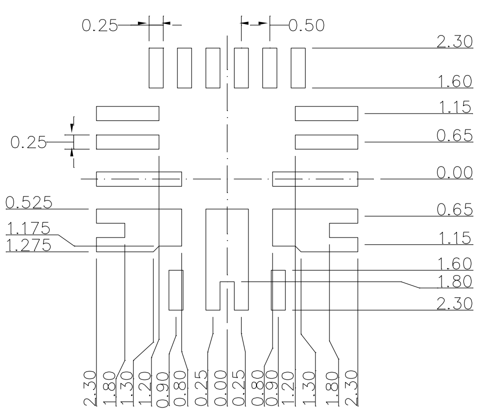
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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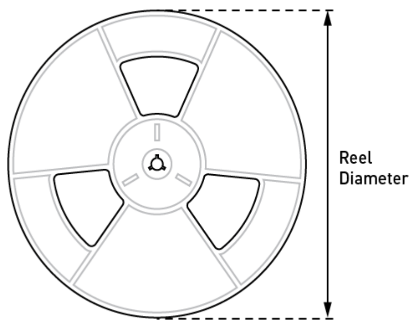
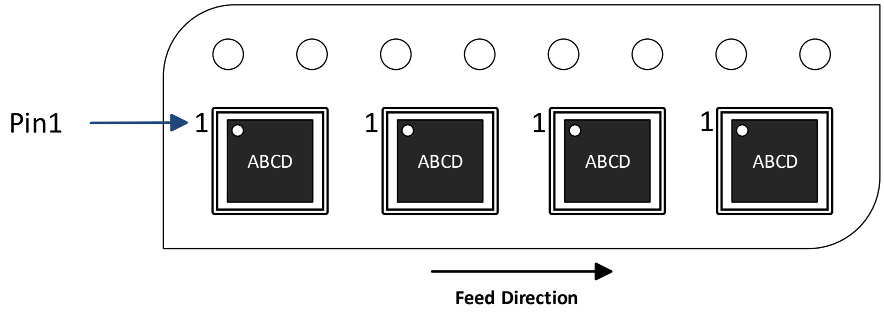
CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (10)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4315GRE-AEC1–Z	QFN-20 (4mmx4mm)	5000	N/A	13in	12mm	8mm

Note:

10) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for 500 pieces partial reel is “–P”, and tape & reel dimensions are the same as for the full reel.)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/3/2021	Initial Release	-

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Monolithic Power Systems (MPS):

MPQ4315GRE-AEC1-P MPQ4315GRE-AEC1-Z