



# MPF42791

## 2 to 16 Stacked Cells Battery Pack Fuel Gauge with Resistance Detection and Thermal Model

### DESCRIPTION

The MPF42791 is a drop-in solution to provide comprehensive status information on lithium-ion battery strings up to 16 series cells. The MPF42791 estimates the internal state-of-charge (SOC) and state-of-health (SOH) for each cell, as well as the full pack. The MPF42791 also determines impedance, remaining runtime, charge time, and instantaneous available power. On-board memory enables the lifetime logging of key parameters.

The MPF42791 is simple to use and supports a variety of lithium cell chemistries and cell sizes. A few basic configurations allow for quick set-up, and advanced configuration capabilities can fine-tune the device for specific applications.

When paired with an MP279x battery monitor, the MPF42791 can achieve SOC accuracy within 2.5% across the temperature range. The MPF42791 can also be paired with other analog front-end (AFE) or battery stack monitors. The 400kHz I<sup>2</sup>C interface provides standard, robust communication. The 5-level LED drivers provide a simple, cost-effective charge level indicator for the device.

The MPF42791 is available in a TQFN-32 (4mmx4mm) package.

### MINIMUM SYSTEM REQUIREMENTS

- BMS AFE Providing Individual Cell Voltages, Pack Currents, and Temperatures
- M0 System MCU with I<sup>2</sup>C and Interrupt, 48KB of Flash and 4KB of RAM

### FEATURES

- Compatible with Commonly Used Battery Monitors for Up to 16 Series Cells
  - $\pm 2.5\%$  State-of-Charge (SOC) Accuracy when Paired with MP279x Battery Monitors
- Provides Critical Battery Information:
  - Pack and Cell SOC
  - Pack and Cell State-of-Health (SOH)
  - Remaining Runtime and Charge Time
  - Instantaneous Available Power
- Supports a Wide Variety of Lithium Cells
- Adaptive Learning Can Be Enabled to:
  - Refine Initial Charge Settings
  - Refine Initial Discharge Settings
  - Update Individual Cells' State-of-Health (SOH) to Track Degradation
  - Update Equivalent Series Resistance (ESR) to Track Degradation
- Provides Lifetime Logging
- Supports 5-Level LED SOC Indicator with Push-Button Trigger
- 2.5V Minimum Supply Voltage
- Low Current Consumption: 6 $\mu$ A in Disabled Mode and 135 $\mu$ A (Average) in Operating Mode during Rest
- Supports Up to 400kHz I<sup>2</sup>C with CRC for Robust Communication
- Available in a Compact TQFN-32 (4mmx4mm) Package
- Available in Turn-Key MPS BMS Module:
  - MBM1xS-P50-B and MBM1xS-P100-B

### APPLICATIONS

- Light EVs: Scooters, Bikes, and Golf Carts
- Energy Storage: Uninterruptable Power Supplies (UPS) and Renewable Energy
- Industrial Robots, Floor Cleaners, and Forklifts
- Cordless Tools and Gardening Equipment

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## TYPICAL APPLICATION

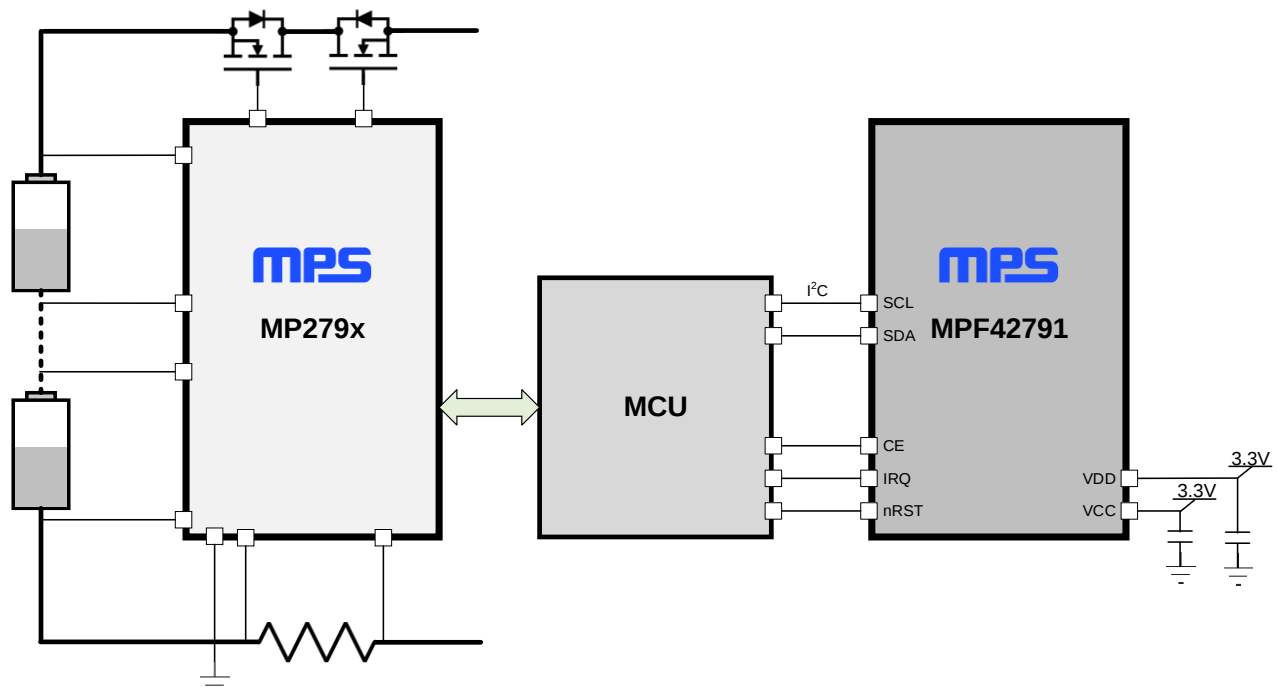


Figure 1: MPF42791 with MP279x AFE Typical Electrical Diagram

## ORDERING INFORMATION

| Part Number*          | Package           | Top Marking | MSL Rating |
|-----------------------|-------------------|-------------|------------|
| MPF42791DRT-0B-yyyy** | TQFN-32 (4mmx4mm) | See Below   | 3          |
| EVKT MPF42791         | Evaluation kit    | -           | -          |
| EVKT-MBM16S-P50-B     | Evaluation kit    | -           | -          |

\* For Tape & Reel, add suffix -Z (e.g. MPF42791DRT-0B-yyyy-Z).

\*\* “-yyyy” refers to the default configuration identifier (“-0000” by default), where each “y” is a hexadecimal value between 0 and F. Work with an MPS FAE to obtain a customized default configuration.

## TOP MARKING

**MPSYWW**  
**M4279X**  
**LLLLLL**

MPF4279X Family generic version

MPS: MPS prefix

Y: Year code

WW: Week code

M4279X: Family part number\*

LLLLLL: Lot number

\* The specific part number is in the IC\_VER register.

## EVALUATION KITS EVKT-MBM1XS-P50-B (MP279X BMS)

### EVKT-MBM16S-P50-B

EVKT-MBM16S-P50-B kit contents (items below can be ordered separately):

| # | Part Number           | Item                                                                         | Quantity |
|---|-----------------------|------------------------------------------------------------------------------|----------|
| 1 | MBM16S-P50-B          | MPF42791DRT-0B-0001 and MP2797DFP-0001 reference design and evaluation board | 1        |
| 2 | EVKT-USB_RS232/I2C-01 | USB to RS232 / I <sup>2</sup> C adapter                                      | 1        |
| 3 | Online resources      | Include datasheet, user guide, product brief, and GUI                        | 1        |

### EVKT-MBM14S-P50-B

EVKT-MBM14S-P50-B kit contents (items below can be ordered separately):

| # | Part Number           | Item                                                                         | Quantity |
|---|-----------------------|------------------------------------------------------------------------------|----------|
| 1 | MBM14S-P50-B          | MPF42791DRT-0B-0001 and MP2791DFP-0001 reference design and evaluation board | 1        |
| 2 | EVKT-USB_RS232/I2C-01 | USB to RS232 / I <sup>2</sup> C adapter                                      | 1        |
| 3 | Online resources      | Include datasheet, user guide, product brief, and GUI                        | 1        |

Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.

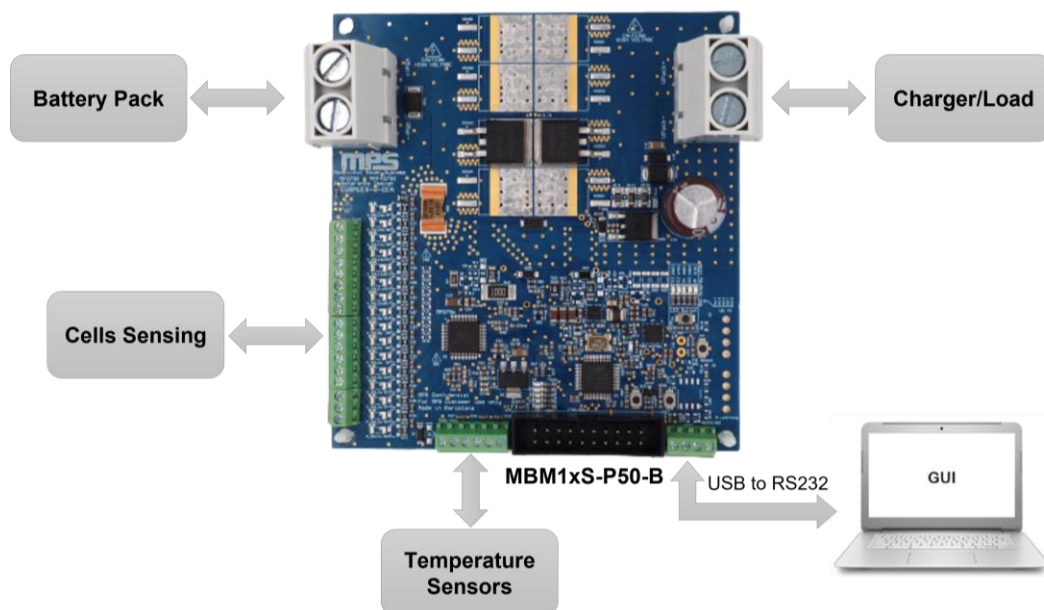
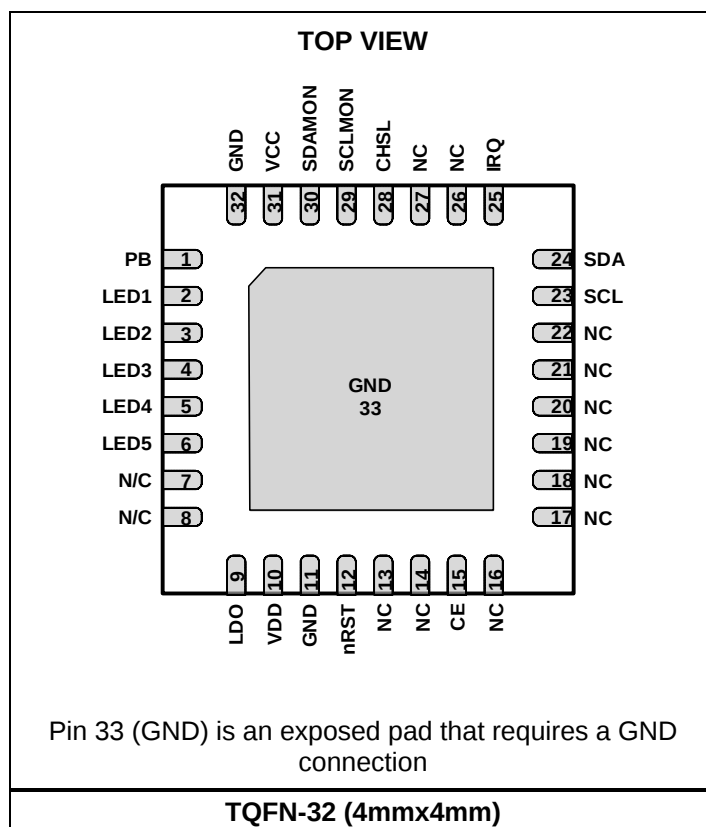


Figure 2: MBM1xS-P50-B Evaluation Kit Set-Up

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name   | I/O   | Description                                                                                                                                                                                             |
|-------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | PB     | I     | <b>Push-button.</b> Triggers state-of-charge (SOC) LED indicator.                                                                                                                                       |
| 2     | LED1   | O     | <b>LED 1 driver.</b> The LED1 pin reports the SOC with a 330Ω resistor in series.                                                                                                                       |
| 3     | LED2   | O     | <b>LED 2 driver.</b> The LED2 pin reports the SOC with a 330Ω resistor in series.                                                                                                                       |
| 4     | LED3   | O     | <b>LED 3 driver.</b> The LED3 pin reports the SOC with a 330Ω resistor in series.                                                                                                                       |
| 5     | LED4   | O     | <b>LED 4 driver.</b> The LED4 pin reports the SOC with a 330Ω resistor in series.                                                                                                                       |
| 6     | LED5   | O     | <b>LED 5 driver.</b> The LED5 pin reports the SOC with a 330Ω resistor in series.                                                                                                                       |
| 7     | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 8     | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 9     | LDO    | Power | <b>Internal LDO.</b> Bypass the LDO pin with a 2.2μF + 100nF ceramic capacitor connected to ground.                                                                                                     |
| 10    | VDD    | Power | <b>Power supply input.</b> Bypass VDD with a 2.2μF ceramic capacitor connected to ground.                                                                                                               |
| 11    | GND    | Power | <b>Ground pin.</b>                                                                                                                                                                                      |
| 12    | nRST   | I     | <b>IC reset control.</b>                                                                                                                                                                                |
| 13    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 14    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 15    | CE     | I     | <b>Chip enabled.</b> Set the CE pin to stop fuel gauge updates and disable the communication interface to minimize current consumption.                                                                 |
| 16    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 17    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 18    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 19    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 20    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 21    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 22    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 23    | SCL    | I/O   | <b>I<sup>2</sup>C interface clock.</b> Connect the SCL pin to the logic rail through a 10kΩ resistor.                                                                                                   |
| 24    | SDA    | I/O   | <b>I<sup>2</sup>C interface data.</b> Connect the SDA pin to the logic rail through a 10kΩ resistor.                                                                                                    |
| 25    | IRQ    | O     | <b>Interrupt request pin.</b> The IRQ pin is the interrupt going to the host system(s).                                                                                                                 |
| 26    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 27    | NC     | -     | <b>No connection.</b>                                                                                                                                                                                   |
| 28    | CHSL   | I     | <b>Channel selection.</b> The CHSL pin selects which I <sup>2</sup> C channel is capable of writing data into the fuel gauge memory. Pull CHSL high to write data using the secondary I <sup>2</sup> C. |
| 29    | SCLMON | I/O   | <b>Secondary I<sup>2</sup>C interface clock.</b> Connect the SCLMON pin to the logic rail through a 10kΩ resistor.                                                                                      |
| 30    | SDAMON | I/O   | <b>Secondary I<sup>2</sup>C interface data.</b> Connect the SDAMON pin to the logic rail through a 10kΩ resistor.                                                                                       |
| 31    | VCC    | Power | <b>3V to 3.3V power supply input.</b> Bypass the VCC pin with a 2.2μF ceramic capacitor connected to ground.                                                                                            |
| 32    | GND    | Power | <b>Ground pin.</b>                                                                                                                                                                                      |
| 33    | GND    | Power | <b>Ground pin.</b>                                                                                                                                                                                      |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                |                                 |
|----------------------------------------------------------------|---------------------------------|
| VCC supply voltage (V <sub>CC</sub> )                          | 3.6V                            |
| VDD supply voltage (V <sub>DD</sub> )                          | 3.6V                            |
| nRST pin                                                       | -0.3V to +3.6V                  |
| All other pins                                                 | -0.3V to V <sub>CC</sub> + 0.3V |
| Total power dissipation (T <sub>A</sub> = 25°C) <sup>(2)</sup> | 500mW                           |
| Storage temperature                                            | -55°C to +150°C                 |
| Junction temperature                                           | -55°C to +150°C                 |

## ESD Ratings

|                        |        |
|------------------------|--------|
| Human body model (HBM) | ±4000V |
|------------------------|--------|

## Recommended Operating Conditions <sup>(3)</sup>

|                                           |                                 |
|-------------------------------------------|---------------------------------|
| Supply voltage (V <sub>DD</sub> )         | 3V to 3.6V                      |
| All other pins                            | -0.3V to V <sub>CC</sub> + 0.3V |
| Operating junction temp (T <sub>J</sub> ) | -40°C to +85°C                  |

| Thermal Resistance <sup>(4)</sup> | $\theta_{JA}$ | $\theta_{JC}$ |
|-----------------------------------|---------------|---------------|
| TQFN-32 (4mmx4mm)                 | 47            | 4.5           |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature, T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

| Parameters                                         | Symbol                   | Condition                                                                                                           | Min                    | Typ  | Max                    | Units |
|----------------------------------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------|------------------------|------|------------------------|-------|
| State-of-Charge (SOC) Performance                  |                          |                                                                                                                     |                        |      |                        |       |
| Pack state-of-charge (SOC) accuracy <sup>(5)</sup> | $\theta_{ERR}$           | MPS MP279x AFE family,<br>15°C ≤ T <sub>A</sub> ≤ 35°C, I <sub>CHG</sub> ≤ 0.5C,<br>I <sub>DIS</sub> ≤ 0.5C         | -2                     | 0    | +2                     | %     |
|                                                    |                          | MPS MP279x AFE family,<br>10°C ≤ T <sub>A</sub> ≤ 50°C, I <sub>CHG</sub> ≤ 1C,<br>I <sub>DIS</sub> ≤ 1C             | -3                     | 0    | +3                     | %     |
|                                                    |                          | MPS MP279x AFE family,<br>10°C ≤ T <sub>A</sub> ≤ 50°C, I <sub>CHG</sub> ≤ 2C,<br>I <sub>DIS</sub> ≤ 2C             | -4                     | 0    | +4                     | %     |
| Power Supply                                       |                          |                                                                                                                     |                        |      |                        |       |
| VDD operating voltage range                        | V <sub>DD</sub>          |                                                                                                                     | 2.5                    | 3.3  | 3.6                    | V     |
| VCC operating voltage range                        | V <sub>CC</sub>          |                                                                                                                     | 2.5                    | 3.3  | 3.6                    | V     |
| Total active current                               | I <sub>DD_ACTIVE</sub>   | V <sub>DD</sub> = 3.3V, LEDs off, fuel gauge updating                                                               |                        | 4.3  |                        | mA    |
| Total standby current                              | I <sub>DD_STANDBY</sub>  | V <sub>DD</sub> = 3.3V, LEDs off, fuel gauge idle                                                                   |                        | 50   |                        | μA    |
| Average operating current during CHG or DSG        | I <sub>DD_CHG/DSG</sub>  | V <sub>DD</sub> = 3.3V, LEDs off, EXE_TIME = 4s, NCELLS_SER = 10, with I <sup>2</sup> C traffic                     |                        | 476  |                        | μA    |
| Average operating current during rest              | I <sub>DD_REST</sub>     | V <sub>DD</sub> = 3.3V, LEDs off, NCELLS_SER = 10, EXE_TIME = 4s, WEXE_TIME_REST = 4, with I <sup>2</sup> C traffic |                        | 192  |                        | μA    |
| Total disabled current                             | I <sub>DD_DIS</sub>      | V <sub>DD</sub> = 3.3V                                                                                              |                        | 6    |                        | μA    |
| Power-On Reset (POR)                               |                          |                                                                                                                     |                        |      |                        |       |
| Release threshold of POR                           | V <sub>ROT</sub>         | V <sub>DD</sub> rising                                                                                              | 1.66                   | 1.79 | 1.9                    | V     |
| nRST Pin                                           |                          |                                                                                                                     |                        |      |                        |       |
| nRST pin threshold voltage                         | V <sub>RST</sub>         |                                                                                                                     | 0.2 x V <sub>DD</sub>  |      | 0.9 x V <sub>DD</sub>  | V     |
| Minimum pulse width on nRST pin                    | t <sub>RST</sub>         | V <sub>DD</sub> = 3.3V                                                                                              |                        | 700  |                        | ns    |
| Timeout after reset                                | t <sub>TOUT</sub>        |                                                                                                                     |                        | 64   | 128                    | ms    |
| CE                                                 |                          |                                                                                                                     |                        |      |                        |       |
| Low input voltage                                  | V <sub>OL_CE</sub>       | I <sub>OL</sub> = 5mA                                                                                               | -0.3                   |      | 0.35 x V <sub>DD</sub> | V     |
| High input voltage                                 | V <sub>OH_CE</sub>       |                                                                                                                     | 0.65 x V <sub>DD</sub> |      | 0.3V + V <sub>DD</sub> | V     |
| Low leakage current                                | I <sub>CE_LKG_LOW</sub>  | V <sub>CE</sub> = 3.3V                                                                                              |                        |      | 3                      | μA    |
| High leakage current                               | I <sub>CE_LKG_HIGH</sub> | V <sub>CE</sub> = 3.3V                                                                                              |                        |      | 3                      | μA    |
| IRQ                                                |                          |                                                                                                                     |                        |      |                        |       |
| Low output voltage                                 | V <sub>IRQL</sub>        | Sink = 4mA                                                                                                          |                        |      | 0.4                    | V     |
| High output voltage                                | V <sub>IRQH</sub>        | Source = 4mA                                                                                                        | V <sub>DD</sub> - 0.4  |      |                        | V     |
| PB                                                 |                          |                                                                                                                     |                        |      |                        |       |
| Low input voltage                                  | V <sub>PBL</sub>         |                                                                                                                     | -0.3                   |      | 0.35 x V <sub>DD</sub> | V     |
| High input voltage                                 | V <sub>PBH</sub>         |                                                                                                                     | 0.65 x V <sub>DD</sub> |      | 0.3V + V <sub>DD</sub> | V     |
| CHSL                                               |                          |                                                                                                                     |                        |      |                        |       |
| Low input voltage                                  | V <sub>PBL</sub>         |                                                                                                                     | -0.3                   |      | 0.35 x V <sub>DD</sub> | V     |
| High input voltage                                 | V <sub>PBH</sub>         |                                                                                                                     | 0.65 x V <sub>DD</sub> |      | 0.3V + V <sub>DD</sub> | V     |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 3.3V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

| Parameters                                   | Symbol        | Condition                  | Min                 | Typ | Max                 | Units   |
|----------------------------------------------|---------------|----------------------------|---------------------|-----|---------------------|---------|
| <b>LEDs</b>                                  |               |                            |                     |     |                     |         |
| High-level output voltage                    | $V_{OH\_LED}$ | Output current = 4 mA      | $V_{DD} - 0.4V$     |     |                     | V       |
| High-level output current                    | $I_{OH\_LED}$ | $V_{LEDx} = V_{DD} - 0.4V$ | 4                   |     |                     | mA      |
| <b>I<sup>2</sup>C DC Characteristics</b>     |               |                            |                     |     |                     |         |
| High input voltage                           | $V_{IH}$      | SCL, SDA                   | $0.7 \times V_{DD}$ |     | $0.3V + V_{DD}$     | V       |
| Low input voltage                            | $V_{IL}$      | SCL, SDA                   | -0.5                |     | $0.3 \times V_{DD}$ | V       |
| Low output voltage                           | $V_{OL}$      | SDA, sink current = 3mA    |                     |     | 0.4                 | V       |
| <b>I<sup>2</sup>C Timing Characteristics</b> |               |                            |                     |     |                     |         |
| Spikes suppressed by input filter            | $t_{SP}$      |                            | 0                   |     | 50                  | ns      |
| Operating frequency range                    | $f_{SCL}$     |                            |                     |     | 400                 | kHz     |
| SCL clock low period                         | $t_{LOW}$     |                            | 1.125               |     |                     | $\mu s$ |
| SCL clock high period                        | $t_{HIGH}$    |                            | 1.125               |     |                     | $\mu s$ |
| SCL and SDA falling time                     | $t_{FALL}$    |                            |                     |     | 0.34                | $\mu s$ |
| SCL and SDA rising time                      | $t_{RISE}$    |                            |                     |     | 0.34                | $\mu s$ |
| Data hold time                               | $t_{HD\_DAT}$ |                            | 0                   |     |                     | ns      |
| Data set-up time                             | $t_{SU\_DAT}$ |                            | 125                 |     |                     | ns      |
| Data valid time                              | $t_{V\_DAT}$  |                            | 475                 |     |                     | ns      |
| Set-up time for a repeated start condition   | $t_{SU\_STA}$ |                            | 125                 |     |                     | ns      |
| Hold time for a repeated start condition     | $t_{HD\_STA}$ |                            | 0                   |     |                     | ns      |
| Set-up time for a stop condition             | $t_{SU\_STO}$ |                            | 125                 |     |                     | ns      |

### Note:

- 5) Validated on a 10S1P Samsung INR18650 25R pack (see the Typical Performance Characteristics section on page 9 for more details). Similar results can be achieved with other cell/pack types after characterization.

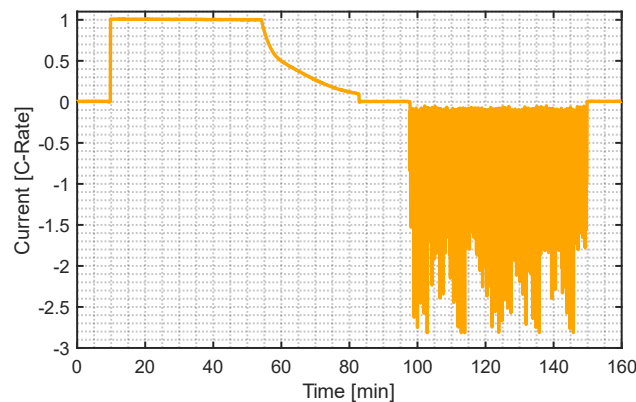
## TYPICAL PERFORMANCE CHARACTERISTICS

The MPF42791 fuel gauge performance depends on multiple factors, such as the accuracy of the measurements, the correctness of the configuration, and the fidelity of the cell mathematical model. This means that fuel gauge performance may vary depending on the battery operating conditions.

This section shows examples of the MPS MPF42791 fuel gauge pack's SOC performance when paired with MPS's MP279x AFE family.

### Constant-Current/Constant-Voltage (CC/CV) Charge and Dynamic Discharge Cycle

The next scenarios consist of charging a 10S1P <sup>(6)</sup> battery using the typical CC/CV method, followed by a highly dynamic discharge at different ambient temperatures. The charge constant current rate is 1C, while the charge termination current in this example is 0.1C. The highly dynamic discharge corresponds to a typical e-bike's current profile, with an average current of 1C and maximum peak currents up to 2.8C. Figure 3 shows the current profile of the complete cycle at 25°C.



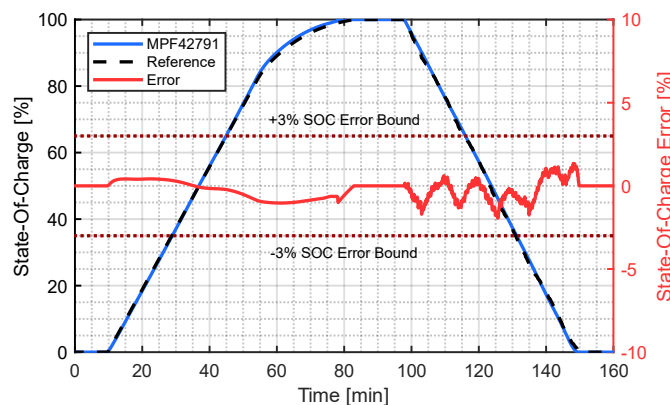
**Figure 3: CC/CV Charge and Dynamic Discharge Current Profile**

Figure 4 shows the MPF42791's performance for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 25°C. During charge, the root-mean-squared <sup>(7)</sup> and maximum pack SOC error are 0.61% and 1.03%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.78% and 1.94%, respectively.

#### Notes:

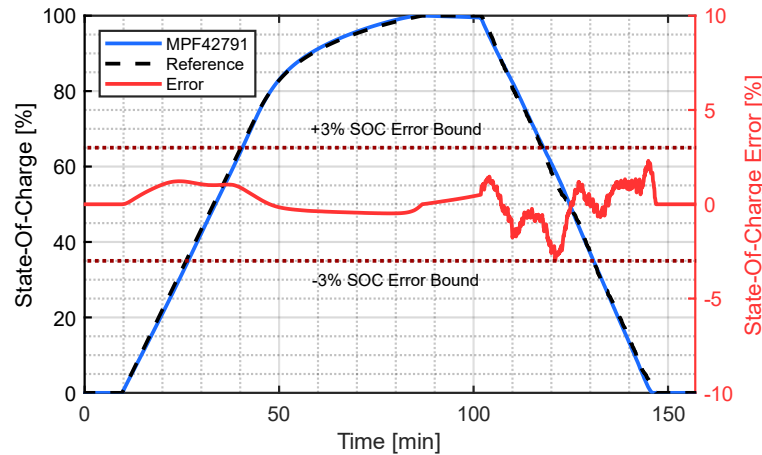
6) 10S1P refers to the battery configuration. There are 10 groups of 1 parallel cell connected in series.

7) The RMS error is equal to  $\sqrt{\frac{\sum_{n=1}^N (\theta_n - \hat{\theta}_n)^2}{N}}$ , where  $\theta$  is the actual SOC,  $\hat{\theta}$  is the estimated SOC, and N is the number of samples.



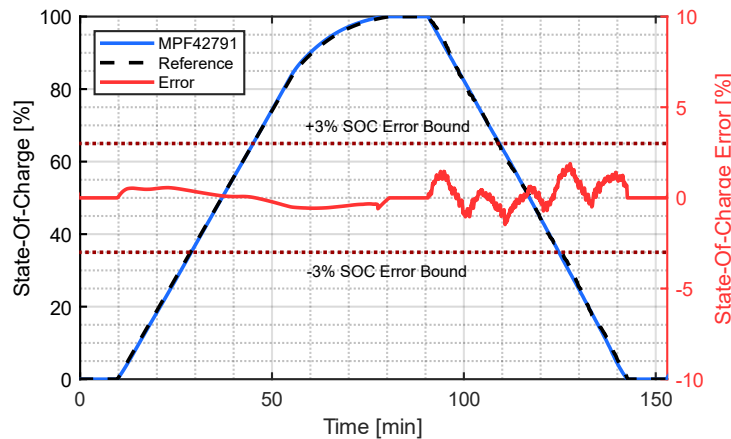
**Figure 4: MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 25°C)**

Figure 5 shows the MPF42791's performance for the CC/CV charge and dynamic discharge cycle at an ambient temperature of 0°C. During charge, the root-mean-squared and maximum pack SOC error are 0.68% and 1.22%, respectively. During discharge, the root-mean-squared and pack SOC error are 1.15% and 2.97%, respectively.



**Figure 5: MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 0°C)**

Figure 6 shows the MPF42791's performance for the CC/CV charge and dynamic discharge cycle at 40°C ambient temperature. During charge, the root-mean-squared and maximum pack SOC error are 0.40% and 0.60%, respectively. During discharge, the root-mean-squared and pack SOC error are 0.77% and 1.89%, respectively.



**Figure 6: MPF42791 Performance for a CC/CV Charge and Dynamic Discharge (Ambient Temperature = 40°C)**

## Performance Summary

This section provides a summary of the MPF42791's real-world performance. Table 2Error! Reference source not found. shows a summary of the pack SOC performance metrics for a 10S1P battery.

**Table 2: MPF42791 SOC Root-Mean-Squared (and Maximum) Error**

| Test Case         | 0°C           | 25°C          | 40°C          |
|-------------------|---------------|---------------|---------------|
| CC/CV charge      | 0.68% (1.22%) | 0.61% (1.03%) | 0.40% (0.60%) |
| Dynamic discharge | 1.15% (2.97%) | 0.78% (1.94%) | 0.77% (1.89%) |

## OPERATION

The MPF42791 relies on a host microcontroller (MCU) to periodically update the fuel gauge's required inputs. This includes the cell voltages (via the VRDG\_CELLxx registers), current (via the IRDG\_CELLxx registers), and temperature (via the TRDG\_TSx registers).

The host MCU is responsible for synchronizing the input data to the fuel gauge's execution time (EXE\_TIME). The host MCU sends the EXE\_CMD command to trigger the fuel gauge execution and waits until the iteration is completed (FG\_EXE\_FLAG = 0). Then the host MCU can read back the fuel gauge's output registers, such as the pack state-of-charge (SOC). The interrupt request (IRQ) pin can be configured to notify several events, such as a completed iteration or other conditions (see the xx\_INTR\_EN registers starting on page 56 for details).

### Operating Modes

#### Active

In active mode, the fuel gauge is either updating the battery internal states or communicating via the I<sup>2</sup>C bus.

#### Standby

In standby mode, the fuel gauge is idle, which means that all triggered updates have been completed and the fuel gauge is waiting for activity on the SDA line to transition to active mode. See the I<sup>2</sup>C Communication Interface section on page 12 for more details.

#### Disabled

In disabled mode, the chip enable (CE) pin is low. I<sup>2</sup>C communication is not available, and the fuel gauge achieves minimal current consumption but still retains all internal state variables in its memory.

### Configuration and Data Exchange

#### Configuration Mode

In the configuration mode, the MPF42791 is set to receive configuration parameters. However, the device will stop operating. This mode is enabled by sending the CONFIG\_MODE\_CMD and can be confirmed by reading the CONFIG\_MODE\_FLAG register. After the fuel gauge configurations are successfully updated, the host system must send the

CONFIG\_EXIT\_CMD command to save the configuration into non-volatile memory (NVM). This ensures that the configuration remains after a hardware reset (cycling the device's power or cycling power on the nRST pin).

#### Editing Mode

As an alternative to the configuration mode, the edit mode allows for partial configuration changes. In this mode, the fuel gauge settings can be updated, but not changes to the fuel gauge cell model. Configuration mode is required to change the fuel gauge cell model.

In this mode, the fuel gauge operation does not stop, which allows for on-the-fly configurations. This mode is enabled by sending the EDIT\_CONFIG\_CMD command and can be confirmed by reading the EDIT\_SETTINGS\_FLAG. The host system can exit this mode by sending the END\_EDIT\_CONFIG\_CMD or CONFIG\_EXIT\_CMD command, which store the updated configuration in the MPF42791's NVM.

#### LED Control

The MPF42791 can drive five external LEDs that report the pack SOC. There are 2 methods for controlling the LEDs, direct control or manual control, which is configured using the LEDS\_ON\_MAN register.

Note that the LED settings can be written at any time during active or standby operating modes without having to enter configuration or edit modes.

#### Direct Control

With direct LED control, the fuel gauge directly controls the LEDs based on the pack SOC (see Table 1 on page 12). When the PB pin is pulled low (if the LEDS\_ON\_BTN register is enabled), or when the battery pack is charging (if LEDS\_ON\_CHG is enabled), the LEDs display pack SOC. The deglitch time between charge and discharge can be configured via the LED\_TRANS register. The LED turn-on time can be configured via the LEDS\_ON\_TIME register.

**Table 1: LED State-of-Charge Indicator Map**

| Pack SOC        | LED Status |     |     |     |     |
|-----------------|------------|-----|-----|-----|-----|
|                 | 1          | 2   | 4   | 4   | 5   |
| SOC > 90%       | On         | On  | On  | On  | On  |
| 90% ≥ SOC > 70% | On         | On  | On  | On  | Off |
| 70% ≥ SOC > 50% | On         | On  | On  | Off | Off |
| 50% ≥ SOC > 30% | On         | On  | Off | Off | Off |
| 30% ≥ SOC > 10% | On         | Off | Off | Off | Off |
| 10% ≥ SOC       | Off        | Off | Off | Off | Off |

### Manual LED Control

With manual LED control, the host manually controls each LED via the corresponding LEDx\_ON register.

### I<sup>2</sup>C COMMUNICATION INTERFACE

The MPF42791 has two I<sup>2</sup>C-compatible interfaces. The primary I<sup>2</sup>C channel communicates with the host MCU which extracts the data from the AFE. The secondary I<sup>2</sup>C channel is designed to monitor the fuel gauge status in real time and configure the fuel gauge using the MPF4279x graphic user interface (GUI). Note that write operations are only accepted from one channel at a time (the primary channel by default). To write to the fuel gauge using the secondary I<sup>2</sup>C channel, the CHSL pin must be pulled high; otherwise, write operations from this channel are ignored.

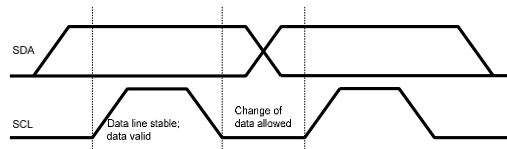
The I<sup>2</sup>C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). The device can be considered a master or a slave when performing data transfers. A device that initiates a data transfer on the bus and generates the clock signals to permit the transfer is considered a master. Any device that the master addresses is considered a slave.

Both MPF42791 I<sup>2</sup>C interfaces operate as slave devices with a configurable address (0x08 by default). They receive control inputs from the master device and ignore general call addresses.

The I<sup>2</sup>C interface supports both standard mode (up to 100kbps), and fast mode (up to 400kbps). The SDA and SCL lines are bidirectional with open drain outputs that should be connected to the positive supply voltage via a current source

or pull-up resistor. When the bus is free, both lines are high.

The data on the SDA line must be stable during the high period of the clock. the high or low state of the data line can only change when the clock signal on the SCL line is low. Note that a single clock pulse is generated for each data bit transferred (see Figure 7).


**Figure 7: Bit Transfer on the I<sup>2</sup>C Bus**

All transactions must begin with a start (S) command and can be terminated with a stop (P) command. Start and stop commands are always generated by the master. A start command is defined by a high-to-low transition on the SDA line while SCL is high (see Figure 8). A stop command is defined by a low-to-high transition on the SDA line while the SCL is high (see Figure 8). The bus is considered busy after a start command and free after a stop command.


**Figure 8: I<sup>2</sup>C Start (S) and Stop (P) Commands**

Every byte on the SDA line must be 8 bits long and must be followed by an acknowledge bit (ACK). Note that data is transferred with the most significant bit (MSB) first.

A slave cannot receive or transmit a complete byte of data while performing other tasks, but it can hold the SCL line low to force the master into a wait state (clock stretching). Then, when the slave is ready, data transfer continues, and the clock line (SCL) is released. Figure 9 shows a complete data transfer.

The acknowledgement takes place after every byte and allows the receiver to signal to the transmitter that the byte was successfully received. All clock pulses are generated by the master, including the 9th clock pulse (ACK).

The transmitter releases the SDA line during the ACK clock pulse so that the receiver pulls the

SDA line low. If the SDA line remains high during the acknowledge clock pulse, it is not acknowledged (NACK). Then the master can generate a stop command to abort the transfer, or it can generate a repeated start (Sr) command to start a new transfer.

After the start command, a 7-bit slave address is sent, followed by the read/write (R/W) bit. A 0 represents a write transmission (W), while a 1 indicates a read request (R). Figure 9 shows a complete data transfer.

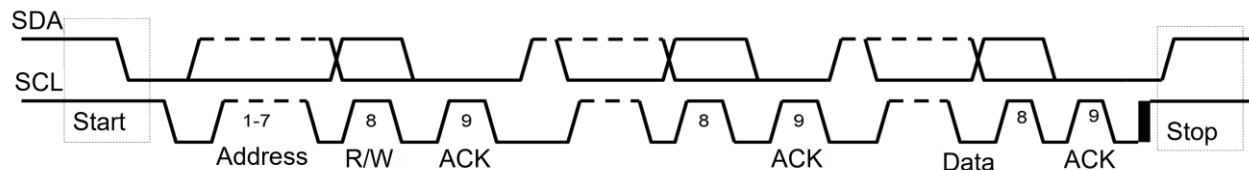


Figure 9: Complete Data Transfer

### Active Mode

The MPF42791 must be in active mode to communicate (see Operating Modes for additional detail). To transition to active mode, the SDA line must be pulled low. There is a 20ms timeout before starting operation, or the device transitions back to standby mode. After the operations are completed (e.g. I<sup>2</sup>C communication or fuel gauge updates) there is a 5ms timeout.

A low 5ms pulse on the SDA line is recommended to transition to active mode. Note that it may take a few additional milliseconds for the MPF42791 to reach active mode and for the I<sup>2</sup>C to be ready. To verify that the MPF42791 is ready for communication, an I<sup>2</sup>C header with the start command, the device address, and the R/W

bit can be sent. The device responds with an ACK signal if it is ready for communication.

### Protocol Layer

The MPF42791 uses a protocol where 2 bytes are used for the register and command addresses. A length field is also provided to declare the number of bytes in each read or write transaction. The maximum allowed transaction length is 82 bytes of data (not including the register address, length byte, or CRC bytes).

A Cyclic Redundancy Check (CRC) can be used to ensure the transaction's integrity. When enabled, the last 4 bytes of the transaction correspond to the CRC. Figure 10 and Figure 11 show an example of read and write transactions with CRC, respectively.

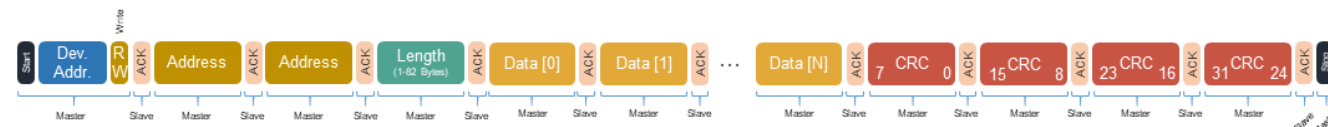


Figure 10: I<sup>2</sup>C Read Transaction with CRC

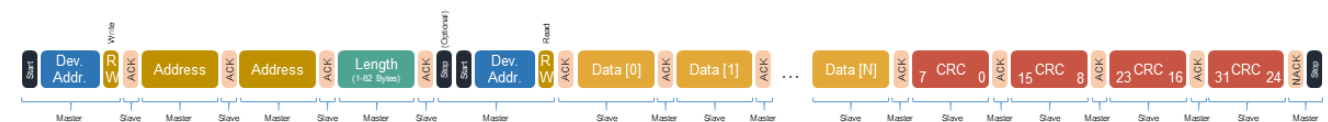


Figure 11: I<sup>2</sup>C Write Transaction with CRC

If CRC is disabled, a write transaction can optionally include the correct CRC bytes to be accepted. During a read, the MPF42791 does not include the CRC, so the NACK signal and stop command from the master come after DATA[x].

I<sup>2</sup>C operations using any address outside of the register map are invalid, even if they are partially

valid addresses. An invalid read operation returns a 0 as the data and correct CRC (if enabled), and an invalid write operation is ignored.

### Cyclic Redundancy Check (CRC)

The CRC spans the register address, length, and data payload. It is generated in blocks of 4 bytes. If the number of bytes is not a multiple of 4, the

block is padded with 0x00. The algorithm to generate the CRC is listed below.

```

unsigned long crc32 (unsigned short Reg_Address, unsigned
char len, unsigned char *data){
    short i;
    unsigned long crc = 0xffffffff;
    unsigned char dataTemp[4];

    for (i=-1; i<len; i++) {
        if(i==-1) {
            dataTemp[0]=len;
            dataTemp[1]=Reg_Address&0x00FF;
            dataTemp[2]=(Reg_Address&0xFF00)>>8;
            dataTemp[3]=0;
        }
        else dataTemp[i%4]=data[i];
        if((i%4)==3 || i == len-1 || i == -1) {
            for (char j=0; j<4; j++) {
                crc ^= dataTemp[3-j] << 24;
                for (char k = 0; k < 8; ++k) {
                    if ((crc & 0x80000000) != 0)
                        crc = (crc << 1) ^ 0x04C11DB7;
                    else
                        crc <<= 1;
                }
            }
            dataTemp[0]=0;
            dataTemp[1]=0;
            dataTemp[2]=0;
            dataTemp[3]=0;
        }
    }
    return crc;
}

```

To disable CRC and configure the slave address as 0x08, send the following message: {0x00, 0x41, 0x01, 0x08, 0x94, 0xA0, 0xDE, 0xDD} (Address = 0x4100, Length = 0x01, Data = 0x08, CRC = 0xDDDE A094).

## I<sup>2</sup>C REGISTER MAP

### Fuel Gauge Input

| Name, Address       | Description                                                   | Bit Length, Position | Type | Encoding                                   | Decoded Default Value | Range                  |
|---------------------|---------------------------------------------------------------|----------------------|------|--------------------------------------------|-----------------------|------------------------|
| VRDG_CELL1, 0x0000  | Inputs cell 1's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL2, 0x0002  | Inputs cell 2's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL3, 0x0004  | Inputs cell 3's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL4, 0x0006  | Inputs cell 4's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL5, 0x0008  | Inputs cell 5's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL6, 0x000A  | Inputs cell 6's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL7, 0x000C  | Inputs cell 7's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL8, 0x000E  | Inputs cell 8's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL9, 0x0010  | Inputs cell 9's voltage reading.                              | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL10, 0x0012 | Inputs cell 10's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL11, 0x0014 | Inputs cell 11's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL12, 0x0016 | Inputs cell 12's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL13, 0x0018 | Inputs cell 13's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL14, 0x001A | Inputs cell 14's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL15, 0x001C | Inputs cell 15's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_CELL16, 0x001E | Inputs cell 16's voltage reading.                             | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 0.1mV       | 0mV                   | 0mV to 6553.5mV        |
| VRDG_PACK, 0x0020   | Inputs the pack's voltage reading if VRDG_PACK_EN is enabled. | 16, [15:0]           | R/W  | 16-bit unsigned integer, LSB = 2mV         | 0mV                   | 0mV to 131070mV        |
| IRDG_CELL1, 0x0022  | Inputs cell 1's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0]           | R/W  | 32-bit signed, 2-comp integer<br>LSB = 1mA | 0mA                   | -524288mA to +524287mA |

|                        |                                                               |            |     |                                                 |     |                                     |
|------------------------|---------------------------------------------------------------|------------|-----|-------------------------------------------------|-----|-------------------------------------|
| IRDG_CELL2,<br>0x0026  | Inputs cell 2's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL3,<br>0x002A  | Inputs cell 3's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL4,<br>0x002E  | Inputs cell 4's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL5,<br>0x0032  | Inputs cell 5's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL6,<br>0x0036  | Inputs cell 6's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL7,<br>0x003A  | Inputs cell 7's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL8,<br>0x003E  | Inputs cell 8's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL9,<br>0x0042  | Inputs cell 9's current reading if IRDG_CELLS_EN is enabled.  | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL10,<br>0x0046 | Inputs cell 10's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL11,<br>0x004A | Inputs cell 11's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL12,<br>0x004E | Inputs cell 12's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL13,<br>0x0052 | Inputs cell 13's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL14,<br>0x0056 | Inputs cell 14's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL15,<br>0x005A | Inputs cell 15's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_CELL16,<br>0x005E | Inputs cell 16's current reading if IRDG_CELLS_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| IRDG_PACK,<br>0x0062   | Inputs the pack's current reading if IRDG_PACK_EN is enabled. | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 1mA      | 0mA | -524288mA to<br>+524287mA           |
| CCRDG,<br>0x0066       | Inputs the Coulomb count reading if CCRDG_EN is enabled.      | 32, [31:0] | R/W | 32-bit signed, 2-comp integer<br>LSB = 0.0005mA | 0mA | -1073741.832mA to<br>+1073741.832mA |
| TRDG_AMB,<br>0x006A    | Inputs the ambient temperature reading.                       | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C   | 0°C | -273.15°C to<br>+327.67°C           |
| TRDG_TS1,<br>0x006C    | Inputs temperature sensor 1's reading.                        | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C   | 0°C | -273.15°C to<br>+327.67°C           |
| TRDG_TS2,<br>0x006E    | Inputs temperature sensor 2's reading.                        | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C   | 0°C | -273.15°C to<br>+327.67°C           |

|                       |                                                                   |            |     |                                               |     |                           |
|-----------------------|-------------------------------------------------------------------|------------|-----|-----------------------------------------------|-----|---------------------------|
| TRDG_TS3,<br>0x0070   | Inputs temperature sensor 3's reading.                            | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C | 0°C | -273.15°C to<br>+327.67°C |
| TRDG_TS4,<br>0x0072   | Inputs temperature sensor 4's reading.                            | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C | 0°C | -273.15°C to<br>+327.67°C |
| TRDG_DIE,<br>0x0074   | Inputs the die temperature reading.                               | 16, [15:0] | R/W | 16-bit signed, 2-comp integer<br>LSB = 0.01°C | 0°C | -273.15°C to<br>+327.67°C |
| BAL_CELL1,<br>0x0076  | Indicates cell 1's balancing status.<br>1: Active<br>0: Inactive  | 1, [0]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL2,<br>0x0076  | Indicates cell 2's balancing status.<br>1: Active<br>0: Inactive  | 1, [1]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL3,<br>0x0076  | Indicates cell 3's balancing status.<br>1: Active<br>0: Inactive  | 1, [2]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL4,<br>0x0076  | Indicates cell 4's balancing status.<br>1: Active<br>0: Inactive  | 1, [3]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL5,<br>0x0076  | Indicates cell 5's balancing status.<br>1: Active<br>0: Inactive  | 1, [4]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL6,<br>0x0076  | Indicates cell 6's balancing status.<br>1: Active<br>0: Inactive  | 1, [5]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL7,<br>0x0076  | Indicates cell 7's balancing status.<br>1: Active<br>0: Inactive  | 1, [6]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL8,<br>0x0076  | Indicates cell 8's balancing status.<br>1: Active<br>0: Inactive  | 1, [7]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL9,<br>0x0077  | Indicates cell 9's balancing status.<br>1: Active<br>0: Inactive  | 1, [0]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL10,<br>0x0077 | Indicates cell 10's balancing status.<br>1: Active<br>0: Inactive | 1, [1]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL11,<br>0x0077 | Indicates cell 11's balancing status.<br>1: Active<br>0: Inactive | 1, [2]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL12,<br>0x0077 | Indicates cell 12's balancing status.<br>1: Active<br>0: Inactive | 1, [3]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL13,<br>0x0077 | Indicates cell 13's balancing status.<br>1: Active<br>0: Inactive | 1, [4]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |
| BAL_CELL14,<br>0x0077 | Indicates cell 14's balancing status.<br>1: Active<br>0: Inactive | 1, [5]     | R/W | Boolean true/false                            | 0   | 0 to 1                    |

|                         |                                                                                                                                                                                                                                                                   |        |     |                    |   |        |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--------------------|---|--------|
| BAL_CELL15,<br>0x0077   | Indicates cell 15's balancing status.<br>1: Active<br>0: Inactive                                                                                                                                                                                                 | 1, [6] | R/W | Boolean true/false | 0 | 0 to 1 |
| BAL_CELL16,<br>0x0077   | Indicates cell 16's balancing status.<br>1: Active<br>0: Inactive                                                                                                                                                                                                 | 1, [7] | R/W | Boolean true/false | 0 | 0 to 1 |
| HARD_RST,<br>0x0078     | Resets the fuel gauge and lifetime log if set to 1 (i.e. FG_RST = LOG_RST = 1). This is a self-clearing register that returns to 0 automatically.                                                                                                                 | 1, [0] | R/W | Boolean true/false | 0 | 0 to 1 |
| FG_RST,<br>0x0078       | Resets the fuel gauge if set to 1 (i.e. STATUS_RST = SOH_RST = SOC_RST = FULL_RST = EMTY_RST = IR_RST = ETAC_RST = IDIS_AVG_RST = IDIS_END_RST = ICHG_END_RST = ICHG_CC_RST = VCHG_CV_RST = 1). This is a self-clearing register that returns to 0 automatically. | 1, [1] | R/W | Boolean true/false | 0 | 0 to 1 |
| LOG_RST,<br>0x0078      | Resets the lifetime log.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                              | 1, [2] | R/W | Boolean true/false | 0 | 0 to 1 |
| WKUP,<br>0x0078         | Wakes up the fuel gauge.<br>1: Wake up (self-clearing)<br>0: No action                                                                                                                                                                                            | 1, [3] | R/W | Boolean true/false | 0 | 0 to 1 |
| STATUS_RST,<br>0x0078   | Resets the pack status.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                               | 1, [4] | R/W | Boolean true/false | 0 | 0 to 1 |
| SOH_RST,<br>0x0078      | Resets the SOH.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                                       | 1, [5] | R/W | Boolean true/false | 0 | 0 to 1 |
| SOC_RST,<br>0x0078      | Resets the SOC.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                                       | 1, [7] | R/W | Boolean true/false | 0 | 0 to 1 |
| FULL_RST,<br>0x0079     | Resets the pack full.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                                 | 1, [0] | R/W | Boolean true/false | 0 | 0 to 1 |
| EMTY_RST,<br>0x0079     | Resets the pack empty.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                                | 1, [1] | R/W | Boolean true/false | 0 | 0 to 1 |
| IDIS_AVG_RST,<br>0x0079 | Resets the average discharge current.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                 | 1, [2] | R/W | Boolean true/false | 0 | 0 to 1 |
| IDIS_END_RST,<br>0x0079 | Resets the discharge termination current.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                             | 1, [3] | R/W | Boolean true/false | 0 | 0 to 1 |
| ICHG_END_RST,<br>0x0079 | Resets the charge termination current.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                | 1, [4] | R/W | Boolean true/false | 0 | 0 to 1 |
| ICHG_CC_RST,<br>0x0079  | Resets the charge CC.<br>1: Reset (self-clearing)<br>0: No action                                                                                                                                                                                                 | 1, [5] | R/W | Boolean true/false | 0 | 0 to 1 |

|                        |                                                                                                                                                                     |        |     |                                      |             |        |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----|--------------------------------------|-------------|--------|
| VCHG_CV_RST,<br>0x0079 | Resets the charge CV.<br>1: Reset (self-clearing)<br>0: No action                                                                                                   | 1, [6] | R/W | Boolean true/false                   | 0           | 0 to 1 |
| RESR_RST,<br>0x0079    | Resets the ESR.<br>1: Reset (self-clearing)<br>0: No action                                                                                                         | 1, [7] | R/W | Boolean true/false                   | 0           | 0 to 1 |
| HCONV_RST,<br>0x007A   | Resets the heat transfer coefficient.<br>1: Reset (self-clearing)<br>0: No action                                                                                   | 1, [0] | R/W | Boolean true/false                   | 0           | 0 to 1 |
| PCHG_SHW,<br>0x007B    | Shows the maximum charge power in PCHG, the limiting cell ID in PCHG_ID, and the limiting factor in PCHG_LIM (PCHG_SHW_EN by default).<br>1: Show<br>0: Do not show | 1, [0] | R/W | Control<br>Enable = 1<br>Disable = 0 | PCHG_SHW_EN | 0 to 1 |
| PDIS_SHW,<br>0x007B    | Shows the maximum discharge power (PDIS_SHW_EN by default).<br>1: Show<br>0: Do not show                                                                            | 1, [1] | R/W | Control<br>Enable = 1<br>Disable = 0 | PDIS_SHW_EN | 0 to 1 |

### Fuel Gauge Backup

| Name, Address                   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Bit Length, Position | Type | Encoding                       | Decoded Default Value | Range |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|--------------------------------|-----------------------|-------|
| RESR_CELL_DIS_1_BKUP,<br>0x0200 | These bits are the backup register for cell 1's discharge ESR (RESR) state. This address is a R/W alias for the RESR_CELL_DIS_1 register.<br><br>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.<br><br>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning. | 32, [31:0]           | R/W  | 32-bit floating point (single) | 0%                    | -     |
| RESR_CELL_DIS_2_BKUP,<br>0x0204 | These bits are the backup register for cell 2's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_2 register.<br><br>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.<br><br>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.       | 32, [31:0]           | R/W  | 32-bit floating point (single) | 0%                    | -     |
| RESR_CELL_DIS_3_BKUP,<br>0x0208 | These bits are the backup register for cell 3's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_3 register.<br><br>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.<br><br>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.       | 32, [31:0]           | R/W  | 32-bit floating point (single) | 0%                    | -     |

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |     |                                |    |   |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|--------------------------------|----|---|
| RESR_CELL_DIS_4_BKUP,<br>0x020C | <p>These bits are the backup register for cell 4's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_4 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_5_BKUP,<br>0x0210 | <p>These bits are the backup register for cell 5's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_5 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_6_BKUP,<br>0x0214 | <p>These bits are the backup register for cell 6's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_6 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_7_BKUP,<br>0x0218 | <p>These bits are the backup register for cell 7's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_7 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_8_BKUP,<br>0x021C | <p>These bits are the backup register for cell 8's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_8 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |

|                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |     |                                |    |   |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|--------------------------------|----|---|
| RESR_CELL_DIS_9_BKUP,<br>0x0220  | <p>These bits are the backup register for cell 9's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_9 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p>   | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_10_BKUP,<br>0x0224 | <p>These bits are the backup register for cell 10's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_10 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_11_BKUP,<br>0x0228 | <p>These bits are the backup register for cell 11's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_11 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_12_BKUP,<br>0x022C | <p>These bits are the backup register for cell 12's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_12 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_13_BKUP,<br>0x0230 | <p>These bits are the backup register for cell 13's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_13 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |

|                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |     |                                |    |   |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|--------------------------------|----|---|
| RESR_CELL_DIS_14_BKUP,<br>0x0234 | <p>These bits are the backup register for cell 14's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_14 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_15_BKUP,<br>0x0238 | <p>These bits are the backup register for cell 15's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_15 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_DIS_16_BKUP,<br>0x023C | <p>These bits are the backup register for cell 16's discharge RESR state. This address is a R/W alias for the RESR_CELL_DIS_16 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_1_BKUP,<br>0x0240  | <p>These bits are the backup register for cell 1's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_1 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p>      | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_2_BKUP,<br>0x0244  | <p>These bits are the backup register for cell 2's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_2 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p>      | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |            |     |                                |    |   |
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| RESR_CELL_CHG_3_BKUP,<br>0x0248 | <p>These bits are the backup register for cell 3's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_3 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_4_BKUP,<br>0x024C | <p>These bits are the backup register for cell 4's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_4 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_5_BKUP,<br>0x0250 | <p>These bits are the backup register for cell 5's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_5 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_6_BKUP,<br>0x0254 | <p>These bits are the backup register for cell 6's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_6 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_7_BKUP,<br>0x0258 | <p>These bits are the backup register for cell 7's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_7 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |

|                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |     |                                |    |   |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|--------------------------------|----|---|
| RESR_CELL_CHG_8_BKUP,<br>0x025C  | <p>These bits are the backup register for cell 8's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_8 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p>   | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_9_BKUP,<br>0x0260  | <p>These bits are the backup register for cell 9's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_9 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p>   | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_10_BKUP,<br>0x0264 | <p>These bits are the backup register for cell 10's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_10 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_11_BKUP,<br>0x0268 | <p>These bits are the backup register for cell 11's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_11 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |
| RESR_CELL_CHG_12_BKUP,<br>0x026C | <p>These bits are the backup register for cell 12's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_12 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single) | 0% | - |

|                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |     |                                             |    |            |
|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|---------------------------------------------|----|------------|
| RESR_CELL_CHG_13_BKUP,<br>0x0270 | <p>These bits are the backup register for cell 13's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_13 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single)              | 0% | -          |
| RESR_CELL_CHG_14_BKUP,<br>0x0274 | <p>These bits are the backup register for cell 14's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_14 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single)              | 0% | -          |
| RESR_CELL_CHG_15_BKUP,<br>0x0278 | <p>These bits are the backup register for cell 15's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_15 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single)              | 0% | -          |
| RESR_CELL_CHG_16_BKUP,<br>0x027C | <p>These bits are the backup register for cell 16's charge RESR state. This address is a R/W alias for the RESR_CELL_CHG_16 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any of the other cell RESR backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the RESR learning.</p> | 32, [31:0] | R/W | 32-bit floating point (single)              | 0% | -          |
| SOH_CELL1_BKUP,<br>0x02A0        | <p>These bits are the backup register for cell 1's SOH. This address is a R/W alias for the SOH_CELL1 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p>                         | 32, [31:0] | R/W | 32-bit unsigned integer<br>LSB = 0.0000001% | 0% | 0% to 255% |

|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |            |     |                                                        |    |            |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|--------------------------------------------------------|----|------------|
| SOH_CELL2_<br>BKUP,<br>0x02A4 | <p>These bits are the backup register for cell 2's SOH. This address is a R/W alias for the SOH_CELL2 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL3_<br>BKUP,<br>0x02A8 | <p>These bits are the backup register for cell 3's SOH. This address is a R/W alias for the SOH_CELL3 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL4_<br>BKUP,<br>0x02AC | <p>These bits are the backup register for cell 4's SOH. This address is a R/W alias for the SOH_CELL4 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL5_<br>BKUP,<br>0x02B0 | <p>These bits are the backup register for cell 5's SOH. This address is a R/W alias for the SOH_CELL5 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL6_<br>BKUP,<br>0x02B4 | <p>These bits are the backup register for cell 6's SOH. This address is a R/W alias for the SOH_CELL6 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |

|                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |     |                                                        |    |            |
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| SOH_CELL7_<br>BKUP,<br>0x02B8  | <p>These bits are the backup register for cell 7's SOH. This address is a R/W alias for the SOH_CELL7 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p>   | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL8_<br>BKUP,<br>0x02BC  | <p>These bits are the backup register for cell 8's SOH. This address is a R/W alias for the SOH_CELL8 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p>   | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL9_<br>BKUP,<br>0x02C0  | <p>These bits are the backup register for cell 9's SOH. This address is a R/W alias for the SOH_CELL9 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p>   | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL10_<br>BKUP,<br>0x02C4 | <p>These bits are the backup register for cell 10's SOH. This address is a R/W alias for the SOH_CELL10 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL11_<br>BKUP,<br>0x02C8 | <p>These bits are the backup register for cell 11's SOH. This address is a R/W alias for the SOH_CELL11 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |

|                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |            |     |                                                        |    |            |
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| SOH_CELL12_<br>BKUP,<br>0x02CC | <p>These bits are the backup register for cell 12's SOH. This address is a R/W alias for the SOH_CELL12 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL13_<br>BKUP,<br>0x02D0 | <p>These bits are the backup register for cell 13's SOH. This address is a R/W alias for the SOH_CELL13 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL14_<br>BKUP,<br>0x02D4 | <p>These bits are the backup register for cell 14's SOH. This address is a R/W alias for the SOH_CELL14 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL15_<br>BKUP,<br>0x02D8 | <p>These bits are the backup register for cell 15's SOH. This address is a R/W alias for the SOH_CELL15 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |
| SOH_CELL16_<br>BKUP,<br>0x02DC | <p>These bits are the backup register for cell 16's SOH. This address is a R/W alias for the SOH_CELL16 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this or any other of the cell SOH backup registers prepares the fuel gauge to use the values written in these registers as a starting point for the SOH learning.</p> | 32, [31:0] | R/W | <p>32-bit unsigned integer</p> <p>LSB = 0.0000001%</p> | 0% | 0% to 255% |

|                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |     |                                                                     |                        |                                                       |
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| <p>IDIS_AVG_BKUP, 0x0360</p> | <p>These bits are the backup register for the average discharge current. This address is a R/W alias for the IDIS_AVG register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p>  | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.001 C-rate</p>            | 0 C-rate               | 0 C-rate to 65.535 C-rate                             |
| <p>IDIS_END_BKUP, 0x0370</p> | <p>These bits are the backup register for the discharge end current. This address is a R/W alias for the IDIS_END register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p>      | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.001 C-rate</p>            | 0 C-rate               | 0 C-rate to 65.535 C-rate                             |
| <p>ICHG_CC_BKUP, 0x0380</p>  | <p>These bits are the backup register for the charge CC current. This address is a R/W alias for the ICHG_CC register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p>           | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.001 C-rate</p>            | 0 C-rate               | 0 C-rate to 65.535 C-rate                             |
| <p>ICHG_END_BKUP, 0x0390</p> | <p>These bits are the backup register for the charge termination current. This address is a R/W alias for the ICHG_END register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.001 C-rate</p>            | 0 C-rate               | 0 C-rate to 65.535 C-rate                             |
| <p>VCHG_CV_BKUP, 0x03A0</p>  | <p>These bits are the backup register for the charge CV voltage. This address is a R/W alias for the VCHG_CV register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p>           | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 2mV</p>                     | 0mV                    | 0mV to 131070mV                                       |
| <p>HCONV_BKUP, 0x03B0</p>    | <p>These bits are the backup register for the heat transfer coefficient. This address is a R/W alias for the HCONV register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register prepares the fuel gauge to use the values written in this register as a starting point for this learning.</p>     | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.01W/(m<sup>2</sup>×K)</p> | 0W/(m <sup>2</sup> ×K) | 0W/(m <sup>2</sup> ×K) to 655.35W/(m <sup>2</sup> ×K) |

|                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |     |                                        |     |                 |
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| RCXN_CELL1_BKUP,<br>0x03C0 | <p>These bits are the backup register for cell 1's connection resistance state. This address is a R/W alias for the RCXN_CELL1 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL2_BKUP,<br>0x03C2 | <p>These bits are the backup register for cell 2's connection resistance state. This address is a R/W alias for the RCXN_CELL2 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL3_BKUP,<br>0x03C4 | <p>These bits are the backup register for cell 3's connection resistance state. This address is a R/W alias for the RCXN_CELL3 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL4_BKUP,<br>0x03C6 | <p>These bits are the backup register for cell 4's connection resistance state. This address is a R/W alias for the RCXN_CELL4 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL5_BKUP,<br>0x03C8 | <p>These bits are the backup register for cell 5's connection resistance state. This address is a R/W alias for the RCXN_CELL5 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |            |     |                                        |     |                 |
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| RCXN_CELL6_<br>BKUP,<br>0x03CA  | <p>These bits are the backup register for cell 6's connection resistance state. This address is a R/W alias for the RCXN_CELL6 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p>   | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL7_<br>BKUP,<br>0x03CC  | <p>These bits are the backup register for cell 7's connection resistance state. This address is a R/W alias for the RCXN_CELL7 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p>   | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL8_<br>BKUP,<br>0x03CE  | <p>These bits are the backup register for cell 8's connection resistance state. This address is a R/W alias for the RCXN_CELL8 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p>   | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL9_<br>BKUP,<br>0x03D0  | <p>These bits are the backup register for cell 9's connection resistance state. This address is a R/W alias for the RCXN_CELL9 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p>   | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL10_<br>BKUP,<br>0x03D2 | <p>These bits are the backup register for cell 10's connection resistance state. This address is a R/W alias for the RCXN_CELL10 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |

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| <p>RCXN_CELL11_BKUP, 0x03D4</p> | <p>These bits are the backup register for cell 11's connection resistance state. This address is a R/W alias for the RCXN_CELL11 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.1mΩ</p> | 0mΩ | 0mΩ to 6553.5mΩ |
| <p>RCXN_CELL12_BKUP, 0x03D6</p> | <p>These bits are the backup register for cell 12's connection resistance state. This address is a R/W alias for the RCXN_CELL12 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.1mΩ</p> | 0mΩ | 0mΩ to 6553.5mΩ |
| <p>RCXN_CELL13_BKUP, 0x03D8</p> | <p>These bits are the backup register for cell 13's connection resistance state. This address is a R/W alias for the RCXN_CELL13 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.1mΩ</p> | 0mΩ | 0mΩ to 6553.5mΩ |
| <p>RCXN_CELL14_BKUP, 0x03DA</p> | <p>These bits are the backup register for cell 14's connection resistance state. This address is a R/W alias for the RCXN_CELL14 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.1mΩ</p> | 0mΩ | 0mΩ to 6553.5mΩ |
| <p>RCXN_CELL15_BKUP, 0x03DC</p> | <p>These bits are the backup register for cell 15's connection resistance state. This address is a R/W alias for the RCXN_CELL15 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W | <p>16-bit unsigned integer</p> <p>LSB = 0.1mΩ</p> | 0mΩ | 0mΩ to 6553.5mΩ |

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| RCXN_CELL16_BKUP, 0x03DE | <p>These bits are the backup register for cell 16's connection resistance state. This address is a R/W alias for the RCXN_CELL16 register.</p> <p>The fuel gauge must be in learning backup mode for this register to be written. For more details, see the FG_BKUP_ENABLE register on page 33 and the FG_BKUP_FLAG register on page 54.</p> <p>Writing to this backup register or any other cell RCXN register prepares the fuel gauge to use the values written in this register as a starting point for the RCXN learning.</p> | 16, [15:0] | R/W        | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| FG_BKUP_ENABLE, 0x03F0   | Enables learning backup mode. See the FG_BKUP_FLAG register on page 54 for more details.                                                                                                                                                                                                                                                                                                                                                                                                                                          | 1, [0]     | Write-only | Control<br>Enable = 1<br>Disable = 0   | 0   | 0 to 1          |

### Fuel Gauge Output

| Name, Address              | Description                                                                                                                                                                                                   | Bit Length, Position | Type   | Encoding           | Decoded Default Value | Range  |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|--------|--------------------|-----------------------|--------|
| IT_DONE_INTR, 0x0400       | Signals an interrupt when an iteration has been completed. Setting this bit to 1 clears the interrupt. This interrupt bit is automatically cleared when a new iteration is requested.                         | 1, [0]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| STATUS_INTR, 0x0400        | Signals an interrupt when there is a change in the STATUS register. Setting this bit to 1 clears the interrupt.                                                                                               | 1, [1]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| EMPTY_LIM_INTR, 0x0400     | Signals an interrupt when there is a change in the EMPTY_LIM register, which indicates that the empty limiting factor has changed. Setting this bit to 1 clears the interrupt.                                | 1, [2]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| FULL_LIM_INTR, 0x0400      | Signals an interrupt when there is a change in the FULL_LIM register, which indicates that the full limiting factor has changed. Setting this bit to 1 clears the interrupt.                                  | 1, [3]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| SOC_PACK_RSLT_INTR, 0x0400 | Signals an interrupt when there is a change in the SOC_PACK_RSLT register, which indicates that the pack SOC result has changed. Setting this bit to 1 clears the interrupt.                                  | 1, [4]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| OT_WARN_INTR, 0x0400       | Signals an interrupt when an over-temperature (OT) condition occurs; check the statuses of OT_ID, WARN_OTDIS, WARN_OTCHG_CC, and WARN_OTCHG_END for more details. Setting this bit to 1 clears the interrupt. | 1, [5]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| IDIS_AVG_INTR, 0x0400      | Signals an interrupt when there is a change in the IDIS_AVG_LRN or IDIS_AVG_RSLT registers, which indicates a change for the average discharge current learning. Setting this bit to 1 clears the interrupt.  | 1, [6]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |
| IDIS_END_INTR, 0x0400      | Signals an interrupt when there is a change in the IDIS_END_LRN or IDIS_END_RSLT registers, which indicates a change for the discharge end current learning. Setting this bit to 1 clears the interrupt.      | 1, [7]               | W1C/RO | Boolean true/false | 0                     | 0 to 1 |

|                             |                                                                                                                                                                                                                     |          |           |                                      |    |            |
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| ICHG_CC_INTR,<br>0x0400     | Signals an interrupt when there is a change in the ICHG_CC_LRN or ICHG_CC_RSLT registers, which indicates a change for the charge CC learning. Setting this bit to 1 clears the interrupt.                          | 1, [8]   | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| ICHG_END_INTR,<br>0x0400    | Signals an interrupt when there is a change in the ICHG_END_LRN or ICHG_END_RSLT registers, which indicates a change for the charge end current learning. Setting this bit to 1 clears the interrupt.               | 1, [9]   | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| VCHG_CV_INTR,<br>0x0400     | Signals an interrupt when there is a change in the VCHG_CV_LRN or VCHG_CV_RSLT registers, which indicates a change for the charge CV learning. Setting this bit to 1 clears the interrupt.                          | 1, [10]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| SORES_CELL_INTR,<br>0x0400  | Signals an interrupt when there is a change in the RESR_LRN_CELLx or RESR_RSLT_CELLx registers, which indicates a change for ESR learning. Setting this bit to 1 clears the interrupt.                              | 1, [11]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| RCXN_CELL_S_INTR,<br>0x0400 | Signals an interrupt when there is a change in the RCXN_LRN_CELLx or RCXN_RSLT_CELLx registers, which indicates a change for the cells' connection resistance learning. Setting this bit to 1 clears the interrupt. | 1, [12]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| HCONV_INTR,<br>0x0400       | Signals an interrupt when there is a change in the HCONV_LRN or HCONV_RSLT registers, which indicates a change for the heat transfer coefficient learning. Setting this bit to 1 clears the interrupt.              | 1, [13]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| SOH_CELL_INTR,<br>0x0400    | Signals an interrupt when there is a change in the SOH_LRN_CELLx or SOH_RSLT_CELLx registers, which indicates a change for the cell's SOH learning. Setting this bit to 1 clears the interrupt.                     | 1, [14]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| PDIS_LIM_INTR,<br>0x0400    | Signals an interrupt when there is a change in the PDIS_LIM register, which indicates a change for the discharge power limiting factor. Setting this bit to 1 clears the interrupt.                                 | 1, [16]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| PCHG_LIM_INTR,<br>0x0400    | Signals an interrupt when there is a change in the PCHG_LIM register, which indicates a change for the charge power limiting factor. Setting this bit to 1 clears the interrupt.                                    | 1, [17]  | W1C/RO    | Boolean true/false                   | 0  | 0 to 1     |
| STATUS,<br>0x0403           | Indicates the pack's current status.<br>0: Charge<br>1: Discharge<br>2: Rest                                                                                                                                        | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1    | 0  | 0 to 2     |
| SOC_ABS_CELL1,<br>0x0524    | Returns cell 1's absolute SOC. Shows as reserved.                                                                                                                                                                   | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL2,<br>0x0525    | Returns cell 2's absolute SOC. Shows as reserved.                                                                                                                                                                   | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL3,<br>0x0526    | Returns cell 3's absolute SOC. Shows as reserved.                                                                                                                                                                   | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL4,<br>0x0527    | Returns cell 4's absolute SOC. Shows as reserved.                                                                                                                                                                   | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |

|                         |                                                    |          |           |                                      |    |            |
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| SOC_ABS_CELL5, 0x0528   | Returns cell 5's absolute SOC. Shows as reserved.  | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL6, 0x0529   | Returns cell 6's absolute SOC. Shows as reserved.  | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL7, 0x052A   | Returns cell 7's absolute SOC. Shows as reserved.  | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL8, 0x052B   | Returns cell 8's absolute SOC. Shows as reserved.  | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL9, 0x052C   | Returns cell 9's absolute SOC. Shows as reserved.  | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL10, 0x052D  | Returns cell 10's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL11, 0x052E  | Returns cell 11's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL12, 0x052F  | Returns cell 12's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL13, 0x0530  | Returns cell 13's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL14, 0x0531  | Returns cell 14's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL15, 0x0532  | Returns cell 15's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| SOC_ABS_CELL16, 0x0533  | Returns cell 16's absolute SOC. Shows as reserved. | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL1, 0x0578 | Returns cell 1's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL2, 0x0579 | Returns cell 2's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL3, 0x057A | Returns cell 3's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL4, 0x057B | Returns cell 4's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL5, 0x057C | Returns cell 5's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL6, 0x057D | Returns cell 6's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL7, 0x057E | Returns cell 7's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |
| EMPTY_SOC_CELL8, 0x057F | Returns cell 8's empty SOC.                        | 8, [7:0] | Read-only | 8-bit unsigned integer<br>LSB = 0.4% | 0% | 0% to 100% |

|                          |                                                                                                                                                                                                             |            |           |                                             |             |                    |
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| EMPTY_SOC_CELL9, 0x0580  | Returns cell 9's empty SOC.                                                                                                                                                                                 | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL10, 0x0581 | Returns cell 10's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL11, 0x0582 | Returns cell 11's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL12, 0x0583 | Returns cell 12's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL13, 0x0584 | Returns cell 13's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL14, 0x0585 | Returns cell 14's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL15, 0x0586 | Returns cell 15's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_SOC_CELL16, 0x0587 | Returns cell 16's empty SOC.                                                                                                                                                                                | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 0%          | 0% to 100%         |
| EMPTY_ID, 0x0588         | Returns the cell ID for the cell that is empty limiting the pack.                                                                                                                                           | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 (cell ID) | 0 (cell ID) | 1 to 16 (cell ID)  |
| EMPTY_RUNTIME, 0x0589    | Returns the remaining time for the pack to become empty. Smoother changes for the remaining time estimate can be achieved by increasing EMPTY_RUNTIME_FILTER with the tradeoff of an increased phase delay. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1s         | 0s          | 0s to 65535s       |
| EMPTY_DTEMP, 0x058B      | Returns the predicted temperature to reach an empty pack.                                                                                                                                                   | 16, [15:0] | Read-only | 16-bit signed, 2-comp integer<br>LSB = 0.01 | 0           | -327.68 to +327.67 |
| EMPTY_LIM, 0x058D        | Outputs the pack's empty limiting factor.<br>0: Cell<br>1: Pack                                                                                                                                             | 8, [7:0]   | Read-only | Non-standard<br>LSB = 1                     | 0           | 0 to 1             |
| FULL_SOC_CELL1, 0x0592   | Returns cell's 1 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL2, 0x0593   | Returns cell's 2 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL3, 0x0594   | Returns cell's 3 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL4, 0x0595   | Returns cell's 4 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL5, 0x0596   | Returns cell's 5 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL6, 0x0597   | Returns cell's 6 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL7, 0x0598   | Returns cell's 7 full SOC.                                                                                                                                                                                  | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |

|                         |                                                                                                                                                                    |            |           |                                             |             |                    |
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| FULL_SOC_CELL8, 0x0599  | Returns cell's 8 full SOC.                                                                                                                                         | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4 %       | 100%        | 0% to 100%         |
| FULL_SOC_CELL9, 0x059A  | Returns cell's 9 full SOC.                                                                                                                                         | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL10, 0x059B | Returns cell's 10 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL11, 0x059C | Returns cell's 11 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL12, 0x059D | Returns cell's 12 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL13, 0x059E | Returns cell's 13 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL14, 0x059F | Returns cell's 14 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL15, 0x05A0 | Returns cell's 15 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_SOC_CELL16, 0x05A1 | Returns cell's 16 full SOC.                                                                                                                                        | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.4%        | 100%        | 0% to 100%         |
| FULL_ID, 0x05A2         | Returns the cell ID for the cell that is full limiting the pack.                                                                                                   | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 (cell ID) | 0 (cell ID) | 1 to 16 (cell ID)  |
| FULL_RUNTIME, 0x05A3    | Returns the remaining time to reach a full pack.                                                                                                                   | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1s         | 0s          | 0s to 65535s       |
| FULL_RUNTIME_CC, 0x05A5 | Returns the remaining time to reach the end of the charge CC region.                                                                                               | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1          | 0           | 0 to 65535         |
| FULL_DTEMP, 0x05A7      | Returns the predicted temperature to reach a full pack.                                                                                                            | 16, [15:0] | Read-only | 16-bit signed 2-comp integer<br>LSB = 0.01  | 0           | -327.28 to +327.27 |
| FULL_DTEMP_CC, 0x05A9   | Returns the predicted temperature increase at the end of the charge CC region.                                                                                     | 16, [15:0] | Read-only | 16-bit signed 2-comp integer<br>LSB = 0.01  | 0           | -327.28 to +327.27 |
| FULL_LIM, 0x05AB        | Returns the pack's full limiting factor.<br>0: Cell<br>1: Pack<br>2: Charger<br>3: Smart charger cell<br>4: Smart charger pack                                     | 3, [2:0]   | Read-only | Non-standard<br>LSB = 1                     | 0           | 0 to 4             |
| SOC_PACK, 0x05AC        | Returns the pack's SOC.                                                                                                                                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.002 %    | 0%          | 0% to 100%         |
| SOC_PACK_UNAVBL, 0x05AF | Indicates whether the pack has an unavailable SOC due to empty or full conditions, or a mismatch between cells. Reflects the quantity of pack's unusable capacity. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.002 %    | 0%          | 0% to 100%         |

|                          |                                                                                                                                               |            |           |                                               |          |                           |
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| IDIS_AVG,<br>0x05B1      | Returns the learned value for the typical load current, which is drained from the battery during its use (the average discharge current).     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0 C-rate | 0 C-rate to 65.535 C-rate |
| IDIS_AVG_LRN,<br>0x05B3  | Returns the state of the discharge average current learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing                                        | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 2                    |
| IDIS_AVG_RSLT,<br>0x05B4 | Returns the result of the detected discharge average current.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min           | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 3                    |
| IDIS_END,<br>0x05B5      | Returns the learned value for the typical discharge termination current.                                                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0 C-rate | 0 C-rate to 65.535 C-rate |
| IDIS_END_LRN,<br>0x05B7  | Returns the state of the discharge termination current learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing                                    | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 3                    |
| IDIS_END_RSLT,<br>0x05B8 | Returns the result of the detected discharge termination current value.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 2                    |
| ICHG_CC,<br>0x05B9       | Returns the learned charge current of the charger in the CC region, as performed by the algorithm.                                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0 C-rate | 0 C-rate to 65.535 C-rate |
| ICHG_CC_LRN,<br>0x05BB   | Returns the state of the charge CC learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing                                                        | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 3                    |
| ICHG_CC_RSLT,<br>0x05BC  | Returns the result of the detected charge CC value.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min                     | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 2                    |
| ICHG_END,<br>0x05BD      | Returns the learned value for the typical end of the discharge current                                                                        | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0 C-rate | 0 C-rate to 131070 C-rate |
| ICHG_END_LRN,<br>0x05CF  | Returns the state of the charge termination current learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing                                       | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1             | 0        | 0 to 3                    |

|                             |                                                                                                                                                |            |           |                                      |      |                 |
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| ICHG_END_RSLT,<br>0x05C0    | Returns the result of the detected charge termination current value.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1    | 0    | 0 to 2          |
| VCHG_CV,<br>0x05C1          | Returns the learned value for the typical charge CV voltage.                                                                                   | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 2mV | 0mV  | 0mV to 131070mV |
| VCHG_CV_LRN,<br>0x05C3      | Returns the state of the charge CV learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing                                                     | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1    | 0    | 0 to 3          |
| VCHG_CV_RSLT,<br>0x05C4     | Returns the state of the detected charge CV result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min                  | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1    | 0    | 0 to 3          |
| RESR_CELL_DIS_1,<br>0x05C5  | Returns cell 1's discharge ESR (RESR) state, which is compared to BOL for discharging.                                                         | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_2,<br>0x05C9  | Returns cell 2's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_3,<br>0x05CD  | Returns cell 3's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_4,<br>0x05D1  | Returns cell 4's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_5,<br>0x05D5  | Returns cell 5's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_6,<br>0x05D9  | Returns cell 6's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_7,<br>0x05DD  | Returns cell 7's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_8,<br>0x05E1  | Returns cell 8's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_9,<br>0x05E5  | Returns cell 9's discharge RESR state, which is compared to BOL for discharging.                                                               | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_10,<br>0x05E9 | Returns cell 10's discharge RESR state, which is compared to BOL for discharging.                                                              | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_11,<br>0x05ED | Returns cell 11's discharge RESR state, which is compared to BOL for discharging.                                                              | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_12,<br>0x05F1 | Returns cell 12's discharge RESR state, which is compared to BOL for discharging.                                                              | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_13,<br>0x05F5 | Returns cell 13's discharge RESR state, which is compared to BOL for discharging.                                                              | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |
| RESR_CELL_DIS_14,<br>0x05F9 | Returns cell 14's discharge RESR state, which is compared to BOL for discharging.                                                              | 32, [31:0] | Read-only | 32-bit floating point (single)       | 100% | -               |

|                                 |                                                                                        |            |           |                                   |      |        |
|---------------------------------|----------------------------------------------------------------------------------------|------------|-----------|-----------------------------------|------|--------|
| RESR_CELL_<br>DIS_15,<br>0x05FD | Returns cell 15's discharge RESR state, which is compared to BOL for discharging.      | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>DIS_16,<br>0x0601 | Returns cell 16's discharge RESR state, which is compared to BOL for discharging.      | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_1,<br>0x0605  | Returns cell 1's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_2,<br>0x0609  | Returns cell 2's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_3,<br>0x060D  | Returns cell 3's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_4,<br>0x0611  | Returns cell 4's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_5,<br>0x0615  | Returns cell 5's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_6,<br>0x0619  | Returns cell 6's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_7,<br>0x061D  | Returns cell 7's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_8,<br>0x0621  | Returns cell 8's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_9,<br>0x0625  | Returns cell 9's charge RESR state, which is compared to BOL for charging.             | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_10,<br>0x0629 | Returns cell 10's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_11,<br>0x062D | Returns cell 11's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_12,<br>0x0631 | Returns cell 12's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_13,<br>0x0635 | Returns cell 13's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_14,<br>0x0639 | Returns cell 14's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_15,<br>0x063D | Returns cell 15's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_CELL_<br>CHG_16,<br>0x0641 | Returns cell 16's charge RESR state, which is compared to BOL for charging.            | 32, [31:0] | Read-only | 32-bit floating point (single)    | 100% | -      |
| RESR_LRN_<br>CELL1,<br>0x0645   | Returns the state of cell 1's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0    | 0 to 2 |
| RESR_LRN_<br>CELL2,<br>0x0646   | Returns the state of cell 2's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0    | 0 to 2 |

|                                |                                                                                         |          |           |                                      |   |        |
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| RESR_LRN_<br>CELL3,<br>0x0647  | Returns the state of cell 3's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL4,<br>0x0648  | Returns the state of cell 4's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL5,<br>0x0649  | Returns the state of cell 5's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL6,<br>0x064A  | Returns the state of cell 6's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL7,<br>0x064B  | Returns the state of cell 7's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL8,<br>0x064C  | Returns the state of cell 8's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL9,<br>0x064D  | Returns the state of cell 9's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL10,<br>0x064E | Returns the state of cell 10's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL11,<br>0x064F | Returns the state of cell 11's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL12,<br>0x0650 | Returns the state of cell 12's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL13,<br>0x0651 | Returns the state of cell 13's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL14,<br>0x0652 | Returns the state of cell 14's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_LRN_<br>CELL15,<br>0x0653 | Returns the state of cell 15's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |

|                                 |                                                                                                                  |          |           |                                      |   |        |
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| RESR_LRN_<br>CELL16,<br>0x0654  | Returns the state of cell 16's RESR learning.<br>0: Disabled<br>1: Paused<br>2: Ongoing                          | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 2 |
| RESR_RSLT_<br>CELL1,<br>0x0655  | Returns the state of cell 1's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL2,<br>0x0656  | Returns the state of cell 2's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL3,<br>0x0657  | Returns the state of cell 3's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL4,<br>0x0658  | Returns the state of cell 4's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL5,<br>0x0659  | Returns the state of cell 5's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL6,<br>0x065A  | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL7,<br>0x065B  | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL8,<br>0x065C  | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL9,<br>0x065D  | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |
| RESR_RSLT_<br>CELL10,<br>0x065E | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned<br>integer<br>LSB = 1 | 0 | 0 to 3 |

|                             |                                                                                                                  |            |           |                                        |     |                 |
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| RESR_RSLT_CELL11,<br>0x065F | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RESR_RSLT_CELL12,<br>0x0660 | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RESR_RSLT_CELL13,<br>0x0661 | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RESR_RSLT_CELL14,<br>0x0662 | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RESR_RSLT_CELL15,<br>0x0663 | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RESR_RSLT_CELL16,<br>0x0664 | Returns the state of cell 6's RESR result.<br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 3          |
| RCXN_CELL1,<br>0x0665       | Returns cell 1's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL2,<br>0x0667       | Returns cell 2's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL3,<br>0x0669       | Returns cell 3's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL4,<br>0x066B       | Returns cell 4's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL5,<br>0x066D       | Returns cell 5's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL6,<br>0x066F       | Returns cell 6's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL7,<br>0x0671       | Returns cell 7's connection resistance learning value.                                                           | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |

|                           |                                                                                                             |            |           |                                        |     |                 |
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| RCXN_CELL8,<br>0x0673     | Returns cell 8's connection resistance learning value.                                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL9,<br>0x0675     | Returns cell 9's connection resistance learning value.                                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL10,<br>0x0677    | Returns cell 10's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL11,<br>0x0679    | Returns cell 11's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL12,<br>0x067B    | Returns cell 12's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL13,<br>0x067D    | Returns cell 13's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL14,<br>0x067F    | Returns cell 14's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL15,<br>0x0681    | Returns cell 15's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL16,<br>0x0683    | Returns cell 16's connection resistance learning value.                                                     | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mΩ | 0mΩ | 0mΩ to 6553.5mΩ |
| RCXN_LRN_CELL1,<br>0x0685 | Returns the state of cell 1's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 2          |
| RCXN_LRN_CELL2,<br>0x0686 | Returns the state of cell 1's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 2          |
| RCXN_LRN_CELL3,<br>0x0687 | Returns the state of cell 3's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 2          |
| RCXN_LRN_CELL4,<br>0x0688 | Returns the state of cell 4's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 2          |
| RCXN_LRN_CELL5,<br>0x0689 | Returns the state of cell 5's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1      | 0   | 0 to 2          |

|                                |                                                                                                              |          |           |                                   |   |        |
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| RCXN_LRN_<br>CELL6,<br>0x068A  | Returns the state of cell 6's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL7,<br>0x068B  | Returns the state of cell 7's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL8,<br>0x068C  | Returns the state of cell 8's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL9,<br>0x068D  | Returns the state of cell 9's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing  | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL10,<br>0x068E | Returns the state of cell 10's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL11,<br>0x068F | Returns the state of cell 11's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL12,<br>0x0690 | Returns the state of cell 12's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL13,<br>0x0691 | Returns the state of cell 13's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL14,<br>0x0692 | Returns the state of cell 14's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL15,<br>0x0693 | Returns the state of cell 15's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |
| RCXN_LRN_<br>CELL16,<br>0x0694 | Returns the state of cell 16's connection resistance learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 2 |

|                                |                                                                                                                                       |          |           |                                   |   |        |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|----------|-----------|-----------------------------------|---|--------|
| RCXN_RSLT_<br>CELL1,<br>0x0695 | Returns the state of cell 1's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL2,<br>0x0696 | Returns the state of cell 2's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL3,<br>0x0697 | Returns the state of cell 3's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL4,<br>0x0698 | Returns the state of cell 4's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL5,<br>0x0699 | Returns the state of cell 5's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL6,<br>0x069A | Returns the state of cell 6's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL7,<br>0x069B | Returns the state of cell 7's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL8,<br>0x069C | Returns the state of cell 8's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |
| RCXN_RSLT_<br>CELL9,<br>0x069D | Returns the state of cell 9's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0] | Read-only | 8-bit unsigned integer<br>LSB = 1 | 0 | 0 to 3 |

|                                 |                                                                                                                                        |            |           |                                                                 |                              |                                                                |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|------------|-----------|-----------------------------------------------------------------|------------------------------|----------------------------------------------------------------|
| RCXN_RSLT_<br>CELL10,<br>0x069E | Returns the state of cell 10's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL11,<br>0x069F | Returns the state of cell 11's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL12,<br>0x06A0 | Returns the state of cell 12's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL13,<br>0x06A1 | Returns the state of cell 13's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL14,<br>0x06A2 | Returns the state of cell 14's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL15,<br>0x06A3 | Returns the state of cell 15's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| RCXN_RSLT_<br>CELL16,<br>0x06A4 | Returns the state of cell 16's connection resistance result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| HCONV,<br>0x06A5                | Returns the heat transfer coefficient.                                                                                                 | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.01W/<br>(m <sup>2</sup> × K) | 23W/<br>(m <sup>2</sup> × K) | 0W/(m <sup>2</sup> × K)<br>to 655.35W/<br>(m <sup>2</sup> × K) |
| HCONV_LRN,<br>0x06A7            | Returns the state of the heat transfer coefficient learning.<br><br>0: Disabled<br>1: Paused<br>2: Ongoing                             | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |
| HCONV_RSLT,<br>0x06A8           | Returns the state of the heat transfer coefficient result.<br><br>0: Default<br>1: Updated<br>2: Updated to max<br>3: Updated to min   | 2, [1:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1                               | 0                            | 0 to 3                                                         |

|                       |                                                                                                                         |            |           |                                             |             |                      |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------|------------|-----------|---------------------------------------------|-------------|----------------------|
| SOH_PACK,<br>0x06A9   | Returns the pack's SOH.                                                                                                 | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL1,<br>0x06AD  | Returns cell 1's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL2,<br>0x06B1  | Returns cell 2's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL3,<br>0x06B5  | Returns cell 3's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL4,<br>0x06B9  | Returns cell 4's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL5,<br>0x06BD  | Returns cell 5's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL6,<br>0x06C1  | Returns cell 6's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL7,<br>0x06C5  | Returns cell 7's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL8,<br>0x06C9  | Returns cell 8's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL9,<br>0x06CD  | Returns cell 9's SOH.                                                                                                   | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL10,<br>0x06D1 | Returns cell 10's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL11,<br>0x06D5 | Returns cell 11's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL12,<br>0x06D9 | Returns cell 12's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL13,<br>0x06DD | Returns cell 13's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL14,<br>0x06E1 | Returns cell 14's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL15,<br>0x06E5 | Returns cell 15's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| SOH_CELL16,<br>0x06E9 | Returns cell 16's SOH.                                                                                                  | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.0000001% | 0%          | 0% to 100%           |
| PRDG,<br>0x07AD       | Returns the power state of the battery pack, which is equal to the pack current multiplied by the battery pack voltage. | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.1mW      | 0mW         | 0mW to 429496729.5mW |
| PDIS,<br>0x07B1       | Returns the maximum possible applicable discharge power.                                                                | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.1mW      | 0mW         | 0mW to 429496729.5mW |
| PDIS_ID,<br>0x07B5    | Returns the cell ID that is most significantly limiting the maximum discharge power estimate.                           | 5, [4:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 (cell ID) | 1 (cell ID) | 1 to 16 (cell ID)    |

|                           |                                                                                            |            |           |                                                                     |             |                      |
|---------------------------|--------------------------------------------------------------------------------------------|------------|-----------|---------------------------------------------------------------------|-------------|----------------------|
| PDIS_LIM,<br>0x07B6       | Returns the limiting factor in the maximum discharge power estimate.<br>0: Cell<br>1: Pack | 1, [0]     | Read-only | 8-bit unsigned integer                                              | 0           | 0 to 1               |
| PCHG,<br>0x07B7           | Returns the maximum possible applicable charge power.                                      | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 0.1mW                              | 0mW         | 0mW to 429496729.5mW |
| PCHG_ID,<br>0x07BB        | Returns the cell ID that is most significantly limiting the maximum charge power estimate. | 5, [4:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 (cell ID)                         | 1 (cell ID) | 1 to 16 (cell ID)    |
| PCHG_LIM,<br>0x07BC       | Returns the limiting factor in the maximum charge power estimate.<br>0: Cell<br>1: Pack    | 1, [0]     | Read-only | 8-bit unsigned integer                                              | 0           | 0 to 1               |
| OT_ID,<br>0x07BD          | Returns the cell ID with the highest temperature, per the cell temperature sensor.         | 3, [2:0]   | Read-only | 8-bit unsigned integer<br>LSB = 1 (cell ID)<br>Offset = 1 (cell ID) | 1 (cell ID) | 1 to 4 (cell ID)     |
| WARN_OTCHG_CC,<br>0x07BE  | Returns the predicted charge CC over-temperature (OT) warning.                             | 1, [0]     | Read-only | Boolean true/false                                                  | 0           | 0 to 1               |
| WARN_OTCHG_END,<br>0x07BE | Returns the predicted charge termination OT warning.                                       | 1, [1]     | Read-only | Boolean true/false                                                  | 0           | 0 to 1               |
| WARN_OTDIS,<br>0x07BE     | Returns the predicted discharge OT warning.                                                | 1, [2]     | Read-only | Boolean true/false                                                  | 0           | 0 to 1               |
| FG_ITER,<br>0x07BF        | Counts the number of iterations executed by the fuel gauge.                                | 32, [31:0] | Read-only | 32-bit unsigned integer<br>LSB = 1                                  | 0           | 0 to 4294967295      |

### Fuel Gauge Lifetime Log

| Name, Address             | Description                                | Bit Length, Position | Type      | Encoding                               | Decoded Default Value | Range           |
|---------------------------|--------------------------------------------|----------------------|-----------|----------------------------------------|-----------------------|-----------------|
| VRDG_MIN_CELL1,<br>0x0C00 | Returns cell 1's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL2,<br>0x0C02 | Returns cell 2's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL3,<br>0x0C04 | Returns cell 3's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL4,<br>0x0C06 | Returns cell 4's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL5,<br>0x0C08 | Returns cell 5's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL6,<br>0x0C0A | Returns cell 6's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL7,<br>0x0C0C | Returns cell 7's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL8,<br>0x0C0E | Returns cell 8's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |
| VRDG_MIN_CELL9,<br>0x0C10 | Returns cell 9's minimum measured voltage. | 16, [15:0]           | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV                | 0mV to 6553.5mV |

|                                |                                             |            |           |                                        |        |                 |
|--------------------------------|---------------------------------------------|------------|-----------|----------------------------------------|--------|-----------------|
| VRDG_MIN_<br>CELL10,<br>0x0C12 | Returns cell 10's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL11,<br>0x0C14 | Returns cell 11's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL12,<br>0x0C16 | Returns cell 12's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL13,<br>0x0C18 | Returns cell 13's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL14,<br>0x0C1A | Returns cell 14's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL15,<br>0x0C1C | Returns cell 15's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MIN_<br>CELL16,<br>0x0C1E | Returns cell 16's minimum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 5000mV | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL1,<br>0x0C20  | Returns cell 1's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL2,<br>0x0C22  | Returns cell 2's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL3,<br>0x0C24  | Returns cell 3's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL4,<br>0x0C26  | Returns cell 4's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL5,<br>0x0C28  | Returns cell 5's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL6,<br>0x0C2A  | Returns cell 6's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL7,<br>0x0C2C  | Returns cell 7's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL8,<br>0x0C2E  | Returns cell 8's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL9,<br>0x0C30  | Returns cell 9's maximum measured voltage.  | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL10,<br>0x0C32 | Returns cell 10's maximum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL11,<br>0x0C34 | Returns cell 11's maximum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL12,<br>0x0C36 | Returns cell 12's maximum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |
| VRDG_MAX_<br>CELL13,<br>0x0C38 | Returns cell 13's maximum measured voltage. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV | 0mV    | 0mV to 6553.5mV |

|                          |                                                                                                                                |            |           |                                                           |             |                   |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------|------------|-----------|-----------------------------------------------------------|-------------|-------------------|
| VRDG_MAX_CELL14, 0x0C3A  | Returns cell 14's maximum measured voltage.                                                                                    | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV                    | 0mV         | 0mV to 6553.5mV   |
| VRDG_MAX_CELL15, 0x0C3C  | Returns cell 15's maximum measured voltage.                                                                                    | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV                    | 0mV         | 0mV to 6553.5mV   |
| VRDG_MAX_CELL16, 0x0C3E  | Returns cell 16's maximum measured voltage.                                                                                    | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 0.1mV                    | 0mV         | 0mV to 6553.5mV   |
| VRDG_DMAX, 0x0C40        | Returns the maximum measured voltage difference between the cells.                                                             | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 2mV                       | 0mV         | 0mV to 131070 mV  |
| VRDG_DMAX_IDMAX, 0x0C41  | Identifies the cell with the highest voltage. This cell is used to calculate the maximum voltage difference between the cells. | 4, [3:0]   | Read-only | Non-standard<br>LSB = 1 (cell ID)<br>Offset = 1 (cell ID) | 1 (cell ID) | 1 to 16 (cell ID) |
| VRDG_DMAX_IDMIN, 0x0C41  | Identifies the cell with the lowest voltage. This cell is used to calculate the maximum voltage difference between the cells.  | 4, [7:4]   | Read-only | Non-standard<br>LSB = 1 (cell ID)<br>Offset = 1 (cell ID) | 1 (cell ID) | 1 to 16 (cell ID) |
| BAL_ETIME_CELL1, 0x0C42  | Returns the total time that cell 1 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL2, 0x0C44  | Returns the total time that cell 2 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL3, 0x0C46  | Returns the total time that cell 3 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL4, 0x0C48  | Returns the total time that cell 4 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL5, 0x0C4A  | Returns the total time that cell 5 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL6, 0x0C4C  | Returns the total time that cell 6 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL7, 0x0C4E  | Returns the total time that cell 7 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL8, 0x0C50  | Returns the total time that cell 8 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL9, 0x0C52  | Returns the total time that cell 9 has been balanced.                                                                          | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL10, 0x0C54 | Returns the total time that cell 10 has been balanced.                                                                         | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL11, 0x0C56 | Returns the total time that cell 11 has been balanced.                                                                         | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL12, 0x0C58 | Returns the total time that cell 12 has been balanced.                                                                         | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL13, 0x0C5A | Returns the total time that cell 13 has been balanced.                                                                         | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |
| BAL_ETIME_CELL14, 0x0C5C | Returns the total time that cell 14 has been balanced.                                                                         | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min  |

|                                  |                                                                                                                                        |            |           |                                                           |             |                  |
|----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|------------|-----------|-----------------------------------------------------------|-------------|------------------|
| BAL_ETIME_<br>CELL15,<br>0x0C5E  | Returns the total time that cell 15 has been balanced.                                                                                 | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min |
| BAL_ETIME_<br>CELL16,<br>0x0C60  | Returns the total time that cell 16 has been balanced.                                                                                 | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1min                     | 0min        | 0min to 65535min |
| TRDG_MIN_<br>TS1,<br>0x0C62      | Returns the minimum temperature measured with temperature sensor 1.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MIN_<br>TS2,<br>0x0C63      | Returns the minimum temperature measured with temperature sensor 2.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MIN_<br>TS3,<br>0x0C64      | Returns the minimum temperature measured with temperature sensor 2.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MIN_<br>TS4,<br>0x0C65      | Returns the minimum temperature measured with temperature sensor 2.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MAX_<br>TS1,<br>0x0C66      | Returns the maximum temperature measured with temperature sensor 1.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MAX_<br>TS2,<br>0x0C67      | Returns the maximum temperature measured with temperature sensor 2.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MAX_<br>TS3,<br>0x0C68      | Returns the maximum temperature measured with temperature sensor 3.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_MAX_<br>TS4,<br>0x0C69      | Returns the maximum temperature measured with temperature sensor 4.                                                                    | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 97.5°C      | -30°C to +97.5°C |
| TRDG_DMAX,<br>0x0C6A             | Returns the maximum measured temperature difference between temperature the sensors.                                                   | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C                     | 0°C         | 0°C to 127.5°C   |
| TRDG_DMAX_<br>IDMAX,<br>0x0C6B   | Identifies the cell with the highest temperature. This cell is used to calculate the maximum temperature difference between the cells. | 4, [3:0]   | Read-only | Non-standard<br>LSB = 1 (cell ID)<br>Offset = 1 (cell ID) | 1 (cell ID) | 1 to 4 (cell ID) |
| TRDG_DMAX_<br>IDMIN,<br>0x0C6B   | Identifies the cell with the lowest temperature. This cell is used to calculate the maximum temperature difference between the cells.  | 4, [7:4]   | Read-only | Non-standard<br>LSB = 1 (cell ID)<br>Offset = 1 (cell ID) | 1 (cell ID) | 1 to 4 (cell ID) |
| TRDG_ETIME_<br>UND0,<br>0x0C6C   | Returns the amount of time that the battery's average temperature has been below 0°C .                                                 | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |
| TRDG_ETIME_<br>0TO5,<br>0x0C6E   | Returns the amount of time that the battery's average temperature has been between 0°C and 5°C.                                        | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |
| TRDG_ETIME_<br>5TO10,<br>0x0C70  | Returns the amount of time that the battery's average temperature has been between 5°C and 10°C.                                       | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |
| TRDG_ETIME_<br>10TO15,<br>0x0C72 | Returns the amount of time that the battery's average temperature has been between 10°C and 15°C.                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |
| TRDG_ETIME_<br>15TO20,<br>0x0C74 | Returns the amount of time that the battery's average temperature has been between 15°C and 20°C.                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |
| TRDG_ETIME_<br>20TO25,<br>0x0C76 | Returns the amount of time that the battery's average temperature has been between 20°C and 25°C.                                      | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr                      | 0hr         | 0hr to 65535hr   |

|                                  |                                                                                                                              |            |           |                                             |               |                                    |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------|------------|-----------|---------------------------------------------|---------------|------------------------------------|
| TRDG_ETIME_<br>25TO30,<br>0x0C78 | Returns the amount of time that the battery's average temperature has been between 25°C and 30°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>30TO35,<br>0x0C7A | Returns the amount of time that the battery's average temperature has been between 30°C and 35°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>35TO40,<br>0x0C7C | Returns the amount of time that the battery's average temperature has been between 35°C and 40°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>40TO45,<br>0x0C7E | Returns the amount of time that the battery's average temperature has been between 40°C and 45°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>45TO50,<br>0x0C80 | Returns the amount of time that the battery's average temperature has been between 45°C and 50°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>50TO55,<br>0x0C82 | Returns the amount of time that the battery's average temperature has been between 50°C and 55°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>55TO60,<br>0x0C84 | Returns the amount of time that the battery's average temperature has been between 55°C and 60°C.                            | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_ETIME_<br>ABV60,<br>0x0C86  | Returns the amount of time that the battery's average temperature exceeds 60°C.                                              | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1hr        | 0hr           | 0hr to<br>65535hr                  |
| TRDG_MIN_<br>DIE,<br>0x0C88      | Returns the minimum temperature measured on the die.                                                                         | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C       | 0°C           | -30°C to<br>+97.5°C                |
| TRDG_MAX_<br>DIE,<br>0x0C89      | Returns the maximum temperature measured on the die.                                                                         | 8, [7:0]   | Read-only | 8-bit unsigned integer<br>LSB = 0.5°C       | -30°C         | -30°C to<br>+97.5°C                |
| IRDG_MAX_<br>CHG,<br>0x0C8A      | Returns the maximum measured charge current.                                                                                 | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 2mA        | 0mA           | 0mA to<br>131070<br>mA             |
| IRDG_MAX_<br>DIS,<br>0x0C8C      | Returns the maximum measured discharge current.                                                                              | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 2mA        | 0mA           | 0mA to<br>131070mA                 |
| NCHG_CYC,<br>0x0C8E              | Returns the number of completed charge cycles, which is when the battery pack's SOC has charged from below 15% to above 85%. | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1 Event(s) | 0<br>event(s) | 0 event(s)<br>to 65535<br>event(s) |
| NCHG_10SOC,<br>0x0C90            | Returns the number of times the pack has been charged by 10%.                                                                | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1 event    | 0<br>event(s) | 0 event(s)<br>to 65535<br>event(s) |
| NSHDN,<br>0x0C92                 | Returns the number of times the fuel gauge has woken up after sleep mode, a hard reset, or a shutdown.                       | 16, [15:0] | Read-only | 16-bit unsigned integer<br>LSB = 1 event    | 0<br>event(s) | 0 event(s)<br>to 65535<br>event(s) |

**Fuel Gauge Flags**

| Name, Address                        | Description                                                                                                                                                                                                        | Bit Length, Position | Type      | Encoding                | Decoded Default Value | Range  |
|--------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------|-------------------------|-----------------------|--------|
| FG_EXE_FLAG,<br>0x0F00               | 1: Fuel gauge calculations are ongoing<br>0: Fuel gauge calculations are complete                                                                                                                                  | 1, [0]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| EDIT_SETTINGS_FLAG,<br>0x0F00        | 1: Fuel gauge settings can be edited on the fly<br>0: Fuel gauge settings cannot be edited on the fly                                                                                                              | 1, [1]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| CONFIG_MODE_FLAG,<br>0x0F00          | 1: The fuel gauge is in configuration mode<br>0: The fuel gauge is in running mode                                                                                                                                 | 1, [2]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| CONFIG_EXIT_FLAG,<br>0x0F00          | 1: There is a pending exit from configuration mode<br>0: There is no pending exit from configuration mode                                                                                                          | 1, [3]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| CONFIG_RST_FLAG,<br>0x0F00           | 1: There is a pending reset to set the configurations to their default values<br>0: There is no pending reset to set the configurations to their default values                                                    | 1, [4]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| FG_RST_FLAG,<br>0x0F00               | 1: There is no pending reset for the fuel gauge algorithm<br>0: There is a pending reset for the fuel gauge algorithm                                                                                              | 1, [5]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| LOG_RST_FLAG,<br>0x0F00              | 1: The lifetime log registers are being reset in the current fuel gauge iteration<br>0: No lifetime log registers are being reset                                                                                  | 1, [6]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| LOG_RST_PNDG_FLAG,<br>0x0F00         | 1: There is a pending reset to the lifetime log registers<br>0: There is no pending reset to the lifetime log registers                                                                                            | 1, [7]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| CUST_BLOCK_FLAG,<br>0x0F00           | 1: Customer block is active<br>0: No customer block is active                                                                                                                                                      | 1, [8]               | Read-only | Non-standard            | 0                     | 0 to 1 |
| CUST_BLOCK_FAIL_CNTR_FLAG,<br>0x0F00 | This counter contains the number of failed attempts at writing the password. If there are four failed attempts, then CUST_BLOCK_LOCKED_FLAG is set and this feature is locked until a hardware reset is performed. | 2, [10:9]            | Read-only | Non-standard<br>LSB = 1 | 0                     | 0 to 3 |
| CUST_BLOCK_LOCKED_FLAG,<br>0x0F00    | 1: The customer block feature is locked and remains locked until a hardware reset is performed<br>0: No customer block feature is locked                                                                           | 1, [11]              | Read-only | Non-standard            | 0                     | 0 to 1 |
| FG_BKUP_FLAG,<br>0x0F00              | 1: The fuel gauge is in learning backup mode<br>0: The fuel gauge is not in learning backup mode<br><br>Use FG_BKUP_ENABLE to exit/enter this mode.                                                                | 1, [12]              | Read-only | Non-standard            | 0                     | 0 to 1 |
| LEDS_ON_BTN_FLAG,<br>0x0F00          | 1: The LEDs are on due to the push-button<br>0: No LEDs are on due to the push-button                                                                                                                              | 1, [13]              | Read-only | Non-standard            | 0                     | 0 to 1 |
| LEDS_ON_CHG_FLAG,<br>0x0F00          | 1: The LEDs are on due to the charge current being detected<br>0: The LEDs are not on due to charge current being detected                                                                                         | 1, [14]              | Read-only | Non-standard            | 0                     | 0 to 1 |
| LEDS_CHG_FLAG,<br>0x0F00             | 1: The LED controller considers the fuel gauge to be in a charge state<br>0: The LED controller does not consider the fuel gauge to be in a charge state                                                           | 1, [15]              | Read-only | Non-standard            | 0                     | 0 to 1 |

**Fuel Gauge Settings**

| Name, Address              | Description                                                                                                                                                                                                                                                                                                                                                                                         | Bit Length, Position | Type | Encoding                                    | Decoded Default Value | Range              |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|---------------------------------------------|-----------------------|--------------------|
| EXE_TIME,<br>0x1000        | Sets the fuel gauge execution time interval.                                                                                                                                                                                                                                                                                                                                                        | 8, [7:0]             | R/W  | 8-bit unsigned integer<br>LSB = 0.1s        | 4s                    | 0.5s to 16s        |
| WE_XE_TIME_REST,<br>0x1001 | Updates the most time-consuming functions when the fuel gauge is resting each (WE_XE_TIME_REST x EXE_TIME), instead of each EXE_TIME. The maximum allowed value for the execution period of this functions is 32s, so if the fuel gauge is set such that (WE_XE_TIME_REST x EXE_TIME) is longer than 32s, then the period used is the multiple of EXE_TIME, that is closes to but shorter than 32s. | 5, [4:0]             | R/W  | 8-bit unsigned integer<br>LSB = 1           | 4                     | 1 to 16            |
| DIS_ITH,<br>0x1002         | Sets the discharge status current threshold.                                                                                                                                                                                                                                                                                                                                                        | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 1mA        | 25 mA                 | 0mA to 65535mA     |
| CHG_ITH,<br>0x1004         | Sets the charge status current threshold.                                                                                                                                                                                                                                                                                                                                                           | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 1mA        | 25 mA                 | 0mA to 65535mA     |
| SOC_DMAX,<br>0x1006        | Sets the maximum SOC for the charge and discharge statuses.                                                                                                                                                                                                                                                                                                                                         | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.00005%/s | 0.07 %/s              | 0.00005%/s to 2%/s |
| SOC_DMAX_REST,<br>0x1008   | Sets the maximum SOC slope for the resting status.                                                                                                                                                                                                                                                                                                                                                  | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.00005%/s | 0.001 %/s             | 0%/s to 2%/s       |
| VRDG_PACK_EN,<br>0x1040    | Enables the VRDG_PACK input.                                                                                                                                                                                                                                                                                                                                                                        | 1, [0]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| IRDG_PACK_EN,<br>0x1040    | Enables the IRDG_PACK input.                                                                                                                                                                                                                                                                                                                                                                        | 1, [1]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| IRDG_CELLS_EN,<br>0x1040   | Enables the IRDG_CELLx inputs.                                                                                                                                                                                                                                                                                                                                                                      | 1, [2]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| CCRDG_EN,<br>0x1040        | Enables the CCRDG input.                                                                                                                                                                                                                                                                                                                                                                            | 1, [3]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| TRDG_AMB_EN,<br>0x1040     | Enables the TRDG_AMB input.                                                                                                                                                                                                                                                                                                                                                                         | 1, [4]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| SOH_LRN_EN,<br>0x1041      | Enables SOH learning.                                                                                                                                                                                                                                                                                                                                                                               | 1, [0]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |
| RESR_LRN_EN,<br>0x1041     | Enables ESR learning.                                                                                                                                                                                                                                                                                                                                                                               | 1, [2]               | R/W  | Control<br>Enable = 1<br>Disable = 0        | 1                     | 0 to 1             |

|                                 |                                                                     |        |     |                                      |   |        |
|---------------------------------|---------------------------------------------------------------------|--------|-----|--------------------------------------|---|--------|
| RCXN_CELLS_LRN_EN,<br>0x1041    | Enables ESR learning.                                               | 1, [3] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| ICHG_CC_LRN_EN,<br>0x1041       | Enables charge CC learning.                                         | 1, [4] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| ICHG_END_LRN_EN,<br>0x1041      | Enables charge termination current learning.                        | 1, [5] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| VCHG_CV_LRN_EN,<br>0x1041       | Enables charge CV learning.                                         | 1, [6] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| IDIS_AVG_LRN_EN,<br>0x1041      | Enables discharge average current learning.                         | 1, [7] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| IDIS_END_LRN_EN,<br>0x1042      | Enables discharge termination current learning.                     | 1, [0] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| IDIS_END_LRN_CONT_EN,<br>0x1042 | Enables continuous discharge termination current learning.          | 1, [1] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| THRM_MDL_EN,<br>0x1042          | Enables continuous discharge termination current learning.          | 1, [2] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| HCONV_LRN_EN,<br>0x1042         | Enables continuous discharge termination current learning.          | 1, [3] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| HCONV_LRN_CONT_EN,<br>0x1042    | Enables continuous discharge termination current learning.          | 1, [4] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| PCHG_SHW_EN,<br>0x1042          | Sets the PCHG_SHW default value.                                    | 1, [7] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| PDIS_SHW_EN,<br>0x1043          | Sets the PDIS_SHW default value.                                    | 1, [0] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| IT_DONE_INTR_EN,<br>0x1080      | Enables an IT_DONE_INTR (iteration complete) interrupt.             | 1, [0] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| STATUS_INTR_EN,<br>0x1080       | Enables a STATUS_INTR (status changes) interrupt.                   | 1, [1] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| EMPTY_LIM_INTR_EN,<br>0x1080    | Enables an EMPTY_LIM_INTR (empty limiting factor change) interrupt. | 1, [2] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |
| FULL_LIM_INTR_EN,<br>0x1080     | Enables a FULL_LIM_INTR (full limiting factor changed) interrupt.   | 1, [3] | R/W | Control<br>Enable = 1<br>Disable = 0 | 1 | 0 to 1 |

|                               |                                                                              |            |     |                                        |        |                 |
|-------------------------------|------------------------------------------------------------------------------|------------|-----|----------------------------------------|--------|-----------------|
| SOC_PACK_RSLT_INTR_EN, 0x1080 | Enables a SOC_PACK_RSLT_INTR (pack SOC result changed) interrupt.            | 1, [4]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| OT_WARN_INTR_EN, 0x1080       | Enables an OT_WARN_INTR interrupt.                                           | 1, [5]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| IDIS_AVG_INTR_EN, 0x1080      | Enables an IDIS_AVG_INTR (average discharge current learning) interrupt.     | 1, [6]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| IDIS_END_INTR_EN, 0x1080      | Enables an IDIS_END_INTR (discharge termination current learning) interrupt. | 1, [7]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| ICHG_CC_INTR_EN, 0x1080       | Enables an ICHG_CC_INTR (charge CC current learning) interrupt.              | 1, [8]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| ICHG_END_INTR_EN, 0x1080      | Enables an ICHG_END_INTR (charge termination current learning) interrupt.    | 1, [9]     | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| VCHG_CV_INTR_EN, 0x1080       | Enables a VCHG_CV_INTR (charge CV learning) interrupt.                       | 1, [10]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| SORES_CELL_INTR_EN, 0x1080    | Enables an SORES_CELLS_INTR (ESR learning) interrupt.                        | 1, [11]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| RCXN_CELLS_INTR_EN, 0x1080    | Enables an RCXN_CELLS_INTR (cell resistance learning) interrupt.             | 1, [12]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| HCONV_INTR_EN, 0x1080         | Enables an HCONV_INTR (heat transfer coefficient learning) interrupt.        | 1, [13]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| SOH_CELLS_INTR_EN, 0x1080     | Enables an SOH_CELLS_INTR (cell SOH learning) interrupt.                     | 1, [14]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| PDIS_LIM_INTR_EN, 0x1080      | Enables a PDIS_LIM_INTR (discharge power limiting factor change) interrupt.  | 1, [16]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| PCHG_LIM_INTR_EN, 0x1080      | Enables a PCHG_LIM_INTR (charge power limiting factor change) interrupt.     | 1, [17]    | R/W | Control<br>Enable = 1<br>Disable = 0   | 1      | 0 to 1          |
| VCELL_MAX, 0x10C0             | Sets the maximum voltage accepted at the cell level.                         | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mV | 4200mV | 0mV to 6553.5mV |
| VCELL_MAX_MRG_N, 0x10C2       | Sets the maximum cell voltage margin.                                        | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5mV  | 5mV    | 0mV to 127.5mV  |
| VCELL_MIN, 0x10C3             | Sets the minimum voltage accepted at the cell level.                         | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mV | 3000mV | 0mV to 6553.5mV |

|                        |                                                                                                                                                                                                                                                                                            |            |     |                                               |             |                               |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|-----------------------------------------------|-------------|-------------------------------|
| VCELL_MIN_MRGN, 0x10C5 | Sets the minimum cell voltage margin.                                                                                                                                                                                                                                                      | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5mV         | 5mV         | 0mV to 127.5mV                |
| VPACK_MAX, 0x10C6      | Sets the maximum voltage that the pack can accept. This value is used for charge power estimate.<br><br>The pack float voltage represents the maximum voltage that the battery pack can reach in a charging scenario. It should be set the be equal to or exceed the charging system's CV. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 2mV          | 66800mV     | 0mV to 131070mV               |
| VPACK_MAX_MRGN, 0x10C8 | Sets the pack's maximum pack voltage margin.                                                                                                                                                                                                                                               | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 4mV           | 48mV        | 0mV to 1020mV                 |
| VPACK_MIN, 0x10C9      | Sets the pack empty voltage, which represents the lowest usable pack voltage. This is the voltage at which the application considers the battery pack to be completely discharged and stops operation.                                                                                     | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 2mV          | 48800mV     | 0mV to 131070mV               |
| VPACK_MIN_MRGN, 0x10CB | Sets the margin for the power learning algorithm, which is applied to the pack empty voltage.                                                                                                                                                                                              | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 4mV           | 48mV        | 0mV to 1020mV                 |
| ICHG_MAX, 0x1100       | Sets the maximum charge current that the pack can accept.                                                                                                                                                                                                                                  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 1 C-rate    | 0.001 C-rate to 65.535 C-rate |
| ICHG_MAX_MRGN, 0x1102  | Sets the maximum charge current margin.                                                                                                                                                                                                                                                    | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.002 C-rate  | 0.02 C-rate | 0 C-rate to 0.51 C-rate       |
| IDIS_MAX, 0x1103       | Sets the maximum discharge current that the pack can accept.                                                                                                                                                                                                                               | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 2 C-rate    | 0.001 C-rate to 65.535 C-rate |
| IDIS_MAX_MRGN, 0x1105  | Sets the maximum discharge current margin.                                                                                                                                                                                                                                                 | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.002 C-rate  | 0.02 C-rate | 0 C-rate to 0.51 C-rate       |
| RCXN_PACK, 0x1140      | Sets the connection resistance between the battery and the battery management system (BMS) terminals.                                                                                                                                                                                      | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 10mΩ        | 0mΩ to 6553.5mΩ               |
| RBMS_HSIDE, 0x1142     | Sets the BMS's high-side resistance.                                                                                                                                                                                                                                                       | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 4mΩ         | 0mΩ to 6553.5mΩ               |
| RBMS_LSIDE, 0x1144     | Sets the BMS's low-side resistance.                                                                                                                                                                                                                                                        | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 2mΩ         | 0mΩ to 6553.5mΩ               |
| RCXN_CELL1, 0x1146     | Sets the connection resistance between cell 1's terminals and its corresponding voltage-sensing probes.                                                                                                                                                                                    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 1mΩ         | 0mΩ to 6553.5mΩ               |
| RCXN_CELL2, 0x1148     | Sets the connection resistance between cell 2's terminals and its corresponding voltage-sensing probes.                                                                                                                                                                                    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 1mΩ         | 0mΩ to 6553.5mΩ               |
| RCXN_CELL3, 0x114A     | Sets the connection resistance between cell 3's terminals and its corresponding voltage-sensing probes.                                                                                                                                                                                    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 1mΩ         | 0mΩ to 6553.5mΩ               |
| RCXN_CELL4, 0x114C     | Sets the connection resistance between cell 4's terminals and its corresponding voltage-sensing probes.                                                                                                                                                                                    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ        | 1mΩ         | 0mΩ to 6553.5mΩ               |

|                        |                                                                                                          |            |     |                                        |     |                 |
|------------------------|----------------------------------------------------------------------------------------------------------|------------|-----|----------------------------------------|-----|-----------------|
| RCXN_CELL5,<br>0x114E  | Sets the connection resistance between cell 5's terminals and its corresponding voltage-sensing probes.  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL6,<br>0x1150  | Sets the connection resistance between cell 6's terminals and its corresponding voltage-sensing probes.  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL7,<br>0x1152  | Sets the connection resistance between cell 7's terminals and its corresponding voltage-sensing probes.  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL8,<br>0x1154  | Sets the connection resistance between cell 8's terminals and its corresponding voltage-sensing probes.  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL9,<br>0x1156  | Sets the connection resistance between cell 9's terminals and its corresponding voltage-sensing probes.  | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL10,<br>0x1158 | Sets the connection resistance between cell 10's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL11,<br>0x115A | Sets the connection resistance between cell 11's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL12,<br>0x115C | Sets the connection resistance between cell 12's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL13,<br>0x115E | Sets the connection resistance between cell 13's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL14,<br>0x1160 | Sets the connection resistance between cell 14's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL15,<br>0x1162 | Sets the connection resistance between cell 15's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| RCXN_CELL16,<br>0x1164 | Sets the connection resistance between cell 16's terminals and its corresponding voltage-sensing probes. | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.1mΩ | 1mΩ | 0mΩ to 6553.5mΩ |
| TSS_CELL1,<br>0x11C0   | Sets cell 1's temperature sensor source.                                                                 | 2, [1:0]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1  | 1   | 1 to 4          |
| TSS_CELL2,<br>0x11C0   | Sets cell 2's temperature sensor source.                                                                 | 2, [3:2]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1  | 1   | 1 to 4          |
| TSS_CELL3,<br>0x11C0   | Sets cell 3's temperature sensor source.                                                                 | 2, [5:4]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1  | 1   | 1 to 4          |
| TSS_CELL4,<br>0x11C0   | Sets cell 4's temperature sensor source.                                                                 | 2, [7:6]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1  | 1   | 1 to 4          |
| TSS_CELL5,<br>0x11C1   | Sets cell 5's temperature sensor source.                                                                 | 2, [1:0]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1  | 1   | 1 to 4          |

|                       |                                                                        |            |     |                                                             |                          |                                                             |
|-----------------------|------------------------------------------------------------------------|------------|-----|-------------------------------------------------------------|--------------------------|-------------------------------------------------------------|
| TSS_CELL6,<br>0x11C1  | Sets cell 6's temperature sensor source.                               | 2, [3:2]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL7,<br>0x11C1  | Sets cell 7's temperature sensor source.                               | 2, [5:4]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL8,<br>0x11C1  | Sets cell 8's temperature sensor source.                               | 2, [7:6]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL9,<br>0x11C2  | Sets cell 9's temperature sensor source.                               | 2, [1:0]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL10,<br>0x11C2 | Sets cell 10's temperature sensor source.                              | 2, [3:2]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL11,<br>0x11C2 | Sets cell 11's temperature sensor source.                              | 2, [5:4]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL12,<br>0x11C2 | Sets cell 12's temperature sensor source.                              | 2, [7:6]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL13,<br>0x11C3 | Sets cell 13's temperature sensor source.                              | 2, [1:0]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL14,<br>0x11C3 | Sets cell 14's temperature sensor source.                              | 2, [3:2]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL15,<br>0x11C3 | Sets cell 15's temperature sensor source.                              | 2, [5:4]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TSS_CELL16,<br>0x11C3 | Sets cell 16's temperature sensor source.                              | 2, [7:6]   | R/W | Non-standard<br>LSB = 1<br>Offset = 1                       | 1                        | 1 to 4                                                      |
| TCHG_MAX,<br>0x11C4   | Sets the application's maximum allowed temperature during charging.    | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5°C                       | 50°C                     | -30°C to +97.5°C                                            |
| TDIS_MAX,<br>0x11C5   | Sets the application's maximum allowed temperature during discharging. | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5°C                       | 60°C                     | -30°C to +97.5°C                                            |
| HCONV_PACK,<br>0x11C6 | Sets the battery pack's heat transfer coefficient.                     | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.01W/(m <sup>2</sup> × K) | 23W/(m <sup>2</sup> × K) | 0.01 W/(m <sup>2</sup> × K) to 655.35W/(m <sup>2</sup> × K) |

|                               |                                                                                                                                                                                                |            |     |                                               |              |                               |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|-----------------------------------------------|--------------|-------------------------------|
| NCELLS_SER,<br>0x1200         | Sets the number of series-connected cells in the battery pack.                                                                                                                                 | 5, [4:0]   | R/W | 8-bit unsigned integer<br>LSB = 1             | 16           | 2 to 16                       |
| NCELLS_PAR,<br>0x1201         | Sets the number of parallel-connected cells in the battery pack.                                                                                                                               | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 1             | 1            | 1 to 255                      |
| NTSS,<br>0x1202               | Sets the number of temperature sensors in the battery pack.                                                                                                                                    | 3, [2:0]   | R/W | 8-bit unsigned integer<br>LSB = 1             | 1            | 1 to 4                        |
| IDIS_AVG_SET,<br>0x1280       | Sets the nominal average discharge current (i.e. IDIS_AVG).                                                                                                                                    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 1 C-rate     | 0.001 C-rate to 65.535 C-rate |
| IDIS_END_SET,<br>0x1282       | Sets the nominal discharge termination current (i.e. IDIS_END).                                                                                                                                | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 1 C-rate     | 0.001 C-rate to 65.535 C-rate |
| ICHG_CC_SET,<br>0x12C0        | Sets the nominal charge constant current (i.e. ICHG_CC). It should be set to the nominal current that applied by the external charger to the battery pack while in the charge CC region.       | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0.5 C-rate   | 0.001 C-rate to 65.535 C-rate |
| ICHG_END_SET,<br>0x12C2       | Sets the nominal charge termination current (i.e. ICHG_END).<br>It should be set to the nominal current, which is used to detect the end of charge while in the charge CV region.              | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 0.001 C-rate | 0.1 C-rate   | 0.001 C-rate to 65.535 C-rate |
| ICHG_END_MRGN,<br>0x12C4      | Sets the charge termination current (i.e. ICHG_END_SET) margin.                                                                                                                                | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.001 C-rate  | 0.005 C-rate | 0 C-rate to 0.255 C-rate      |
| VCHG_CV_SET,<br>0x12C5        | Sets the nominal charge constant voltage (i.e. VCHG_CV).<br>This value should be set to the nominal voltage, which is applied to the battery pack by the external charger during CV charge.    | 16, [15:0] | R/W | 16-bit unsigned integer<br>LSB = 2mV          | 66400mV      | 0mV to 131070mV               |
| EMPTY_RTIME_FILTER,<br>0x1304 | Sets the filter time constant for the remaining time-to-empty (i.e. EMPTY_RTIME).<br>Increasing EMPTY_RTIME_FILTER results in a smoother estimate at the tradeoff of an increased phase delay. | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 1s            | 60s          | 0s to 255s                    |
| EMPTY_DTEMP_FILTER,<br>0x1305 | Sets the filter time constant for the predicted remaining time-to-empty (i.e. EMPTY_RTIME).                                                                                                    | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 1s            | 60s          | 0s to 255s                    |
| FULL_RTIME_FILTER,<br>0x1345  | Sets the filter time constant for the remaining time-to-full (i.e. FULL_RTIME).                                                                                                                | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 1s            | 60s          | 0s to 255s                    |
| FULL_DTEMP_FILTER,<br>0x1346  | Sets the filter time constant for the predicted temperature-to-full (i.e. FULL_DTEMP).                                                                                                         | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 1s            | 60s          | 0s to 255s                    |
| ICHG_CC_LRN_RNG,<br>0x1380    | If ICHG_CC_LRN_EN is enabled, these bits set the charge CC (i.e. ICHG_CC) learning range.                                                                                                      | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5%          | 10%          | 0% to 100%                    |
| ICHG_CC_LRN_SOCTH,<br>0x1381  | Sets the SOC threshold for charge CC learning (i.e. ICHG_CC).                                                                                                                                  | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.5 %         | 80%          | 0% to 100%                    |
| ICHG_CC_LRN_DITH,<br>0x1382   | Sets the charge current derivative threshold for charge CC learning (i.e. ICHG_CC).                                                                                                            | 8, [7:0]   | R/W | 8-bit unsigned integer<br>LSB = 0.01 mA/s     | 0.1mA/s      | 0mA/s to 2.55mA/s             |

|                             |                                                                                                                             |          |     |                                             |              |                         |
|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------|----------|-----|---------------------------------------------|--------------|-------------------------|
| ICHG_CC_LRN_CNTRTH, 0x1384  | Sets the sample counter threshold for charge CC learning (i.e. ICHG_CC).                                                    | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1 sample(s) | 20 sample(s) | 0 to 255 sample(s)      |
| ICHG_END_LRN_RNG, 0x13C0    | If ICHG_END_LRN_EN enabled, these bits set the charge termination current (i.e. ICHG_END) learning range.                   | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5 %       | 10%          | 0% to 100%              |
| ICHG_END_LRN_SOCTH, 0x13C1  | Sets the SOC threshold for charge termination current learning (i.e. ICHG_END).                                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5 %       | 80%          | 0% to 100%              |
| ICHG_END_LRN_ITH, 0x13C2    | Sets the charge current threshold for charge termination current learning, (i.e. ICHG_END).                                 | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate | 0.01 C-rate  | 0 C-rate to 2.55 C-rate |
| ICHG_END_LRN_DVTH, 0x13C3   | Sets the charge voltage derivative threshold for charge termination current learning (i.e. ICHG_END).                       | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01mV/s    | 0.1mV/s      | 0mV/s to 2.55mV/s       |
| VCHG_CV_LRN_RNG, 0x1400     | If VCHG_CV_LRN_EN is enabled, these bits set the charge CV (i.e. VCHG_CV) learning range.                                   | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 10%          | 0% to 100%              |
| VCHG_CV_LRN_SOCTH, 0x1401   | Sets the SOC threshold for charge CV learning (i.e. VCHG_CV).                                                               | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 80%          | 0% to 100%              |
| VCHG_CV_LRN_ITH, 0x1402     | Sets the charge current threshold for charge CV learning, (i.e. VCHG_CV).                                                   | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate | 0.01 C-rate  | 0 C-rate to 25.5 C-rate |
| VCHG_CV_LRN_DVTH, 0x1403    | Sets the charge voltage derivative threshold for charge CV learning (i.e. VCHG_CV).                                         | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01mV/s    | 0.1mV/s      | 0mV/s to 2.55mV/s       |
| IDIS_AVG_LRN_RNG, 0x1440    | If IDIS_END_LRN_EN is enabled, these bits set the discharge termination current (i.e. IDIS_END) learning range.             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 100%         | 0% to 100%              |
| IDIS_AVG_LRN_ITH, 0x1441    | Sets the discharge current threshold for learnings (i.e. IDIS_AVG and IDIS_END).                                            | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate | 0.05 C-rate  | 0 C-rate to 2.55 C-rate |
| IDIS_AVG_LRN_FILTER, 0x1442 | Sets the filter time constant for the discharge current learnings (i.e. IDIS_AVG and IDIS_END).                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1s          | 10s          | 0s to 255s              |
| IDIS_END_LRN_RNG, 0x1480    | If IDIS_END_LRN_EN is enabled, these bits set the discharge termination current (i.e. IDIS_END) learning range.             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 10%          | 0% to 100%              |
| IDIS_END_LRN_SOCTH, 0x1481  | If IDIS_END_LRN_EN is enabled, these bits set the SOC discharge termination current (i.e. IDIS_END) learning threshold.     | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 50%          | 0% to 100%              |
| IDIS_END_LRN_KPEAK, 0x1482  | If IDIS_END_LRN_EN is enabled, these bits set the discharge termination current (i.e. IDIS_END) learning peak current gain. | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%        | 70%          | 0% to 100%              |
| IDIS_END_LRN_ITH, 0x1483    | Sets the discharge termination current threshold for learnings (i.e. IDIS_AVG, IDIS_END).                                   | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate | 0.05 C-rate  | 0 C-rate to 2.55 C-rate |
| IDIS_END_LRN_FILTER, 0x1484 | Sets the filter time constant for discharge current learnings (i.e. IDIS_AVG and IDIS_END).                                 | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1s          | 10 s         | 0s to 255s              |
| SOH_LRN_K, 0x14C0           | If SOH_LRN_EN is enabled, these bits set the SOH learning gain.                                                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.001       | 0.1          | 0 to 0.255              |
| SOH_LRN_DMAX, 0x14C1        | If SOH_LRN_EN is enabled, these bits set the maximum increase for SOH learning.                                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1%        | 1%           | 0% to 25.5%             |

|                                |                                                                                                                                             |          |     |                                                                         |                                       |                                                                                   |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|-------------------------------------------------------------------------|---------------------------------------|-----------------------------------------------------------------------------------|
| SOH_LRN_DMAX,<br>0x14C1        | If SOH_LRN_EN is enabled, these bits set the maximum increase for SOH learning.                                                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1%                                    | 1%                                    | 0% to 25.5%                                                                       |
| SOH_LRN_DMIN,<br>0x14C2        | If SOH_LRN_EN is enabled, these bits set the maximum decrease for SOH learning.                                                             | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1%                                    | 1%                                    | 0% to 25.5%                                                                       |
| SOH_LRN_MAX,<br>0x14C3         | If SOH_LRN_EN is enabled, these bits set the maximum value for SOH learning.                                                                | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1%                                      | 110%                                  | 100% to 200%                                                                      |
| SOH_LRN_MIN,<br>0x14C4         | If SOH_LRN_EN is enabled, these bits set the minimum value for SOH learning.                                                                | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1%                                      | 80%                                   | 0% to 100%                                                                        |
| SOH_LRN_TMAX,<br>0x14C5        | If SOH_LRN_EN is enabled, these bits set the maximum temperature for SOH learning                                                           | 8, [7:0] | R/W | 8-bit signed, 2-comp integer<br>LSB = 1°C                               | 30°C                                  | -128°C to +127°C                                                                  |
| SOH_LRN_TMIN,<br>0x14C6        | If SOH_LRN_EN is enabled, these bits set the minimum temperature for SOH learning                                                           | 8, [7:0] | R/W | 8-bit signed, 2-comp integer<br>LSB = 1°C                               | 10°C                                  | -128°C to +127°C                                                                  |
| SOH_LRN_IMIN,<br>0x14C7        | If SOH_LRN_EN is enabled, these bits set the minimum current for SOH learning.                                                              | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate                             | 0.1 C-rate                            | 0 C-rate to 2.55 C-rate                                                           |
| SOH_LRN_IMAX,<br>0x14C8        | If SOH_LRN_EN is enabled, these bits set the maximum current for SOH learning.                                                              | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate                             | 2 C-rate                              | 0 C-rate to 2.55 C-rate                                                           |
| RESR_LRN_DITH,<br>0x1540       | Sets the minimum current variation for equivalent series resistance learning.                                                               | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate/s                           | 0.5 C-rate/s                          | 0 C-rate/s to 2.55 C-rate/s                                                       |
| RESR_LRN_DRSTD,<br>0x1541      | Sets the maximum (standard) resistance variation for ESR learning.                                                                          | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1%                                    | 2.5%                                  | 0% to 25.5%                                                                       |
| RESR_LRN_DR_EXT,<br>0x1542     | Sets the maximum (extended) resistance variation for ESR learning.                                                                          | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1 %                                   | 10%                                   | 0% to 25.5%                                                                       |
| RESR_LRN_NHI_T2EXT,<br>0x1543  | Sets the number of times the standard resistance variation must be reached before using the extended resistance variation for ESR learning. | 4, [3:0] | R/W | 8-bit unsigned integer<br>LSB = 1                                       | 4                                     | 0 to 8                                                                            |
| RCXN_CELLS_LRN_NAVG,<br>0x1580 | Sets the number of events required for pack connection resistance learning.                                                                 | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1 event                                 | 100 event(s)                          | 1 to 255 event(s)                                                                 |
| RCXN_CELLS_LRN_DITH,<br>0x1581 | Sets the current derivative threshold for pack connection resistance learning.                                                              | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01 C-rate/s                           | 0.5 C-rate/s                          | 0 to 2.55 C-rate/s                                                                |
| RCXN_CELLS_LRN_RMIN,<br>0x1582 | Sets the minimum resistance for pack connection resistance learning.                                                                        | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1mΩ                                     | 0mΩ                                   | 0mΩ to 255mΩ                                                                      |
| RCXN_CELLS_LRN_RMAX,<br>0x1583 | Sets the maximum resistance for pack connection resistance learning.                                                                        | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1mΩ                                     | 20mΩ                                  | 0mΩ to 255mΩ                                                                      |
| HCONV_LRN_K,<br>0x15C0         | Sets the heat transfer coefficient gain.                                                                                                    | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1W/(m <sup>2</sup> × K <sup>2</sup> ) | 1W/(m <sup>2</sup> × K <sup>2</sup> ) | 0W/(m <sup>2</sup> × K <sup>2</sup> ) to 25.5W/(m <sup>2</sup> × K <sup>2</sup> ) |
| HCONV_LRN_RNG,<br>0x15C1       | Sets the heat transfer coefficient range.                                                                                                   | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.5%                                    | 10%                                   | 0% to 100%                                                                        |
| HCONV_LRN_DTIMETH,<br>0x15C2   | Sets the heat transfer coefficient learning time derivative threshold.                                                                      | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 1s                                      | 10s                                   | 0s to 255s                                                                        |

|                                 |                                                                               |          |     |                                        |       |               |
|---------------------------------|-------------------------------------------------------------------------------|----------|-----|----------------------------------------|-------|---------------|
| HCONV_LRN_<br>DTEMPH,<br>0x15C3 | Sets the heat transfer coefficient learning temperature derivative threshold. | 8, [7:0] | R/W | 8-bit unsigned integer<br>LSB = 0.01°C | 0.2°C | 0°C to 2.55°C |
|---------------------------------|-------------------------------------------------------------------------------|----------|-----|----------------------------------------|-------|---------------|

## Fuel Gauge Model

| Name, Address                   | Description                                                                                 | Bit Length, Position | Type | Encoding                                          | Decoded Default Value | Range                                    |
|---------------------------------|---------------------------------------------------------------------------------------------|----------------------|------|---------------------------------------------------|-----------------------|------------------------------------------|
| MDLCELL_MFR,<br>0x2000          | Sets the cell manufacturer.                                                                 | 128, [127:0]         | R/W  | ASCII character(s)                                | Default               | -                                        |
| MDLCELL_<br>TYPE,<br>0x2010     | Sets the cell type model.                                                                   | 128, [127:0]         | R/W  | ASCII character(s)                                | Default               | -                                        |
| MDLCELL_<br>QNOM,<br>0x2020     | Sets the nominal capacity of the cell, which is reported by the manufacturer.               | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 5mAh             | 2500mAh               | 5mAh to 32767mAh                         |
| MDLCELL_CP,<br>0x2028           | Sets the cell's specific heat.                                                              | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.001J/(g x K)   | 0.85J/(g x K)         | 0.001J/(g x K) to 65.535J/(g x K)        |
| MDLCELL_<br>MASS,<br>0x202A     | Sets the cell mass.                                                                         | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.5g             | 45g                   | 0.5g to 32767.5g                         |
| MDLCELL_<br>AREA,<br>0x202C     | Sets the cell surface area.                                                                 | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 5mm <sup>2</sup> | 4262mm <sup>2</sup>   | 1mm <sup>2</sup> to 32767mm <sup>2</sup> |
| MDLINFO_<br>ICHG_MAX,<br>0x2098 | Sets the maximum charge current that the cell can handle, according to the manufacturer.    | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.001 C-rate     | 1 C-rate              | 0 C-rate to 65.535 C-rate                |
| MDLINFO_<br>IDIS_MAX,<br>0x209A | Sets the maximum discharge current that the cell can handle, according to the manufacturer. | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 0.001 C-rate     | 2 C-rate              | 0 C-rate to 65.535 C-rate                |
| MDLINFO_<br>TCHG_MIN,<br>0x209C | Sets the minimum temperature that the cell can handle, according to the manufacturer.       | 8, [7:0]             | R/W  | 8-bit unsigned integer<br>LSB = 0.5°C             | 0°C                   | -30°C to +97.5°C                         |
| MDLINFO_<br>TCHG_MAX,<br>0x209D | Sets the maximum temperature that the cell can handle, according to the manufacturer.       | 8, [7:0]             | R/W  | 8-bit unsigned integer<br>LSB = 0.5°C             | 50°C                  | -30°C to +97.5°C                         |
| MDLINFO_<br>QMEAS,<br>0x20A0    | Sets the capacity measured in the cell characterization test.                               | 16, [15:0]           | R/W  | 16-bit unsigned integer<br>LSB = 5mAh             | 2437mAh               | 5mAh to 32767mAh                         |

## LED Settings

| Name, Address              | Description                                                                                                                                                                                                                             | Bit Length, Position | Type | Encoding                             | Decoded Default Value | Range  |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|--------------------------------------|-----------------------|--------|
| LEDS_ON_<br>MAN,<br>0x4000 | 1: The LEDs are controlled manually using the dedicated register bits<br>0: The LEDs are directly controlled to report the SOC                                                                                                          | 1, [0]               | R/W  | Control<br>Enable = 1<br>Disable = 0 | 0                     | 0 to 1 |
| LEDS_ON_<br>CHG,<br>0x4000 | 1: The LEDs display the pack SOC while charging, if the manual LED controls are set to 0<br>0: The LEDs do not display the pack SOC while the charging and manual LED controls are set to 0                                             | 1, [1]               | R/W  | Control<br>Enable = 1<br>Disable = 0 | 1                     | 0 to 1 |
| LEDS_ON_BTN,<br>0x4000     | 1: The LEDs display the pack SOC after the LED push-button is pressed if the manual LED controls are set to 0<br>0: The LEDs do not display the pack SOC after the LEDs push-button is pressed and the manual LED controls are set to 0 | 1, [2]               | R/W  | Control<br>Enable = 1<br>Disable = 0 | 1                     | 0 to 1 |
| LED1_ON,<br>0x4000         | 1: If manual LED control is set to 1 the LED turns on<br>0: If manual LED control is set to 1 the LED turns off                                                                                                                         | 1, [3]               | R/W  | Control<br>On = 1<br>Off = 0         | 0                     | 0 to 1 |

|                         |                                                                                                                   |          |     |                                                   |    |             |
|-------------------------|-------------------------------------------------------------------------------------------------------------------|----------|-----|---------------------------------------------------|----|-------------|
| LED2_ON,<br>0x4000      | 1: If manual LED control is set to 1 the LED turns on<br>0: If manual LED control is set to 1 the LED turns off   | 1, [4]   | R/W | Control<br>On = 1<br>Off = 0                      | 0  | 0 to 1      |
| LED3_ON,<br>0x4000      | 1: If manual LED control is set to 1 the LED turns on<br>0: If manual LED control is set to 1 the LED turns off   | 1, [5]   | R/W | Control<br>On = 1<br>Off = 0                      | 0  | 0 to 1      |
| LED4_ON,<br>0x4000      | 1: If manual LED control is set to 1 the LED turns on<br>0: If manual LED control is set to 1 the LED turns off   | 1, [6]   | R/W | Control<br>On = 1<br>Off = 0                      | 0  | 0 to 1      |
| LED5_ON,<br>0x4000      | 1: If manual LED control is set to 1 the LED turns on<br>0: If manual LED control is set to 1 the LED turns off   | 1, [7]   | R/W | Control<br>On = 1<br>Off = 0                      | 0  | 0 to 1      |
| LED_TRANS,<br>0x4001    | Sets the deglitch time to control when the LED turns on/off upon transitioning between charge and discharge mode. | 7, [6:0] | R/W | 8-bit unsigned integer<br>LSB = 0.1s              | 4s | 0s to 12.7s |
| LEDS_ON_TIME,<br>0x4002 | Sets the time during which the LEDs are on after pressing the LED push-button.                                    | 4, [3:0] | R/W | 8-bit unsigned integer<br>LSB = 1s<br>Offset = 1s | 5s | 1s to 16s   |

### I<sup>2</sup>C Settings and Info

| Name, Address           | Description                                                                                                                                                                                                                                                                                                                                                                      | Bit Length, Position | Type      | Encoding                             | Decoded Default Value | Range    |
|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------|--------------------------------------|-----------------------|----------|
| I2C_ADDRESS,<br>0x4100  | Selects the slave I <sup>2</sup> C address of the device.                                                                                                                                                                                                                                                                                                                        | 7, [6:0]             | R/W       | 8-bit unsigned integer<br>LSB = 1    | 8                     | 0 to 127 |
| I2C_CRC_EN,<br>0x4100   | 1: Enable CRC for I <sup>2</sup> C communication. Only write commands with the correct CRC are accepted. The response after a read command includes the 4 CRC bytes at the end<br>0: Disable CRC for I <sup>2</sup> C communication. Write commands with no CRC bytes (or with the correct CRC) are accepted. The response after a read command does not include the 4 CRC bytes | 1, [7]               | R/W       | Control<br>Enable = 1<br>Disable = 0 | 1                     | 0 to 1   |
| I2C_CHANNEL,<br>0x4200  | This RO register returns to the master, and the I <sup>2</sup> C channel is used for the current transaction.<br>1: The master is connected to the secondary I <sup>2</sup> C channel<br>0: The master is connected to the primary I <sup>2</sup> C channel                                                                                                                      | 1, [0]               | Read-only | Boolean true/false                   | 0                     | 0 to 1   |
| I2C_CHAN_SEL,<br>0x4200 | Returns the state of the I2C_SEL pin, which determines the selected I <sup>2</sup> C channel to accept write operations.<br>1: The secondary I <sup>2</sup> C channel is selected for write operations<br>0: The primary I <sup>2</sup> C channel is selected for write operations                                                                                               | 1, [1]               | Read-only | Boolean true/false                   | 0                     | 0 to 1   |

**Customer Block**

| Name, Address                      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Bit Length, Position | Type | Encoding                             | Decoded Default Value | Range           |
|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|--------------------------------------|-----------------------|-----------------|
| CUST_BLOCK_PASSWORD,<br>0x5000     | <p>Sets the password to allow editing to the customer block feature. To set a new password, write a value to this register while in configuration mode when CUST_BLOCK_PASS_EDIT_EN = 1. After the new password is set, CUST_BLOCK_PASS_EDIT_EN resets to 0. When writing a new value for the password, only the four password bytes must be written, so the address used must be 0x5000, and the data length must be 4. Users must exit configuration mode for the new password to be stored in the fuel gauge's NVM.</p> <p>To enable the customer block feature or the editing of the password, send a write command to address 0x5000 with a data length of 3. This command should contain the correct password and the correct values for CUST_BLOCK_EN and CUST_BLOCK_PASS_EDIT_EN.</p> <p>The content of this register can only be read when CUST_BLOCK_FLAG = 0.</p> <p>This register can only be written when CONFIG_MODE_FLAG = 1.</p> | 32, [31:0]           | R/W  | 32-bit unsigned integer<br>LSB = 1   | 4294967295            | 0 to 4294967295 |
| CUST_BLOCK_EN,<br>0x5004           | <p>Enables the customer block feature. To enable the customer block feature, send a write command to address 0x5000, with a data length of 5. This command should contain the correct password, and the correct value for this register must be sent.</p> <p>The CUST_BLOCK_FLAG flag is a mirror of this register.</p> <p>The content of this register can only be read when CUST_BLOCK_FLAG = 0.</p> <p>This register can only be written when CONFIG_MODE_FLAG = 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 1, [0]               | R/W  | Control<br>Enable = 1<br>Disable = 0 | 0                     | 0 to 1          |
| CUST_BLOCK_PASS_EDIT_EN,<br>0x5004 | <p>Enables customer block password editing. To enable the customer block feature, send a write command to address 0x5000, with a data length of 5. This command should contain the correct password, and the correct value for this register must be sent.</p> <p>This register can only be set when CUST_BLOCK_FLAG = 0; otherwise, it stays at 0.</p> <p>The content of this register can only be read when CUST_BLOCK_FLAG = 0.</p> <p>This register can only be written when CONFIG_MODE_FLAG = 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                       | 1, [1]               | R/W  | Control<br>Enable = 1<br>Disable = 0 | 0                     | 0 to 1          |

## IC Version

| Name, Address              | Description                                                                                                                                                                                                                                                                        | Bit Length, Position | Type      | Encoding           | Decoded Default Value | Range |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------|--------------------|-----------------------|-------|
| IC_VER,<br>0x6100          | Returns the IC version.<br><br>42790: 2 to 16 cells in series with LED support<br>42792: 2 to 16 cells in series cells<br>42795: 2 to 10 cells with LED support<br>42797: 2S to 10 in series cells<br>42791: 2 to 16 cells in series with resistance detection and a thermal model | 40, [39:0]           | Read-only | ASCII character(s) | 42791                 | -     |
| SP_CSTR_REQ_VER,<br>0x6109 | Returns the optional special request from the costumer.                                                                                                                                                                                                                            | 32, [31:0]           | Read-only | ASCII character(s) | 0000                  | -     |

## Commands

| Name, Address                  | Description                                                                                                                                                                                                                                                                                                                             | Bit Length, Position | Type       | Encoding                                      | Decoded Default Value | Range    |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------|-----------------------------------------------|-----------------------|----------|
| RST_CMD,<br>0x7FFF             | Resets the fuel gauge calculations.<br><br>0x01: Reset the fuel gauge. This is a self-clearing function                                                                                                                                                                                                                                 | 8, [7:0]             | Write-only | Active high command<br>1 = execute<br>LSB = 1 | 0                     | 0 to 255 |
| EXE_CMD,<br>0x7FFE             | Triggers the fuel gauge calculations. The system MCU is responsible for periodically writing this register to trigger an SOC update. This function should be triggered after providing all the updated voltage and current readings that are used to produce the updated SOC estimate.<br><br>0x01: Trigger a fuel gauge update refresh | 8, [7:0]             | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0                     | 0 to 255 |
| EDIT_CONFIG_CMD,<br>0x7FFD     | 0x01: The fuel gauge settings can be edited                                                                                                                                                                                                                                                                                             | 8, [7:0]             | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0                     | 0 to 255 |
| END_EDIT_CONFIG_CMD,<br>0x7FFC | 0x01: The fuel gauge settings cannot be edited                                                                                                                                                                                                                                                                                          | 8, [7:0]             | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0                     | 0 to 255 |
| CONFIG_MODE_CMD,<br>0x7FFB     | Directs the fuel gauge to enter configuration mode (cell profile, battery pack, and algorithm tuning).<br><br>0x01: Enter configuration mode                                                                                                                                                                                            | 8, [7:0]             | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0                     | 0 to 255 |
| CONFIG_EXIT_CMD,<br>0x7FFA     | Directs the fuel gauge to exit configuration mode (saves configuration values to flash) and reset. If not in configuration mode, the device stores the fuel gauge and LED settings from the volatile memory to the NVM.<br><br>0x01: Exit configuration mode. The new configuration is stored in the NVM                                | 8, [7:0]             | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0                     | 0 to 255 |

|                               |                                                                                                                                                                                     |          |            |                                               |   |          |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------|-----------------------------------------------|---|----------|
| CONFIG_<br>RST_CMD,<br>0x7FF9 | The configuration values are re-initialized to the default values and the fuel gauge calculations are reset.<br><br>0x01: Reset the configuration. This is a self-clearing function | 8, [7:0] | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0 | 0 to 255 |
| LOG_RST_<br>CMD,<br>0x7FF8    | Re-initializes lifetime logging.<br><br>0x01: Re-initialize the lifetime log registers. This is a self-clearing function                                                            | 8, [7:0] | Write-only | Active high command<br>1 = Execute<br>LSB = 1 | 0 | 0 to 255 |

## APPLICATION INFORMATION

### CORE ALGORITHM

The fuel gauge core algorithm accurately estimates core cell-level and pack-level parameters. These core parameters can be found in the Fuel Gauge Output register map.

#### **Cell Mathematical Model**

Cell dynamics are influenced by multiple factors, such as chemistry, SOC, current, and temperature. A mathematical model that captures the cell's most important dynamics is required to accurately measure internal variables.

Cell mathematical models are provided by MPS. These models are either from a database or they are a result of the cell characterization routine.

#### **Cell State-of-Charge (SOC)**

Cell SOC (SOC\_ABS\_CELLx) refers to the cell capacity that is currently available, as a function of the rated capacity. SOC is an unknown, internal variable that cannot be directly measured, meaning it must be estimated using available measurements. The MPF42791 uses voltage, current, and temperature measurements observed over time to produce accurate SOC estimates across a wide range of operating conditions.

#### **Empty State-of-Charge (SOC)**

Empty SOC (EMPTY\_SOC\_CELLx) refers to the SOC level at which the battery pack is unable to discharge further without reaching the voltage cutoff limits defined in VPACK\_EMPTY. The empty SOC prediction relies on the operating conditions of the different cells, as well as the discharge current supplied to the load, which is specific to each application.

In addition, the MPF42791 can predict whether the battery pack discharge is limited by the pack or one of the cells (the cell ID is provided). This is extremely important for accurate empty SOC estimation in unbalanced packs, since the fuel gauge must track the condition that limits the battery pack discharge.

#### **Full State-of-Charge (SOC)**

Full SOC (FULL\_SOC\_CELLx) refers to the SOC level at which the battery pack is unable to charge further without leaving the safe operating

area (SOA). The full SOC prediction relies on the operating conditions of the different cells, as well as the constant-current/constant-voltage (CC/CV) charging sequence, which is specific to each application.

The MPF42791 can predict whether the battery pack charge is limited by the pack or one of the cells (the cell ID is provided). This is extremely important for accurate full SOC estimation in unbalanced packs, since the fuel gauge must track the condition that limits the battery pack charge.

#### **Thermal Modeling**

The MPF42791 incorporates battery thermal modeling, which is extremely important to account for battery self-heating.

The internal resistance of each cell causes the cell's temperature to rise during charge and discharge due to the Joule heating effect. As temperature of cells increases, internal resistance decreases and this can dramatically impact performance, especially at low temperatures.

The ability to predict this temperature rise allows the fuel gauge to determine state-of-charge more accurately.

#### **Pack State-of-Charge (SOC)**

Pack SOC (SOC\_PACK) provides the capacity, which is a function of the available capacity given the actual pack operating conditions. Pack SOC relies on cell-level quantities and tracks the remaining capacity that the battery can charge or discharge without reaching the cutoff limits.

Pack SOC can be considered the most vital estimate since it is typically the value shown to the application end user.

#### **Pack Unavailable State-of-Charge (SOC)**

Pack unavailable SOC (SOC\_PACK\_UNAVBL) refers to the capacity that is not available due to the actual pack operating conditions (e.g. mismatched cells and battery pack configurations). Pack unavailable SOC provides the capacity that the battery cannot use without violating the defined SOA.

## INDICATORS

In addition to the core parameters, an extensive set of fuel gauge indicators are provided, based on the internal battery estimates. These indicators can be found in the Fuel Gauge Output register map.

### ***Remaining Time-to-Empty***

Remaining time-to-empty (EMTY\_RUNTIME) refers to how much time is left until the battery pack reaches the empty state while assuming the application-specific discharge current. This estimate informs the user of the remaining runtime until the pack reaches 0% SOC.

### ***Remaining Time-to-Full***

Remaining time-to-full (FULL\_RUNTIME) refers to how much time is left until the battery pack reaches the cutoff limits using the application-specific charge parameters (i.e., the CC and CV levels). This estimate informs the user of the remaining charge time until the pack reaches 100% SOC.

### ***Maximum Discharge Power***

The maximum discharge power (PDIS) refers to how much power the pack can deliver to the load without reaching the pack empty levels and leaving the SOA.

The MPF42791 can predict whether the limiting factor under the maximum discharge power is caused by the pack or one of the cells (the cell ID is provided).

### ***Maximum Charge Power***

The maximum charge power (PCHG) refers to how much power the pack can accept for charging without breaching the cutoff limits.

The MPF42791 can predict whether the limiting factor under the maximum charge power is caused by the pack or one of the cells (the cell ID is provided).

## LEARNINGS

The MPF42791 includes the ability to learn and adjust key fuel gauge parameters, allowing for autonomous fine-tuning of the algorithm. This also provides a method to account for aging to keep estimates accurate across the device's lifetime.

### ***Charge Constant Current (CC)***

The charge CC learning feature (ICHG\_CC\_LRN) refines the initial charge CC value defined by the user. This smart adjustment compensates for when the charge CC deviates from its nominal settings, such as when there are production tolerances to the charging system. This feature minimizes the need for tuning while maintaining optimal SOC accuracy. The learning can be completed and leveraged within the same charge cycle.

### ***Charge Termination Current***

The charge termination current learning (ICHG\_END\_LRN) feature refines the initial charge termination current value defined by the user. This smart adjustment compensates for when the charge termination current deviates from its nominal settings, such as when there are production tolerances to the charging system.

Charge termination current smart adjustments are applied in subsequent charge cycles following the cycle in which the learning occurred.

### ***Charge Constant Voltage (CV)***

The charge CV learning feature (VCHG\_CV\_LRN) refines the initial charge CV value defined by the user. This smart adjustment compensates for when the charge CV deviates from its nominal settings, such as production tolerances to the charging system. Charge CV smart adjustments are applied in subsequent charge cycles following the cycle in which the learning occurred.

### ***Discharge Average Current***

The discharge average current learning (IDIS\_AVG\_LRN) feature calculates the load average discharge current to accurately provide the time-to-empty estimate.

### ***Discharge Termination Current***

The discharge termination current learning (IDIS\_END\_LRN) feature refines the initial discharge termination current value defined by the user. This value adapts to load dynamics and keeps the SOC accurate with minimal user tuning.

In addition, this feature includes two different operation modes depending on the application requirements: continuous and past-cycle

learning. In continuous learning mode, the discharge termination current updates continuously while the pack discharges to accurately determine the empty SOC. Past-cycle learning uses the previous discharge cycle data to learn. Continuous learning is recommended for unpredictable discharge termination currents, whereas past-cycle learning is recommended for consistent discharge termination currents.

### **State-of-Health (SOH)**

As battery cells age, their total capacity decreases due to unwanted side reactions and structural deterioration (often referred to as capacity fading). Up-to-date state-of-health (SOH) information is important since it has a major impact on the battery pack's available energy.

The MPF42791 incorporates an SOH learning (SOH\_LRN) feature that can track individual cells' capacities (SOH\_CELLx) with respect to their nominal capacity. This feature can identify cells that are negatively impacting the overall pack performance.

### **Equivalent Series Resistance (ESR)**

As battery cells age, their equivalent series resistance (ESR) increases due to unwanted side reactions and structural deterioration (often referred to as power fading). Up-to-date ESR information is important since it has a major impact on the battery pack's available power and SOC estimates.

The MPF42791 incorporates an ESR learning (RESR\_LRN) feature that tracks individual cells' ESR (RESR\_CELL\_DIS\_x) with respect to their characterized value. This feature can identify cells that are negatively impacting the overall pack performance.

### **LIFETIME LOG SOC**

Important events and certain conditions are reported in the lifetime log to gain insight on how the battery pack has been operating. The MPF42791 backs the relevant registers up to its non-volatile memory (NVM) every time the part enters disabled mode (or for each elapsed hour).

### **Count Log**

The count log is the number of times the pack has been charged from below 15% to above 85%. The number of times the pack has been charged by 10% and the number of shutdowns are also reported in the lifetime log. Full shutdowns and entering disabled mode are considered shutdowns, and increase the counter.

### **Current Log**

The current log is the maximum charge and discharge current that has been applied to the pack. It is reported in the lifetime log.

### **Voltage Log**

The voltage log tracks the maximum and minimum voltage for each cell. This is reported in the lifetime log. In addition, the maximum cell voltage difference between two cells is also reported, as well as their corresponding cell IDs.

### **Temperature Log**

The temperature log tracks the maximum and minimum temperature sensed on the pack. It also reports the maximum temperature difference between two sensors, and their corresponding temperature sensor IDs.

The lifetime log details how much time the pack has operated under different temperature ranges.

### **Balancing Log**

The balancing log tracks the number of times each cell has been balanced.

### **PCB Layout Guidelines**

Place the bypass capacitor between each pair of VDD and GND pins, and as close as possible to the pin.

# TYPICAL APPLICATION CIRCUIT

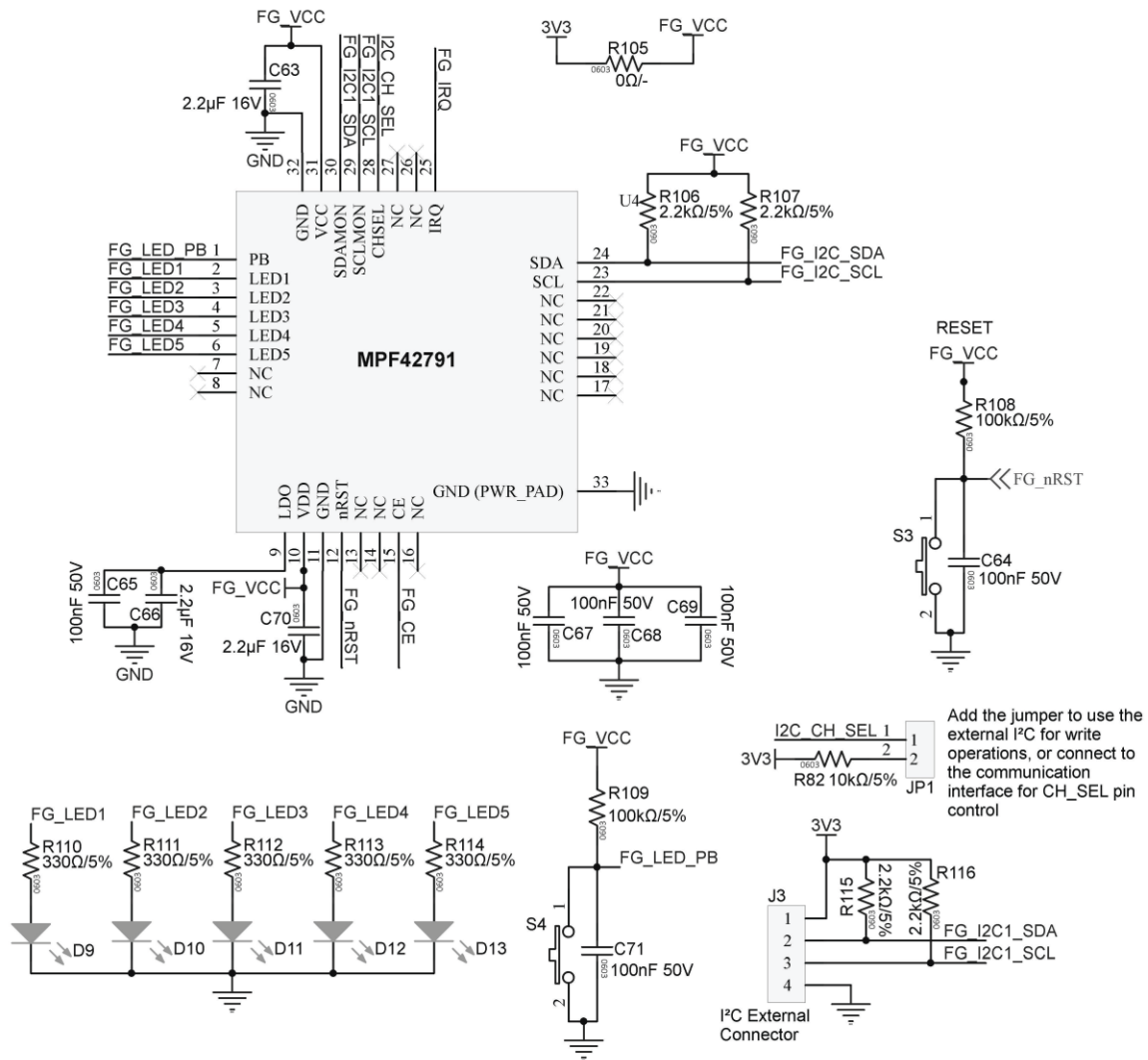
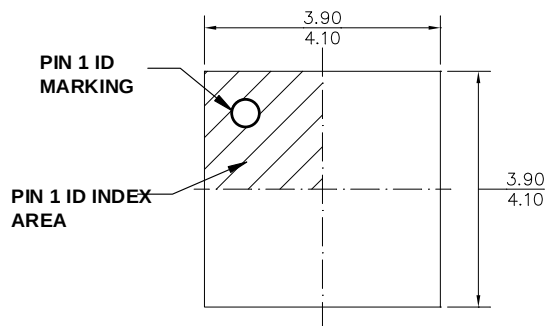


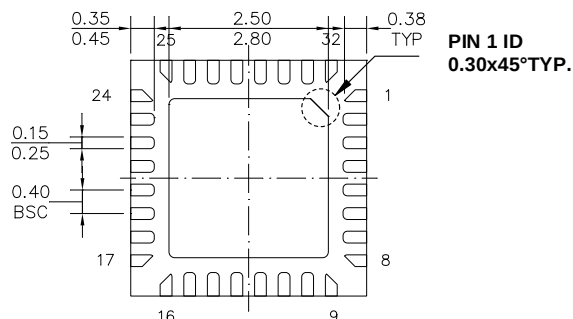
Figure 12: Typical Application Circuit

# PACKAGE INFORMATION

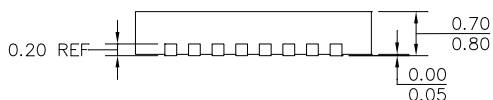
## TQFN-32 (4mmx4mm)



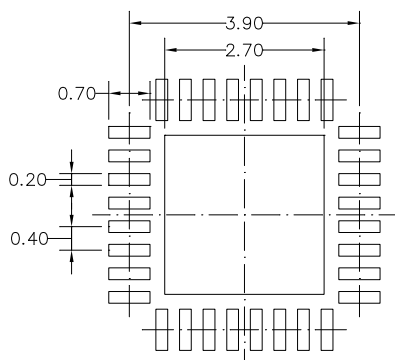
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

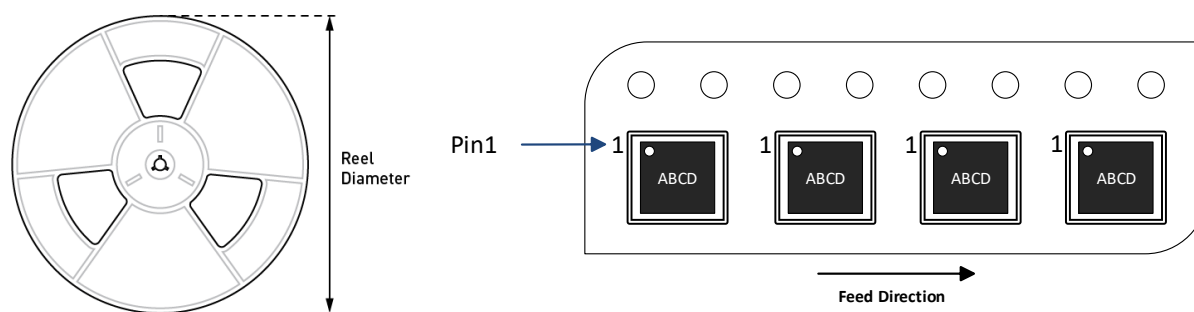


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number               | Package Description  | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---------------------------|----------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MPF42791DRT-0B-<br>yyyy-Z | TQFN-32<br>(4mmx4mm) | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/19/2022     | Initial Release | -             |

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