

DESCRIPTION

The MP6613 is an H-bridge motor driver IC designed to drive stepper motors, brushed DC motors, and other loads.

The MP6613 operates across a 4.5V to 45V input voltage (V_{IN}) range. It can deliver motor current up to 5A, depending on the ambient temperature (T_A) and PCB layout.

Internal safety and diagnostic features include over-current protection (OCP), input overvoltage protection (OVP), input under-voltage protection (UVP), and thermal shutdown.

The MP6613 has several control modes that are configurable via pins. The MP6613 is available in QFN-28 (4mmx5mm) and TSSOP-28EP packages.

FEATURES

- 4.5V to 45V Operating Input Voltage (V_{IN}) Range
- 5A Maximum Output Current (I_{OUT_MAX})
- Single H-Bridge Driver
- Low 75m Ω On Resistance (R_{DS(ON)}) per MOSFET
- Protection Functions Include:
 - Over-Current Protection (OCP)
 - Over-Voltage Protection (OVP)
 - Under-Voltage Protection (UVP)
 - Over-Temperature (OT) Shutdown
 - Fault Indication Output
- Available in QFN-28 (4mmx5mm) and TSSOP-28EP Packages

APPLICATIONS

- Bipolar Stepper Motors
- Stage Lighting
- 3D Printers
- Laser Printers and Copiers
- Textile Machines

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6613GV	QFN-28 (4mmx5mm)	See Below	2
MP6613GF	TSSOP-28EP	See Below	2a

* For Tape & Reel, add suffix -Z (e.g. MP6613GV-Z).

* For Tape & Reel, add suffix -Z (e.g. MP6613GF-Z).

TOP MARKING (MP6613GV) MPSYWW MP6613 LLLLLL

MPS: MPS prefix Y: Year code WW: Week code MP6613: Part number LLLLL: Lot number

TOP MARKING (MP6613GF) MPSYYWW MP6613 LLLLLLLL

MPS: MPS prefix YY: Year code WW: Week code MP6613: Part number LLLLLLL: Lot number



PACKAGE REFERENCE



PIN FUNCTIONS

Pin # (QFN)	Pin # (TSSOP)	Name	Description
1, 8	4, 11	VIN	Input supply voltage. Decouple the VIN pin to ground using a minimum 100nF ceramic capacitor. Additional bulk capacitance may be required.
2, 7	5, 10	OUT1	Bridge output terminal 1. Connect the OUT1 pins together on the PCB.
3, 6	6, 9	PGND	Power ground for H-bridge outputs.
4, 5	7, 8	OUT2	Bridge output terminal 2. Connect the OUT2 pins together on the PCB.
11, 24	14, 28	GND	Ground.
12	15	VREG	Internal regulator. Connect a 1µF, 16V ceramic capacitor (X7R) to ground.
13	16	nRESET	Reset input. Pull the nRESET pin active low to reset the protection circuits and disable the outputs. This pin is pulled down internally.
14	17	nSLEEP	Sleep mode input. Pull the nSLEEP pin logic low to enter low-power sleep mode. This pin is pulled down internally.
15	18	nFAULT	Fault indication. The nFAULT pin is an open-drain output. During fault conditions, pull nFAULT logic low using an external pull-up resistor.
		IN2	Output 2 control input. If INM[1:0] = 00, this pin configures output 2's pulse- width modulation (PWM) input pin. Set the IN2 pin to 1 for output H.
16	20	PHASE	Phase node. If INM[1:0] = 01, this pin configures the H-bridge's DIR input pin. The PHASE pin sets the motor rotation direction.
		INH1	High-side (HS) output 1 control input. If INM[1:0] = 10, this pin configures output 1's HS input. Set the INH1 pin to 1 to enable HS output 1.
		IN1	Output 1 control input. If INM[1:0] = 00, this pin configures output 1's PWM input pin. Set the IN1 pin to 1 for output H.
17	21	ENBL	H-bridge enable input. If INM[1:0] = 01, this pin configures the H-bridge's enable input pin. Set the ENBL pin to 1 to enable the entire H-bridge.
		INL1	Low-side (LS) output 1 control input. If INM[1:0] = 10, this pin configures output 1's LS input. Set the INL1 pin to 1 to enable LS output 1.
		nEN2	Output 2 enable input. If INM[1:0] = 00, this pin configures output 2's enable input pin. Set the nEN2 pin to 0 to enable the input.
19	23	BRK	Brake. If INM[1:0] = 01, this pin configures the brake input. Set the BRK pin to 1 to allow the H-bridge to enter brake mode.
		INH2	HS output 2 control input. If INM[1:0] = 10, this pin configures output 2's HS input. Set the INH2 pin to 1 to enable HS output 2.
		nEN1	Output 1 enable input. If INM[1:0] = 00, this pin configures output 1's enable input pin. Set the nEN1 pin to 0 to enable the input.
20	24	BMOD	Brake mode. If INM[1:0] = 01, this pin configures the BMOD input. Set the BMOD pin to 1 for the HS brake; set BMOD to 0 for the LS brake.
		INL2	LS output 2 control input. If INM[1:0] = 10, this pin configures output 2's LS input. Set INL2 to 1 to enable LS output 2.
22	26	INM0	Input mode selection. If INM[1:0] = 00, this pin sets ENA/PWM as the input. If
23	27	INM1	INM[1:0] = 01, this pin sets PHASE/ENBL as the input. If INM[1:0] = 10, this pin sets HS/LS as the input.
25	2	CPA	Charge pump capacitor. Connect a 100nF ceramic capacitor (X7R) between
26	1	CPB	the CPA and CPB pins. This capacitor must be rated for at least V _{IN} .
27	3	VCP	Charge pump output. The VCP pin requires a 1μ F, 16V ceramic capacitor connected to VIN.



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V _{IN})	0.3V to +48V
OUTx voltage (Vout1, Vout2)	0.7V to +48V
VCP, CPB	V_{IN} to V_{IN} + 6.5V
PGND to GND	0.3V to +0.3V
All other pins to GND	0.3V to +6.5V
Continuous power dissipation (Γ _A = 25°C) ⁽²⁾
QFN-28 (4mmx5mm)	3.125W
TSSOP-28EP	3.9W
Storage temperature	-55°C to +150°C
Junction temperature	150°C
Lead temperature (solder)	260°C

ESD Ratings

Human body model (HE	BM) .	±2kV
Charged device model ((CDM)±	2kV

Recommended Operating Conditions ⁽³⁾

Supply voltage (VIN)	4.5V to 45V
PGND to GND	0.2V to +0.2V
Operating junction temp (T _J))40°C to +125°C

Thermal Resistance $^{(4)}$ θ_{JA} θ_{JC}

QFN-28 (4mmx5mm)	40	9	°C
TSSOP-28EP	32	6	°C

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-toambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, a 4-layer PCB.



ELECTRICAL CHARACTERISTICS

$V_{IN} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Тур	Max	Units	
Power Supply							
Input supply voltage	VIN		4.5		45	V	
Quiescent ourrent	I _{INQ}	nSLEEP = 1, with no load		2.8		mA	
	I _{INSLEEP}	nSLEEP = 0		0.9	10	μA	
Internal MOSFETs		-	_	-		-	
Output on registance	R _{DS(ON)_HS}	Ι _{ουτ} = 1Α, Τ _J = 25°C		67.5	85	mΩ	
Ouput on resistance	Rds(on)_ls	Ι _{ουτ} = 1Α, Τ _J = 25°C		75	92.5	mΩ	
Body diode forward voltage	VF	I _{OUT} = 1A			1.1	V	
Control Logic Inputs			_	-		-	
Logic-low input threshold	VIL				0.8	V	
Logic-high input threshold	VIH		2			V	
Logic input current	I _{IN_H}	$V_{IN} = 5V$	-100		+100	μA	
	I _{IN_L}	$V_{IN} = 0V$	-20		+20	μA	
Internal pull-down resistance	R _{PD}	To GND		100		kΩ	
nFAULT Output							
Output low voltage	V _{OUT_L}	I _{OUT} = 5mA			0.5	V	
Output high leakage current	lout_н	Vout = 5V			1	μA	
Protection Circuits				-			
V _{IN} under-voltage lockout (UVLO) rising threshold	V _{IN_ULVO_RISING}				4.5	V	
V _{IN} UVLO hysteresis	V _{IN_UVLO_HYS}			300		mV	
V _{IN} over-voltage protection (OVP) threshold	V _{OVP}		45		48	V	
Over-current (OC) trip level	I _{OCP1}	Sinking	6	9		A	
	I _{OCP2}	Sourcing	6	9		A	
OC deglitch time	t _{OCP}			1		μs	
Thermal shutdown	T _{TSD}			165		°C	
Thermal shutdown hysteresis	T _{TSD_HYS}			15		°C	



TYPICAL TIMIMG CHARACTERISTICS

 $V_{IN} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.



Figure 1: Timing Diagram

Parameter	Symbol	Condition	Min	Тур	Max	Units
INx high to OUTx high delay time	t1		40		360	ns
INx low to OUTx low delay time	t ₂		40		360	ns
Output rise time	t ₃		1		55	ns
Output fall time	t4		1		165	ns
Dead time					80	ns



TYPICAL CHARACTERISTICS







TYPICAL CHARACTERISTICS (continued)





TYPICAL PERFORMANCE CHARACTERISTICS

 V_{IN} = 24V, nSLEEP = 3.3V, INM[1:0] = 00, OUT1 switching with 20kHz frequency, OUT2 LS-FET on, T_A = 25°C, resistor + inductor load: 4 Ω + 1.5mH between OUT1 and OUT2, unless otherwise noted.







Start-Up through nENx





MP6613 Rev. 1.1 5/12/2023



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 V_{IN} = 24V, nSLEEP = 3.3V, INM[1:0] = 00, OUT1 switching with 20kHz frequency, OUT2 LS-FET on, T_A = 25°C, resistor + inductor load: 4 Ω + 1.5mH between OUT1 and OUT2, unless otherwise noted.



 CH1: VIN1
 Image: CH1: VIN1



FUNCTIONAL BLOCK DIAGRAM



Figure 2: Functional Block Diagram



OPERATION

The MP6613 is a general-purpose H-bridge motor driver designed to drive bipolar stepper motors, brushed DC motors, solenoids, and other loads. It integrates four N-channel power MOSFETs connected as a full H-bridge, with a 5A current capability. The device operates across a wide 4.5V to 45V supply input voltage (V_{IN}) range.

nSLEEP and **nRESET**

Pull the nSLEEP pin low to force the MP6613 to enter low-power sleep mode. In this mode, the gate drive charge pump stops, and all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

Once entering sleep mode, 600µs must pass before the motor can exit sleep mode. This allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

Pull the nRESET pin low to reset the latched protection features, including over-current protection (OCP) and over-voltage protection (OVP), as well as to disable the outputs to a high-impedance (Hi-Z) state.

Input Interface

The MP6613 contains a single full H-bridge or two half H-bridges that operate independently, depending on the configuration set by the INM1 and INM0 pins.

The two OUT1 pins and two OUT2 pins must be externally connected in parallel on the PCB. Three configurable input modes are available on the MP6613, allowing for several different control methods to be used. INM1 and INM0 configure the input interface. Table 2 shows the input logic when INM[1:0] = 00.

Table 2: Input Logic for INM[1:0] = 00⁽⁵⁾

nENx	INx	OUTx
L	Н	VIN
L	L	GND
Н	Х	Hi-Z

Note:

5) "X" means not applicable.

Table 3 shows the input logic when INM[1:0] = 01.

Table 3:	Input	Logic 1	for INM	[1:0] =	01	(6)
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ENBL	PHASE	BRK	BMOD	OUT1	OUT2
L	Х	Х	Х	Hi-Z	Hi-Z
Н	Х	Н	L	GND	GND
Н	Х	Н	Н	VIN	VIN
Н	L	L	Х	GND	VIN
Н	Н	L	Х	VIN	GND

Note:

6) "X" means not applicable.

Table 4 shows the input logic when INM[1:0] = 10.

Table 4: Input Logic for INM[1:0] = 10

INHx	INLx	OUTx
L	L	Hi-Z
L	Н	GND
Н	L	VIN
Н	Н	Hi-Z

Note that all logic inputs have weak, internal pull-down resistors.

Automatic Synchronous Rectification

If the output high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are turned off, then the recirculation current must continue to flow when driving current through an inductive load. This current is typically passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6613 implements automatic synchronous rectification.

If both the HS-FET and LS-FET are turned off and the voltage on an OUTx pin (V_{OUTx}) is pulled below ground, then the LS-FET turns on until the current flowing through it approaches 0A or the HS-FET turns on. Similarly, if V_{OUTx} exceeds V_{IN} , then the HS-FET turns on until the current approaches 0A or the LS-FET turns on.

Internal Supply Voltages (V_{REG} and V_{CP})

The internal regulators generate a 5V supply voltage (V_{REG}) for the low-side (LS) gate drive, and a supply exceeding V_{IN} by 5V (V_{CP}) for the high-side (HS) gate drive. These supplies require external capacitors.

The VREG pin requires a 1μ F ceramic capacitor connected to ground. The VCP pin requires a 1μ F ceramic capacitor connected to VIN. Both capacitors should be X7R ceramic



capacitors, and rated for a voltage of at least 16V.

Connect the charge pump flying capacitor between the CPA and CPB pins using a 100nF ceramic capacitor (X7R) that is rated for at least the maximum V_{IN} .

nFAULT

The MP6613 provides an nFAULT pin to report to the system if a fault condition such as OCP, OVP, or over-temperature protection (OTP) occurs. nFAULT is an open-drain output, and is pulled low during fault conditions. If used, nFAULT should be pulled high via an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the HS-FET and LS-FET by disabling the gate driver. If the over-current (OC) limit threshold is reached and lasts for longer than the OC deglitch time (t_{OCP}), then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low or by cycling the power on the MP6613. OC conditions on the HS and LS devices (e.g. an OC condition to ground, supply, or across a motor winding) all result in an OC shutdown.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the OVP threshold (V_{OVP}), then the H-bridge output is disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low or cycling the power on the MP6613.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the under-voltage lockout (UVLO) threshold (V_{IN_UVLO}), then all circuitry in the device is disabled and the internal logic resets. Once V_{IN} exceeds V_{IN_UVLO} , the device starts up again and resumes normal operation.

Thermal Shutdown

If the die temperature exceeds safe limits, then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. Once the die temperature returns to a safe level, the MP6613 automatically starts up again and resumes normal operation.



APPLICATION INFORMATION

Selecting the External Components

Bypass the two VIN pins to GND using a minimum 100nF ceramic capacitor with X7R dielectrics, placed as close to the IC as possible. Place an additional 1μ F to 10μ F ceramic capacitor close to the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN.

Connect a 100nF ceramic capacitor rated for V_{IN} between the CPA and CPB pins. Connect a 1µF, 16V ceramic capacitor between the VIN and VCP pins.

Connect a 1μ F, 16V ceramic capacitor with X7R dielectrics from the VREG pin to GND.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and Figure 4, and follow the guidelines below:

- 1. Place the supply bypass and charge pump capacitors as close to the IC as possible, ideally adjacent to the pins on the same PCB layer.
- 2. Each VIN pin requires a bypass capacitor.
- 3. Place as much copper on the long pads as possible.
- 4. Place large copper areas on the pads and the device's outer copper layer.
- 5. The thermal pad should be soldered directly to the copper on the PCB.
- 6. Add thermal vias to transfer heat to the other PCB layers.



Figure 3: Recommended PCB Layout (MP6613GF)



Figure 4: Recommended PCB Layout (MP6613GV)



TYPICAL APPLICATION CIRCUIT



Figure 5: Typical Application Circuit



PACKAGE INFORMATION



RECOMMENDED LAND PATTERN



PACKAGE INFORMATION (continued)



- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
- 6) DRAWING IS NOT TO SCALE.



CARRIER INFORMATION





Part Number	Package	Quantity/	Quantity/	Reel	Carrier	Carrier
	Description	Reel	Tube	Diameter	Tape Width	Tape Pitch
MP6613GV-Z	QFN-28 (4mmx5mm)	5000	N/A	13in	12mm	8mm



Part Number	Package	Quantity/	Quantity/	Reel	Carrier	Carrier
	Description	Reel	Tube	Diameter	Tape Width	Tape Pitch
MP6613GF-Z	TSSOP-28EP	2500	50	N/A	13in	16mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/19/2022	Initial Release	-
1.1	5/12/2023	Updated the MSL rating of the MP6613GV orderable SKU to "2" in the Ordering Information section	2

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