MP6604B

4.5V to 45V, 2.5A, Simple Dual H-Bridge Driver (PHASE/EN)

DESCRIPTION

The MP6604B is a dual H-bridge motor driver IC designed to drive stepper motors, brushed DC motors, and other loads.

The MP6604B operates across a 4.5V to 45V input voltage (V_{IN}) range. It can deliver an output current up to 2.5A per phase, depending on the ambient temperature (T_A) and PCB layout.

Internal safety and diagnostic features include over-current protection (OCP), input over-voltage protection (OVP), input under-voltage lockout (UVLO), and thermal shutdown.

The MP6604B has PHASE, ENBL, BRAKE, and BMOD input signals for each H-bridge.

The MP6604B is available in QFN-28 (4mmx5mm) and TSSOP-28EP packages.

FEATURES

- 4.5V to 45V Operating Input Voltage (V_{IN}) Range
- 2.5A Maximum Output Current (I_{OUT})
- Dual, Full H-Bridge Driver
- 150mΩ Low On Resistance per MOSFET
- Protection Functions Include:
  - Over-Current Protection (OCP)
  - Over-Voltage Protection (OVP)
  - Under-Voltage Lockout (UVLO)
  - Thermal Shutdown
  - Fault Indication Output
- Available in QFN-28 (4mmx5mm) and TSSOP-28EP Packages

APPLICATIONS

- Bipolar Stepper Motors
- Stage Lighting
- 3D Printers
- Laser Printers and Copiers
- Textile Machines

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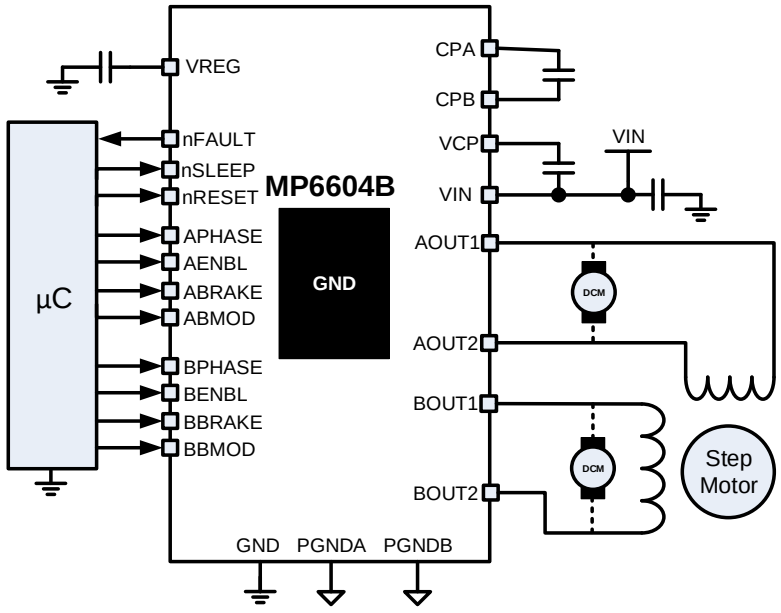
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6604BGV	QFN-28 (4mmx5mm)	*See Below*	2
MP6604BGF	TSSOP-28EP	*See Below*	2a

* For Tape & Reel, add suffix -Z (e.g. MP6604BGV-Z).

* For Tape & Reel, add suffix -Z (e.g. MP6604BGF-Z).

TOP MARKING (MP6604BGV)

MPSYWW
M6604B
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6604B: part number
LLLLLL: Lot number

TOP MARKING (MP6604BGF)

MPSYYWW
MP6604B
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6604B: part number
LLLLLLLLL: Lot number

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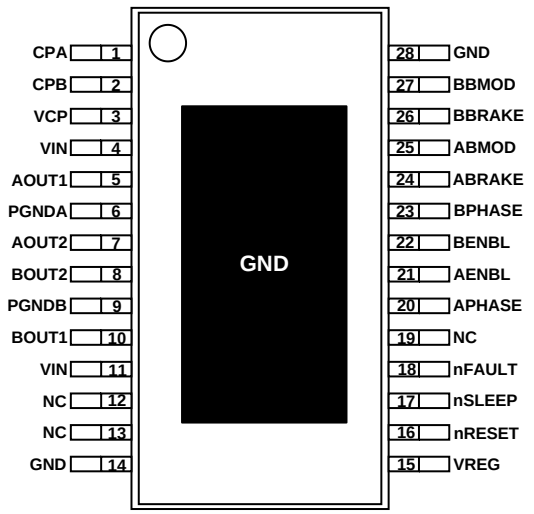
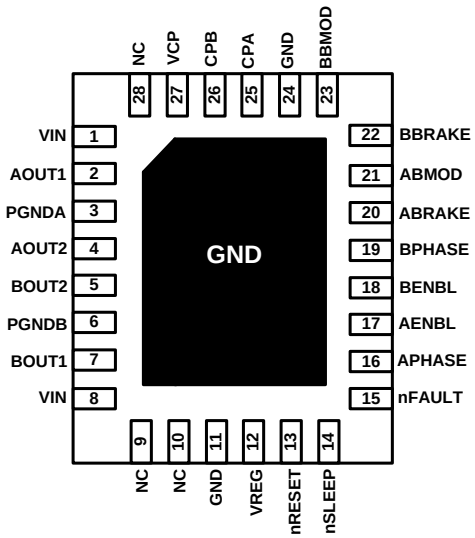
PACKAGE REFERENCE

TOP VIEW



MP6604BGF
TSSOP-28EP

TOP VIEW



MP6604BGV
QFN-28 (4mmx5mm)

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PIN FUNCTIONS

Pin # (QFN-28)	Pin # (TSSOP-28EP)	Name	Description
1, 8	4, 11	VIN	**Input supply voltage.** Decouple the VIN pin to ground using a minimum 100nF ceramic capacitor. Additional bulk capacitance may be required.
2	5	AOUT1	**Bridge A output terminal 1.**
3	6	PGNDA	**Power ground for the H-bridge A outputs.**
4	7	AOUT2	**Bridge A output terminal 2.**
5	8	BOUT2	**Bridge B output terminal 2.**
6	9	PGNDB	**Power ground for the H-bridge B outputs.**
7	10	BOUT1	**Bridge B output terminal 1.**
11, 24	14, 28	GND	**Signal ground.**
12	15	VREG	**Internal regulator.** Connect a 1µF, 16V ceramic capacitor (X7R) from the VREG pin to ground.
13	16	nRESET	**Reset input.** Pull the nRESET pin active low to reset the protection circuits and disable the outputs. This pin has an internal pull-down resistor.
14	17	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin logic low to enter low-power sleep mode. This pin has an internal pull-down resistor.
15	18	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. nFAULT requires an external pull-up resistor if it is used. If a fault occurs, nFAULT is pulled low.
16	20	APHASE	**H-bridge A's direction setting.** The APHASE pin is internally pulled down.
17	21	AENBL	**Enable H-bridge A.** Pull the AENBL pin to logic high to enable H-bridge A. The AENBL pin is internally pulled down.
18	22	BENBL	**Enable H-bridge B.** Pull the BENBL pin to logic high to enable H-bridge A. The BENBL pin is internally pulled down.
19	23	BPHASE	**H-bridge B's direction setting.** The BPHASE pin is internally pulled down.
20	24	ABRAKE	**Enable H-bridge A braking.** Pull the ABRAKE pin to logic high to enable braking on H-bride A. The ABRAKE pin is pulled down internally.
21	25	ABMOD	**Logic level for bridge A braking setting.** The ABMOD pin is pulled down internally.
22	26	BBRAKE	**Enable H-bridge B braking.** Pull the BBRAKE pin to logic high to enable braking on H-bride B. The BBRAKE pin is internally pulled down.
23	27	BBMOD	**Logic level for bridge B braking setting.** The ABMOD pin is pulled down internally.
25	1	CPA	**Charge pump capacitor.** Connect a 100nF ceramic capacitor rated for the VIN voltage between the CPA and CPB terminals.
26	2	CPB	
27	3	VCP	**Charge pump output.** Connect the VCP pin to VIN using a 1µF, 16V ceramic capacitor.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +48V
xOUTx voltage (V_{AOUT1}, V_{AOUT2}, V_{BOUT1}, V_{BOUT2})...
.....-0.7V to +48V
VCP, CPB .....V_{IN} to V_{IN} + 6.5V
PGNDx to GND.....-0.3V to +0.3V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28…….…… 3.125W
TSSOP-28EP……..3.9W
Storage temperature ..... -55°C to +150°C
Junction temperature .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM).....±2kV

Recommended Operating Conditions (3)

Supply Voltage (V_{IN}).....4.5V to 45V
PGNDx to GND.....-0.2V to +0.2V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm).....40.....9..... °C/W
TSSOP-28EP.....32.....6..... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5		45	V
Quiescent current	I_{INQ}	nSLEEP = 1, with no load		2.8		mA
	$I_{INSLEEP}$	nSLEEP = 0		0.9	10	µA
Internal MOSFETs						
Output on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_J = 25°C		135	170	mΩ
	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_J = 25°C		150	185	mΩ
Body diode forward voltage	V_F	I_{OUT} = 1A			1.1	V
Control Logic Inputs						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	I_{IN_H}	V_{IN} = 5V	-100		+100	µA
	I_{IN_L}	V_{IN} = 0V	-20		+20	µA
Internal pull-down resistance	R_{PD}	To GND		100		kΩ
nFAULT Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 5V			1	µA
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{UVLO}				4.5	V
V_{IN} UVLO hysteresis	ΔV_{UVLO}			300		mV
V_{IN} over-voltage protection (OVP) threshold	V_{OVP}		45		48	V
Over-current (OC) trip level	I_{OCP1}	Sinking	3	4.5		A
	I_{OCP2}	Sourcing	3	4.5		A
Over-current deglitch time	t_{OCP}			1		µs
Thermal shutdown temp.	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			15		°C

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TYPICAL TIMING CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Delay time from xBMOD high to xOUTx high	t1		40		360	ns
Delay time from xBMOD low to xOUTx low	t2		40		360	ns
Output rising time	t3		1		55	ns
Output falling time	t4		1		165	ns
Dead time					80	ns

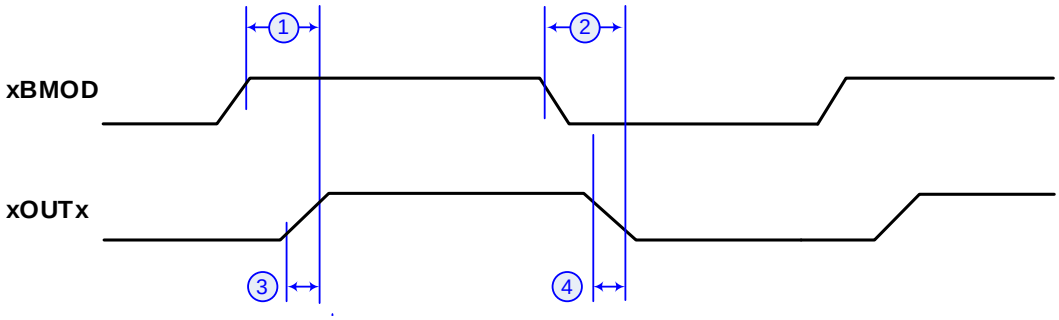

Figure 1: Timing Diagram

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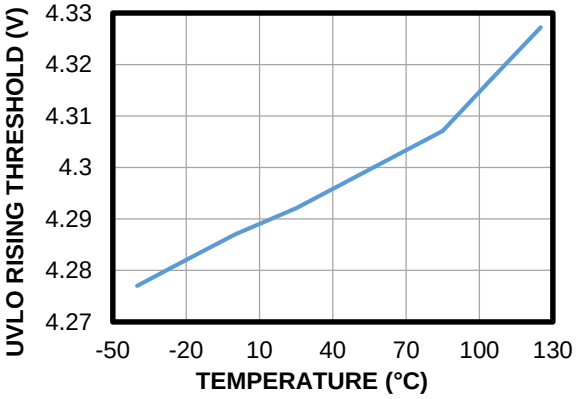
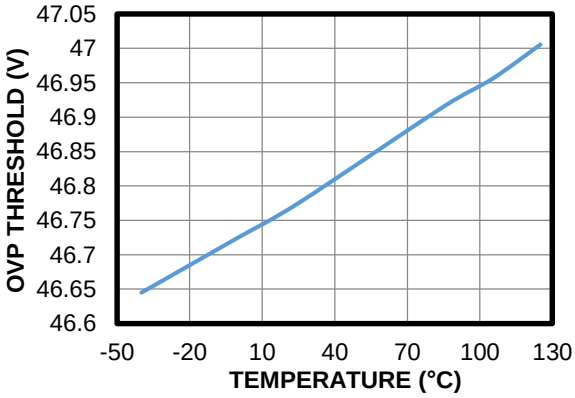
TYPICAL CHARACTERISTICS

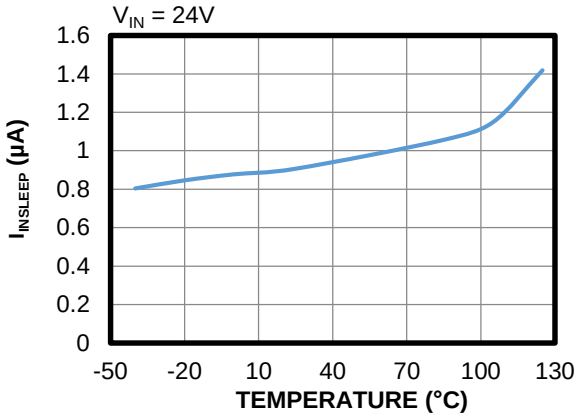
UVLO Rising Threshold vs. Temperature



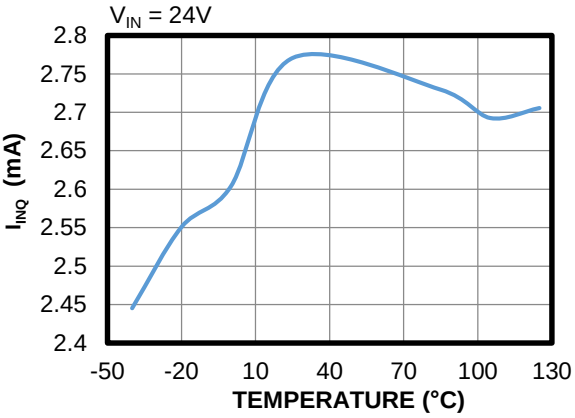
OVP Threshold vs. Temperature



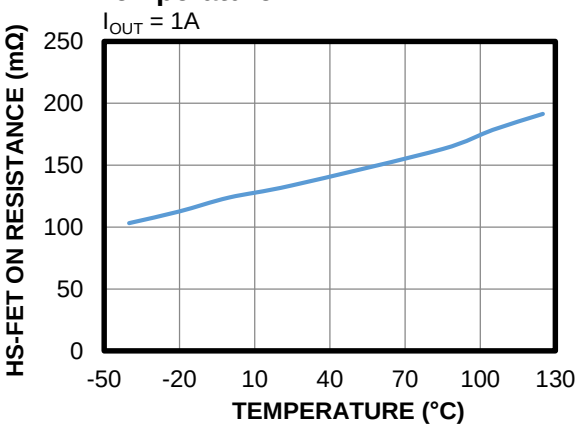
Quiescent Current ($I_{INSLEEP}$) vs. Temperature



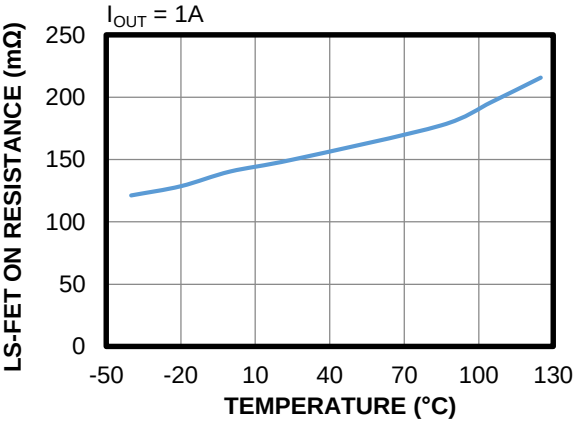
Quiescent Current (I_{INQ}) vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature



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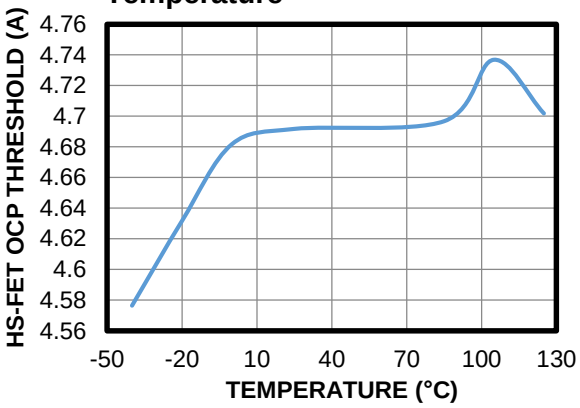
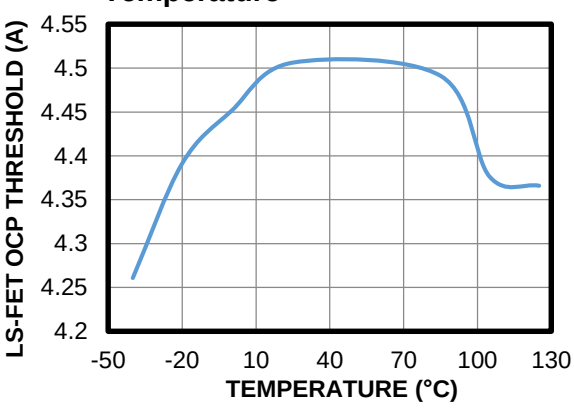
TYPICAL CHARACTERISTICS *(continued)*

HS-FET OCP Threshold vs. Temperature



LS-FET OCP Threshold vs. Temperature



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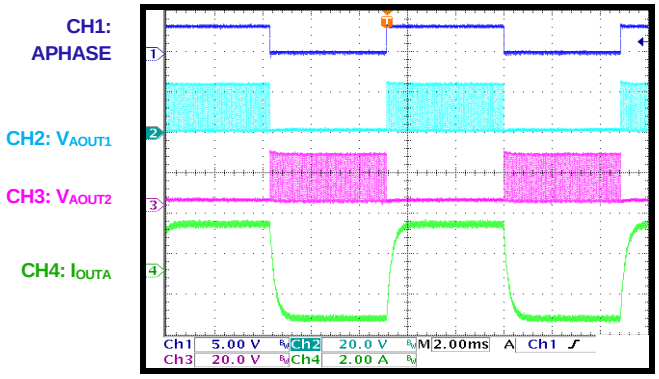
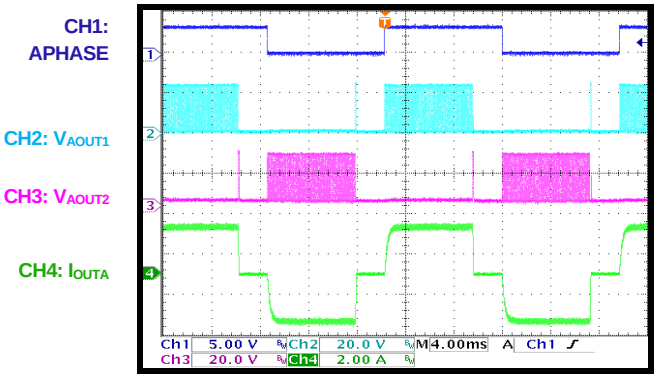
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, f_{SWITCH} = 20kHz, duty = 50%, slow decay (two LS-FETs on), T_A = 25°C, resistor + inductor load: 6Ω + 1.5mH, unless otherwise noted.

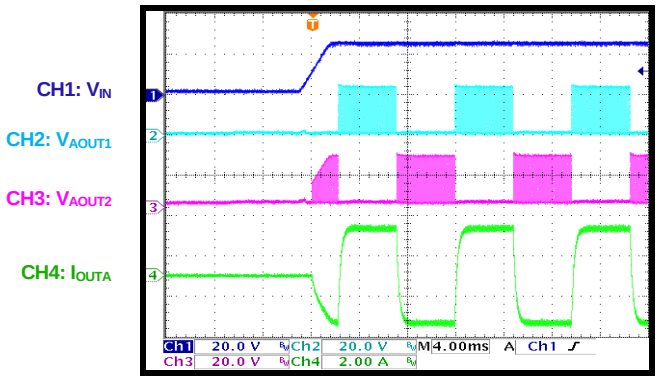
Steady State
Full step



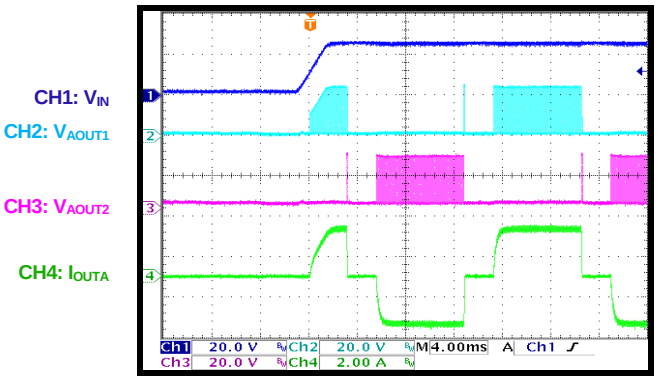
Steady State
Half-step



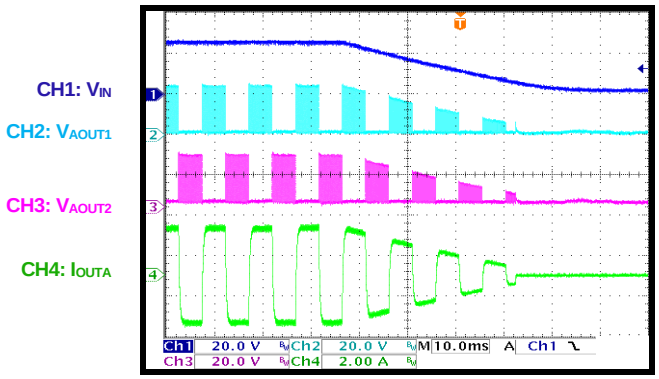
Power Ramping Up
Full step



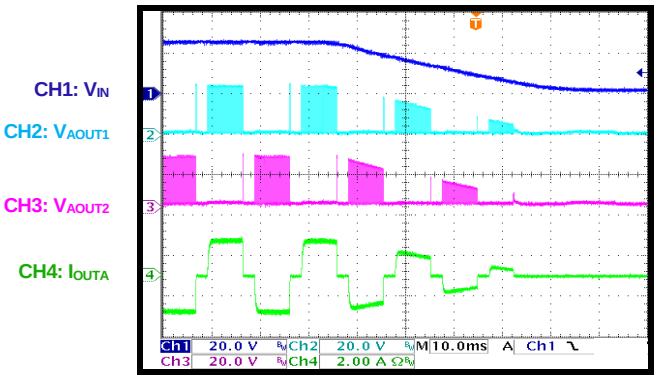
Power Ramping Up
Half-step



Power Ramping Down
Full step



Power Ramping Down
Half-step



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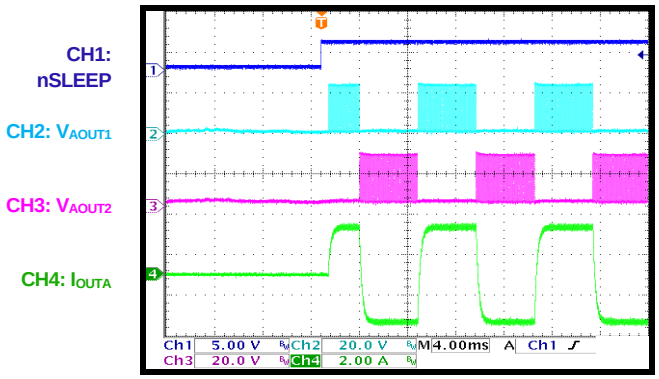
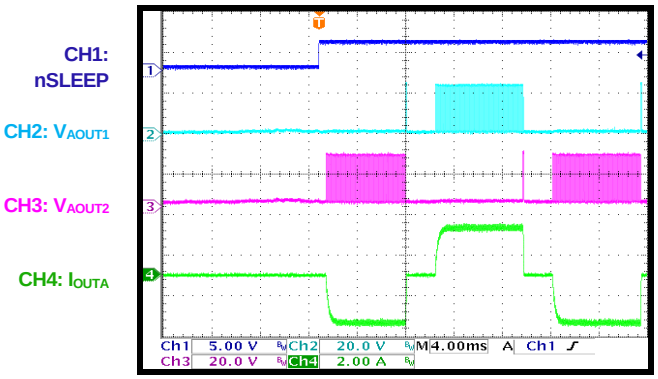
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, f_{SWITCH} = 20kHz, duty = 50%, slow decay (two LS-FETs on), T_A = 25°C, resistor + inductor load: 6Ω + 1.5mH, unless otherwise noted.

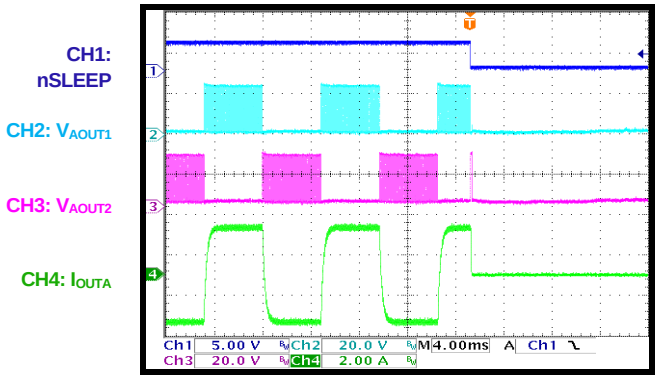
Sleep Recovery
Full step



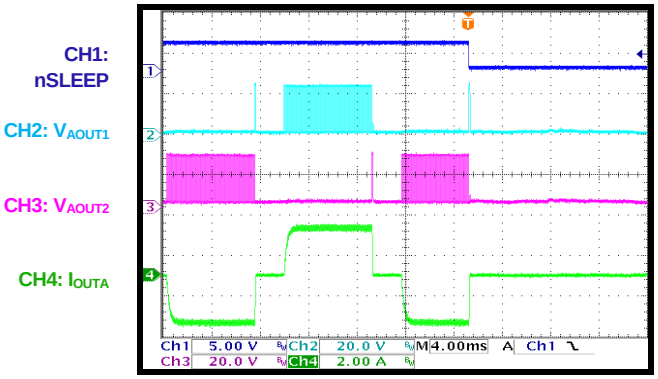
Sleep Recovery
Half-step



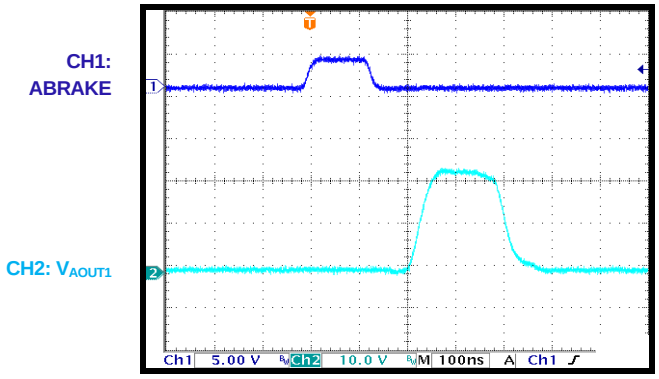
Sleep Entry
Full step



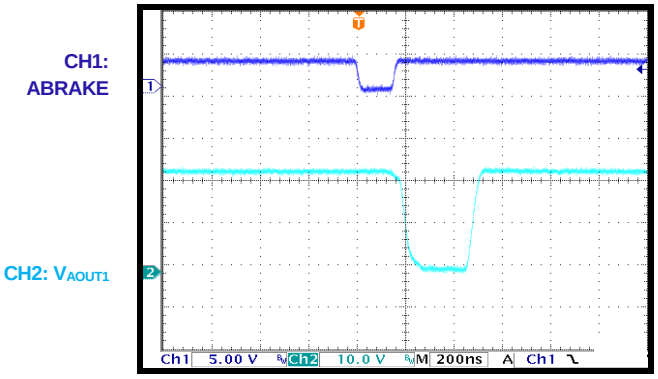
Sleep Entry
Half-step



HS-FET Minimum On Time
No load



LS-FET Minimum On Time
No load



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FUNCTIONAL BLOCK DIAGRAM

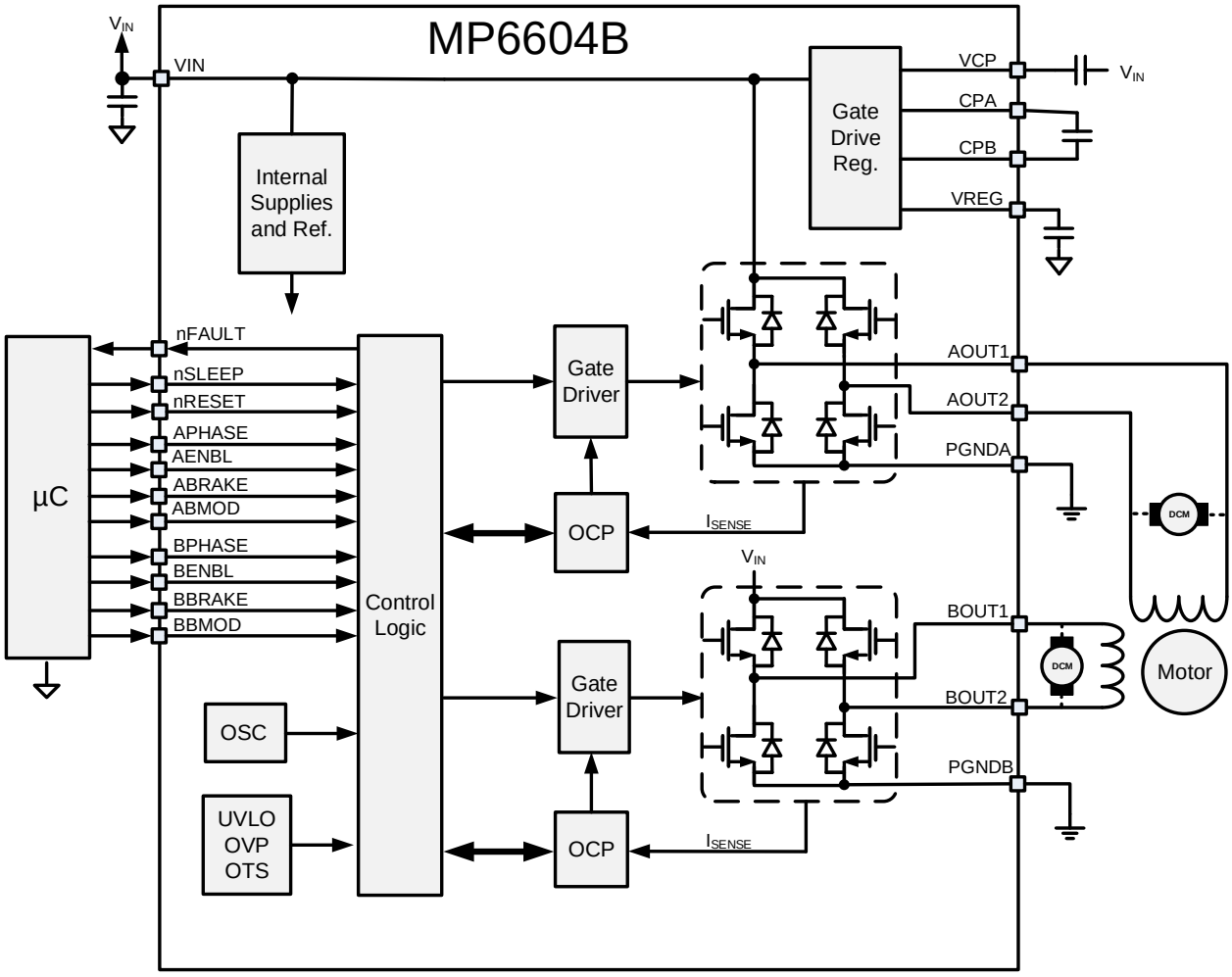

Figure 2: Functional Block Diagram

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OPERATION

The MP6604B is a general-purpose dual H-bridge motor driver designed to drive bipolar stepper motors, brushed DC motors, solenoids, and other loads. It integrates eight N-channel power MOSFETs connected as two full H-bridges, with a 2.5A current capability. The device operates across a wide 4.5V to 45V supply input voltage (V_{IN}) range.

nSLEEP and nRESET Operation

Drive nSLEEP low to put the device into a low power sleep state. In this state, the gate driver charge pump is stopped; all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

There is a delay time (600µs) between when the part exits sleep mode and when the part begins driving the motor to allow the internal circuitry to stabilize. The nSLEEP pin has an internal pull-down resistor.

Drive the nRESET pin low to reset the latched protection features, including over-current protection (OCP) and over-voltage protection (OVP), as well as to disable the outputs to a high-impedance state.

Input Interface

The device contains two full H-bridges that operate independently.

The MP6604B has a PHASE/ENBL interface. This interface uses a set of pins to control both halves of the H-bridge (typically, to drive a DC motor). Table 1 describes the input logic.

Table 1: Pin Input Logic

xENBL	xPHASE	xBRAKE	xBMODE	xOUT1	xOUT2
Low	-	-	-	Hi-Z	Hi-Z
High	-	High	Low	GND	GND
High	-	High	High	VIN	VIN
High	Low	Low	-	GND	VIN
High	High	Low	-	VIN	GND

Note that all logic inputs have weak, internal pull-down resistors.

Automatic Synchronous Rectification

If both output MOSFETs are off while driving current through an inductive load, the recirculation current must continue to flow. Generally, this current passes through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6604B implements an automatic synchronous rectification feature.

If both the high-side MOSFETs (HS-FETs) HS and low-side MOSFETs (LS-FETs) are turned off, and the voltage on an xOUTx (V_{xOUTx}) output pin is driven below ground, then the LS-FET turns on until the current flowing through it approaches zero, or until the HS-FET is commanded to turn on. Similarly, if V_{xOUTx} exceeds V_{IN}, the HS-FET turns on until the current approaches zero, or until the LS-FET turns on.

Internal Supplies (VREG and VCP)

The internal regulators generate a 5V supply (V_{REG}) for the LS gate drive, and a supply exceeding V_{IN} by 5V (V_{CP}) for the HS gate drive. These supplies require external capacitors.

The VREG pin requires a 1µF ceramic capacitor connected to ground. Meanwhile, the VCP pin requires a 1µF ceramic capacitor connected to VIN. Both capacitors should be X7R ceramic capacitors, and rated for a voltage of at least 16V.

Connect the charge pump flying capacitor between the CPA and CPB pins using a 100nF ceramic capacitor (X7R) that is rated for at least the maximum V_{IN}.

nFAULT Pin

The MP6604B provides a nFAULT pin to report to the system if a fault condition such as OCP, OVP, or thermal shutdown occur. nFAULT is an open-drain output, and is pulled low during fault conditions. If used, nFAULT should be pulled high via an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the HS-FET and LS-FET by disabling the gate driver. If the OC limit threshold is reached and lasts for longer than the OC deglitch time, then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low, or by removing and reapplying the power supply.

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OC conditions on the HS and LS devices (e.g. an OC condition to ground, supply, or across a motor winding) all result in an OC shutdown.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the OVP threshold, then the H-bridge output is disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low, or by removing and reapplying the power supply.

Input Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the under-voltage lockout (UVLO) threshold, then all of circuitry in the device is disabled and the internal logic resets. Normal operation resumes once V_{IN} exceeds its UVLO threshold.

Thermal Shutdown

If the die temperature exceeds safe limits, all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. Normal operation resumes once the die temperature returns to a safe level.

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APPLICATION INFORMATION

Selecting the External Components

Bypass the two VIN pins to GND using a minimum 100nF ceramic capacitor with X7R dielectrics, placed as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor close to the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN.

Connect a 100nF ceramic capacitor rated for the VIN voltage between the CPA and CPB pins. Connect a 1µF, 16V ceramic capacitor between the VIN and VCP pins.

Connect a 1µF, 16V ceramic capacitor with X7R dielectrics from the VREG pin to GND.

PCB Layout Guidelines

The PCB layout is critical for stable operation. For the best results, refer to Figure 2 and Figure 3, and follow the guidelines below:

1. Place the supply bypass and charge pump capacitors as close as possible to the IC (ideally, place them adjacent to the IC pins on the same PCB layer).
2. Each VIN pin must have a bypass capacitor.
3. Place as much copper as possible on the long pads.
4. Place large copper areas on the pads, and on the same outer copper layer as the device.
5. The thermal pad should be soldered directly to copper on the PCB.
6. Add thermal vias to transfer heat to the other layers of the PCB.

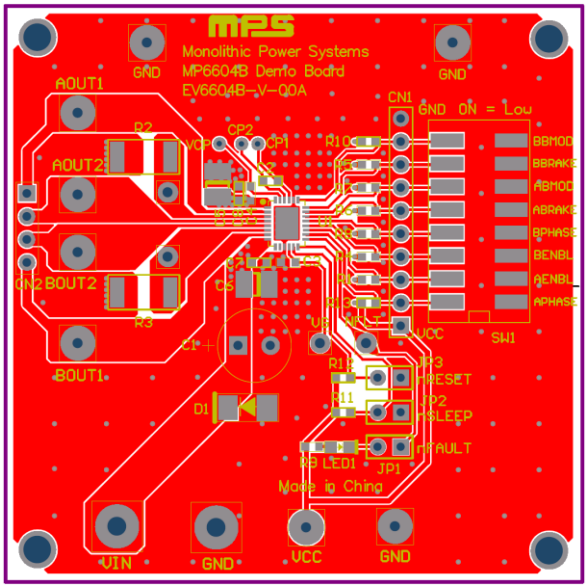

Figure 2: Recommended PCB Layout for the MP6604BGV

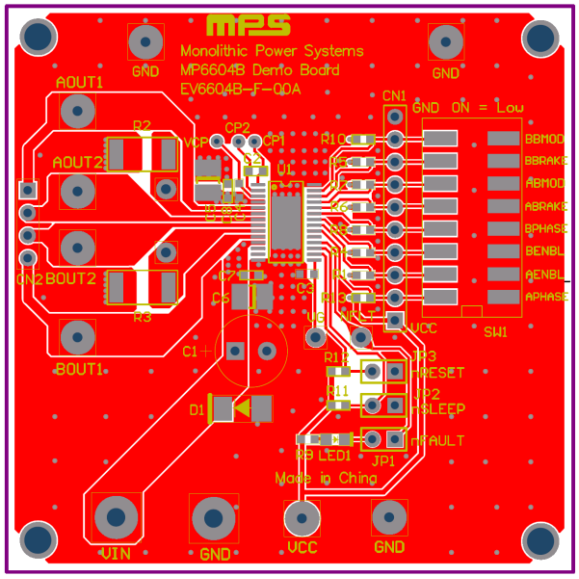

Figure 3: Recommended PCB Layout for the MP6604BGF

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TYPICAL APPLICATION CIRCUIT

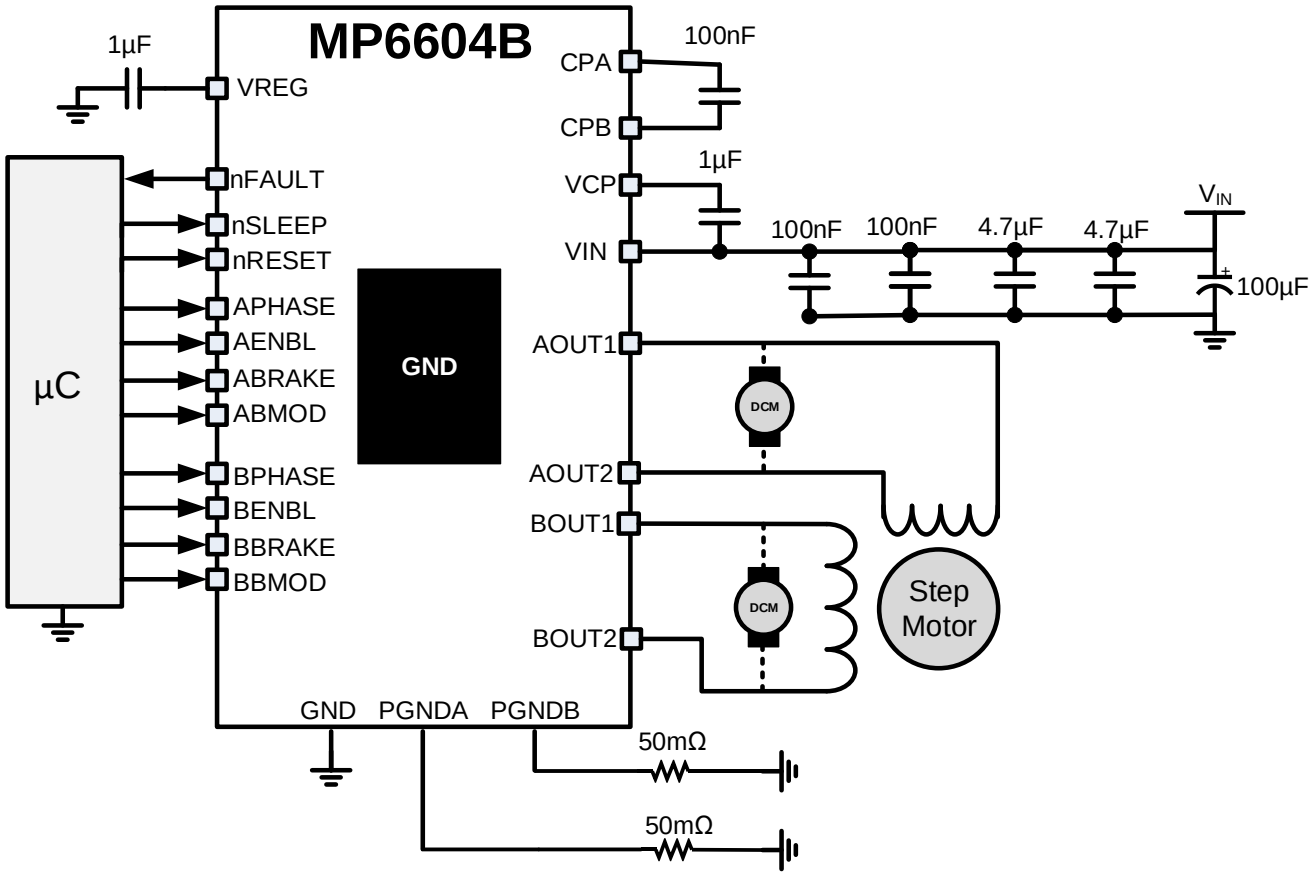

Figure 3: Typical Application Circuit

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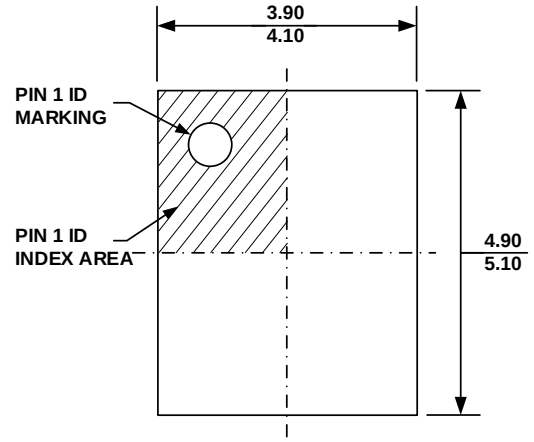
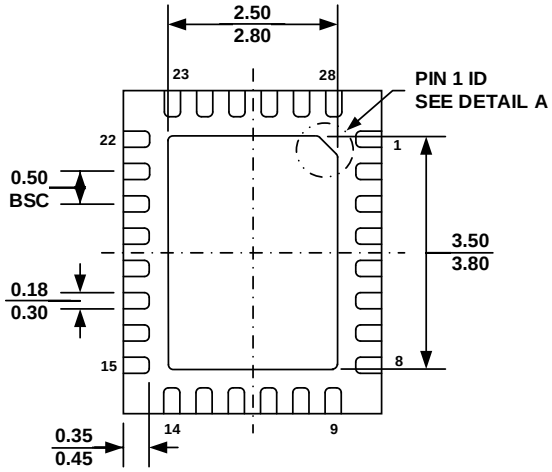
PACKAGE INFORMATION

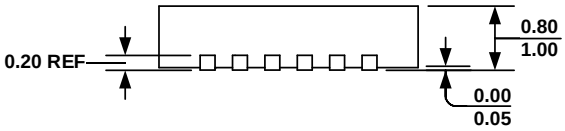
QFN-28 (4mmx5mm)



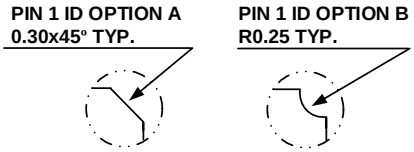
TOP VIEW



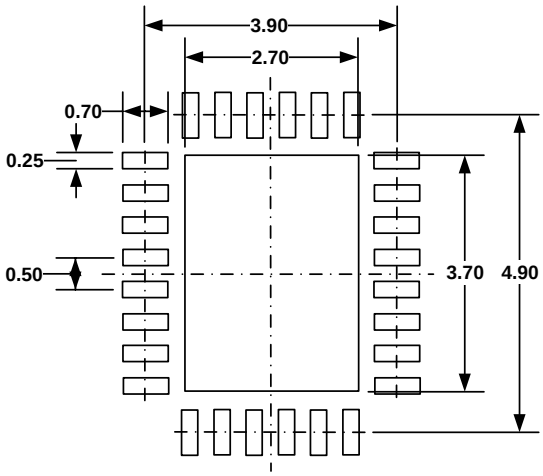
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

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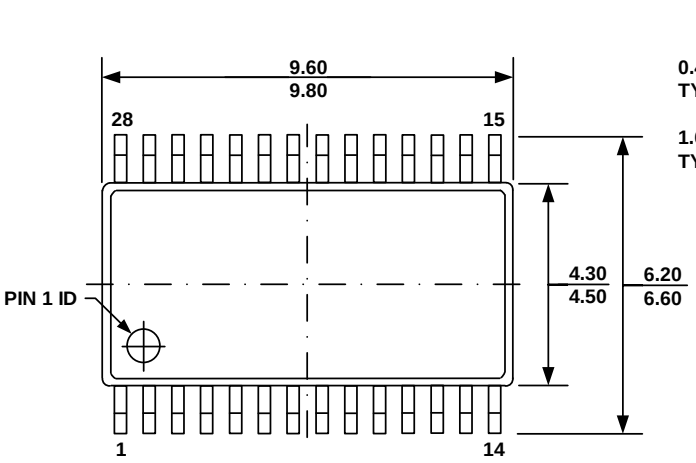
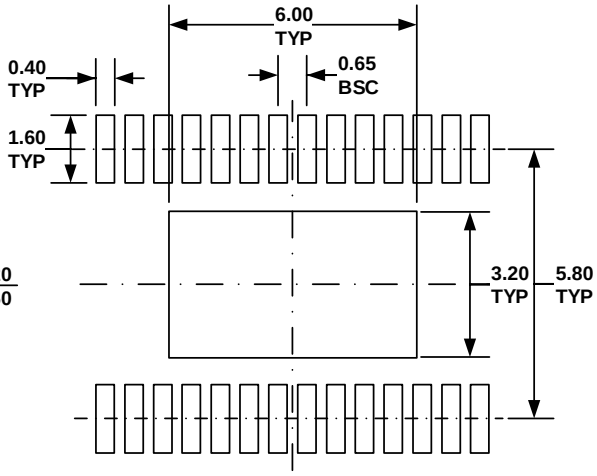
PACKAGE INFORMATION *(continued)*

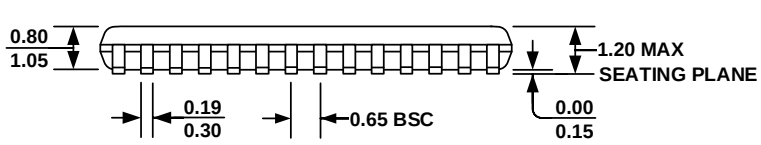
TSSOP-28 EP



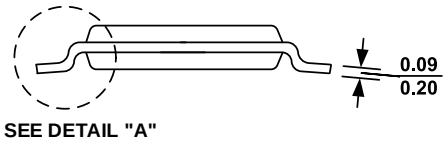
TOP VIEW



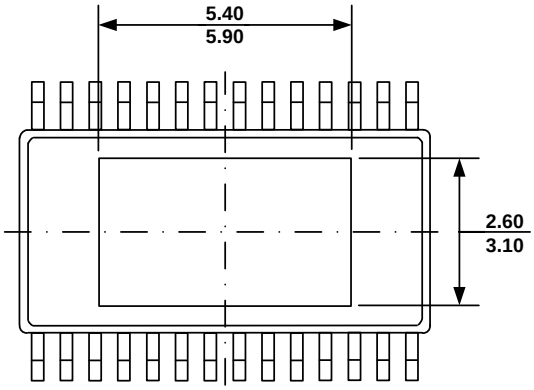
RECOMMENDED LAND PATTERN



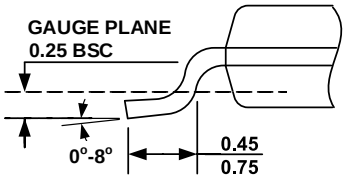
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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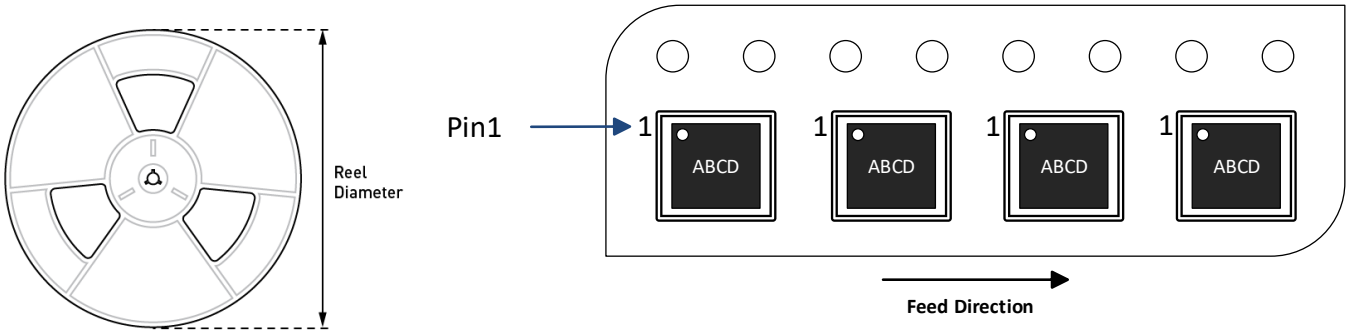
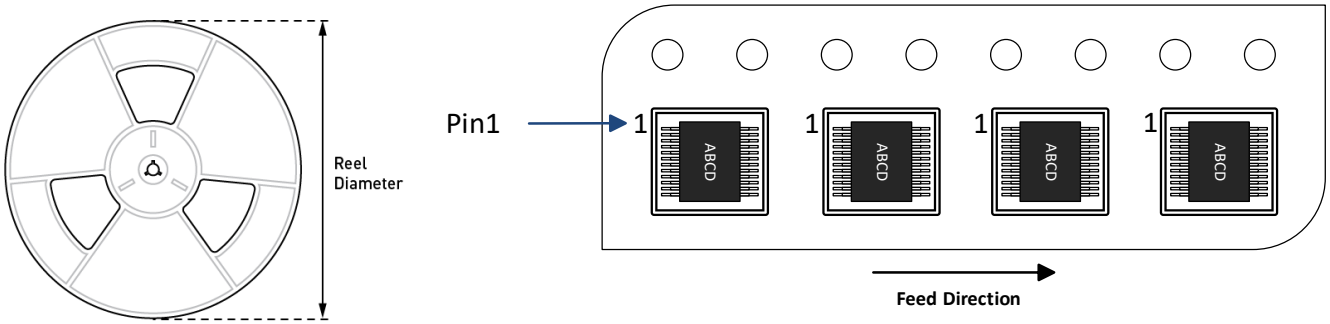
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6604BGV-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6604BGF-Z	TSSOP-28EP	2500	50	N/A	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/21/2022	Initial Release	-
1.1	5/12/2023	Updated the MSL rating for the MP6604BGV to “2” in the Ordering Information section	2

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