

DESCRIPTION

The MP62061 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62061 Analog switch features 80mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with a guaranteed current limit, making it ideal for load switching applications. The MP62061 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62061 is available in SOIC8E package.

FEATURES

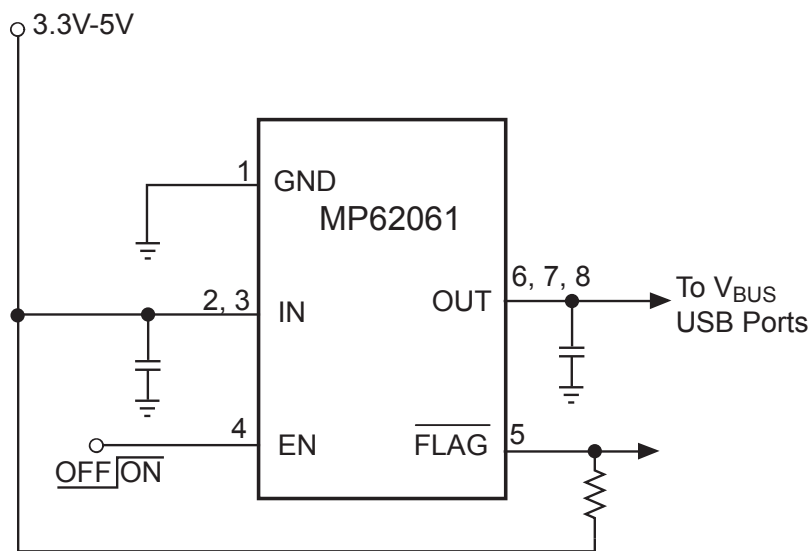
- 700mA Continuous Current
- 1A Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 140uA Quiescent Current
- 80mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- SOIC8E package
- UL Recognized: E322138

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Set-top-box
- USB Power Distribution

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TYPICAL APPLICATION



SINGLE-CHANNEL



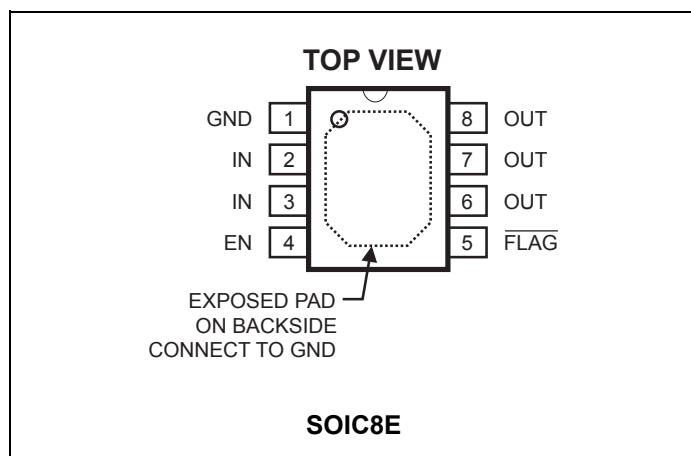
UL Recognized Component

ORDERING INFORMATION

| Part Number* | Enable | Switch | Maximum Continuous Load Current | Maximum Short-Circuit Current @ T _A =25°C | Package | Top Marking | Temperature |
|--------------|-------------|--------|---------------------------------|--|---------|-------------|----------------|
| MP62061DN | Active High | Single | 700mA | 1250mA | SOIC8E | 62061D | –40°C to +85°C |

*For Tape & Reel, add suffix –Z (eg. MP62061DN–Z); For RoHS Compliant Packaging, add suffix –LF ; (eg. MP62061DN–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|--|-----------------|
| IN | –0.3V to +6.0V |
| EN, FLAG, OUT to GND | –0.3V to +6.0V |
| Continuous Power Dissipation (T _A = +25°C) ⁽²⁾ | |
| SOIC8E | 2.5W |
| Junction Temperature | 150°C |
| Lead Temperature | 260°C |
| Storage Temperature | –65°C to +150°C |
| Operating Temperature | –40°C to +85°C |

Thermal Resistance ⁽³⁾

| | θ_{JA} | θ_{JC} |
|--------------|---------------|---------------|
| SOIC8E | 50 | 10 ... °C/W |

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)–T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7 4-layer PCB

ELECTRICAL CHARACTERISTICS ⁽⁴⁾

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

| Parameter | Condition | Min | Typ | Max | Units |
|--|---|-----|------|------|-------|
| IN Voltage Range | | 2.7 | | 5.5 | V |
| Supply Current | Single Channel | | 140 | 160 | μA |
| Shutdown Current | Device Disable, V _{OUT} =float, V _{IN} =5.5V | | 1 | | μA |
| Off Switch Leakage | Device Disable, V _{IN} =5.5V | | 1 | | μA |
| Current Limit | | 750 | 1000 | 1250 | mA |
| Trip Current | Current Ramp (slew rate ≤ 100A/s) on Output | | 1.4 | 1.8 | A |
| Under-voltage Hysteresis | | | 250 | | mV |
| FET On Resistance | I _{OUT} =100mA and -40°C<T _A <85°C | | 80 | 130 | mΩ |
| EN Input Logic High Voltage | | 2 | | | V |
| EN Input Logic Low Voltage | | | | 0.8 | V |
| FLAG Output Logic Low Voltage | I _{SINK} =5mA | | | 0.4 | V |
| FLAG Output High Leakage Current | V _{IN} =V _{FLAG} =5.5V | | | 1 | μA |
| Thermal Shutdown | | | 140 | | °C |
| Thermal Shutdown Hysteresis | | | 20 | | °C |
| V _{OUT} Rising Time, Tr ⁽⁵⁾ | V _{IN} =5.5V, C _L =1μF, R _L =11Ω | | 0.9 | | ms |
| | V _{IN} =2.7V, C _L =1μF, R _L =11Ω | | 1.7 | | ms |
| V _{OUT} Falling Time, Tf ⁽⁵⁾ | V _{IN} =5.5V, C _L =1μF, R _L =11Ω | | | 0.5 | ms |
| | V _{IN} =2.7V, C _L =1μF, R _L =11Ω | | | 0.5 | ms |
| Turn On Time, Ton ⁽⁶⁾ | C _L =100μF, R _L =11Ω | | | 3 | ms |
| Turn Off Time, Toff ⁽⁶⁾ | C _L =100μF, R _L =11Ω | | | 10 | ms |
| FLAG Deglitch Time | | 4 | 8 | 15 | ms |
| EN Input Leakage | | | 1 | | μA |
| Reverse Leakage Current | OUT=5.5V, IN=GND | | 0.2 | | μA |

NOTE:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

5) Measured from 10% to 90%.

6) Measured from (50%) EN signal to (90%) output signal.

PIN FUNCTIONS

| Pin # SOIC8E | Name | Description |
|-----------------|--------------------------|--|
| 1 | GND, Exposed Pad | Ground. Connect exposed pad to GND plane for optimal thermal performance |
| 2, 3 | IN | Input Voltage. Accepts 2.7V to 5.5V input. |
| 4 | EN | Enable Input. Active High. |
| 5 | $\overline{\text{FLAG}}$ | IN-to-OUT Over-current, active-low output flag. Open-Drain. |
| 6, 7, 8 | OUT | Power-Distribution Switch Output. |

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

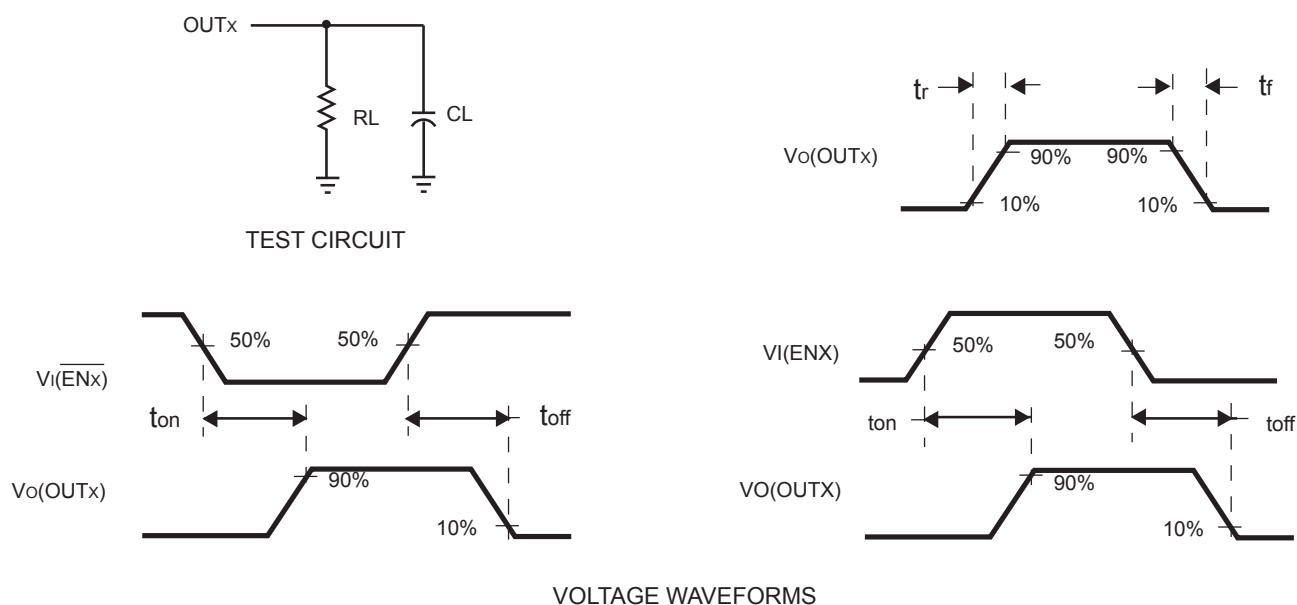
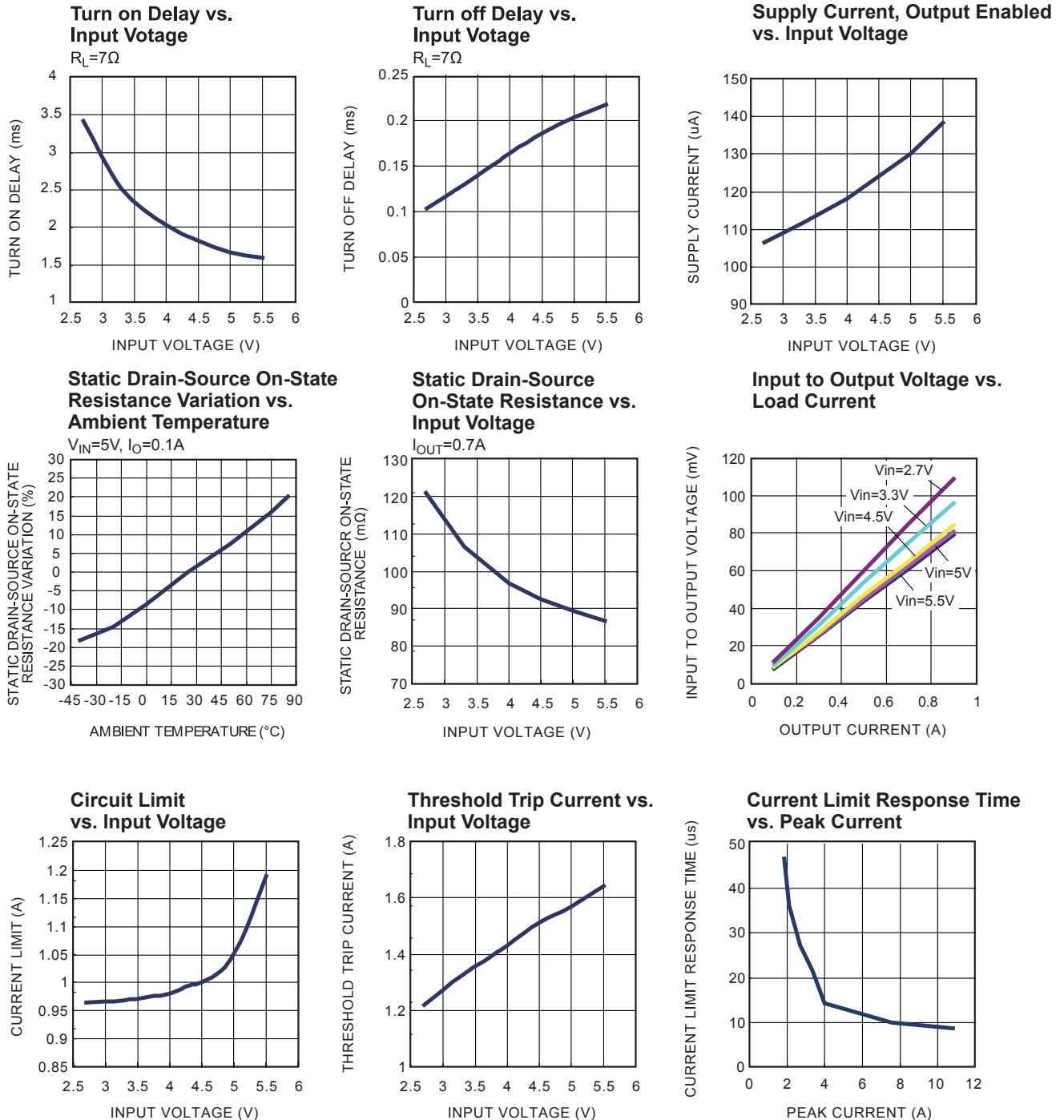


Figure 1—Test Circuit and Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

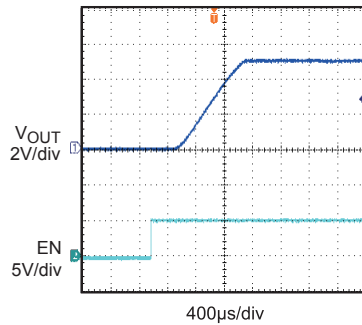
$V_{IN}=5.5V$, $V_{EN}=5V$, $C_L=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.



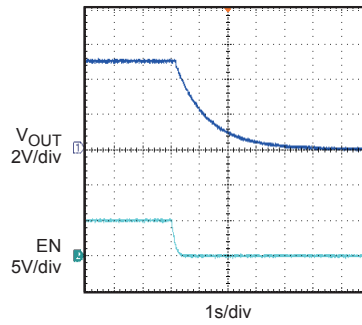
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}=5.5V$, $V_{EN}=5V$, $C_L=2.2\mu F$, $T_A=25^\circ C$, unless otherwise noted.

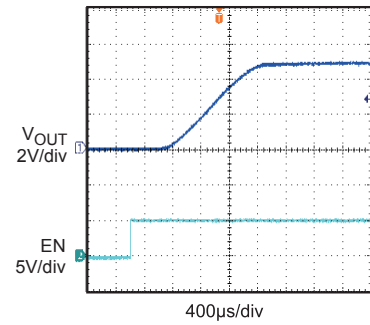
Turn On Delay and Rise Time with 0.1 μF Load
 $C_L=0.1\mu F$



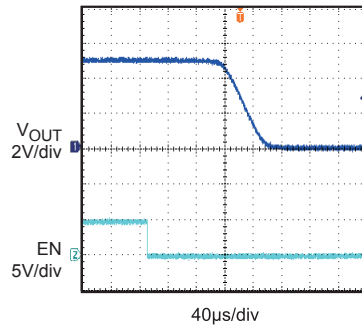
Turn Off Delay and Fall Time with 0.1 μF Load
 $C_L=0.1\mu F$



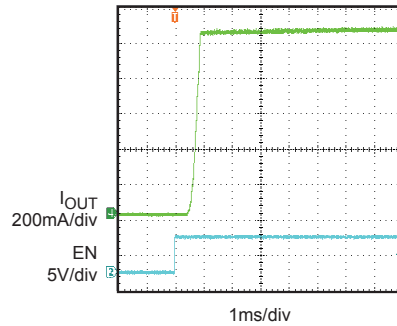
Turn On Delay and Rise Time with 1 μF Load
 $R_L=7\Omega$, $C_L=1\mu F$



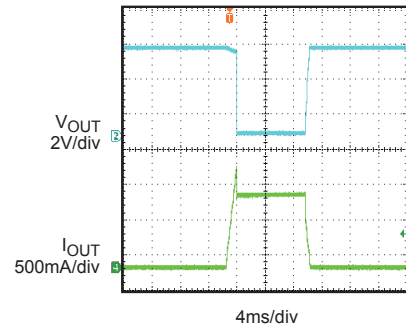
Turn Off Delay and Fall Time with 1 μF Load
 $R_L=7\Omega$, $C_L=1\mu F$



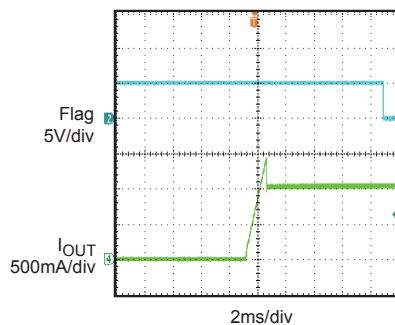
Short Circuit Current Device Enabled into Short



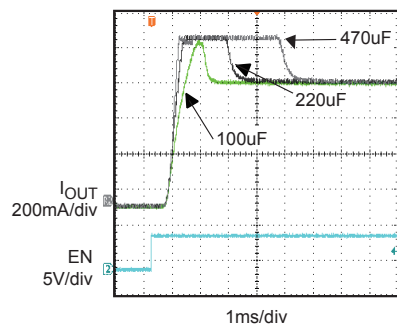
Threshold Trip Current with Ramped Load on Enabled Device



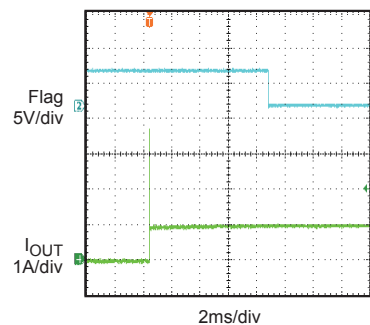
Ramped Load on Enabled Device



Inrush Current with Different Load Capacitance
 $R_L=7\Omega$



1 Ω Load Connected to Enabled Device



FUNCTION BLOCK DIAGRAM

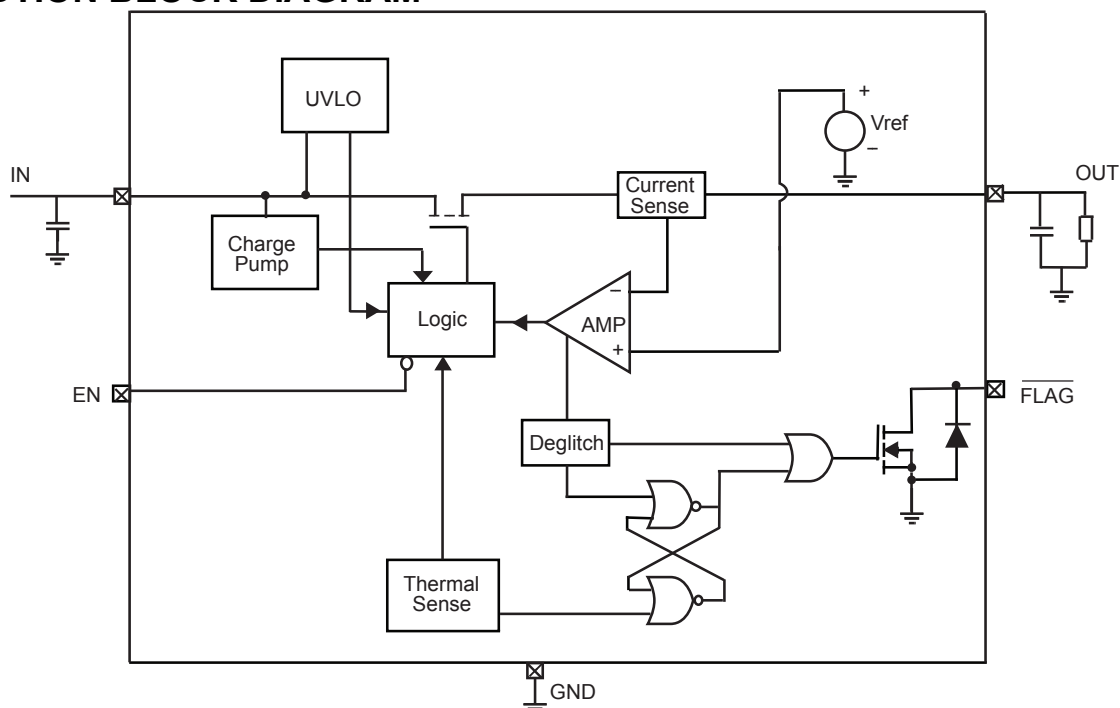


Figure 2—Functional Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62061 switches into to a constant-current mode (current limit value). MP62061 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

- 1) The output has been shorted or overloaded before the device is enabled or input applied. MP62061 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.

- 3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62061 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing excessive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62061 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

APPLICATION INFORMATION

Power-Supply Considerations

Over 10 μ F capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

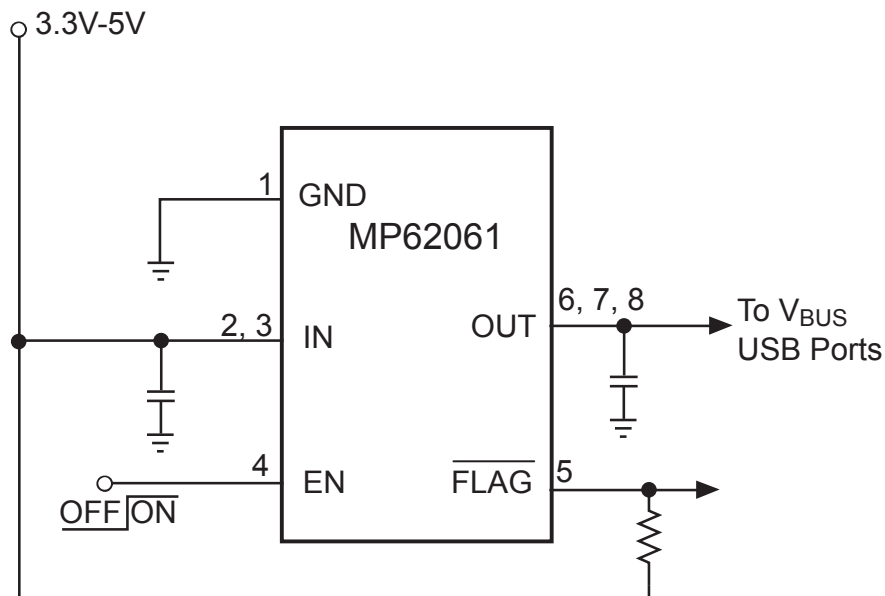
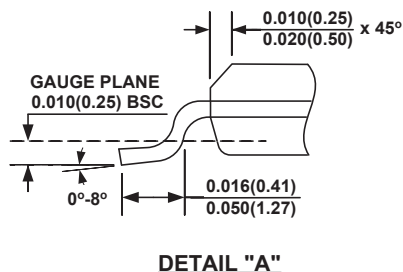
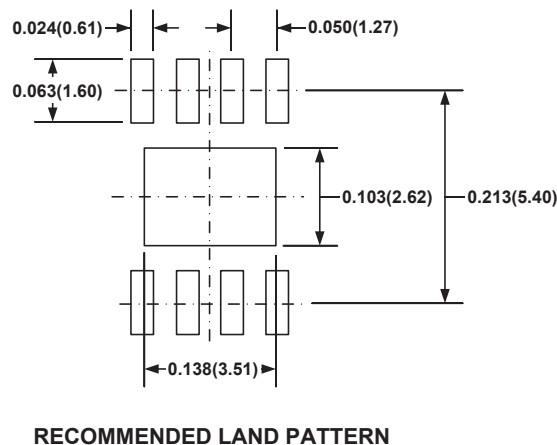
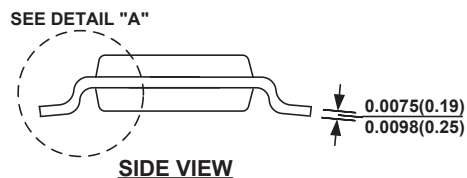
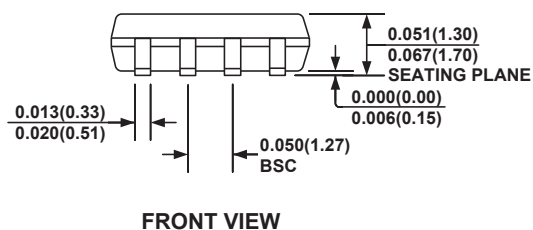
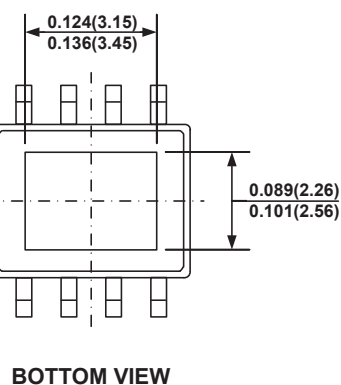
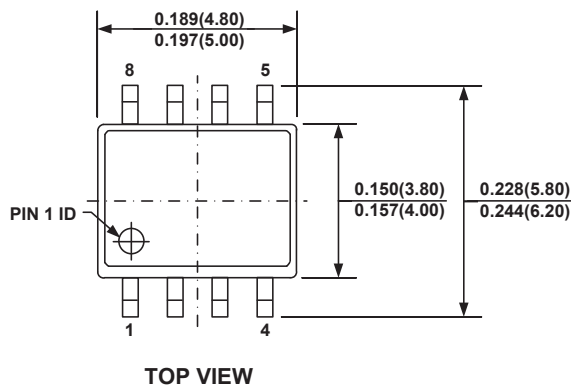


Figure 3—Application Circuit

PACKAGE INFORMATION

SOIC8E (EXPOSED PAD)



NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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