MP3385B

4-String, 80V Output WLED Controller with I²C Interface

DESCRIPTION

The MP3385B is a step-up controller with four regulated LED current (I_{LED}) channels, designed to drive WLED arrays for mid-sized and large-sized LCD panel backlighting applications.

The MP3385B employs peak current control mode and pulse-width modulation (PWM) control architecture for system loop regulation. The MP3385B drives an external MOSFET to boost the output voltage (V_{OUT}) from a 4.5V to 33V input voltage (V_{IN}) supply.

The MP3385B provides an I²C digital interface to flexibly set the operation and protection modes, including dimming mode, the dimming current and dimming ratio, over-current protection (OCP), over-voltage protection (OVP), the LED short protection threshold, and the switching frequency (f_{SW}).

For ease of use and board debugging, the MP3385B automatically detects and disables the unused LED strings during start-up to avoid charging the output to the OVP threshold.

The MP3385B achieves 1.8% current matching between each string. The low regulation voltage on the LED current sources improves efficiency and reduces power loss, which can result in a higher current output.

The MP3385B supports analog, PWM, and combined analog and PWM dimming modes to meet different application requirements. Full protection features include OCP, over-temperature protection (OTP), under-voltage protection (UVP), OVP, LED short and open protection, and inductor and diode short protection.

The MP3385B is available in a QFN-20 (4mmx4mm) package.

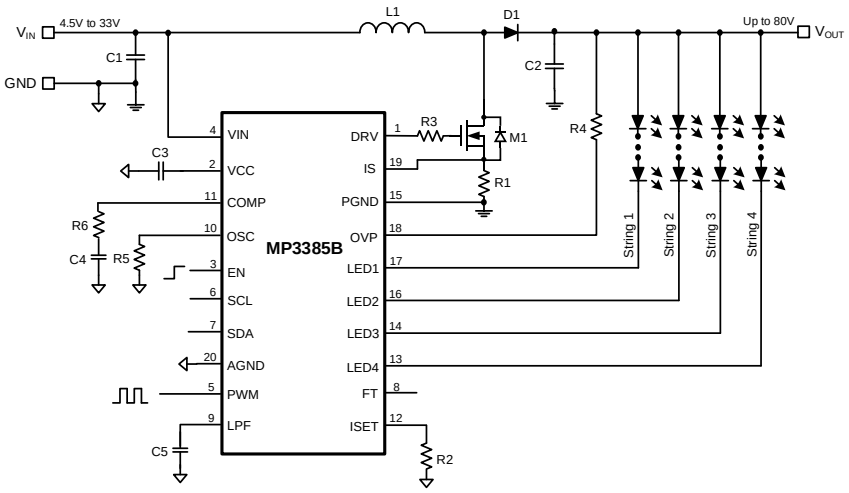
FEATURES

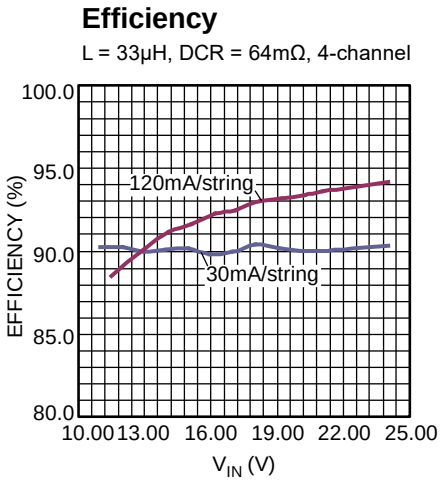
- 4-String, Max 300mA/String WLED Driver
- 4.5V to 33V Input Voltage (V_{IN}) Range
- 80V Absolute Maximum Rating for Each String
- 1.8% Current Matching Accuracy between Each String
- Unused Channel Auto-Detection during Start-Up
- 100kHz to 900kHz Configurable Switching Frequency (f_{SW})
- Multiple Dimming Modes Selectable via the I²C Interface:
  - Direct Pulse-Width Modulation (PWM) Dimming Mode
  - Internal, Fixed 23kHz PWM Dimming Mode via I²C
  - Analog Dimming Mode via Input Pulse
  - Internal Analog Dimming Mode via I²C
  - Mixed Dimming Mode via Input Pulse
  - Internal Mixed Dimming Mode via I²C
- 2% to 100% Configurable Full-Scale Current with 8-Bit Resolution
- 0% to 100% LED Dimming Range with 10-Bit Resolution for Internal Dimming Mode
- Cascading Capability with a Single Power Source
- 18V to 80V Over-Voltage Protection (OVP), 2V/Step
- 0.15V to 0.5V Latch-Off and Recoverable Over-Current Protection (OCP) Threshold, 50mV/Step
- Recoverable Thermal Shutdown Protection
- Available in a QFN-20 (4mmx4mm) Package

APPLICATIONS

- Desktop LCD Flat-Panel Displays
- All-in-One PCs
- 2D and 3D LCD TVs

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3385BGR	QFN-20 (4mmx4mm)	*See Below*	1

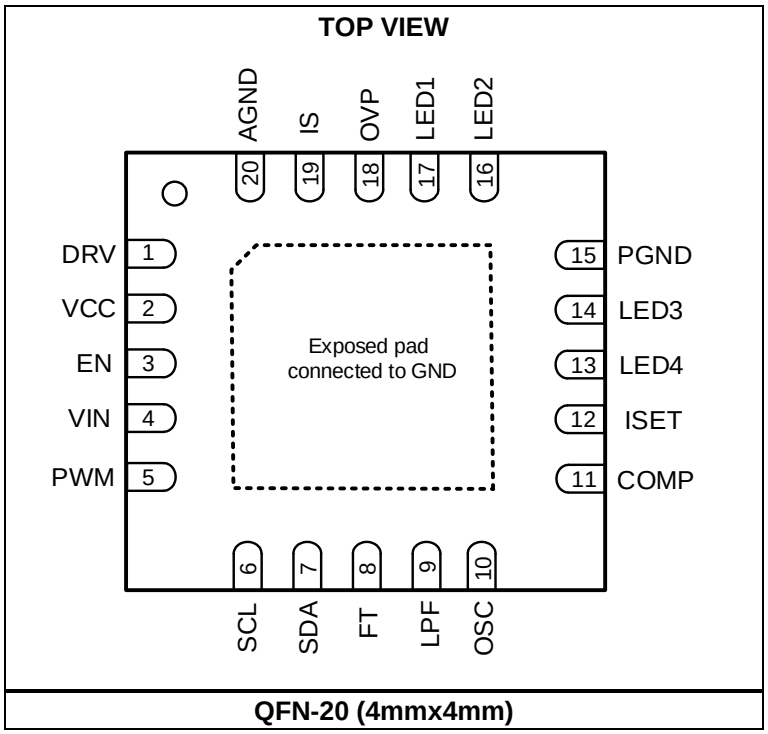
* For Tape & Reel, add suffix -Z (e.g. MP3385BGR-Z).

TOP MARKING

MPSYWW
M3385B
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M3385B: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	DRV	**Power MOSFET gate output of the step-up converter.** The DRV pin drives the external N-channel power MOSFET. Connect a resistor (e.g. 10Ω) to DRV.
2	VCC	**Internal 6V linear regulator output.** The VCC pin provides the power supply for the external MOSFET gate driver and the internal control circuitry. Bypass VCC to ground using a ceramic capacitor.
3	EN	**Enable control input.** Pull EN above 1.5V to turn on the part; pull EN below 0.6V to turn off the part. Do not float the EN pin.
4	VIN	**Supply input.** The VIN pin must be bypassed locally.
5	PWM	**Pulse-width modulation (PWM) input signal for brightness control.** Ensure that the PWM amplitude voltage level (V_{PWM}) exceeds the PWM input high threshold (V_{PWM_HI}), and that the low-level voltage is below the PWM input low threshold (V_{PWM_LO}). When the MP3385B works in direct PWM dimming mode, the LED current (I_{LED}) duty cycle (D_{ILED}) directly follows the PWM input signal duty cycle (D_{PWM}). For external analog and mixed dimming modes, the PWM pulse is filtered to a DC signal by an LPF capacitor, and I_{LED} is proportional to D_{PWM}. If PWM is floated, then weakly pull PWM to ground internally.
6	SCL	**I²C clock input.**
7	SDA	**I²C data input.**
8	FT	**Fault indication output.** The FT pin is an open drain during normal operation. FT is pulled low during a fault condition.
9	LPF	**Low-pass filter output for analog dimming with PWM input.** Connect a capacitor (C_{LPF}) between the LPF pin and ground when the MP3385B operates in external PWM input analog dimming or mixed dimming mode. Remove C_{LPF} when the part operates in direct PWM dimming mode.
10	OSC	**Switching frequency (f_{SW}) setting.** Connect a resistor (R_{OSC}) between the OSC pin and ground to set the step-up converter's f_{SW}. The clock frequency is proportional to the current sourced from OSC. If connected to a 100kΩ R_{OSC}, then select a 100kHz to 900kHz f_{SW} via the I²C interface.
11	COMP	**Step-up converter compensation.** The COMP pin compensates for the regulation control loop. Connect a ceramic capacitor and resistor from COMP to ground.
12	ISET	**LED current (I_{LED}) setting.** Connect a current-setting resistor from the ISET pin to ground to configure the current for each LED string.
13	LED4	**LED string 4 current input.** The LED4 pin is the open-drain output of an internal dimming control switch. Connect LED4 to the LED string 4 cathode.
14	LED3	**LED string 3 current input.** The LED3 pin is the open-drain output of an internal dimming control switch. Connect LED3 to the LED string 3 cathode.
15	PGND	**Power ground.**
16	LED2	**LED string 2 current input.** The LED2 pin is the open-drain output of an internal dimming control switch. Connect LED2 to the LED string 2 cathode.
17	LED1	**LED string 1 current input.** The LED1 pin is the open-drain output of an internal dimming control switch. Connect LED1 to the LED string 1 cathode.
18	OVP	**Output over-voltage protection (OVP).**
19	IS	**Current-sense input.** During normal operation, the IS pin senses the voltage across the external inductor current-sense resistor (R_{SENSE}) for peak current mode control. IS also limits the inductor current (I_L) during every switching cycle. If the MP3385B is used for cascading applications, then connect the slave chip's IS pin to ground. Do not float IS.
20	AGND	**Signal ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +40V
V_{OVP}, V_{LED1} to V_{LED4} .....-0.3V to +80V
All other pins ... -0.3V (-0.5V for <10ns) to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-20 (4mmx4mm) 2.97W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±1800V
Charged device model (CDM) ..... ±2000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 33V
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)	42	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, a 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Operating input voltage	V_{IN}		4.5		33	V
Quiescent supply current	I_Q	V_{IN} = 12V, no switching		3		mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 12V			1	μA
Low-dropout (LDO) output voltage	V_{CC}	7V < V_{IN} < 28V, 0 < I_{VCC} < 10mA	5.4	6	6.3	V
V_{CC} under-voltage lockout (UVLO) threshold	V_{CC_UVLO}	Rising edge	3.7	4	4.3	V
V_{CC} UVLO hysteresis				340		mV
Enable (EN) high voltage	V_{EN_HIGH}	V_{EN} rising	1.5			V
EN low voltage	V_{EN_LOW}	V_{EN} falling			0.6	V
Step-Up Converter						
Gate driver source impedance		V_{CC} = 6V, V_{GATE} = 6V		4		Ω
Gate driver sink impedance		V_{CC} = 6V, I_{GATE} = 10mA		2		Ω
Switching frequency	f_{SW}	FS[3:0] = 0010b, R_{OSC} = 100kΩ	156	195	234	kHz
		FS[3:0] = 1001b, R_{OSC} = 100kΩ	672	820	967	kHz
OSC pin voltage	V_{OSC}	R_{OSC} = 100kΩ, f_{SW} = 900kHz	1.75	1.79	1.83	V
Maximum duty cycle	D_{MAX}		90			%
Cycle-by-cycle IS pin current limit		OCP[2:0] = 000b	130	150	170	mV
		OCP[2:0] = 111b	465	500	535	mV
COMP source current limit	I_{COMP_SOLI}	1V < COMP < 2.9V		75		μA
COMP sink current limit	I_{COMP_SILI}	1V < COMP < 2.9V		15		μA
COMP transconductance	G_{COMP}	ΔI_{COMP} = ±10μA		100		μA/V
Current Dimming						
Pulse-width modulation (PWM) input low threshold	V_{PWM_LO}	V_{PWM} falling			0.4	V
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.5			V
Dimming transfer point		MODE[1:0] = 10b		25		%
		MODE[1:0] = 11b		50		%
Internal dimming frequency			20	23		kHz
Dimming ratio		Dimming resolution		0.098		%
		DIM[9:0] = 1111111111b		100		%
Current Regulation						
ISET pin voltage	V_{ISET}		1.93	1.98	2.03	V
LEDx average current	I_{LEDx}	R_{ISET} = 100.8kΩ, ILED[7:0] = FFh	192	201	210	mA
		R_{ISET} = 100.8kΩ, I_{LED} = 3mA	2.7	3	3.3	
Full-scale current		ILED[7:0] = 00h		2		%
		ILED[7:0] = FFh (6)		100		
Current matching (5)		I_{LED} = 200mA			1.8	%
		I_{LED} = 3mA			3	
LEDx regulation voltage	V_{LEDx}	I_{LED} = 330mA		820		mV
		I_{LED} = 200mA		700		
		I_{LED} = 60mA		500		

ELECTRICAL CHARACTERISTICS *(continued)*

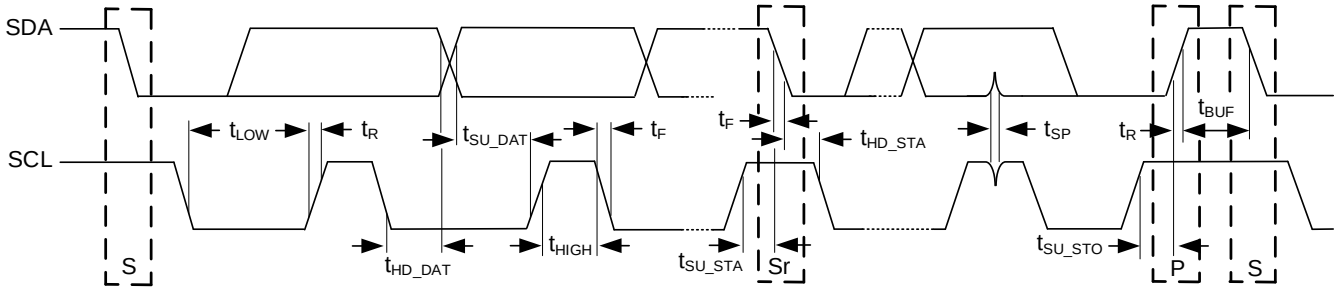
V_{IN} = 12V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Protections						
Over-voltage protection (OVP) threshold	V_{OVP}	OVP[4:0] = 00000b	16.8	18	18.9	V
		OVP[4:0] = 11100b	71.5	74	75.5	V
OVP UVLO threshold	V_{OVP_UVLO}	Step-up converter fails		2.5		V
LEDx UVLO threshold	V_{LEDx_UVLO}		147	206	265	mV
LEDx over-voltage (OV) threshold	V_{LEDx_OV}	LEDS[2:0] = 000b		4		V
		LEDS[2:0] = 111b		11		V
Thermal protection threshold (6)	T_{ST}			150		°C
Thermal protection hysteresis (6)				25		°C
I²C Interface Specifications						
Input logic low (6)	V_{IL}				0.4	V
Input logic high (6)	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (6)	f_{SCL}				400	kHz
SCL high time (6)	t_{HIGH}		0.6			µs
SCL low time (6)	t_{LOW}		1.3			µs
Data set-up time (6)	t_{SU_DAT}		100			ns
Data hold time (6)	t_{HD_DAT}		0		0.9	µs
Set-up time for a repeated start condition (6)	t_{SU_STA}		0.6			µs
Hold time for a start condition (6)	t_{HD_STA}		0.6			µs
Bus free time between a start and stop condition (6)	t_{BUF}		1.3			µs
Set-up time for a stop condition (6)	t_{SU_STO}		0.6			µs
SCL and SDA rising time (6)	t_R		20 + 0.1 x C_B		300	ns
SCL and SDA falling time (6)	t_F		20 + 0.1 x C_B		300	ns
Pulse width of suppressed spike (6)	t_{SP}		0		50	ns
Capacitance for each bus line (6)	C_B				400	pF

Notes:

5) Matching is defined as the difference between the maximum to minimum current divided by twice the average currents.
6) Guaranteed by characterization. Not tested in production.

TIMING DIAGRAM



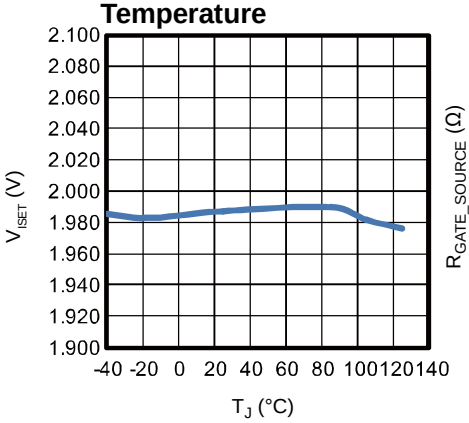
S = Start Command
Sr = Repeated Start Command
P = Stop Command

Figure 1: I²C-Compatible Interface Timing Diagram

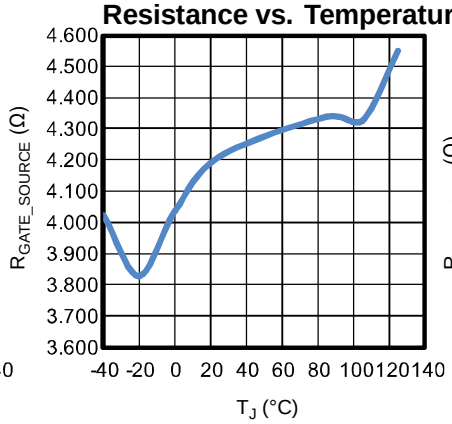
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 3.3V, unless otherwise noted.

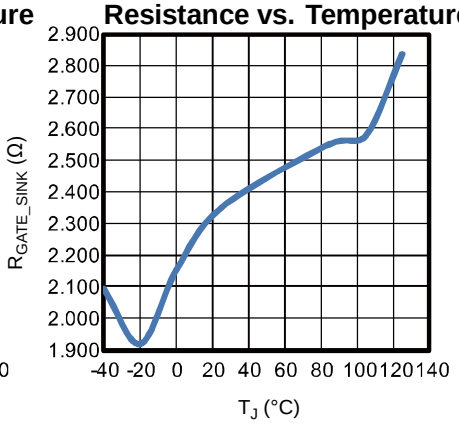
ISET Voltage vs. Temperature



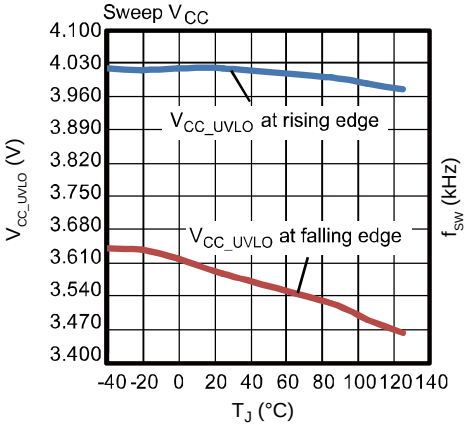
Gate Driver Source Resistance vs. Temperature



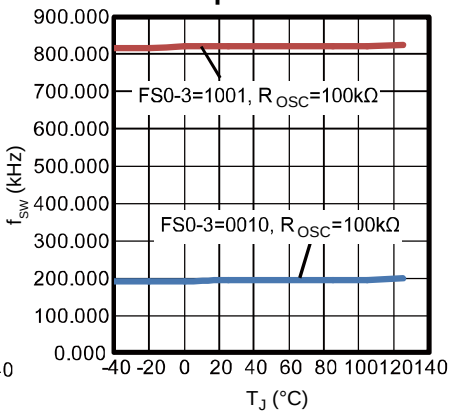
Gate Driver Sink Resistance vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



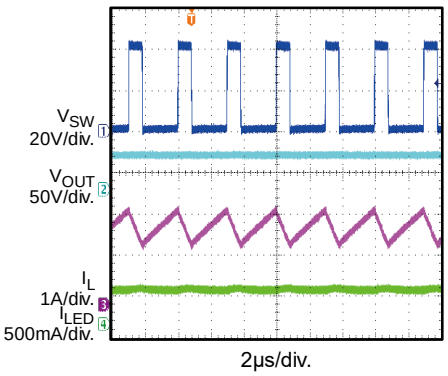
Switching Frequency vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

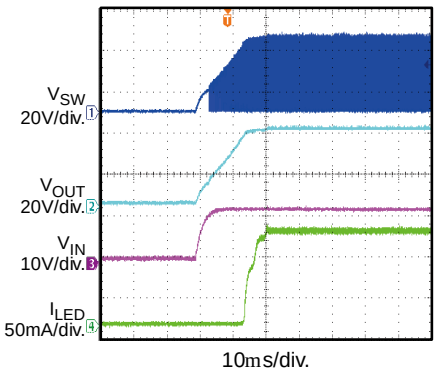
V_{IN} = 12V, V_{EN} = 3.3V, L = 33µH, 120mA/string, 4 strings, 14 LEDs, T_A = 25°C, unless otherwise noted.

Steady State



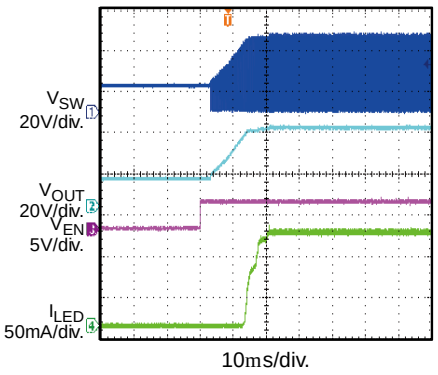
Start-Up through VIN

30mA/string



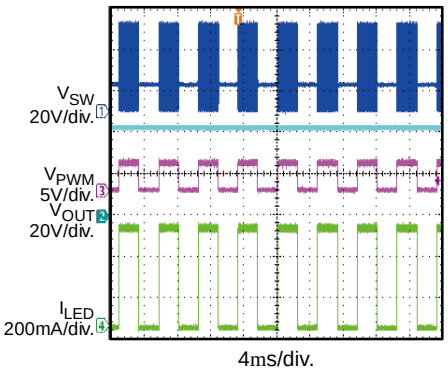
Start-Up through EN

30mA/string



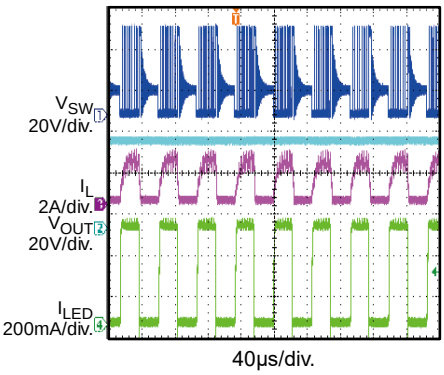
PWM Dimming via the PWM Input

f_{PWM} = 200Hz, D_{PWM} = 50%



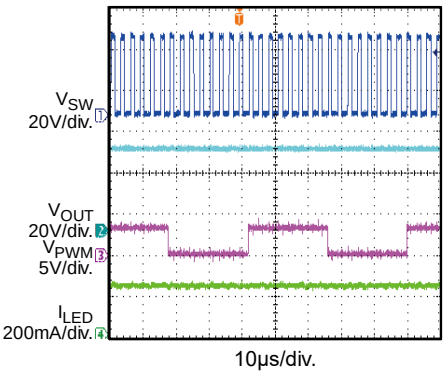
PWM Dimming via the I²C Interface

D_{DIM} = 50%



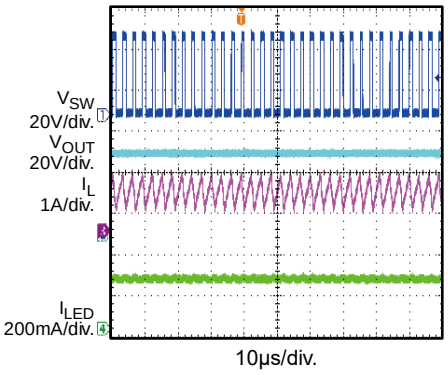
Analog Dimming via the PWM Input

f_{PWM} = 20kHz, D_{PWM} = 50%



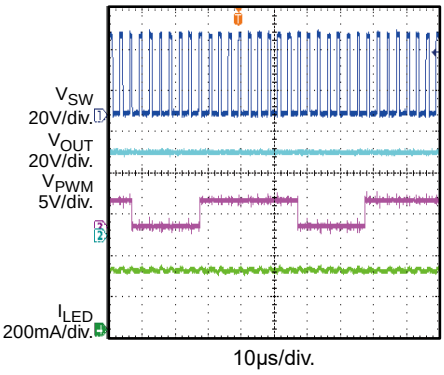
Analog Dimming via the I²C Interface

D_{DIM} = 50%



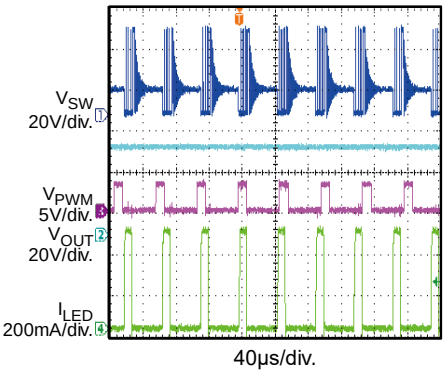
Mixed Dimming via the PWM Input

f_{PWM} = 20kHz, D_{PWM} = 60%



Mixed Dimming via the PWM Input

f_{PWM} = 20kHz, D_{PWM} = 20%

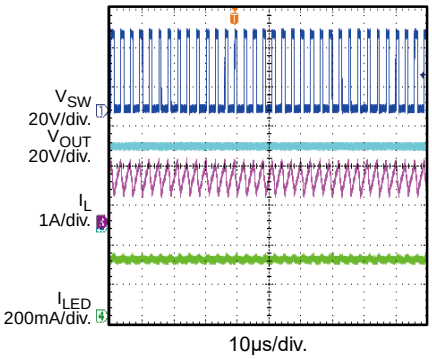


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 3.3V, 120mA/string, 4 strings, 14 LEDs, T_A = 25°C, unless otherwise noted.

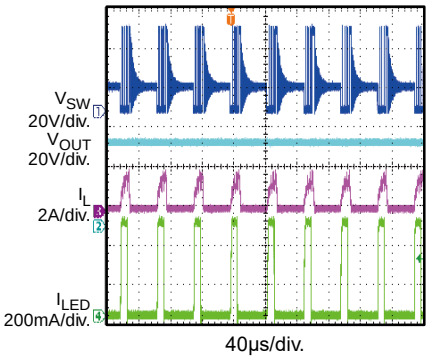
Mixed Dimming via the I²C Interface

D_{DIM} = 60%

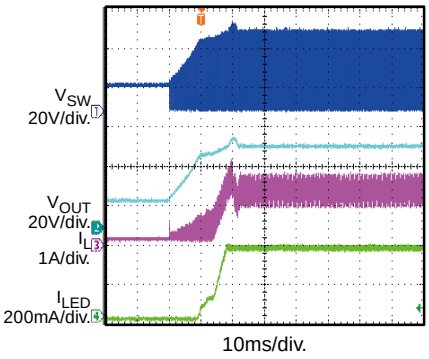


Mixed Dimming via the I²C Interface

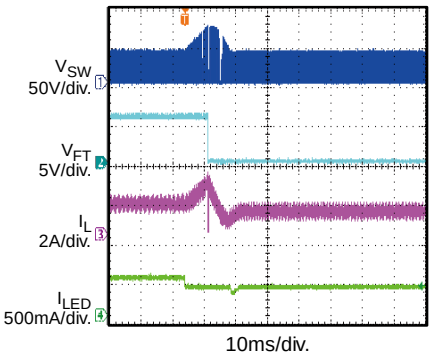
D_{DIM} = 20%



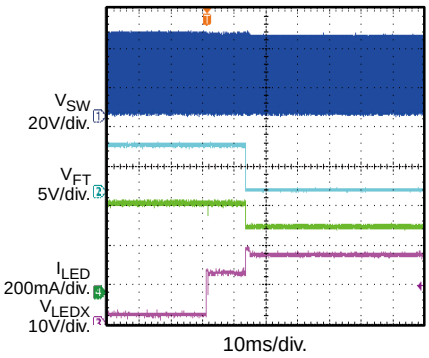
Unused String Protection during Start-Up through VIN



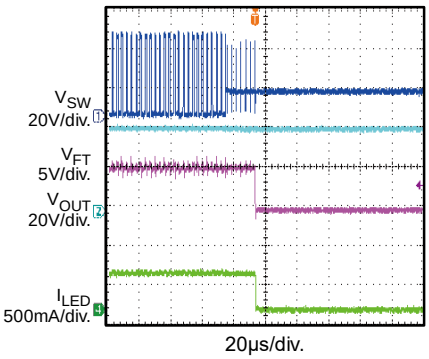
One String Open



One-String Short

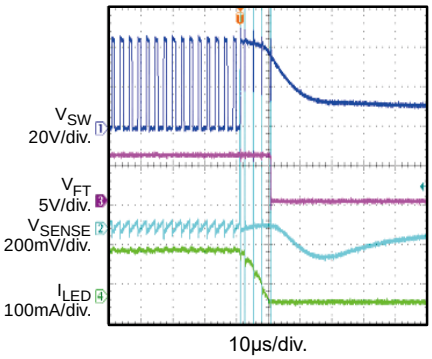


Short Inductor Protection



Short Diode Protection

30mA/string



FUNCTIONAL BLOCK DIAGRAM

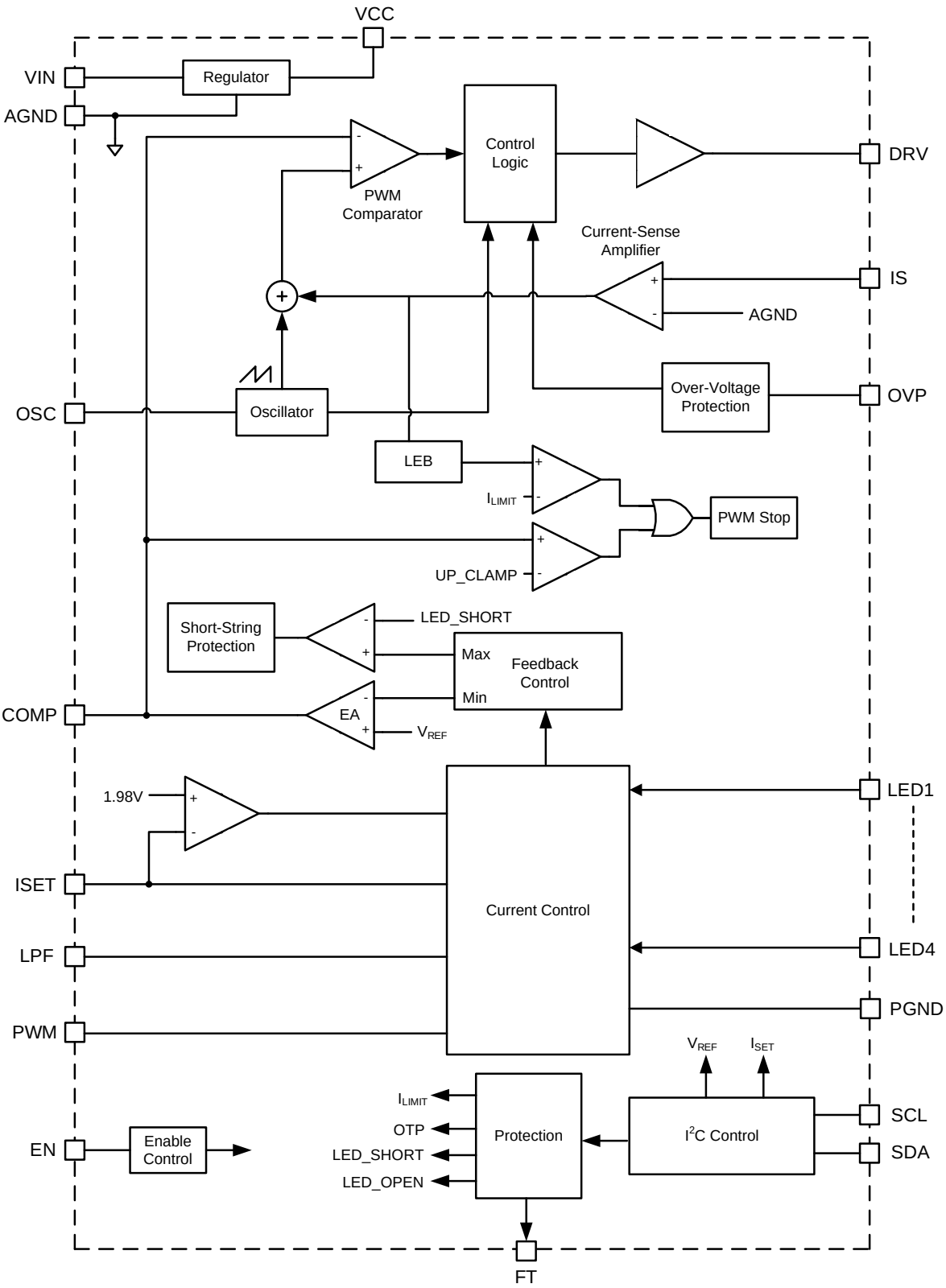


Figure 2: Functional Block Diagram

OPERATION

The MP3385B is a configurable, constant-frequency, peak current control mode, step-up converter with 4-channel regulated current sources to drive an array of four white LED strings. The MP3385B provides an I²C interface for easy communication, which can be used to flexibly set the operation modes.

Internal 6V Regulator

The MP3385B includes an internal linear regulator (VCC). When the input voltage (V_{IN}) exceeds 6.5V, VCC outputs a 6V power supply to the external MOSFET gate driver and the internal control circuitry. The VCC voltage (V_{CC}) drops to 0V when the chip shuts down. The MP3385B features under-voltage lockout (UVLO). The chip is disabled until V_{CC} exceeds the UVLO threshold. The UVLO hysteresis is approximately 340mV.

System Start-Up

When enabled, the MP3385B checks the topology connection first by monitoring the over-voltage protection (OVP) pin. This determines whether a Schottky diode is connected or the boost output is shorted to ground. An OVP voltage exceeding 2.5V allows the chip to switch normally. Otherwise, switching is disabled. The MP3385B checks additional safety limits after passing the OVP test, including LED open and short protection, UVLO, over-temperature protection (OTP), and over-current protection (OCP). If all protection tests pass, then the chip begins boosting the step-up converter with an internal soft start (SS).

Step-Up Converter

At the beginning of each switching cycle, the internal clock turns on the external MOSFET. During normal operation, the minimum turn-on time for the external MOSFET is about 150ns. Add a stabilizing ramp to the current-sense amplifier's output to prevent subharmonic oscillations when the duty cycle exceeds 50%. Then the summed output of the stabilizing ramp and current-sense amplifier is fed into the PWM comparator. When the summed voltage reaches the error amplifier (EA)'s output voltage (V_{COMP}), the external MOSFET turns off.

V_{COMP} is an amplified signal of the difference between the reference voltage (V_{REF}) and the feedback voltage (V_{FB}). The converter automatically chooses the lowest active LEDx pin voltage (V_{LEDx}) to provide a sufficient bus voltage to power all of the LED arrays.

If V_{FB} drops below V_{REF}, then V_{COMP} increases. This results in more current flowing through the MOSFET, increasing the power delivered to the output and forming a closed loop that regulates the output voltage (V_{OUT}).

Under light-load operation, especially if $V_{OUT} \approx V_{IN}$, the converter runs in pulse-skip mode. In this mode, the MOSFET turns on for a minimum on time and then the converter discharges the power to the output for the remaining period. The external MOSFET remains off until V_{OUT} must be boosted again.

Dimming Control

The MP3385B provides three flexible dimming methods: PWM dimming, analog dimming, and mixed dimming.

For PWM dimming, set MODE to 00b. If INTERFACE = 0, the LED current (I_{LED}) duty cycle (D_{ILED}) directly follows the PWM input signal duty cycle (D_{PWM}). If INTERFACE = 1, then the IC works in internal PWM dimming mode, and D_{ILED} is set by internal registers 03h and 04h. The internal dimming frequency is fixed at 23kHz.

For analog dimming, set MODE to 01b. If INTERFACE = 0, the I_{LED} amplitude follows D_{PWM}. If INTERFACE = 1, the IC works in internal analog dimming mode, where the I_{LED} amplitude follows the values of internal registers 03h and 04h.

For mixed dimming, there are two transfer points from analog to PWM dimming (25% or 50%), which can be set via the I²C interface.

If MODE is set to 10b when the dimming duty cycle (D_{DIM}) exceeds the 25% threshold, then the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. If MODE is set to 11b when D_{DIM} exceeds the 50% threshold, then the IC works in analog dimming mode.

Otherwise, the IC works in PWM dimming mode.

If INTERFACE = 0 in mixed dimming mode, then the I_{LED} amplitude is proportional to the external PWM signal ratio when D_{PWM} exceeds the transfer point (25% or 50%). The I_{LED} amplitude is fixed to 100% brightness, while D_{ILED} is equal to the input PWM ratio (if D_{PWM} is below the transfer point). If INTERFACE = 1, then the I_{LED} amplitude and D_{ILED} are set by registers 03h and 04h.

Regardless of the INTERFACE setting (1 or 0), the I_{LED} frequency is fixed at 23kHz in mixed dimming mode when D_{PWM} is below the transfer point (25% or 50%).

To avoid noise at the small dimming ratio, the IC turns off the current sources if the current is below 1.2% of the full-scale current.

For the external PWM signal input dimming modes (INTERFACE = 0), the PWM signal's minimum pulse width is limited to 2µs to avoid noise interruption.

Operating Switching Frequency (f_{SW})

The MP3385B's switching frequency (f_{SW}) can be changed by the OSC resistor (R_{OSC}) and register 01h, FS[3:0]. f_{SW} ranges from 100kHz to 900kHz, and can be set via the I²C register bits when a 100kΩ resistor is connected to the OSC pin. This optimizes the size of the external components and system efficiency.

Open-String Protection

Open-string protection is achieved by detecting the OVP pin voltage and V_{LEDx} (where "LEDx" can be LED1, LED2, LED3, or LED4). If one or more strings are open, then the respective LEDx pins are pulled to ground and the IC continues charging V_{OUT} until it reaches the OVP threshold. If the OVP threshold is triggered, then the chip stops switching and marks off the strings for which V_{LEDx} is below 206mV. Once marked, the remaining LED strings force V_{OUT} back to normal regulation. The string with the largest voltage drop determines the output regulation value.

The MP3385B always attempts to light at least one string. If all strings are open, the MP3385B shuts down the step-up converter. The strings remain in this marked state until the chip resets.

Unused LED String Auto-Detection

If an LED string is open or unused before start-up, the IC automatically detects and marks off the open channel to prevent the output from charging to the OVP threshold. This prevents a start-up failure from LED short-string misprotection caused by OVP being triggered, which is useful for application use and test board debugging. The unused LED string auto-detection function is disabled if the I²C is active and the OVP threshold is changed by the I²C after EN and VIN start-up.

The MP3385B disables the unused LED string by disabling the corresponding register control bit for each 4-channel current source. In some applications, if fewer than four LED strings are required, then the unused LED current sources can be disabled by setting LED[4:0] to 0 in register 00h.

Short-String Protection

The MP3385B monitors V_{LEDx} to determine whether a short-string fault has occurred. If one or more strings are shorted, then the respective LEDx pins tolerate high-voltage stress. If V_{LEDx} exceeds the protection threshold, which is configurable by register 01h, LEDS[2:0], then short-string fault detection is triggered. When a short-string fault remains for longer than 10ms, the fault string is marked off and disabled. Once a string is marked off, it disconnects from the V_{OUT} loop until V_{IN} or EN restarts.

Cycle-by-Cycle Current Limit

To prevent the external components from exceeding their respective current stress ratings, the IC employs cycle-by-cycle current-limit protection. The current limit threshold is configurable from 150mV to 500mV via register 05h, OCP[2:0].

If the current exceeds the current limit threshold and OCPM = 0, the IC latches off until the power is reset or EN is toggled while operating in latch-off mode. If OCPM = 1, the device restarts once the current drops below the current limit again.

Short Inductor and Diode Protection

When the external inductor or diode is shorted, the IC provides protection by detecting the current flowing through the power MOSFET.

Once the current-sense voltage across the sense resistor (connected between IS and GND) reaches the current protection threshold and lasts for four switching cycles, the IC stops switching and latches off.

Thermal Shutdown Protection

The MP3385B monitors the silicon die temperature to prevent the IC from operating at exceedingly high temperatures. If the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down. Once the die temperature drops below the lower threshold, the IC starts up again and resumes normal operation. The hysteresis value is typically 25°C.

Fault Flag Output and Fault Register Indicator

The FT pin is an open drain when the LED driver is in normal operation. FT is connected to VCC via an external 100kΩ resistor, and pulled to logic high when there is no fault. If a fault occurs, FT is pulled to logic low. Set the corresponding fault bit in register 03h to 1.

I²C INTERFACE

I²C Chip Address

After a start (S) command, the I²C-compatible master sends a 7-bit address, followed by an 8th data direction bit (where 1 = read and 0 = write, respectively).

Figure 3 shows the register address to/from which the data is written and read.

0	1	1	0	0	0	1	R/W

Figure 3: I²C-Compatible Device Address

REGISTER MAP

Address	D7	D6	D5	D4	D3	D2	D1	D0
00h	LED4	LED3	LED2	LED1	NA	INTERFACE	MODE1	MODE0
01h	OCPM	LEDS2	LEDS1	LEDS0	FS3	FS2	FS1	FS0
02h	ILED7	ILED6	ILED5	ILED4	ILED3	ILED2	ILED1	ILED0
03h	DIODEO_F	OVP_F	OCP_F	LEDS_F	LEDO_F	OTP_F	DIM1	DIM0
04h	DIM9	DIM8	DIM7	DIM6	DIM5	DIM4	DIM3	DIM2
05h	OVP4	OVP3	OVP2	OVP1	OVP0	OCP2	OCP1	OCP0
06h	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

REG00h

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	LED[4:0]	R/W	1111b	Enables the LED current source. LED1, LED2, LED3, and LED4 control the following internal LED current sources, respectively: LED1: LED current source 1 1 = Enabled 0 = Disabled LED2: LED current source 2 1 = Enabled 0 = Disabled LED3: LED current source 3 1 = Enabled 0 = Disabled LED4: LED current source 4 1= Enabled 0 = Disabled
3	N/A	R/W	N/A	N/A
2	INTERFACE	R/W	0b	Sets the dimming input interface. 0 = Dimming control via the pulse-width modulation (PWM) input signal 1 = Dimming control via the I²C interface
1:0	MODE[1:0]	R/W	00b	Sets the dimming mode. 00 = PWM dimming mode. If INTERFACE = 0, then the I_{LED} duty cycle (D_{ILED}) directly follows the PWM input signal duty cycle (D_{PWM}). If INTERFACE = 1, then the IC works in internal PWM dimming mode and D_{ILED} is set by internal registers 03h and 04h. The internal dimming frequency is fixed at 23kHz. 01 = Analog dimming mode. If INTERFACE = 0, then the I_{LED} amplitude follows D_{PWM}. If INTERFACE = 1, then the I_{LED} amplitude follows the values of internal registers 03h and 04h. 10 = Mixed dimming mode. If the dimming duty cycle (D_{DIM}) exceeds the 25% threshold, then the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. 11 = Mixed dimming mode. If D_{DIM} exceeds the 50% threshold, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode.

REG01h

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	OCPM	R/W	0b	Selects the cycle-by-cycle current limiting mode. 0 = Latch-off mode current limit 1 = Recoverable mode current limit
4:6	LEDS[2:0]	R/W	100b	LED short protection threshold, 1V/step. The default value is 8V. 000 = 4V 001 = 5V 111 = 11V
3:0	FS[3:0]	R/W	0100b	Sets the boost converter switching frequency (f_{SW}). The default f_{SW} is 400kHz. 0000b = Boost converter off 0001b = 100kHz 0010b = 200kHz 0011b = 300kHz 0100b = 400kHz 0101b = 500kHz 0110b = 600kHz 0111b = 700kHz 1000b = 800kHz 1001b = 900kHz

REG02h

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ILED[7:0]	R/W	3Bh	Sets the full-scale I_{LED} value, which corresponds to the 2% to 100% external current value set by a resistor, with 0.39% per step. The default value is 23.5%. 00h~04h = 2% 05h = 2.39% 06h = 2.78% FFh = 100%

REG03h

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	DIODEO_F	R	0b	Diode open fault indication. 1 = Fault 0 = Normal
6	OVP_F	R	0b	Output over-voltage (OV) fault indication. 1 = Fault 0 = Normal
5	OCP_F	R	0b	Converter over-current (OC) fault indication. 1 = Fault 0 = Normal
4	LEDS_F	R	0b	LED string short fault indication. 1 = Fault 0 = Normal
3	LEDO_F	R	0b	LED string open fault indication. 1 = Fault 0 = Normal
2	OTP_F	R	0b	IC over-temperature (OT) fault indication. 1 = Fault 0 = Normal
1:0	DIM[1:0]	R/W	11b	Sets LED dimming brightness, 2 least significant bits (LSB).

REG04h

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	DIM[9:2]	R/W	7Fh	Sets LED dimming brightness, 8 most significant bits (MSB), with 0.098% per step. The default value is 50% dimming brightness.

REG05h

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:3	OVP[4:0]	R/W	11100b	Sets the output over-voltage protection (OVP) threshold based on the OVP pin connected to the LED anode, 2V/step. The default value is 74V. 00000 = 18V 00001 = 20V 11100 = 74V 11111 = 80V
2:0	OCP[2:0]	R/W	111b	Sets the converter over-current protection (OCP) threshold, 50mV/step. The default value is 0.5V. 000 = 0.15V 111 = 0.5V

REG06h

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	ID[7:0]	R	01h	Vendor ID information.

APPLICATION INFORMATION

Selecting the Switching Frequency (f_{SW})

The converter's f_{SW} depends on both R_{OSC} and register 01h, FS[3:0]. If a 100kΩ resistor is selected for R_{OSC} and connected to OSC, then f_{SW} is set from 100kHz to 900kHz via the I²C interface. 0001b to 1001b corresponds to 100kHz to 900kHz, respectively. Table 1 shows the corresponding values between f_{SW} and FS[3:0].

Table 1: Switching Frequencies

FS[3:0]	f_{SW}	Units
0000b	Converter off	--
0001b	100	kHz
0010b	200	
0011b	300	
0100b	400	
0101b	500	
0110b	600	
0111b	700	
1000b	800	
1001b	900	

Without the I²C interface, R_{OSC} sets the internal f_{SW} for the step-up converter, which can be calculated using Equation (1):

$$f_{SW}(kHz) = \frac{40000}{R_{OSC}(k\Omega)} \quad (1)$$

If R_{OSC} is set to 100kΩ, then f_{SW} is 400kHz.

Setting the Full-Scale LED Current

The full-scale I_{LED} amplitude is set via the current-setting resistor on ISET (R_{ISET}) and register 02h, ILED[7:0], which sets the full-scale I_{LED}. The full-scale I_{LED} amplitude can be calculated using Equation (2):

$$I_{LED}(mA) = \frac{20196}{R_{ISET}(k\Omega)} \times K_{FULLSCALE} \quad (2)$$

Where $K_{FULLSCALE}$ is the ratio set by register 02h, ILED[7:0].

Without the I²C interface, the I_{LED} amplitude is set via R_{ISET}, and can be calculated using Equation (3):

$$I_{LED}(mA) = \frac{4633}{R_{ISET}(k\Omega)} \quad (3)$$

If R_{ISET} = 46.4kΩ, then I_{LED} is set to 100mA. Do not leave ISET open.

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply as well as the switching noise from the device. The C_{IN} impedance at f_{SW} should be below the input source impedance to prevent high-frequency switching current from passing through to the input. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low-ESR and small temperature coefficients. For most applications, it is recommended to use a 4.7µF ceramic capacitor in parallel with a 220µF electrolytic capacitor.

Selecting the Inductor and Current-Sense Resistor

A larger-value inductor results in reduced ripple current and peak inductor current (I_{L_PEAK}), which reduces stress on the N-channel MOSFET. However, it also has a larger physical size, higher series resistance, and lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductance (L) to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and good EMI performance.

The required inductance (L) can be calculated using Equation (4):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1\text{-}D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (4)$$

Where I_{LOAD} is the LED load current, η is the efficiency, and D is the switching duty cycle.

D can be calculated using Equation (5):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (5)$$

The switching current is typically used for peak current mode control. To avoid reaching the current limit (I_{LIMIT}), the voltage across the current-sense resistor (R_{SENSE}) must be below 70% of the current limit voltage (V_{SENSE}) in the worst-case scenario. R_{SENSE} can be calculated using Equation (6):

$$R_{SENSE} = \frac{0.7 \times V_{SENSE}}{I_{L\_PEAK}} \quad (6)$$

I_{L_PEAK} can be calculated using Equation (7):

$$I_{L\_PEAK} = \frac{V_{OUT} \times I_{LOAD}}{\eta V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times f_{SW} \times V_{OUT}} \quad (7)$$

V_{SENSE} is set by register 05h, OCP[2:0].

Selecting the Power MOSFET

The MP3385B can drive a wide variety of N-channel MOSFETS. The critical MOSFET selection parameters include maximum drain-to-source voltage (V_{DS_MAX}), maximum current (I_{D_MAX}), on resistance ($R_{DS(ON)}$), gate-source charge (Q_{GS}), gate-drain charge (Q_{GD}), and total gate charge (Q_G).

Ideally, the off-state voltage across the MOSFET is equal to V_{OUT}. Consider the voltage spike when the MOSFET turns off, where V_{DS_MAX} should exceed V_{OUT} by 1.5 times.

The maximum current through the power MOSFET occurs at the minimum V_{IN} (V_{IN_MIN}) and the maximum output power. The maximum RMS current through the MOSFET (I_{RMS_MAX}) can be calculated using Equation (8):

$$I_{RMS\_MAX} = I_{IN\_MAX} \times \sqrt{D_{MAX}} \quad (8)$$

The maximum duty cycle (D_{MAX}) can be calculated using Equation (9):

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN\_MIN}}{V_{OUT}} \quad (9)$$

The MOSFET's current rating should exceed I_{RMS_MAX} by 1.5 times. The MOSFET's $R_{DS(ON)}$ determines the conduction loss (P_{COND}), which can be calculated using Equation (10):

$$P_{COND} = I_{RMS}^{2} \times R_{DS\,(ON)} \times k \quad (10)$$

Where *k* is the MOSFET's temperature coefficient.

The switching loss is related to Q_{GD} and Q_{GS}, which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, and can be read in the V_{GS} vs. Q_G chart in the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage.

These two parameters are required to estimate the turn-on and turn-off losses (P_{SW}), which can be calculated using Equation (11):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW} \quad (11)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, and V_{DS} is the drain-source voltage.

Note that calculating the switching loss is the most difficult part of loss estimation. Equation (11) provides a simplified equation. For more accurate estimates, the equation becomes much more complex. Q_G is used to calculate the gate driver loss (P_{DR}), which can be calculated using Equation (12):

$$P_{DR} = Q_G \times V_{DR} \times f_{SW} \quad (12)$$

Where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the V_{OUT} ripple small and ensures feedback loop stability. C_{OUT} impedance must be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7μF ceramic capacitor in parallel with a 22μF electrolytic capacitor is sufficient.

Setting the Over-Voltage Protection (OVP) Threshold

Open-string protection is achieved through detecting the OVP pin voltage. In some cases, an LED string failure results in V_{FB} remaining at 0V. The MP3385B continues boosting V_{OUT} higher and higher. If V_{OUT} reaches the configured OVP threshold, then OVP is triggered.

To ensure that the chip functions properly, an appropriate V_{OVP} is required. The recommended OVP level is about 1.1 to 1.2 times above V_{OUT} for normal operation. If the OVP pin is connected to the LED load anode, V_{OVP} is set via register 05h, OVP[4:0]. It is not recommended to set the OVP value above 80V, considering the LED return pin voltage rating.

If the MP3385B is utilized for >80V V_{OUT} applications via an external extension, then connect a proper resistor (R_{OVP}) between the LED anode and OVP pins to change the OV level of V_{OVP}. This V_{OVP} level can be calculated with R_{OVP} using Equation (13):

$$V_{OVP}(V)=\frac{R_{OVP}(k\Omega)+1600}{40}\times 1.9 \quad (13)$$

Where register 05h, OVP[4:0] is the default setting.

Expanding LED Channels

The MP3385B expands the number of LED channels by using two or three ICs in parallel. To connect two ICs for a total of eight LED strings, connect the master IC's VCC pins to the slave IC's VCC pins, which powers the slave IC internal logic circuitry. Connect the slave IC's COMP pins to the master IC's COMP pins to regulate the voltage of all eight strings. The slave IC's MOSFET driving signals are not used. The boost converter can only be driven by the master IC. Do not leave the slave IC's IS pin floating; instead, connect it to ground. Apply the EN and DIM signals to both ICs. The master IC's OVP threshold should exceed the slave IC's OVP threshold.

PCB Layout Guidelines

Efficient PCB layout is critical to reduce EMI noise and achieve stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. A high-frequency pulse current flows through the loop between the external MOSFET, output diode, C_{OUT}, R_{SENSE}, and PGND. Keep this loop as short as possible to reduce noise and EMI.
2. Internally connect the IC's exposed pad to the AGND pin, and refer all logic signals to AGND.
3. Externally connect PGND to AGND, routing PGND away from the logic signals.
4. Place the ceramic capacitors for VIN and VCC as close to the IC as possible.

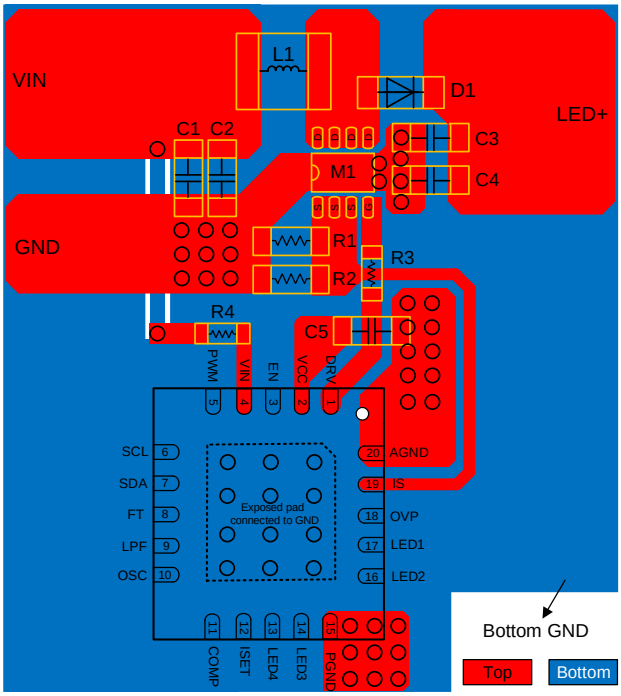


Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

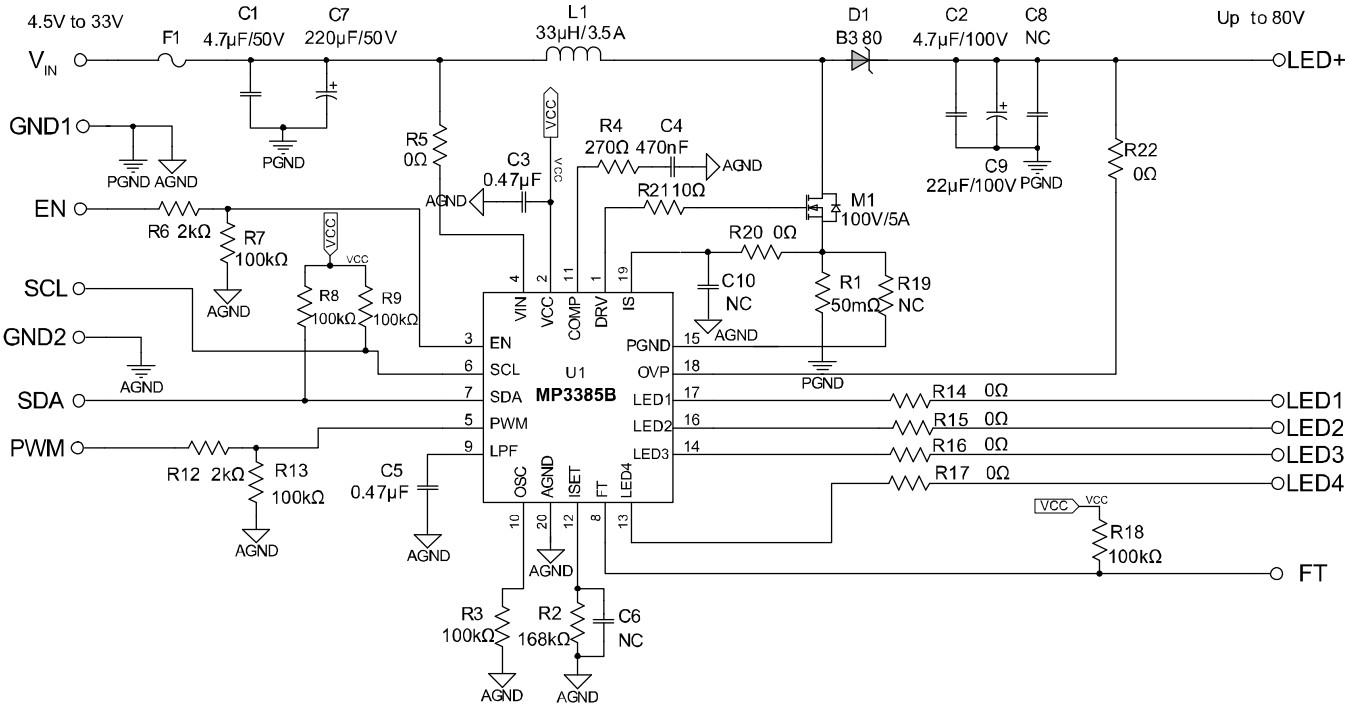


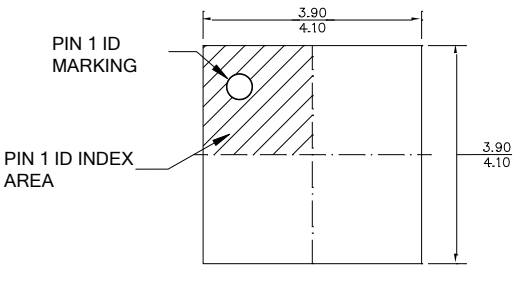
Figure 5: Typical Application Circuit (Driving 4 LED Strings) (7)

Note:

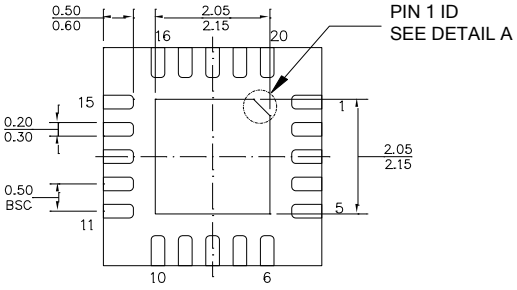
7) Remove the LPF capacitor (C5) when the MP3385B works in direct PWM dimming. Some component values may need to be adjusted for different application conditions.

PACKAGE INFORMATION

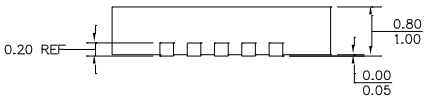
QFN-20 (4mmx4mm)



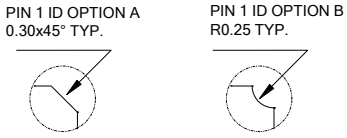
TOP VIEW



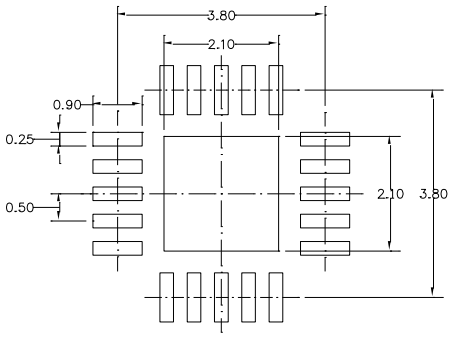
BOTTOM VIEW



SIDE VIEW



DETAIL A

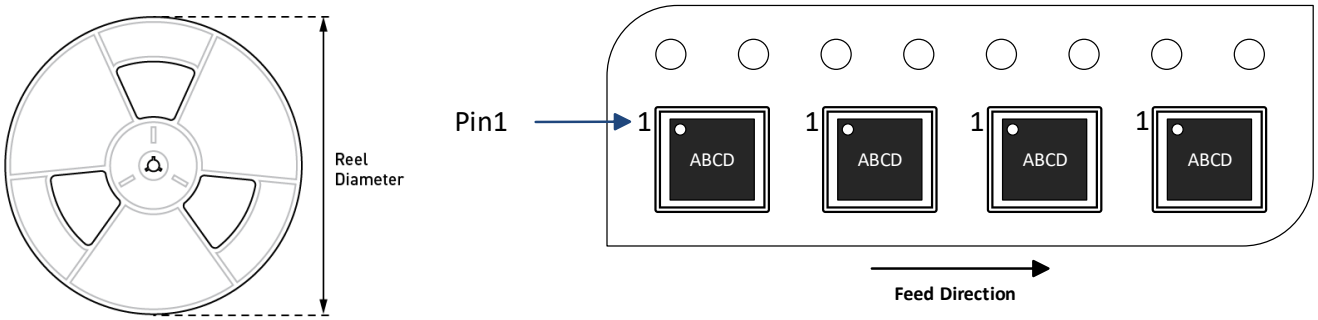


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3385BGR-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/20/2022	Initial Release	-

Mouser Electronics

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Monolithic Power Systems (MPS):

MP3385BGR-P MP3385BGR-Z