MP3326

16 Channels, 50mA/Ch, LED Driver with Separated PWM Analog Dimming and I²C Interface

DESCRIPTION

The MP3326 is a 16-channel WLED driver that can operate from a wide 4V to 16V input voltage range. The MP3326 applies 16 internal current sources in each LED string terminal. The LED current of each channel is set by an external current-setting resistor. The maximum current of each channel is up to 50mA (V_{IN} ≥ 4.5V).

The device integrates an I^2C interface with up to 10 configurable I^2C addresses via an external resistor. This means the MP3326 can support up to 10 cascaded ICs to drive the LED array. Each channel can be enabled or disabled through the I^2C.

The MP3326 employs both separated PWM dimming and analog dimming for each LED channel, as well as 12-bit resolution PWM dimming and 6-bit analog dimming for each channel. To optimize EMI/EMC performance, the LED current ramp rate and phase shift can be configured.

The device can output a refresh signal from the RFSH/FLT pin, and the refresh signal frequency can be set by the register.

Open-load protection, short protection, and over-temperature protection (OTP) are integrated into the device. The fault indicator pulls low if a protection is triggered, and then the corresponding fault register is set.

The MP3326 is available in a QFN-24 (4mmx4mm) package.

FEATURES

- Wide 4V to 16V Input Voltage Range
- 16 Channels, 50mA/Ch Maximum (V_{IN} ≥ 4.5V)
- LED Current Configured by External Resistor
- 6-Bit Analog Dimming for Each Channel
- 12-Bit PWM Dimming for Each Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency
- Refresh Signal Output
- I^2C Interface
- 10 Addresses Configurable via External Resistor
- Configurable LED Current Slew Rate
- 40µs Phase Shift
- Fault Indicator
- LED Open-Load Protection
- LED Short Protection with Configurable Threshold
- Under-Voltage Lockout (UVLO)
- Over-Temperature Protection (OTP)
- ELV Directive II Compliance
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- RGB Drivers
- LED Indicators
- Instrument Clusters
- General Displays
- LED Backlighting

TYPICAL APPLICATION

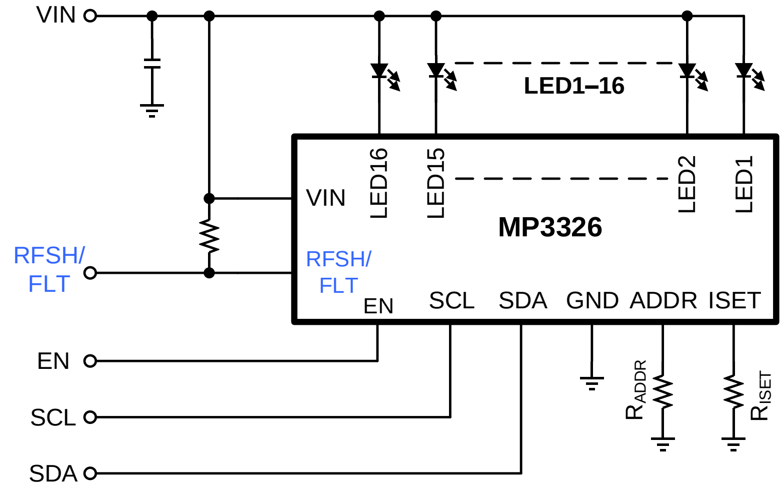


Figure 1: Typical Application Circuit

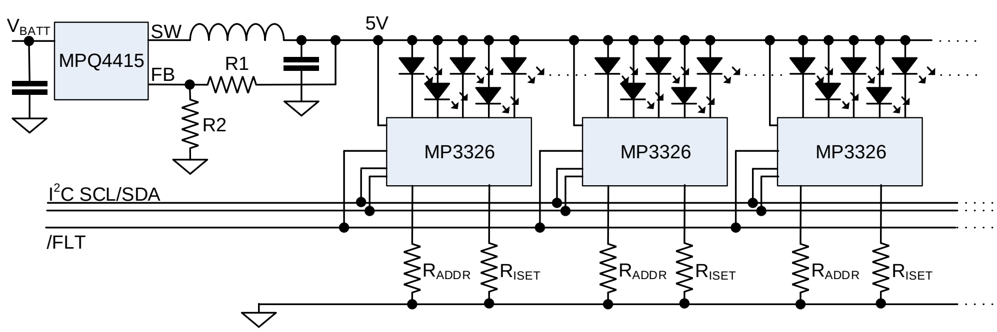


Figure 2: System Application Circuit

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3326GR	QFN-24 (4mmx4mm)	*See Below*	*1*

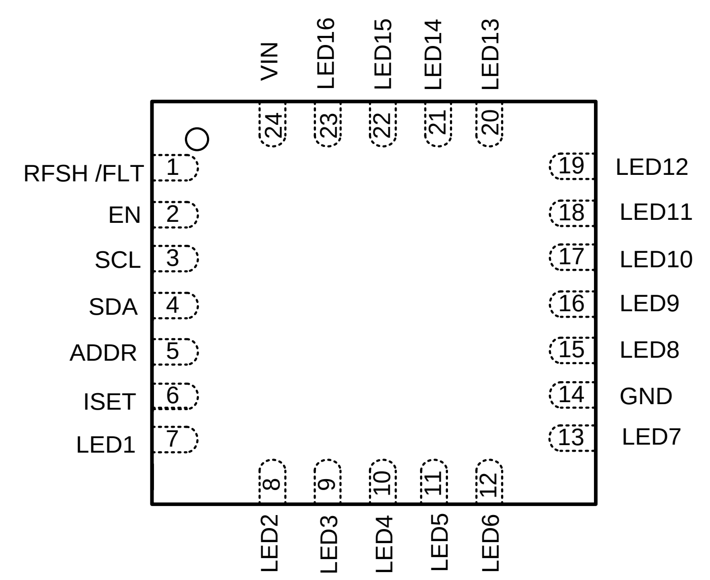
* For Tape & Reel, add suffix –Z (e.g. MP3326GR–Z).

TOP MARKING

MPSYWW
MP3326
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP3326: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If FLTEN = 0, the RFSH/FLT pin outputs a synchronized signal set by the FRFSH register. If FLTEN = 1, the RFSH/FLT pin indicates a fault condition, and this pin is pulled low if a fault is triggered.
2	EN	**Enable.** Pull EN low to disable the IC; pull EN high to enable the IC.
3	SCL	**I^2C interface clock input.**
4	SDA	**I^2C interface data input.**
5	ADDR	**I^2C address setting.** Connect a resistor to ADDR and GND to configure the 4LSB of the I^2C address. There are 10 configurable addresses.
6	ISET	**LED current setting.** Connect a current-setting resistor from this pin to ground to configure the current in each LED string.
7	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin.
8	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin.
9	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin.
10	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin.
11	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin.
12	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin.
13	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin.
14	GND	**Ground.**
15	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin.
16	LED9	**LED channel 9 current input.** Connect the LED channel 9 cathode to this pin.
17	LED10	**LED channel 10 current input.** Connect the LED channel 10 cathode to this pin.
18	LED11	**LED channel 11 current input.** Connect the LED channel 11 cathode to this pin.
19	LED12	**LED channel 12 current input.** Connect the LED channel 12 cathode to this pin.
20	LED13	**LED channel 13 current input.** Connect the LED channel 13 cathode to this pin.
21	LED14	**LED channel 14 current input.** Connect the LED channel 14 cathode to this pin.
22	LED15	**LED channel 15 current input.** Connect the LED channel 15 cathode to this pin.
23	LED16	**LED channel 16 current input.** Connect the LED channel 16 cathode to this pin.
24	VIN	**Power supply input.** VIN supplies the power to the IC, and must be locally bypassed.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ....-0.3V to +18V
V_{LED1} to V_{LED16} ....-0.5V to +18V
All other pins ....-0.3V to +5V
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm).............................. 2.97W

ESD Ratings

Human body model (HBM)...........+1.25kV, -2kV
Charged device model (CDM) .... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....4V to 16V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-24 (4mmx4mm)	42	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 3.5V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage range	V_{IN}		4		16	V
Quiescent supply current	I_Q				4	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 16V			2	μA
Input UVLO threshold	V_{IN_UVLO}	Rising edge	3.45	3.7	3.95	V
		Falling edge	3.15	3.5	3.85	V
Enable						
EN rising threshold	V_{EN_ON}	EN rising	2.1			V
EN falling threshold	V_{EN_OFF}	EN falling			0.8	V
EN pull-down resistor	R_{EN}			1		MΩ
RFSH/FLT						
RFSH/FLT output frequency	f_{RFSH}	FRFSH9:0 = 0x1A9, FPWM2:0 = 01	285	300	315	Hz
RFSH/FLT pull-down resistor		FLTEN = 1, fault is triggered			100	Ω
LED Regulator						
ISET voltage	V_{ISET}		1.174	1.2	1.226	V
LED current	I_{LED}	R_{ISET} = 20kΩ, ICHX, bits[5:0] = 0x3F	-2%	25	+2%	mA
Current sink headroom	V_{LEDX}	I_{LED} = 25mA		150	210	mV
Dimming						
PWM frequency	f_{PWM}		230	245	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		0.97		μs
Phase shift	t_{DELAY}	PS, EN = 1		40		μs
LED current step		I_{LED} = 25mA, analog dimming step		0.4		mA
LED current slew rate in PWM dimming		SLEW, bits [1:0] = 01, rising edge		5		μs
		SLEW, bits [1:0] = 11, rising edge		20		μs
Protection						
LED string short protection threshold	V_{SLP}	STH, bits[1:0] = 01	2.75	3	3.25	V
LED string short protection time	t_{SLP}	V_{LEDX} > STH		4		ms
LED string short protection hiccup time	t_{SLP_HICCUP}			1		ms
LED string short protection hiccup detection time	V_{SLP_DET}			32		μs
LED string open-load protection threshold	V_{LED_UV}			100	160	mV

ELECTRICAL CHARACTERISTICS *(continued)*

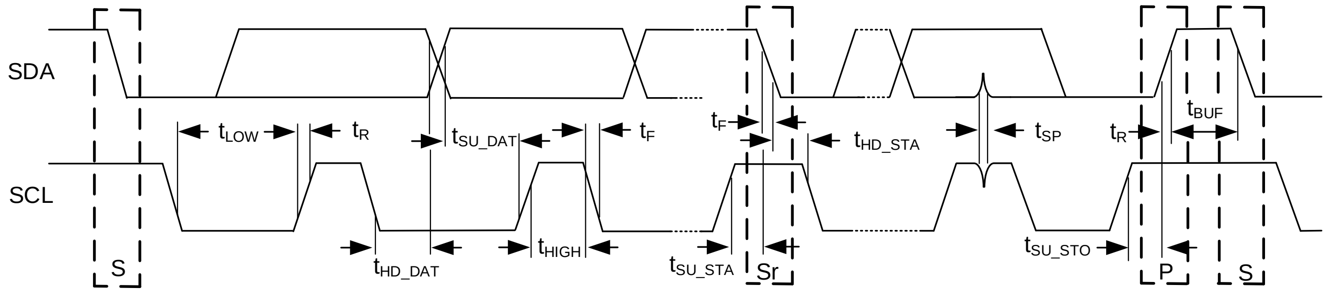
V_{IN} = 5V, V_{EN} = 3.5V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED string open-load protection time	t_{LEDO}	V_{LEDX} < 100mV		4		ms
LED string open-load protection hiccup time	t_{SLP_HICCUP}			1		ms
LED string open-load protection hiccup detection time	V_{SLP_DET}			32		µs
Thermal shutdown threshold (5)	T_{ST}			170		℃
Thermal shutdown hysteresis (5)	T_{ST_HYS}			20		℃
I²C Interface						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				1200	kHz
SCL high time	t_{HIGH}		0.32			µs
SCL low time	t_{LOW}		0.12			µs
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0		0.15	µs
Repeated start set-up time	t_{SU_STA}		0.16			µs
Hold time for start	t_{HD_STA}		0.16			µs
Stop condition set-up time	t_{SU_STO}		0.16			µs
SCL rise time after a repeated start condition and an acknowledge bit	t_{RCL1}		20		160	ns
SCL rise	t_{RCL}		20		80	ns
SCL fall time	t_{FCL}		20		80	ns
SDA rise time	t_{RDA}		20		160	ns
SDA fall time	t_{FDA}		20		160	ns
Pulse width of suppressed spike	t_{SP}		0		10	ns
Capacitance bus for each bus line	C_B				400	pF

Note:

5) Not tested in production. Guaranteed by characterization.

I²C TIMING INTERFACE DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

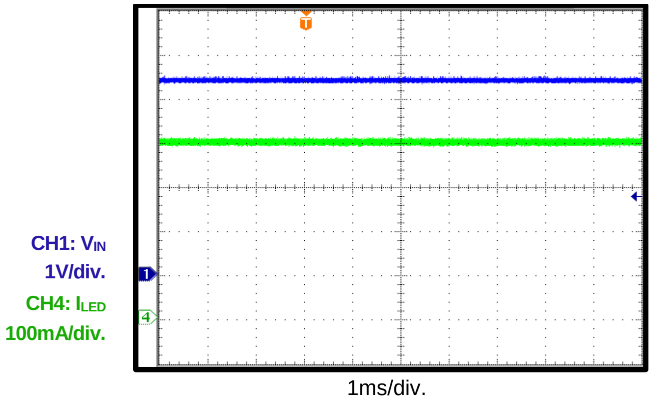
Figure 3: I²C Compatible Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

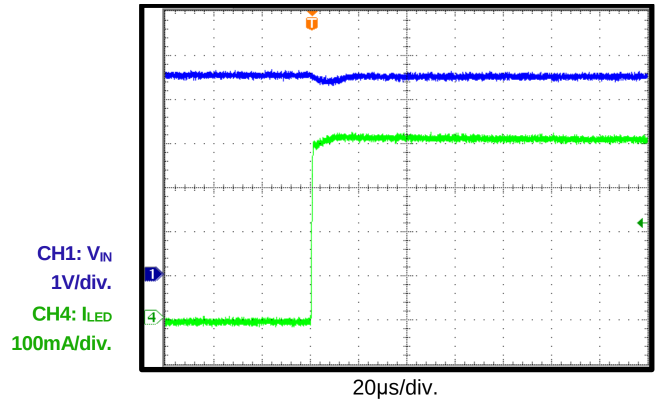
V_{IN} = 4.5V, LED = 16P/1S, I_{SET} = 25mA/string, T_J = 25°C, unless otherwise noted.

Steady State

V_{IN} = 4.5V, 16P1S, 25mA/string

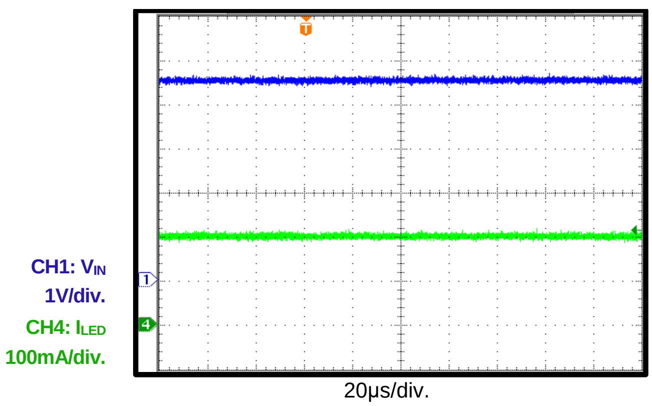


Start-Up through EN_Bit



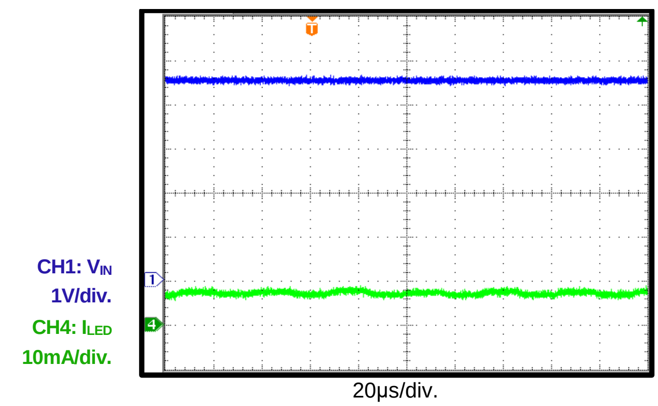
Analog Dimming

12.5mA/string



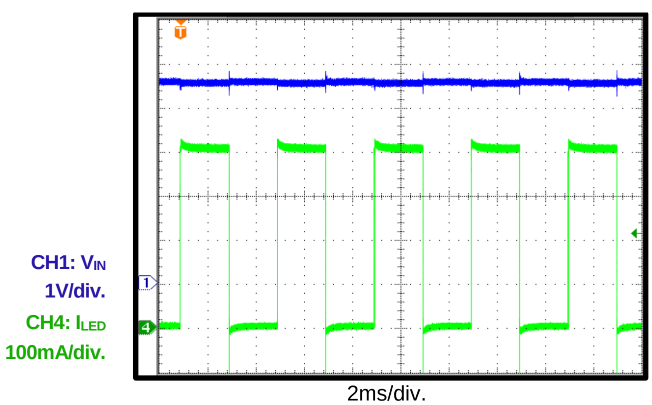
Analog Dimming

0.39mA/string



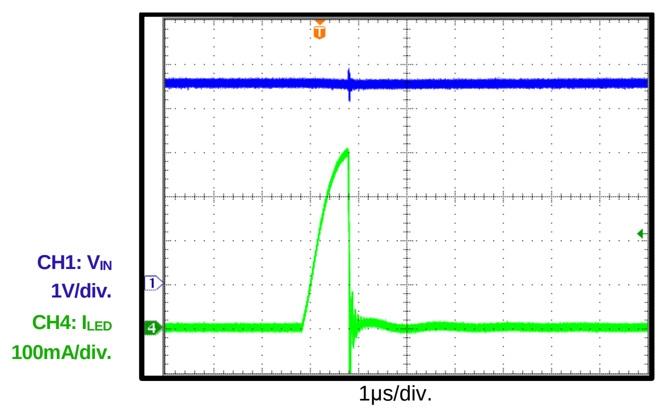
PWM Dimming

PWM duty = 50%



PWM Dimming

PWM duty = 0.024%

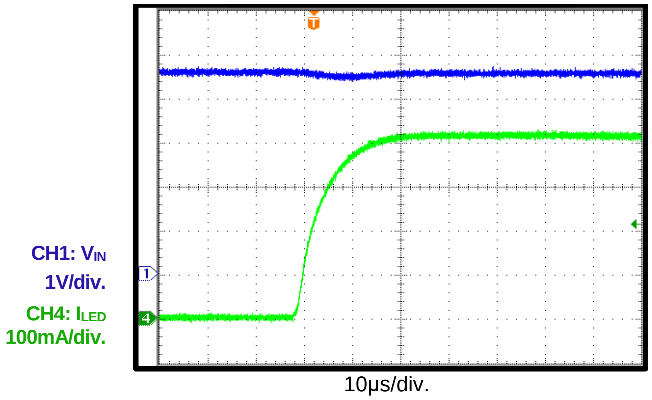


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4.5V, LED = 16P/1S, I_{SET} = 25mA/string, T_J = 25°C, unless otherwise noted.

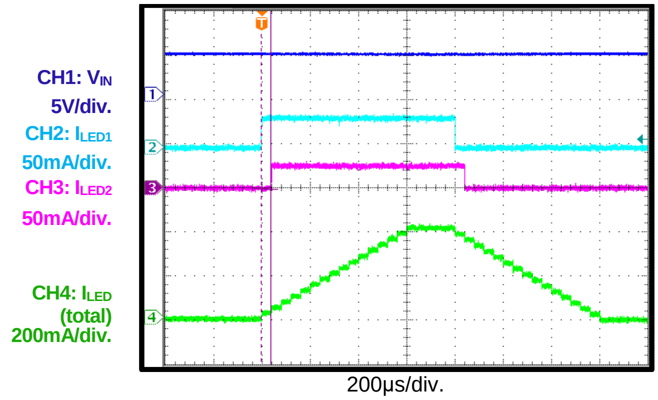
Slew Rate

PWM dimming, slew rate = 5µs



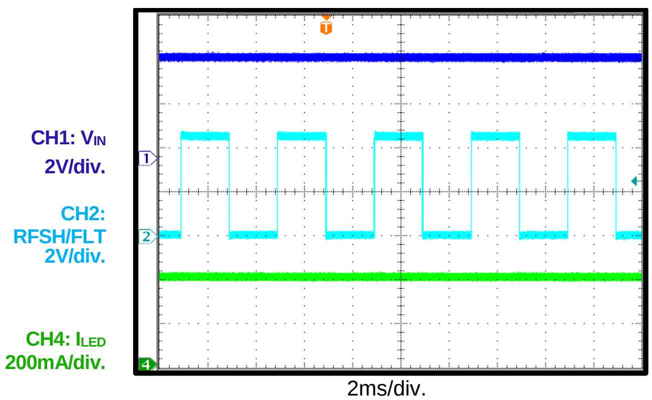
Phase Shift

PWM dimming, duty = 20%



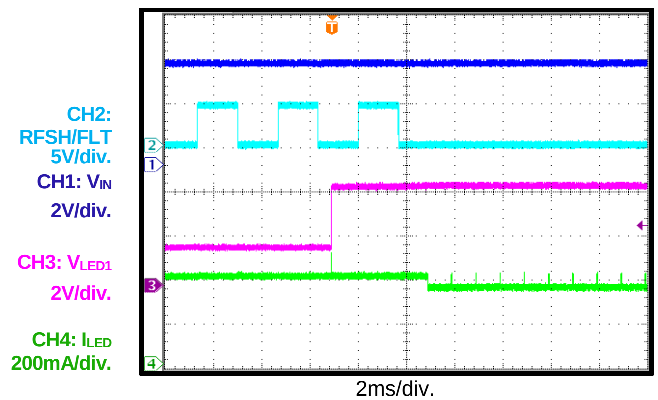
Refresh Function

f_{PWM} = 250Hz, RFRSH = 1FF



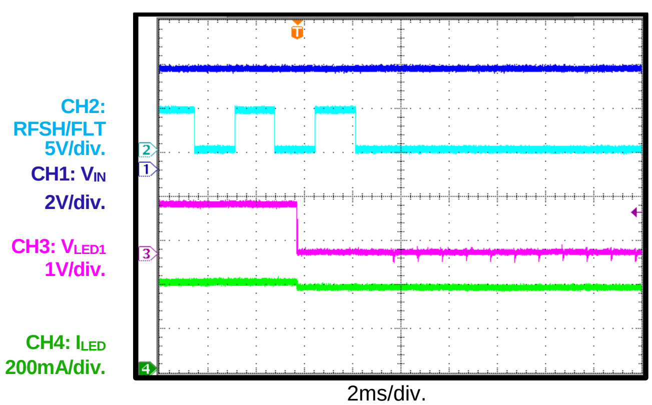
LED Short Protection

RFSH/FLT fault enabled



LED Open-Load Protection

RFSH/FLT fault enabled



FUNCTIONAL BLOCK DIAGRAM

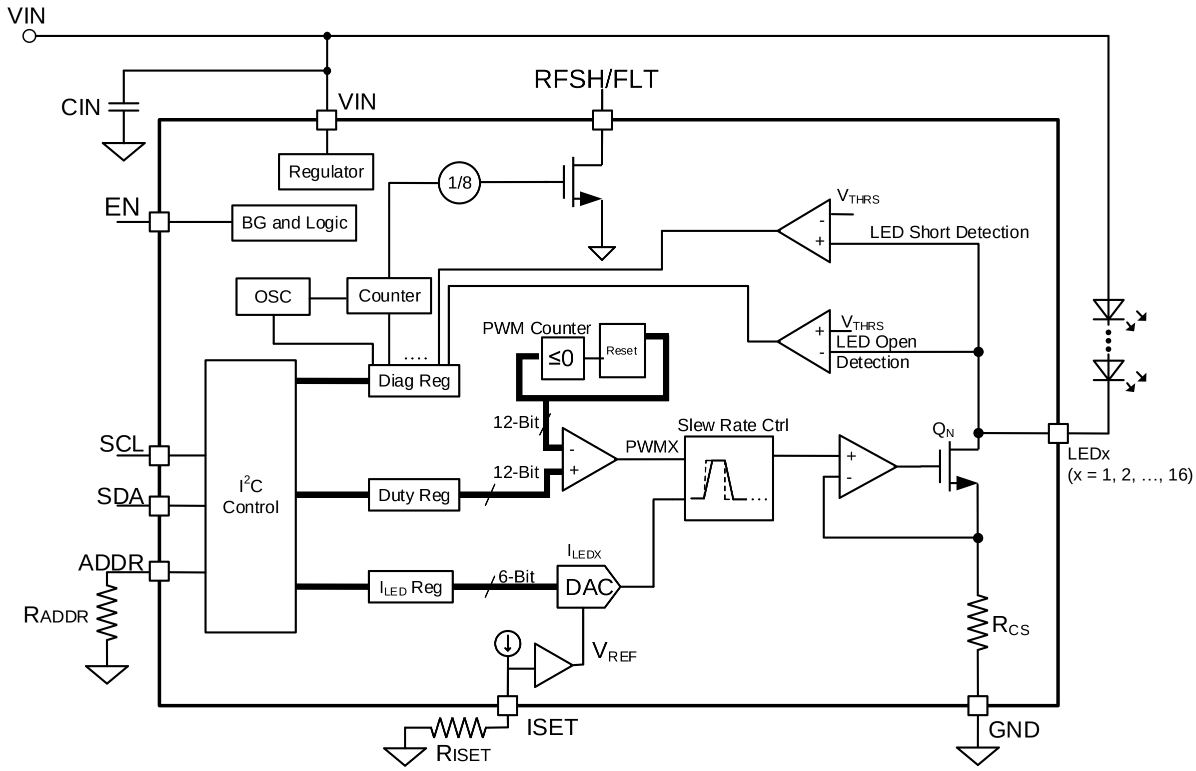


Figure 4: Functional Block Diagram

OPERATION

The MP3326 applies 16 internal current sources in each LED string terminal. The LED current of each channels is set by an external current-setting resistor. The maximum current is 50mA.

Enable (EN) and Start-Up

When the input voltage exceeds the under-voltage lockout (UVLO) threshold and the EN pin exceeds its rising threshold, the MP3326 enters standby mode, and the I²C is active. After setting the I²C register, set the EN bit high to start up the system. The start-up sequence is as follows:

1. VIN
2. EN
3. I²C setting
4. Set EN bit

Channel Selection

The channel can be disabled by setting the corresponding CHxEN bit (e.g. x = 1, 2, ..., 16) low, or by connecting the channel to GND.

Dimming

Each channel has its own 6-bit analog dimming register and 12-bit PWM dimming register. The MP3326 supports analog dimming and PWM dimming for each channel.

In analog dimming, the LED current amplitude changes when the analog dimming register changes. Change the code in the ICHx register (e.g. x = 1, 2, ..., 16) to choose analog dimming for the corresponding channel. The LED current (I_{LED}) amplitude can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times ISET \quad (1)$$

Where ICHx is the analog dimming code for the corresponding channel.

For example, if ICHx = 0, I_{LED} is 0A.

In PWM dimming, LED current is a PWM waveform. The LED current amplitude stays the same, and the LED current duty varies with the PWM dimming register.

The PWM dimming duty is set by the PWMx register (e.g x = 1, 2, ..., 16). The duty can be calculated with Equation (2):

$$D = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the PWM dimming duty code for each corresponding channel. The duty changes only when the 8MSB of PWM duty register are written. When PWMx = 0, the corresponding LED channel current is 0A.

The PWM dimming frequency can be selected via register FPWM1:0. The potential frequencies are listed below:

- FPWM 1:0 = 00, 220Hz
- FPWM 1:0 = 01, 250Hz (default)
- FPWM 1:0 = 10, 280Hz
- FPWM 1:0 = 11, 330Hz

To avoid a glitch during operation, the following conditions must be met:

- Change the FPWM1:0 value only when the EN bit is set 0.
- Write the FPWM register and wait for a 10µs delay before writing other registers.

Phase Shift

A channel-by-channel phase shift function can be implemented. This function is enabled by setting the PS_EN bit high.

When the phase shift function is enabled, the channel x + 1 (e.g. x = 1, 2, ..., 15) LED current rising edge is delayed for 40µs after channel x's LED current rising edge.

SYNC Output for LCD Refresh Frequency

The fault indicator function can be enabled by the FLTEN bit. If FLTEN = 0, the fault indicator function is disabled. RFSH/FLT keeps the output refresh signal even if a protection is triggered.

If FLTEN = 1, the fault indicator function is enabled. The SYNC/FLT pin is pulled low if a protection occurs. Table 1 shows the details of RFSH/FLT pin output status.

Table 1: RFSH/FLT Pin Output Status

FLTEN	RFSH/FLT Pin Output			
	FRFSH = 0x000		FRFSH = 0x001~0x3FF	
	No fault condition	Fault condition	No fault condition	Fault condition
1	Externally pulled high	Low	Rectangle signal	Low
0	Externally pulled high		Rectangle signal	

The refresh signal frequency is set by FRFSH 9:0. If FRFSH 9:0 = 0x000, then the RFSH/FLT pin outputs high. If FRFSH 9:0 = 0x001 to 0x3FF, then the RFSH/FLT pin outputs a rectangle signal, and the refresh frequency can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH9:0} \tag{3}$$

Note that if FPWM1:0 = 01, the PWM dimming frequency is 250Hz. If RFSH 9:0 = 0x000, the RFSH/FLT pin outputs high.

The refresh frequency is also related to the PWM dimming frequency, estimated with Equation (4):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250}(Hz) \tag{4}$$

Where $f_{REFRESH}$ is the refresh frequency, FRFSH is the value of register FRFSH 9:0, and f_{PWM} is PWM dimming frequency set by register FPWM1:0 (it can be either 200Hz, 250Hz, 280Hz, or 330Hz).

For this equation, FRFSH9:0 > 0.

Note that all numbers in the equation have a decimal base, and that the refresh frequency does not change until the 8MSB are written.

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH register sets the counter number (see Figure 5).

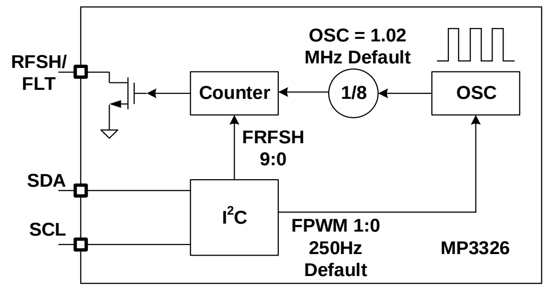


Figure 5: Refresh Frequency Generation

LED Current Slew Rate Control

Changing the LED current's rising/falling slew rate in PWM dimming can optimize EMI performance. The LED current rising/falling slew rate is controlled by the SLEW register, bits[1:0], and can be set to the values listed below:

- SLEW1:0 = 00, no slew rate
- SLEW1:0 = 01, 5µs
- SLEW1:0 = 10, 10µs
- SLEW1:0 = 11, 20µs

Protection

The MP3326 employs VIN under-voltage lockout (UVLO), LED short protection, LED open-load protection, and thermal shutdown.

The /FLT pin is active low, open drain, and should be pulled high to an external voltage source. If a protection is triggered, the corresponding fault bit is set, and /FLT is pulled low.

In hiccup mode, the /FLT pin is pulled high once the fault condition is removed.

In latch-off mode, the /FLT pin is released if all of the fault bits are read.

For LED open-load and short protection, hiccup mode or latch-off mode can be selected by the LATCH bit through the I2C.

If LATCH = 1, the MP3326 is in latch-off mode. This means that if a fault is triggered, the fault channel stays off until VIN or EN is turned off and reset.

If LATCH = 0, the MP3326 is in hiccup mode. In this mode, the fault channel tries to conduct for 32µs to detect if the fault is cleared in every 1ms. /FLT is released if fault condition is removed.

VIN Under-Voltage Lockout (UVLO)

If the input voltage drops to the VIN under-voltage lockout (UVLO) threshold, the IC stops working and all I2C registers are reset.

LED Open-Load Protection

When an LED open fault occurs, the LEDx (e.g. x = 1, 2, ..., 16) voltage drops. If the LEDx voltage drops below the protection threshold (about 100mV) for 4ms, LED open-load protection is triggered. Once this occurs, the fault channel turns off, the corresponding open fault bit CHxO (x = 1, 2, ..., 16) is set, and the /FLT pin is pulled low. The fault bit is reset when it is read, and the /FLT pin is pulled high.

LED Short Protection

If an LED short condition occurs, the VIN - VLEDx voltage drops. If the VLEDx (e.g. x = 1, 2, ..., 16) voltage exceeds the voltage set by STH for 4ms, LED short protection is triggered. Once this occurs, the short channel turns off, the corresponding CHxS fault bit is set, and /FLT pulls low.

The LED short protection threshold is configured by STH 1:0, and can be set to the following values:

- STH1:0 = 00, 2V
- STH1:0 = 01, 3V
- STH1:0 = 10, 4V
- STH1:0 = 11, 5V

The fault bit is reset when it is read, and the /FLT pin is pulled high.

Over-Temperature Protection (OTP)

When the IC temperature exceeds 170°C, over-temperature protection (OTP) is triggered. All channels turn off, the /FLT pin is pulled low, and the FT_OTP bit is set. If the temperature drops by 20°C, the IC recovers, all channels turn on, and the part resumes normal operation.

I2C INTERFACE REGISTER DESCRIPTION

I2C Chip Address

The device address is 0x30~0x39, and is configured by the ADDR resistor. The internal current source flows to the ADDR resistor, then the voltage of ADDR determines the I2C address. 10 different addresses can be configured through the ADDR resistor. Table 2 shows how the I2C address resistor relates to the ISET resistor.

Table 2: I2C Address Setting

R_{ADDR} / R_{ISET}	I2C Address (A3, A2, A1, A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the I2C address first; this address remains the same during operation unless the IC power is reset.

After the start condition, the I2C-compatible master sends a 7-bit address followed by an 8th read (1) or write (0) bit. The 8th bit indicates the register address to/from which the data will be written/read.

0	1	1	A3	A2	A1	A0	R/W

Figure 6: The I2C-Compatible Device Address

To avoid a glitch during operation, ensure that the following conditions are met:

- Change the FPWM1:0 value only when the EN bit is set 0.
- Write the FPWM register and wait for a 10µs delay before writing other registers.

REGISTER MAP

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	01	RESERVED						FPWM 1:0	
01H	00	FLTEN	LATCH	STH1:0		SLEW1:0		PS_EN	EN
02H	01	RESERVED					FT_OTP	FRFSH1:0	
03H	6A	FRFSH 9:2							
04H	FF	CH16EN	CH15EN	CH14EN	CH13EN	CH12EN	CH11EN	CH10EN	CH9EN
05H	FF	CH8EN	CH7EN	CH6EN	CH5EN	CH4EN	CH3EN	CH2EN	CH1EN
06H	00	CH16O	CH15O	CH14O	CH13O	CH12O	CH11O	CH10O	CH9O
07H	00	CH8O	CH7O	CH6O	CH5O	CH4O	CH3O	CH2O	CH1O
08H	00	CH16S	CH15S	CH14S	CH13S	CH12S	CH11S	CH10S	CH9S
09H	00	CH8S	CH7S	CH6S	CH5S	CH4S	CH3S	CH2S	CH1S
0AH	3F	RESERVED		ICH1 5:0					
0BH	0F	RESERVED				PWM1 3:0			
0CH	FF	PWM1 11:4							
0DH	3F	RESERVED		ICH2 5:0					
0EH	0F	RESERVED				PWM2 3:0			
0FH	FF	PWM2 11:4							
10H	3F	RESERVED		ICH3 5:0					
11H	0F	RESERVED				PWM3 3:0			
12H	FF	PWM3 11:4							
13H	3F	RESERVED		ICH4 5:0					
14H	0F	RESERVED				PWM4 3:0			

REGISTER MAP *(continued)*

Add	Default	D7	D6	D5	D4	D3	D2	D1	D0
15H	FF	PWM4[11:4]							
16H	3F	RESERVED		ICH5[5:0]					
17H	0F	RESERVED				PWM5[3:0]			
18H	FF	PWM5[11:4]							
19H	3F	RESERVED		ICH6[5:0					
1aH	0F	RESERVED				PWM6[3:0]			
1BH	FF	PWM6[11:4]							
1CH	3F	RESERVED		ICH7[5:0]					
1DH	0F	RESERVED				PWM7[3:0]			
1EH	FF	PWM7[11:4]							
1FH	3F	RESERVED		ICH8[5:0]					
20H	0F	RESERVED				PWM8[3:0]			
21H	FF	PWM8[11:4]							
22H	3F	RESERVED		ICH9[5:0]					
23H	0F	RESERVED				PWM9[3:0]			
24H	FF	PWM9[11:4]							
25H	3F	RESERVED		ICH10[5:0]					
26H	0F	RESERVED				PWM10[3:0]			
27H	FF	PWM10[11:4]							
28H	3F	RESERVED		ICH11[5:0]					
29H	0F	RESERVED				PWM11[3:0]			

REGISTER MAP *(continued)*

<table>
<tr><th>Add</th><th>Default</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>2AH</td><td>FF</td><td colspan="8">PWM11[11:4]</td></tr>
<tr><td>2BH</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH12[5:0]</td></tr>
<tr><td>2CH</td><td>0F</td><td colspan="4">RESERVED</td><td colspan="4">PWM12[3:0]</td></tr>
<tr><td>2DH</td><td>FF</td><td colspan="8">PWM12[11:4]</td></tr>
<tr><td>2EH</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH13[5:0]</td></tr>
<tr><td>2FH</td><td>0F</td><td colspan="4">RESERVED</td><td colspan="4">PWM13[3:0]</td></tr>
<tr><td>30H</td><td>FF</td><td colspan="8">PWM13[11:4]</td></tr>
<tr><td>31H</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH14[5:0]</td></tr>
<tr><td>32H</td><td>0F</td><td colspan="4">RESERVED</td><td colspan="4">PWM14[3:0]</td></tr>
<tr><td>33H</td><td>FF</td><td colspan="8">PWM14[11:4]</td></tr>
<tr><td>34H</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH15[5:0]</td></tr>
<tr><td>35H</td><td>0F</td><td colspan="4">RESERVED</td><td colspan="4">PWM15[3:0]</td></tr>
<tr><td>36H</td><td>FF</td><td colspan="8">PWM15[11:4]</td></tr>
<tr><td>37H</td><td>3F</td><td colspan="2">RESERVED</td><td colspan="6">ICH16[5:0]</td></tr>
<tr><td>38H</td><td>0F</td><td colspan="4">RESERVED</td><td colspan="4">PWM16[3:0]</td></tr>
<tr><td>39H</td><td>FF</td><td colspan="8">PWM16[11:4]</td></tr>
</table>

PWM Dimming Frequency Setting Register

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:2	RESERVED	R	000000	Reserved.
1:0	FPWM	R/W	01	PWM dimming frequency (f_{PWM}) setting bit. 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz The following conditions must be met to avoid glitches: • Change the FPWM setting only when the EN bit is set 0. • Write the FPWM register, then wait for 10µs before writing other registers.

Control Register

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	FLTEN	R/W	0	RFSH/FLT pin fault indicator enable bit. 0: Disabled. The RFSH/FLT pin refreshes the signal output 1: Enabled
6	LATCH	R/W	1	Latch-off fault response enable bit. 0: Disabled. The device enters hiccup mode if a fault condition is detected 1: Enabled
5:4	S_TH[1:0]	R/W	00	LED short protection threshold setting register. 00: 2V 01: 3V 10: 4V 11: 5V
3:2	SLEW[1:0]	R/W	00	LED current slew rate setting register. 00: No slew rate 01: 5µs 10: 10µs 11: 20µs
1	PS_EN	R/W	0	Phase shift enable bit. 0: Disable the phase shift function 1: Enable the phase shift function. The rising edge of channel x + 1 occurs 40µs after channel x (e.g. x = 1, 2, ..., 15)
0	EN	R/W	0	Enable bit. 0: Disable the IC 1: Enable the IC

Refresh Frequency Setting and OTP Fault Register

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:3	RESERVED	R	0	Reserved.
2	FT_OTP	R	0	Over-temperature (OT) fault indication bit. 0: An OT fault has not occurred 1: An OT fault has occurred
1:0	FRFSH[1:0]	R/W	01	Refresh frequency setting register, 2LSB. If FPWM[1:0] = 01, the PWM dimming frequency is 250Hz. If RFSH[9:0] = 0x000, the RFSH/FLT pin outputs high If FRFSH[9:0] = 0x001 to 0x3FF, $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} (Hz)$ All numbers in the above equation are decimal-based. The refresh frequency does not change until the 8MSB are written. The default $f_{REFRESH}$ value is 300Hz.

Refresh Frequency Setting Register

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	FRFSH[9:2]	R/W	6A	Refresh frequency setting register, 2LSB. If FPWM[1:0] = 01, the PWM dimming frequency is 250Hz. If RFSH[9:0] = 0x000, the RFSH/FLT pin outputs high If FRFSH[9:0] = 0x001 to 0x3FF, $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} (Hz)$ All numbers in the above equation are decimal-based. The refresh frequency does not change until the 8MSB are written. The default $f_{REFRESH}$ is 300Hz.

Channel Enable Register (Channels 9–16)

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH16EN	R/W	1	Channel 16 enable bit. 0: Disabled 1: Enabled
6	CH15EN	R/W	1	Channel 15 enable bit. 0: Disabled 1: Enabled
5	CH14EN	R/W	1	Channel 14 enable bit. 0: Disabled 1: Enabled

4	CH13EN	R/W	1	Channel 13 enable bit. 0: Disabled 1: Enabled
3	CH12EN	R/W	1	Channel 12 enable bit. 0: Disabled 1: Enabled
2	CH11EN	R/W	1	Channel 11 enable bit. 0: Disabled 1: Enabled
1	CH10EN	R/W	1	Channel 10 enable bit. 0: Disabled 1: Enabled
0	CH9EN	R/W	1	Channel 9 enable bit. 0: Disabled 1: Enabled

Channel Enable Register (Channels 1–8)

Addr: 0x05				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH8EN	R/W	1	Channel 8 enable bit. 0: Disabled 1: Enabled
6	CH7EN	R/W	1	Channel 7 enable bit. 0: Disabled 1: Enabled
5	CH6EN	R/W	1	Channel 6 enable bit. 0: Disabled 1: Enabled
4	CH5EN	R/W	1	Channel 5 enable bit. 0: Disabled 1: Enabled
3	CH4EN	R/W	1	Channel 4 enable bit. 0: Disabled 1: Enabled
2	CH3EN	R/W	1	Channel 3 enable bit. 0: Disabled 1: Enabled
1	CH2EN	R/W	1	Channel 2 enable bit. 0: Disabled 1: Enabled
0	CH1EN	R/W	1	Channel 1 enable bit. 0: Disabled 1: Enabled

Channel Open Fault Register (Channels 9–16)

Addr: 0x06				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH16O	R	0	Channel 16 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
6	CH15O	R	0	Channel 15 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
5	CH14O	R	0	Channel 14 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
4	CH13O	R	0	Channel 13 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
3	CH12O	R	0	Channel 12 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
2	CH11O	R	0	Channel 11 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
1	CH10O	R	0	Channel 10 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
0	CH9O	R	0	Channel 9 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred

Channel Open Fault Register (Channels 1–8)

Addr: 0x07				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH8O	R	0	Channel 8 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
6	CH7O	R	0	Channel 7 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
5	CH6O	R	0	Channel 6 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
4	CH5O	R	0	Channel 5 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred

3	CH4O	R	0	Channel 4 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
2	CH3O	R	0	Channel 3 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
1	CH2O	R	0	Channel 2 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred
0	CH1O	R	0	Channel 1 open-load protection fault flag. 0: No open-load fault has occurred 1: An open-load fault has occurred

Channel Short Fault Register (Channels 9–16)

Addr: 0x08				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH16S	R	0	Channel 16 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
6	CH15S	R	0	Channel 15 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
5	CH14S	R	0	Channel 14 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
4	CH13S	R	0	Channel 13 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
3	CH12S	R	0	Channel 12 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
2	CH11S	R	0	Channel 11 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
1	CH10S	R	0	Channel 10 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred
0	CH9S	R	0	Channel 9 short protection fault flag. 0: No short fault has occurred 1: A short fault has occurred

Channel Short Fault Register (Channels 1–8)

Addr: 0x09				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	CH8S	R	0	Channel 8 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
6	CH7S	R	0	Channel 7 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
5	CH6S	R	0	Channel 6 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
4	CH5S	R	0	Channel 5 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
3	CH4S	R	0	Channel 4 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
2	CH3S	R	0	Channel 3 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
1	CH2S	R	0	Channel 2 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred
0	CH1S	R	0	Channel 1 short protection fault flag. 0: No short fault has occurred 1: A fault has occurred

Channel 1 LED Current Setting Register

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH1[5:0]	R/W	111111	Channel 1 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 1 PWM Dimming Duty Setting Register (LSB)

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM1[3:0]	R/W	1111	Channel 1 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 1 PWM Dimming Duty Setting Register (MSB)

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM1[11:4]	R/W	11111111	Channel 1 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 2 LED Current Setting Register

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH2[5:0]	R/W	111111	Channel 2 LED current analog dimming register. The current can be calculated with the following equation: $$I_{LED}=\frac{Code}{63}\times ISET$$

Channel 2 PWM Dimming Duty Setting Register (LSB)

Addr: 0x0E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM2[3:0]	R/W	1111	Channel 2 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 2 PWM Dimming Duty Setting Register (MSB)

Addr: 0x0F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM2[11:4]	R/W	11111111	Channel 2 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 3 LED Current Setting Register

Addr: 0x10				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH3[5:0]	R/W	111111	Channel 3 LED current analog dimming register. The current can be calculated with the following equation: $$I_{LED}=\frac{Code}{63}\times ISET$$

Channel 3 PWM Dimming Duty Setting Register (LSB)

Addr: 0x11				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM3[3:0]	R/W	1111	Channel 3 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 3 PWM Dimming Duty Setting Register (MSB)

Addr: 0x12				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM3[11:4]	R/W	11111111	Channel 3 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 4 LED Current Setting Register

Addr: 0x13				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH4[5:0]	R/W	111111	Channel 4 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 4 PWM Dimming Duty Setting Register (LSB)

Addr: 0x14				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM4[3:0]	R/W	1111	Channel 4 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 4 PWM Dimming Duty Setting Register (MSB)

Addr: 0x15				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM4[11:4]	R/W	11111111	Channel 4 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 5 LED Current Setting Register

Addr: 0x16				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH5[5:0]	R/W	111111	Channel 5 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 5 PWM Dimming Duty Setting Register (LSB)

Addr: 0x17				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM5[3:0]	R/W	1111	Channel 5 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 5 PWM Dimming Duty Setting Register (MSB)

Addr: 0x18				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM5[11:4]	R/W	11111111	Channel 5 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 6 LED Current Setting Register

Addr: 0x19				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH6[5:0]	R/W	111111	Channel 6 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times ISET$

Channel 6 PWM Dimming Duty Setting Register (LSB)

Addr: 0x1A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM6[3:0]	R/W	1111	Channel 6 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 6 PWM Dimming Duty Setting Register (MSB)

Addr: 0x1B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM6[11:4]	R/W	11111111	Channel 6 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 7 LED Current Setting Register

Addr: 0x1C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH7[5:0]	R/W	111111	Channel 7 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times ISET$

Channel 7 PWM Dimming Duty Setting Register (LSB)

Addr: 0x1D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM7[3:0]	R/W	1111	Channel 7 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 7 PWM Dimming Duty Setting Register (MSB)

Addr: 0x1E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM7[11:4]	R/W	11111111	Channel 7 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 8 LED Current Setting Register

Addr: 0x1F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH8[5:0]	R/W	111111	Channel 8 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 8 PWM Dimming Duty Setting Register (LSB)

Addr: 0x20				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM8[3:0]	R/W	1111	Channel 8 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 8 PWM Dimming Duty Setting Register (MSB)

Addr: 0x21				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM8[11:4]	R/W	11111111	Channel 8 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 9 LED Current Setting Register

Addr: 0x22				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH9[5:0]	R/W	111111	Channel 9 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 9 PWM Dimming Duty Setting Register (LSB)

Addr: 0x23				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM9[3:0]	R/W	1111	Channel 9 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 9 PWM Dimming Duty Setting Register (MSB)

Addr: 0x24				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM9[11:4]	R/W	11111111	Channel 9 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 10 LED Current Setting Register

Addr: 0x25				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH10[5:0]	R/W	111111	Channel 10 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 10 PWM Dimming Duty Setting Register (LSB)

Addr: 0x26				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM10[3:0]	R/W	1111	Channel 10 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 10 PWM Dimming Duty Setting Register (MSB)

Addr: 0x27				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM10[11:4]	R/W	11111111	Channel 10 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 11 LED Current Setting Register

Addr: 0x28				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH11[5:0]	R/W	111111	Channel 11 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 11 PWM Dimming Duty Setting Register (LSB)

Addr: 0x29				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM11[3:0]	R/W	1111	Channel 11 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 11 PWM Dimming Duty Setting Register (MSB)

Addr: 0x2A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM11[11:4]	R/W	11111111	Channel 11 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 12 LED Current Setting Register

Addr: 0x2B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH12[5:0]	R/W	111111	Channel 12 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 12 PWM Dimming Duty Setting Register (LSB)

Addr: 0x2C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM12[3:0]	R/W	1111	Channel 12 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 12 PWM Dimming Duty Setting Register (MSB)

Addr: 0x2D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM12[11:4]	R/W	11111111	Channel 12 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 13 LED Current Setting Register

Addr: 0x2E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH13[5:0]	R/W	111111	Channel 13 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 13 PWM Dimming Duty Setting Register (LSB)

Addr: 0x2F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM13[3:0]	R/W	1111	Channel 13 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 13 PWM Dimming Duty Setting Register (MSB)

Addr: 0x30				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM13[11:4]	R/W	11111111	Channel 13 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 14 LED Current Setting Register

Addr: 0x31				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH14[5:0]	R/W	111111	Channel 14 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 14 PWM Dimming Duty Setting Register (LSB)

Addr: 0x32				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM14[3:0]	R/W	1111	Channel 14 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 14 PWM Dimming Duty Setting Register (MSB)

Addr: 0x33				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM14[11:4]	R/W	11111111	Channel 14 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 15 LED Current Setting Register

Addr: 0x34				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH15[5:0]	R/W	111111	Channel 15 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 15 PWM Dimming Duty Setting Register (LSB)

Addr: 0x35				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM15[3:0]	R/W	1111	Channel 15 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 15 PWM Dimming Duty Setting Register (MSB)

Addr: 0x36				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM15[11:4]	R/W	11111111	Channel 15 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

Channel 16 LED Current Setting Register

Addr: 0x37				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	R	00	Reserved.
5:0	ICH16[5:0]	R/W	111111	Channel 16 LED current analog dimming register. The current can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times ISET$

Channel 16 PWM Dimming Duty Setting Register (LSB)

Addr: 0x38				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:4	RESERVED	R	0000	Reserved.
3:0	PWM16[3:0]	R/W	1111	Channel 16 LED current PWM dimming duty setting register, 4LSB. The dimming duty only changes when the 8MSB are written.

Channel 16 PWM Dimming Duty Setting Register (MSB)

Addr: 0x39				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	PWM16[11:4]	R/W	11111111	Channel 16 LED current PWM dimming duty setting register, 8MSB. The dimming duty only changes when the 8MSB are written.

APPLICATION INFORMATION

LED Current Setting

Connect a resistor from the ISET pin to GND to set the LED current for all 16 channels. The LED current (I_{LED}) can be calculated with Equation (5):

$$I_{LED}(mA) = \frac{500}{R_{ISET}(k\Omega)} \quad (5)$$

For a maximum 50mA I_{LED}, ensure that $V_{IN} \geq 4.5V$ to power the IC.

PCB Layout Guidelines

The traces from the LED anode to the LEDx pins must be wide enough to support the set current (up to 50mA) (see Figure 6).

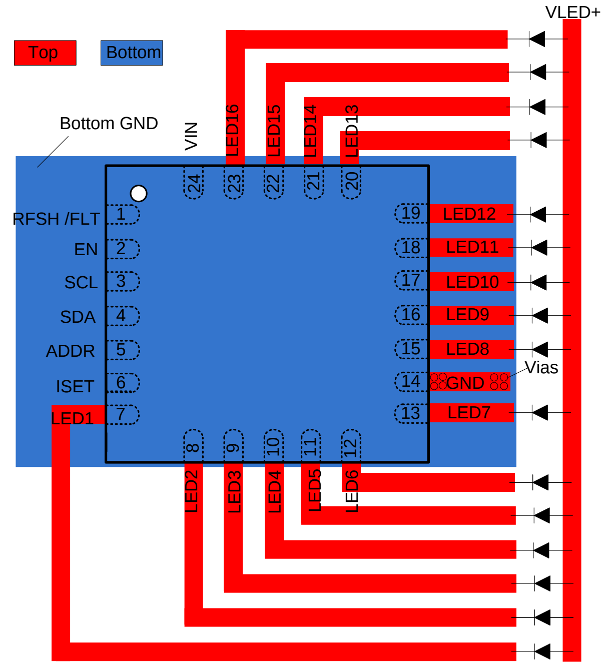


Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

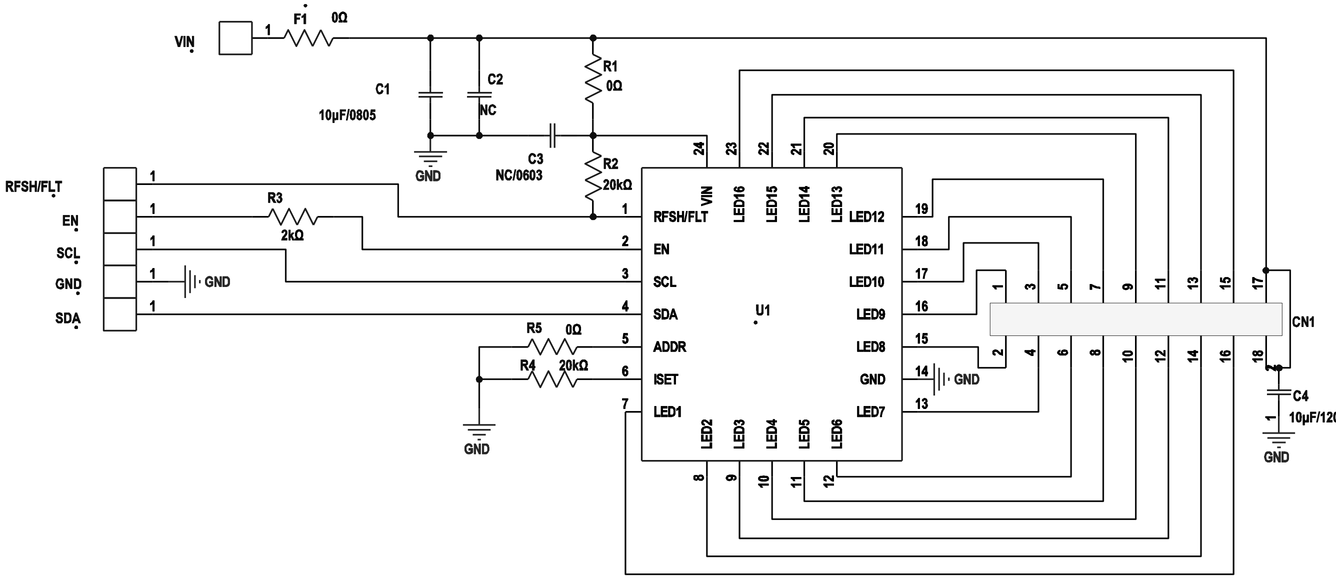


Figure 7: Typical Application Circuit

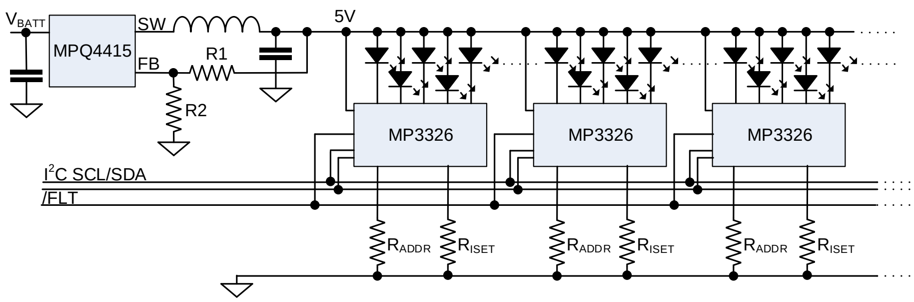
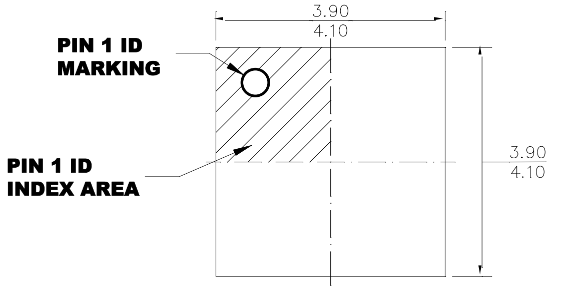


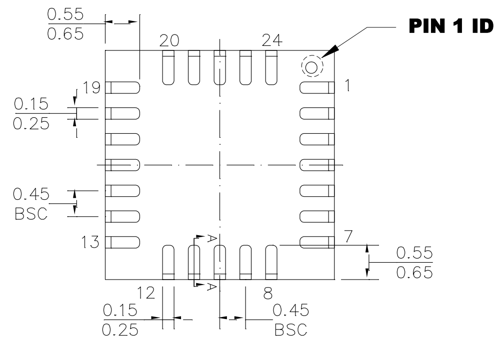
Figure 8: Typical System Application Circuit

PACKAGE INFORMATION

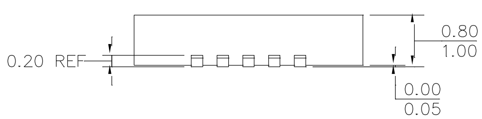
QFN-24 (4mmx4mm) with Wettable Flank



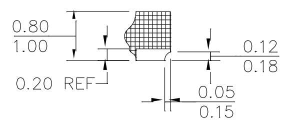
TOP VIEW



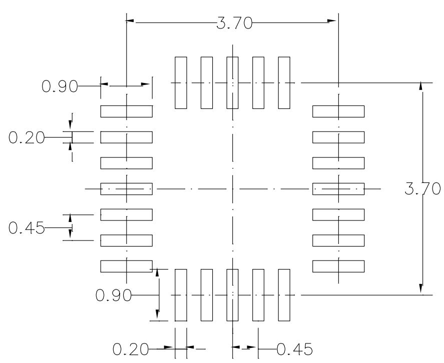
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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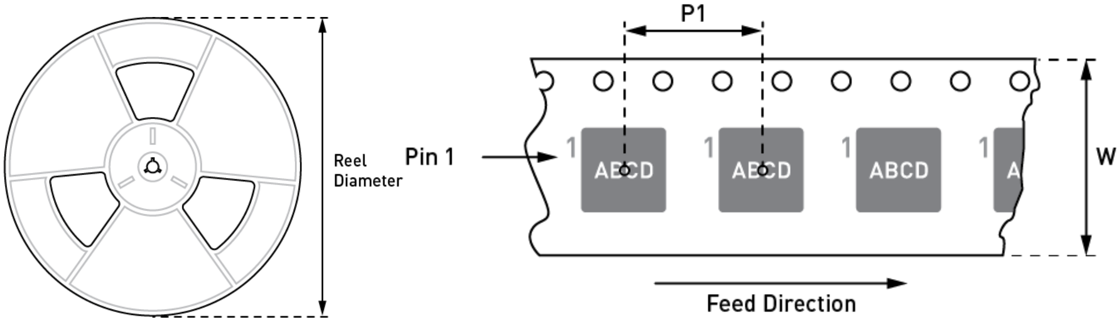
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3326GR–Z	QFN-24 (4mmx4mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/4/2021	Initial Release	-