MP3324

8-Channel, 100mA/Ch, LED Driver with Separated PWM/Analog Dimming and I²C Interface

DESCRIPTION

The MP3324 is an 8-channel white LED (WLED) driver that operates from a wide 4V to 16V input voltage (V_{IN}) range. The MP3324 applies eight internal current sources in each LED string terminal. The LED current (I_{LED}) of each channel is set by an external current-setting resistor. Each channel has a 100mA maximum current (while $V_{IN} \geq 4.5V$).

The device integrates an I²C interface. There are ten different I²C addresses that can be configured via an external resistor. This means the MP3324 can support up to ten ICs that have been cascaded to drive an LED array. Each channel can be enabled or disabled via the I²C.

The MP3324 employs both separated pulse-width modulation (PWM) dimming and analog dimming for each LED channel, with a 12-bit PWM dimming resolution and 6-bit analog dimming per channel. The I_{LED} ramping rate and phase shift can be configured to reduce EMI and EMC.

The MP3324 can output a refresh signal from the RFSH/FLT pin. The refresh signal frequency ($f_{REFRESH}$) can be set via the I²C.

Full protections features include LED open-load protection (OLP), LED short-load protection (SLP), and over-temperature protection (OTP). The device also features fault indication. If a protection function is triggered, then the RFSH/FLT pin is pulled low, and the corresponding fault register is set.

The MP3324 is available in a QFN-24 (4mmx4mm) package.

FEATURES

- Wide 4V to 16V Input Voltage (V_{IN}) Range
- 8 Channels, Maximum 100mA per Channel ($V_{IN} \geq 4.5V$)
- LED Current (I_{LED}) Configured via an External Resistor
- 6-Bit Analog Dimming per Channel
- 12-Bit Pulse-Width Modulation (PWM) Dimming per Channel
- Selectable 220Hz, 250Hz, 280Hz, or 330Hz PWM Dimming Frequency (f_{PWM})
- Refresh Signal Output
- I²C Interface
- 10 Addresses Configurable via an External Resistor
- Configurable I_{LED} Slew Rate
- 80μs Phase Shift
- Fault Indication
- LED Open Protection
- LED Short Protection with Configurable Threshold
- Under-Voltage Lockout (UVLO) Protection
- Over-Temperature Protection (OTP)
- ELV Directive II Compliant
- Available in a QFN-24 (4mmx4mm) Package

APPLICATIONS

- LED Lights
- Instruments Clusters
- General Displays

TYPICAL APPLICATION

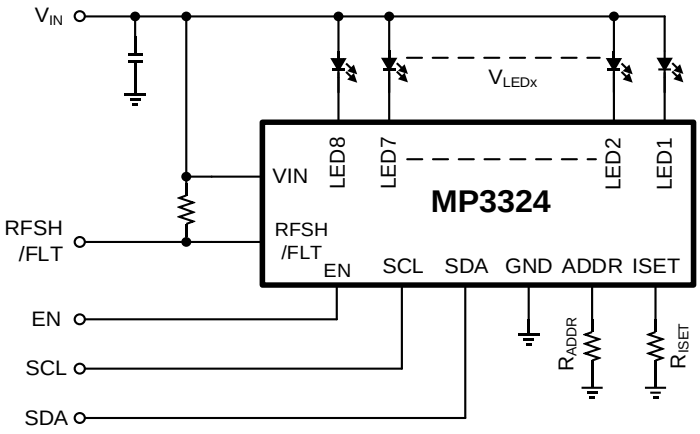


Figure 1: Typical Application

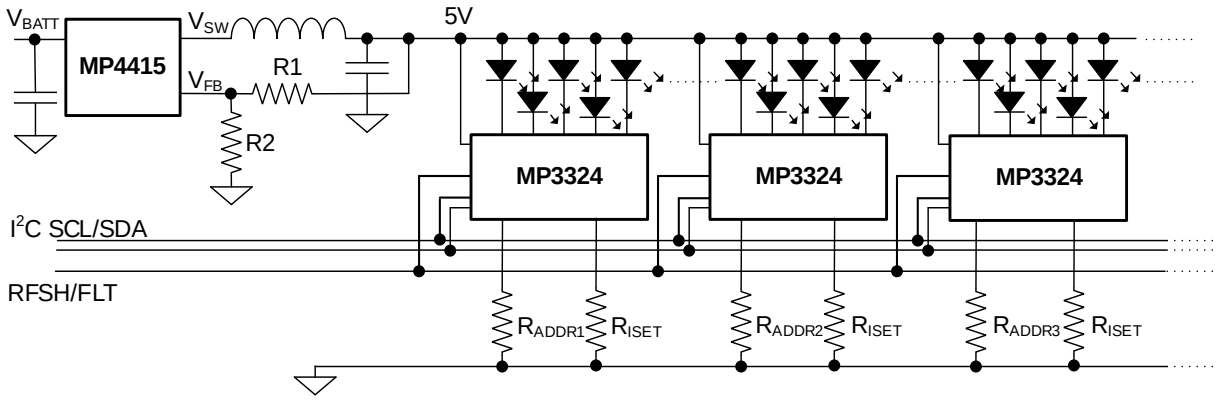


Figure 2: System Application

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3324GRE	QFN-24 (4mmx4mm)	*See Below*	1

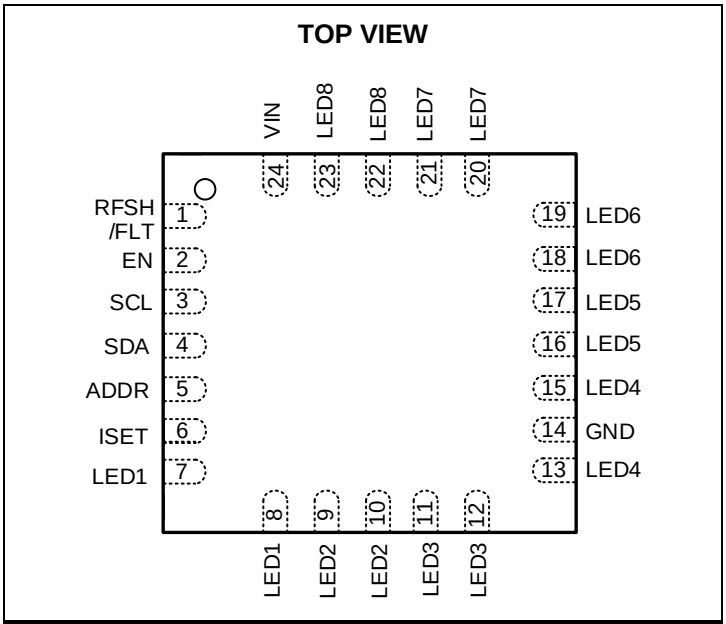
* For Tape & Reel, add suffix -Z (e.g. MP3324GRE-Z).

TOP MARKING

MPSYWW
MP3324
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP3324: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-24 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	RFSH/FLT	**Refresh signal output or fault flag.** If the FLTEN bit is set to 0, then the RFSH/FLT pin outputs a synchronized signal that is set by the FRFSH[9:0] register. If the FLTEN bit is set to 1, then RFSH/FLT is used to indicate whether a fault has occurred. RFSH/FLT is pulled low if a fault occurs.
2	EN	**Enable control.** Pull the EN pin high to turn the LED driver on; pull EN low to turn it off.
3	SCL	**I²C interface clock input.**
4	SDA	**I²C interface data input.**
5	ADDR	**I²C address setting.** Configure the I²C addresses by attaching different resistors between the ADDR and GND pins. ADDR sets the 4LSB of the I²C address. There are 10 configurable addresses.
6	ISET	**LED current setting.** Connect a current-setting resistor between the ISET and GND pins to configure the current in each LED string.
7, 8	LED1	**LED channel 1 current input.** Connect the LED channel 1 cathode to this pin. Each channel has two LED1 pins, and both LED1 pins should be connected to the LED channel 1 cathode.
9, 10	LED2	**LED channel 2 current input.** Connect the LED channel 2 cathode to this pin. Each channel has two LED2 pins, and both LED2 pins should be connected to the LED channel 2 cathode.
11, 12	LED3	**LED channel 3 current input.** Connect the LED channel 3 cathode to this pin. Each channel has two LED3 pins, and both LED3 pins should be connected to the LED channel 3 cathode.
13, 15	LED4	**LED channel 4 current input.** Connect the LED channel 4 cathode to this pin. Each channel has two LED4 pins, and both LED4 pins should be connected to the LED channel 4 cathode.
14	GND	**Ground.**
16, 17	LED5	**LED channel 5 current input.** Connect the LED channel 5 cathode to this pin. Each channel has two LED5 pins, and both LED5 pins should be connected to the LED channel 5 cathode.
18, 19	LED6	**LED channel 6 current input.** Connect the LED channel 6 cathode to this pin. Each channel has two LED6 pins, and both LED6 pins should be connected to the LED channel 6 cathode.
20, 21	LED7	**LED channel 7 current input.** Connect the LED channel 7 cathode to this pin. Each channel has two LED7 pins, and both LED7 pins should be connected to the LED channel 7 cathode.
22, 23	LED8	**LED channel 8 current input.** Connect the LED channel 8 cathode to this pin. Each channel has two LED8 pins, and both LED8 should be connected to the LED channel 8 cathode.
24	VIN	**Power supply input.** The VIN pin supplies power to the IC. Connect a capacitor between the VIN and GND pins.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +18V
V_{LED1} to V_{LED8}.....-0.5V to +18V
All other pins .....-0.3V to +5V
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-24 (4mmx4mm) 2.97W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4V to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-24 (4mmx4mm) ……..…..42…….9.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage	V_{IN}		4		16	V
Quiescent current	I_Q				4	mA
Shutdown current	I_{SD}	V_{EN} = 0V, V_{IN} = 16V			2	μA
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	Rising edge	3.45	3.7	3.95	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	Falling edge	3.15	3.5	3.85	V
Enable						
EN rising threshold	V_{EN_RISING}	V_{EN} rising	2.1			V
EN falling threshold	$V_{EN\_FALLING}$	V_{EN} falling			0.8	V
EN pull-down resistance	R_{EN}			1		MΩ
RFSH/FLT						
Refresh signal frequency	$f_{REFRESH}$	FRFSH[9:0] = 0x1A9, FPWM[2:0] = 01	285	300	315	Hz
RFSH/FLT pull-down resistance	$R_{RFSH/FLT}$	FLTEN = 1, a fault has occurred			100	Ω
LED Regulator						
ISET voltage	V_{ISET}	T_A = 25°C	1.174	1.2	1.226	V
LED current	I_{LED}	R_{ISET} = 20kΩ, ICHx[5:0] = 0x3F, T_A = 25°C	-2%	50	+2%	mA
Current sink headroom	V_{LEDx}	I_{LED} = 40mA		150	210	mV
Dimming						
Pulse-width modulation (PWM) frequency	f_{PWM}	FPWM[1:0] = 01	230	245	260	Hz
PWM duty step	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz		0.97		μs
Phase shift	t_{DELAY}	PS_EN = 1		80		μs
LED current step		I_{LED} = 50mA, analog dimming step		0.8		mA
LED current slew rate during PWM dimming		SLEW[1:0] = 01, rising edge		5		μs
		SLEW[1:0] = 11, rising edge		20		μs
Protections						
LED string short-load protection (SLP) threshold	V_{SLP}	STH[1:0] = 01	2.75	3	3.25	V
LED string SLP time	t_{SLP}	V_{LEDx} > STH[1:0]		4		ms
LED string SLP hiccup time	t_{SLP_HICCUP}			1		ms
LED string SLP hiccup detection time	t_{SLP_DET}			32		μs
LED string open-load protection (OLP) threshold	V_{OLP}			100	160	mV
LED string OLP time	t_{OLP}	V_{LEDx} < 100mV		4		ms
LED string OLP hiccup time	t_{OLP_HICCUP}			1		ms
LED string OLP hiccup detection time	t_{OLP_DET}			32		μs

ELECTRICAL CHARACTERISTICS *(continued)*

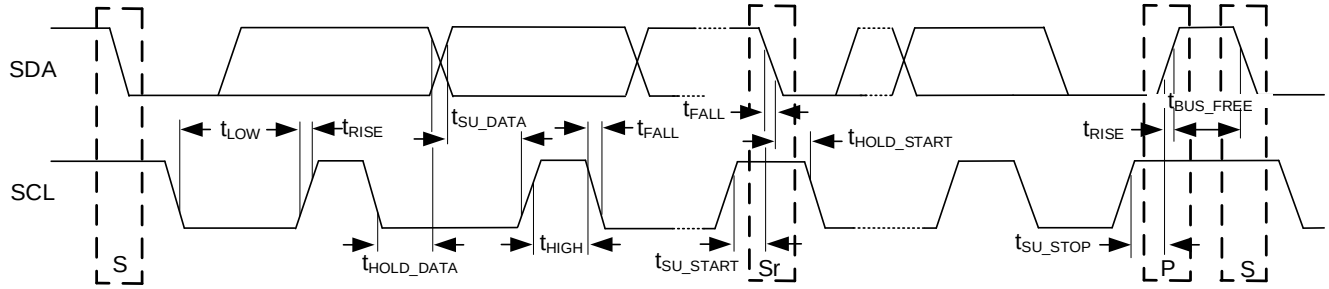
V_{IN} = 5V, V_{EN} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown threshold (5)	T_{SD}			170		°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			20		°C
I²C Interface						
Input logic low voltage	V_{IN_LOW}		0		0.4	V
Input logic high voltage	V_{IN_HIGH}		1.3			V
Output logic low voltage (5)	V_{OUT_LOW}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency (5)	f_{SCL}		10		1000	kHz
Bus free time (5)	t_{BUS_FREE}	Between stop and start conditions	0.5			µs
Holding time after start/ repeated start condition (5)	t_{HOLD_START}	The first clock is generated after this period	0.26			µs
Repeated start condition set-up time (5)	t_{SU_START}		0.26			µs
Stop condition set-up time (5)	t_{SU_STOP}		0.26			µs
Data hold time (5)	t_{HOLD_DATA}		0			ns
Data set-up time (5)	t_{SU_DATA}		50			ns
Clock low timeout (5)	$t_{TIMEOUT}$		25		35	ms
Clock low time (5)	t_{LOW}		0.5			µs
Clock high time (5)	t_{HIGH}		0.26			µs
Clock/data fall time (5)	t_{FALL}				120	ns
Clock/data rise time (5)	t_{RISE}				120	ns

Notes:

5) Guaranteed by characterization. Not tested in production.

I²C INTERFACE TIMING DIAGRAM



S = Start Condition
Sr = Repeated Start Condition
P = Stop Condition

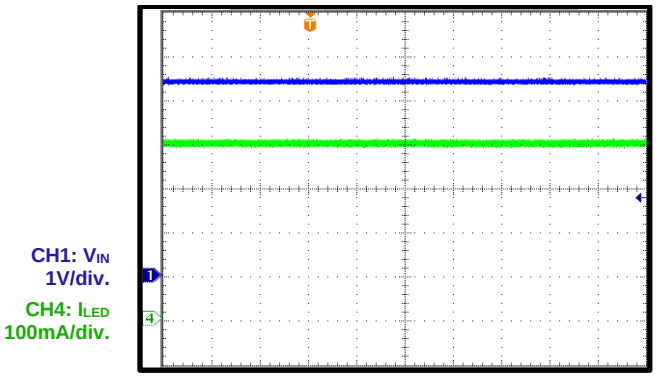
Figure 3: I²C Interface Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

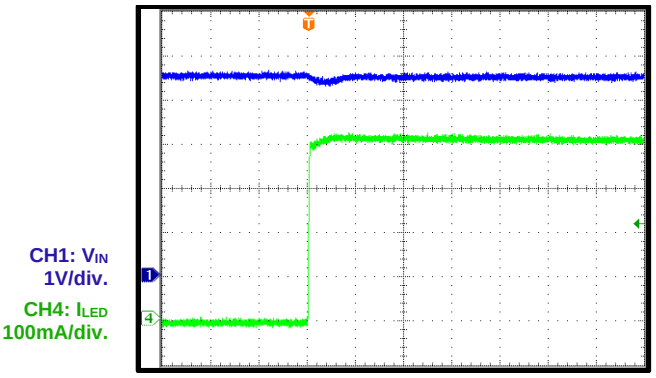
V_{IN} = 4.5V, LED = 8P/1S, I_{SET} = 50mA/string, T_A = 25°C, unless otherwise noted.

Steady State

V_{IN} = 4.5V, LED = 8P/1S, I_{SET} = 50mA/string

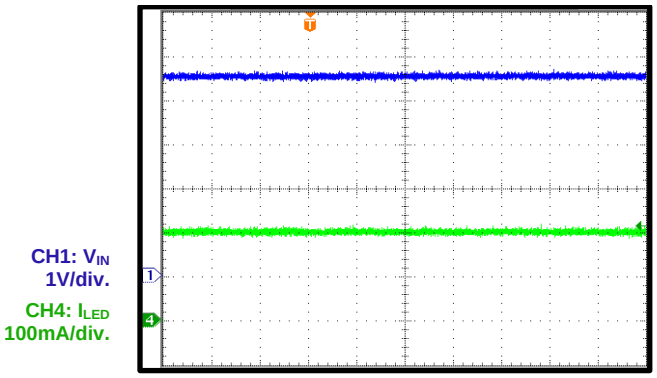


Start-Up through the EN Bit



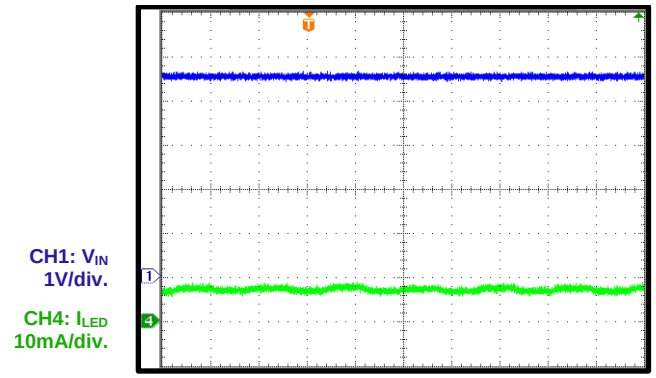
Analog Dimming

I_{SET} = 25mA/string



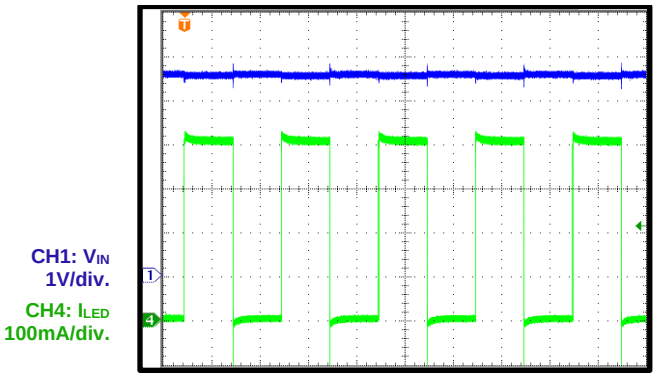
Analog Dimming

I_{SET} = 0.78mA/string



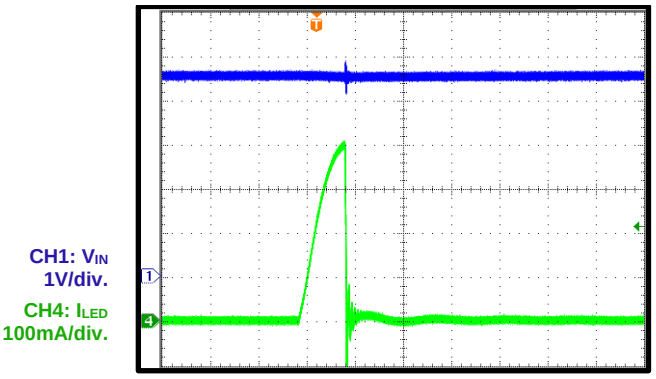
PWM Dimming

PWM duty = 50%



PWM Dimming

PWM duty = 0.024%

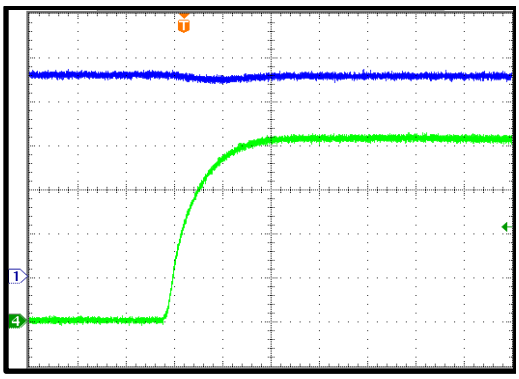


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4.5V, LED = 8P/1S, I_{SET} = 50mA/string, T_A = 25°C, unless otherwise noted.

Slew Rate

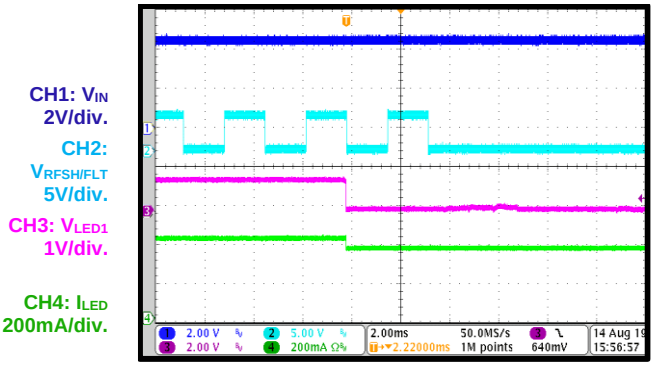
PWM dimming, 10μs slew rate



10μs/div.

LED Open-Load Protection

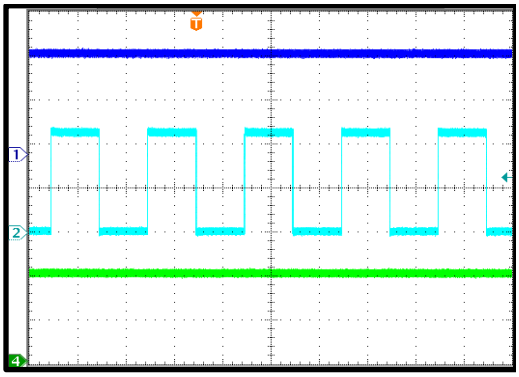
RFSH/FLT fault indication enabled



2ms/div.

Refresh Function

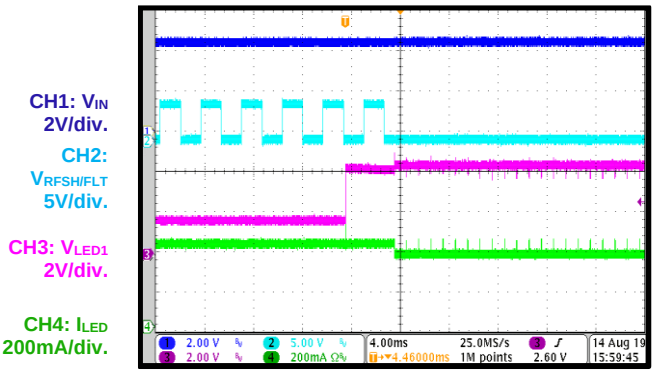
f_{PWM} = 250Hz, FRFSH[9:0] = 1FF



2ms/div.

LED Short Protection

RFSH/FLT fault indication enabled



4ms/div.

FUNCTIONAL BLOCK DIAGRAM

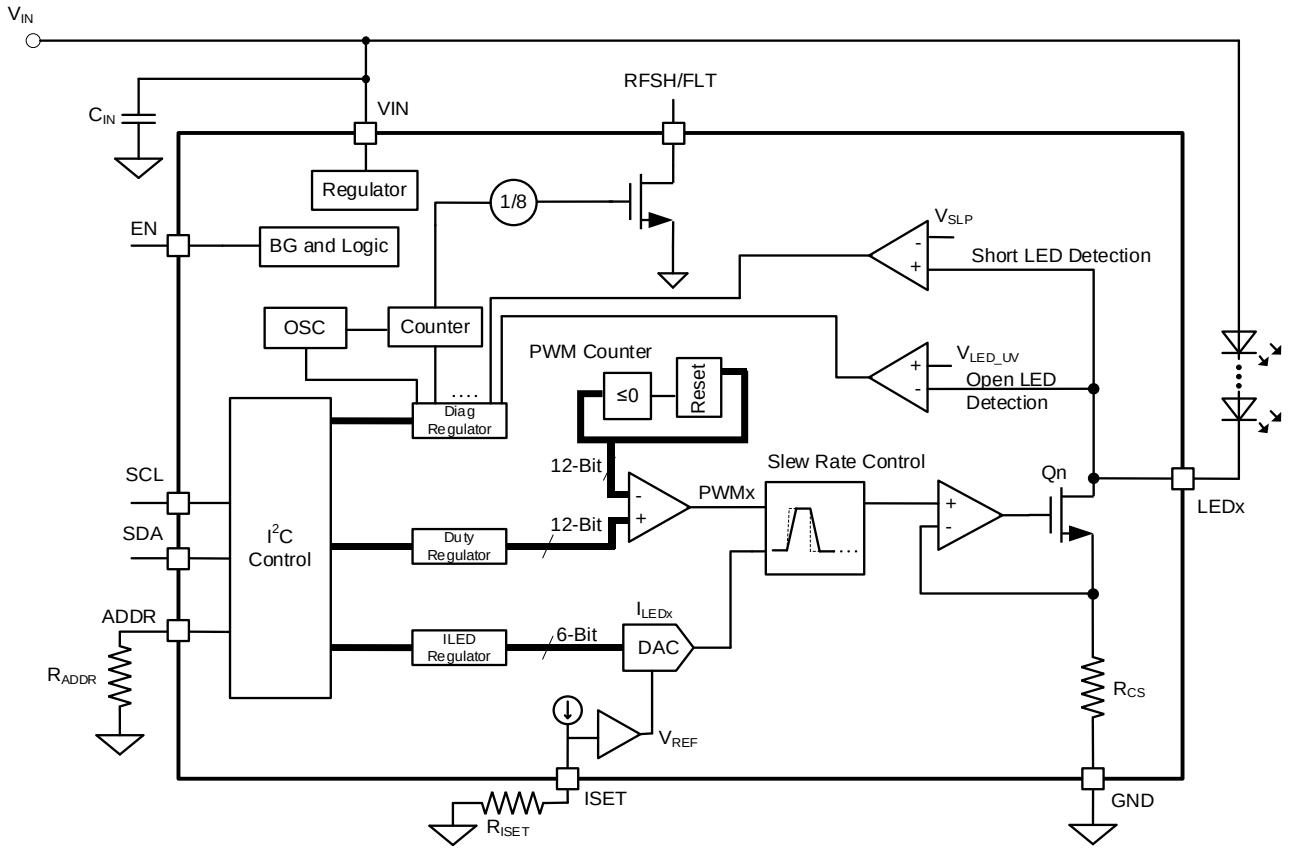


Figure 4: Functional Block Diagram

OPERATION

The MP3324 applies eight internal current sources per LED string terminal. The LED current (I_{LED}) of the channels is set via an external current-setting resistor. The maximum current is 100mA.

Enable (EN) and Start-Up

If the input voltage (V_{IN}) and the EN voltage (V_{EN}) both exceed their respective under-voltage lockout (UVLO) thresholds, then the MP3324 enters standby mode, and the I²C is active. After setting the I²C register, pull the EN bit high to start up the system. The start-up sequence is listed below:

1. V_{IN}
2. V_{EN}
3. Set the I²C register
4. Set the EN bit

Channel Selection

Channels can be disabled by setting the corresponding CHxEN bit (e.g. CH1EN, CH2EN, etc.) low.

Dimming

Each channel has its own 6-bit analog dimming register and 12-bit pulse-width modulation (PWM) dimming register. The MP3324 can use analog dimming and PWM dimming for each channel.

In analog dimming, the I_{LED} amplitude changes as the analog dimming register changes. Set the ICHx bit to set the analog dimming for the corresponding channel. I_{LED} can be estimated with Equation (1):

$$I_{LED} = \frac{ICHx}{63} \times I_{SET} \quad (1)$$

Where ICHx is the analog dimming code for each corresponding channel.

For example, if ICHx is set to 0, then the corresponding I_{LED} is 0A.

In PWM dimming, I_{LED} is a PWM waveform. The I_{LED} amplitude stays the same, and the I_{LED} duty varies with the PWM dimming register.

The PWM dimming duty is set by PWMx. The duty (D) can be calculated with Equation (2):

$$D = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the PWM dimming duty code for each corresponding channel.

The duty only changes once the 8MSB of the PWM duty register is written. For example, if PWMx is set to 0, then the corresponding I_{LED} is 0A.

The PWM dimming frequency (f_{PWM}) can be selected via register FPWM[1:0]. Table 1 shows the FPWM[1:0] settings for the different PWM frequencies.

Table 1: PWM Frequency Setting

FPWM[1:0]	f_{PWM}
00	220Hz
01	250kHz (default)
10	280kHz
11	330kHz

To avoid a glitch during normal operation, the following conditions must be met:

- Only change the FPWM[1:0] value if the EN bit is set 0.
- Write the FPWM register, and wait for 10µs before writing to any other registers.

Phase Shift

A channel-by-channel phase shift function can be implemented. Set the PS_EN bit high to enable the phase shift function.

If phase shift is enabled, the LEDx + 1 current's rising edge is delayed for 80µs after the LEDx current's rising edge (x = 1, 2, 3, 4, 5, 6, or, 7).

Synchronized Output for the LCD Refresh Frequency

The fault indication function can be enabled by the FLTEN bit.

If FLTEN is set to 0, fault indication is disabled. RFSH/FLT maintains the output refresh signal, even if a protection function is triggered.

If FLTEN is set to 1, fault indication is enabled. RFSH/FLT is pulled low if a fault occurs. Table 2 on page 12 shows RFSH/FLT's output status.

Table 2: RFSH/FLT Pin Output Status

FLTEN	RFSH/FLT Pin Output			
	FRFSH[9:0] = 0x000		FRFSH[9:0] = 0x001 to 0x3FF	
	No fault	Fault	No fault	Fault
1	Pulled high externally	Low	Rectangular signal	Low
0	Pulled high externally		Rectangular signal	

The refresh signal frequency ($f_{REFRESH}$) is set by FRFSH[9:0]. If FRFSH[9:0] is set to 0x000, then the RFSH/FLT pin outputs high. If FRFSH[9:0] is set between 0x001 and 0x3FF, then the RFSH/FLT pin outputs a rectangular signal. $f_{REFRESH}$ can be calculated with Equation (3):

$$f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250} \quad (Hz) \qquad (3)$$

Where FRFSH is the FRFSH[9:0] value (>0), and f_{PWM} is PWM dimming frequency set by register FPWM[1:0] (220Hz, 250Hz, 280Hz, or 330Hz).

Note that all numbers in the equation have a decimal base, and that $f_{REFRESH}$ should not change until the 8MSB are written.

The internal oscillator is divided by 8. As the clock refreshes the frequency generation, the FRFSH[9:0] register sets the counter number (see Figure 5).

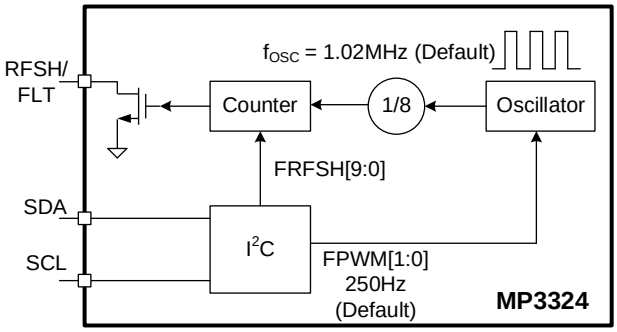


Figure 5: Refresh Frequency Generation

LED Current Slew Rate Control

Changing the I_{LED} rising/falling slew rate during PWM dimming can reduce EMI. The I_{LED} rising/falling slew rate is controlled by SLEW[1:0]. Table 3 shows the SLEW[1:0] settings for the different slew rates.

Table 3: Slew Rate Setting

SLEW[1:0]	Slew Rate
00	No slew rate
01	5µs
10	10µs
11	20µs

Protections

The MP3324 employs V_{IN} under-voltage lockout (UVLO) protection, LED short protection, LED open-load protection (OLP), and thermal shutdown.

The RFSH/FLT pin is an active-low open drain, and should be pulled high to an external voltage source. If a fault occurs, the corresponding fault bit is set, and RFSH/FLT is pulled low.

In hiccup mode, the RFSH/FLT pin is pulled high once the fault is removed.

In latch-off mode, the RFSH/FLT pin is released once all of the fault bits are read.

For LED open and short protection, hiccup mode or latch-off mode can be selected by the LATCH bit via the I²C.

If the LATCH bit is set to 1, the device initiates latch-off mode if a fault occurs. The fault channel is off until either VIN or EN is turned off and reset.

If the LATCH bit is set to 0, the device operates in hiccup mode. In hiccup mode, the fault channel attempts to conduct for 32µs to detect whether the fault has cleared. This process is repeated every 1ms. RFSH/FLT is released once the fault is removed.

V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops to the V_{IN} UVLO threshold, then the IC shuts down, and the I²C registers are reset.

LED Open-Load Protection (OLP)

If an LED open fault occurs, the LEDx voltage (V_{LEDx}) drops. If V_{LEDx} drops below the protection threshold (about 100mV) for 4ms, then LED open-load protection (OLP) is triggered. Once OLP is triggered, the fault channel turns off, the corresponding CHxO open fault bit is set, and RFSH/FLT is pulled low.

LED Short-Load Protection (SLP)

If an LED short occurs, V_{LEDx} exceeds the voltage set by STH[1:0] for 4ms, and LED short-load protection (SLP) is triggered. Once SLP is triggered, the short channel turns off, the corresponding CHxS fault bit is set, and RFSH/FLT is pulled low.

The LED SLP threshold (V_{SLP}) can be configured by STH[1:0]. Table 4 shows the STH[1:0] settings for the different LED SLP thresholds.

Table 4: LED SCP Threshold Setting

STH[1:0]	V_{SLP}
00	2V
01	3V
10	4V
11	5V

Over-Temperature Protection (OTP)

If the IC temperature exceeds 170°C, then over-temperature protection (OTP) is triggered. All channels turn off, RFSH/FLT is pulled low, and the FT_OTP bit is set. If the temperature drops to about 150°C, then the IC recovers, all channels turn on again, and the part resumes normal operation.

I²C INTERFACE

I²C Chip Address

The MP3324's address is 0x30 to 0x39, which can be configured via the ADDR resistor (R_{ADDR}). The internal current source flows to R_{ADDR}, and the ADDR voltage (V_{ADDR}) determines the I²C address. Ten different addresses can be configured via R_{ADDR}. Table 5 shows the relationship between the I²C address and the resistor ratio (R_{ADDR} / R_{ISET}).

Table 5: I²C Address Setting

R_{ADDR} / R_{ISET}	I²C Address (A3, A2, A1, A0)
<0.05	0000
>0.05, <0.15	0001
>0.15, <0.25	0010
>0.25, <0.35	0011
>0.35, <0.45	0100
>0.45, <0.55	0101
>0.55, <0.65	0110
>0.65, <0.75	0111
>0.75, <0.85	1000
>0.85, <0.95	1001

At start-up, the IC checks the I²C address first. This address remains the same during normal operation, unless the IC's power is reset.

After the start condition, the I²C-compatible master sends a 7-bit address followed by an 8th read (1) or write (0) bit. The 8th bit indicates the register address to/from which the data will be written/read (see Figure 6).

0	1	1	A3	A2	A1	A0	R/W

Figure 6: I²C-Compatible Device Address

To avoid any glitches during normal operation, ensure that the following conditions are met:

- The FPWM[1:0] value can only be changed once the EN bit is set to 0.
- Write the FPWM register, then wait for 10μs before writing any other registers.

I²C REGISTER MAP

Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
00h	01	RESERVED						FPWM[1:0]	
01h	40	FLTEN	LATCH	STH[1:0]		SLEW[1:0]		PS_EN	EN
02h	01	RESERVED					FT_OTP	FRFSH[1:0]	
03h	6A	FRFSH[9:2]							
04h	FF	CH8EN	CH8EN	CH7EN	CH7EN	CH6EN	CH6EN	CH5EN	CH5EN
05h	FF	CH4EN	CH4EN	CH3EN	CH3EN	CH2EN	CH2EN	CH1EN	CH1EN
06h	00	RESERVED	CH8O	RESERVED	CH7O	RESERVED	CH6O	RESERVED	CH5O
07h	00	RESERVED	CH4O	RESERVED	CH3O	RESERVED	CH2O	RESERVED	CH1O
08h	00	RESERVED	CH8S	RESERVED	CH7S	RESERVED	CH6S	RESERVED	CH5S
09h	00	RESERVED	CH4S	RESERVED	CH3S	RESERVED	CH2S	RESERVED	CH1S
0Ah	3F	RESERVED		ICH1 5:0					
0Bh	0F	RESERVED				PWM[3:0]			
0Ch	FF	PWM1[11:4]							
0Dh	3F	RESERVED		ICH1[5:0]					
0Eh	0F	RESERVED				PWM1[3:0]			
0Fh	FF	PWM1[11:4]							
10h	3F	RESERVED		ICH2[5:0]					
11h	0F	RESERVED				PWM2[3:0]			
12h	FF	PWM2[11:4]							
13h	3F	RESERVED		ICH2[5:0]					
14h	0F	RESERVED				PWM2 3:0			
15h	FF	PWM2[11:4]							
16h	3F	RESERVED		ICH3[5:0]					
17h	0F	RESERVED				PWM3[3:0]			
18h	FF	PWM3[11:4]							
19h	3F	RESERVED		ICH3[5:0]					
1Ah	0F	RESERVED				PWM3[3:0]			
1Bh	FF	PWM3[11:4]							
1Ch	3F	RESERVED		ICH4[5:0]					
1Dh	0F	RESERVED		PWM4[3:0]					
1Eh	FF	PWM4[11:4]							
1Fh	3F	RESERVED		ICH4[5:0]					
20h	0F	RESERVED				PWM4[3:0]			
21h	FF	PWM4[11:4]							
22h	3F	RESERVED		ICH5[5:0]					
23h	0F	RESERVED				PWM5[3:0]			

I²C REGISTER MAP *(continued)*

Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
24h	FF	PWM5[11:4]							
25h	3F	RESERVED		ICH5[5:0]					
26h	0F	RESERVED				PWM5[3:0]			
27h	FF	PWM5[11:4]							
28h	3F	RESERVED		ICH6[5:0]					
29h	0F	RESERVED				PWM6[3:0]			
2Ah	FF	PWM6[11:4]							
2Bh	3F	RESERVED		ICH6[5:0]					
2Ch	0F	RESERVED				PWM6[3:0]			
2Dh	FF	PWM6[11:4]							
2Eh	3F	RESERVED		ICH7[5:0]					
2Fh	0F	RESERVED				PWM7[3:0]			
30h	FF	PWM7[11:4]							
31h	3F	RESERVED		ICH7[5:0]					
32h	0F	RESERVED				PWM7[3:0]			
33h	FF	PWM7[11:4]							
34h	3F	RESERVED		ICH8[5:0]					
35h	0F	RESERVED				PWM8[3:0]			
36h	FF	PWM8[11:4]							
37h	3F	RESERVED		ICH8[5:0]					
38h	0F	RESERVED				PWM8[3:0]			
39h	FF	PWM8[11:4]							

I²C REGISTERS

Reg 00h: PWM Dimming Frequency Setting

Bits	Name	R/W	Default	Description
7:2	RESERVED	R	000000	Reserved.
1:0	FPWM	R/W	01	Sets the pulse-width modulation (PWM) dimming frequency. 00: 220Hz 01: 250Hz 10: 280Hz 11: 330Hz To avoid any glitches during normal operation, ensure that the following conditions are met: • FPWM[1:0] can only be changed once the EN bit is set to 0 • Write the FPWM register, then wait 10µs before writing any other registers

Reg 01h: Control Register

Bits	Name	R/W	Default	Description
7	FLTEN	R/W	0	Enables the RFSH/FLT pin's fault indication. 0: Disabled, the RFSH/FLT pin refreshes the signal output 1: Enabled, the RFSH/FLT pin indicates if a fault has occurred
6	LATCH	R/W	1	Enables latch-off mode. 0: Disabled, the part operates in hiccup mode if a fault occurs 1: Enabled, the part operates in latch-off mode if a fault occurs
5:4	STH[1:0]	R/W	00	Sets the LED short-load protection (SLP) threshold (V_{SLP}). 00: 2V 01: 3V 10: 4V 11: 5V
3:2	SLEW[1:0]	R/W	00	Sets the LED current (I_{LED}) slew rate. 00: No slew rate 01: 5µs 10:10µs 11: 20µs
1	PS_EN	R/W	0	Enables the phase shift function. 0: Disabled 1: Enabled, the rising edge of LEDx + 1 occurs 80µs after LEDx (x = 1, 2, 3, 4, 5, 6, or 7).
0	EN	R/W	0	Enables the IC. 0: Disabled 1: Enabled

Reg 02h: Refresh Frequency Setting and Over-Temperature (OT) Fault

Bits	Name	R/W	Default	Description
7:3	RESERVED	R	0	Reserved.
2	FT_OTP	R	0	Indicates whether an over-temperature (OT) fault has occurred. 0: An OT fault has not occurred 1: An OT fault has occurred
1:0	FRFSH[1:0]	R/W	01	Sets the 2LSB of the refresh frequency ($f_{REFRESH}$). FRFSH 9:0 = 0x000: Output a high-level voltage FRFSH 9:0 > 0: $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250}$ (Hz) Note that all of the numbers in the equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB is written. The default refresh frequency is 300Hz.

Reg 03h: Refresh Frequency Setting

Bits	Name	R/W	Default	Description
7:0	FRFSH[9:2]	R/W	6A	Sets the 8MSB of $f_{REFRESH}$). FRFSH[9:0] = 0x000: Output high-level voltage FRFSH[9:0] > 0: $f_{REFRESH}$ can be calculated with the following equation: $f_{REFRESH} = \frac{127500}{FRFSH} \times \frac{f_{PWM}}{250}$ (Hz) Note that all of the numbers in the equation have a decimal base. $f_{REFRESH}$ does not change until the 8MSB is written. The default refresh frequency is 300Hz.

Reg 04h: Channel 5, Channel 6, Channel 7, and Channel 8 Enable

Bits	Name	R/W	Default	Description
7:6	CH8EN	R/W	11	Enables channel 8. 00: Disabled 11: Enabled
5:4	CH7EN	R/W	11	Enables channel 7. 00: Disabled 11: Enabled
3:2	CH6EN	R/W	11	Enables channel 6. 00: Disabled 11: Enabled
1:0	CH5EN	R/W	11	Enables channel 5. 00: Disabled 11: Enabled

Reg 05h: Channel 1, Channel 2, Channel 3, and Channel 4 Enable

Bits	Name	R/W	Default	Description
7:6	CH4EN	R/W	11	Enables channel 4. 00: Disabled 11: Enabled
5:4	CH3EN	R/W	11	Enables channel 3. 00: Disabled 11: Enabled
3:2	CH2EN	R/W	11	Enables channel 2. 00: Disabled 11: Enabled
1:0	CH1EN	R/W	11	Enables channel 1. 00: Disabled 11: Enabled

Reg 06h: Channel 5, Channel 6, Channel 7, and Channel 8 LED Open Fault

Bits	Name	R/W	Default	Description
7	RESERVED	-	-	Reserved.
6	CH8O	R	0	Channel 8 LED open fault flag. 0: An LED open fault has not occurred on channel 8 1: An LED open fault has occurred on channel 8
5	RESERVED	-	-	Reserved.
4	CH7O	R	0	Channel 7 LED open fault flag. 0: An LED open fault has not occurred on channel 7 1: An LED open fault has occurred on channel 7
3	RESERVED	-	-	Reserved.
2	CH6O	R	0	Channel 6 LED open fault flag. 0: An LED open fault has not occurred on channel 6 1: An LED open fault has occurred on channel 6
1	RESERVED	-	-	Reserved.
0	CH5O	R	0	Channel 5 LED open fault flag. 0: An LED open fault has not occurred on channel 5 1: An LED open fault has occurred on channel 5

Reg 07h: Channel 1, Channel 2, Channel 3, and Channel 4 LED Open Fault

Bits	Name	R/W	Default	Description
7	RESERVED	-	-	Reserved.
6	CH4O	R	0	Channel 4 LED open fault flag. 0: An LED open fault has not occurred on channel 4 1: An LED open fault has occurred on channel 4
5	RESERVED	-	-	Reserved.
4	CH3O	R	0	Channel 3 LED open fault flag. 0: An LED open fault has not occurred on channel 3 1: An LED open fault has occurred on channel 3
3	RESERVED	-	-	Reserved.
2	CH2O	R	0	Channel 2 LED open fault flag. 0: An LED open fault has not occurred on channel 2 1: An LED open fault has occurred on channel 2
1	RESERVED	-	-	Reserved.
0	CH1O	R	0	Channel 1 LED open fault flag. 0: An LED open fault has not occurred on channel 1 1: An LED open fault has occurred on channel 1

Reg 08h: Channel 5, Channel 6, Channel 7, and Channel 8 LED Short Fault

Bits	Name	R/W	Default	Description
7	RESERVED	-	-	Reserved.
6	CH8S	R	0	Channel 8 LED short fault flag. 0: An LED short fault has not occurred on channel 8 1: An LED short fault has occurred on channel 8
5	RESERVED	-	-	Reserved.
4	CH7S	R	0	Channel 7 LED short fault flag. 0: An LED short fault has not occurred on channel 7 1: An LED short fault has occurred on channel 7
3	RESERVED	-	-	Reserved.
2	CH6S	R	0	Channel 6 LED short fault flag. 0: An LED short fault has not occurred on channel 6 1: An LED short fault has occurred on channel 6
1	RESERVED	-	-	Reserved.
0	CH5S	R	0	Channel 5 LED short fault flag. 0: An LED short fault has not occurred on channel 5 1: An LED short fault has occurred on channel 5

Reg 09h: Channel 1, Channel 2, Channel 3, and Channel 4 LED Short Fault

Bits	Name	R/W	Default	Description
7	RESERVED	-	-	Reserved.
6	CH4S	R	0	Channel 4 LED short fault flag. 0: An LED short fault has not occurred on channel 4 1: An LED short fault has occurred on channel 4
5	RESERVED	-	-	Reserved.
4	CH3S	R	0	Channel 3 LED short fault flag. 0: An LED short fault has not occurred on channel 3 1: An LED short fault has occurred on channel 3
3	RESERVED	-	-	Reserved.
2	CH2S	R	0	Channel 2 LED short fault flag. 0: An LED short fault has not occurred on channel 2 1: An LED short fault has occurred on channel 2
1	RESERVED	-	-	Reserved.
0	CH1S	R	0	Channel 1 LED short fault flag. 0: An LED short fault has not occurred on channel 1 1: An LED short fault has occurred on channel 1

Reg 0Ah and Reg 0Dh: Channel 1 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH1[5:0]	R/W	111111	Sets the LED channel 1 current for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

Reg 0Bh and Reg 0Eh: Channel 1 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM1[3:0]	R/W	1111	Sets the 4LSB for the LED channel 1 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 0Ch and Reg 0Fh: Channel 1 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM1[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 1 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 10h and Reg 13h: Channel 2 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH2[5:0]	R/W	111111	Sets the LED channel 2 current for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

Reg 11h and Reg 14h: Channel 2 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM2[3:0]	R/W	1111	Sets the 4LSB for the LED channel 2 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 12h and Reg 15h: Channel 2 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM2[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 2 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 16h and Reg 19h: Channel 3 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH3[5:0]	R/W	111111	Sets the LED channel 3 current for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

Reg 17h and Reg 1Ah: Channel 3 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM3[3:0]	R/W	1111	Sets the 4LSB for the LED channel 3 current for PWM dimming duty. The dimming duty only changes once 8MSB is written.

Reg 18h and Reg 1Bh: Channel 3 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM3[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 3 current for PWM dimming duty. The dimming duty only changes once 8MSB is written.

Reg 1Ch and Reg 1Fh:Channel 4 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH4[5:0]	R/W	111111	Sets the LED channel 4 current for analog dimming, which can be calculated with the following equation: $I_{LED} = \frac{Code}{63} \times I_{SET}$

Reg 1Dh and Reg 20h: Channel 4 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM4[3:0]	R/W	1111	Sets the 4LSB for the LED channel 4 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 1Eh and Reg 21h: Channel 4 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM4[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 4 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 22h and Reg 25h: Channel 5 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH5[5:0]	R/W	111111	Sets the LED channel 5 current for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

Reg 23h and Reg 26h: Channel 5 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM5[3:0]	R/W	1111	Sets the 4LSB for the LED channel 5 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 24h and Reg 27h: Channel 5 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM5[11:4]	R/W	11111111	Sets the 8MSB for the channel 5 I_{LED} PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 28h and Reg 2Bh: Channel 6 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH6[5:0]	R/W	111111	Sets the LED channel 6 current for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

Reg 29h and Reg 2Ch: Channel 6 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM6[3:0]	R/W	1111	Sets the 4LSB for the LED channel 6 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 2Ah and Reg 2Dh: Channel 6 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM6[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 6 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 2Eh and Reg 31h: Channel 7 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH[5:0]	R/W	111111	Sets the LED channel 7 current for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

Reg 2Fh and Reg 32h: Channel 7 PWM Dimming Duty Setting (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM7[3:0]	R/W	1111	Sets the 4LSB for the LED channel 7 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 30h and Reg 33h: Channel 7 PWM Dimming Duty Setting (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM7[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 7 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 34h and Reg 37h: Channel 8 LED Current Setting

Bits	Name	R/W	Default	Description
7:6	RESERVED	R	00	Reserved.
5:0	ICH8[5:0]	R/W	111111	Sets the LED channel 8 current for analog dimming, which can be calculated with the following equation: $I_{LED}=\frac{Code}{63}\times I_{SET}$

Reg 35h and Reg 38h: Channel 8 PWM Dimming Duty Setting Register (LSB)

Bits	Name	R/W	Default	Description
7:4	RESERVED	R	0000	Reserved.
3:0	PWM8[3:0]	R/W	1111	Sets the 4LSB for the LED channel 8 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

Reg 36h and Reg 39h: Channel 8 PWM Dimming Duty Setting Register (MSB)

Bits	Name	R/W	Default	Description
7:0	PWM8[11:4]	R/W	11111111	Sets the 8MSB for the LED channel 8 current for PWM dimming duty. The dimming duty only changes once the 8MSB is written.

APPLICATION INFORMATION

LED Current Setting

Connect a resistor between the ISET and GND pins to set the LED current (I_{LED}) for all eight channels. I_{LED} can be calculated with Equation (4):

$$I_{LED}(mA)=\frac{1000}{R_{ISET}(k\Omega)} \quad (4)$$

For a maximum I_{LED} (about 100mA), ensure that $V_{IN} \geq 4.5V$ to power the IC.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Ensure that the traces from the LED anode to the LEDx pins is wide enough to support the set current (up to 100mA).
2. The VIN capacitor should be close to VIN pin. And adding some vias in the GND of the VIN capacitor.

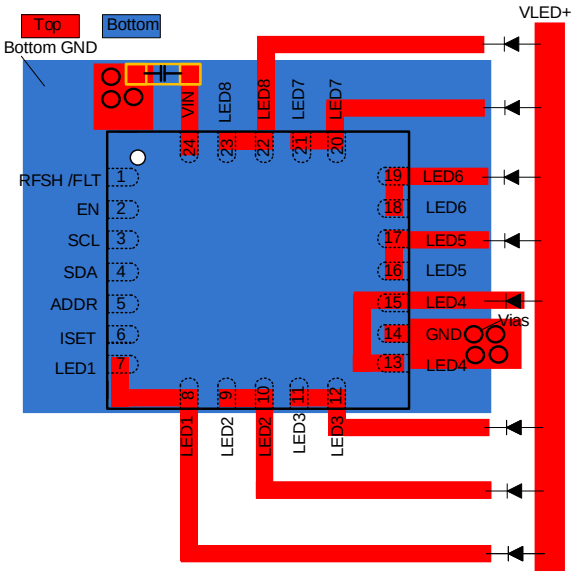


Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

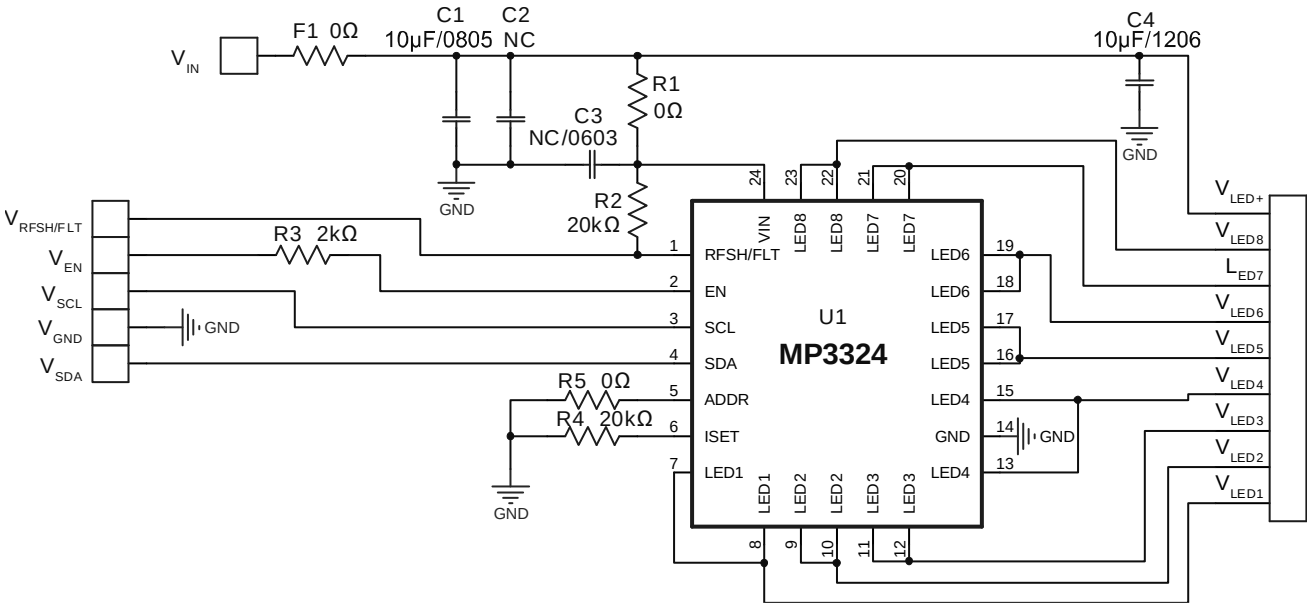


Figure 7: Typical Application Circuit

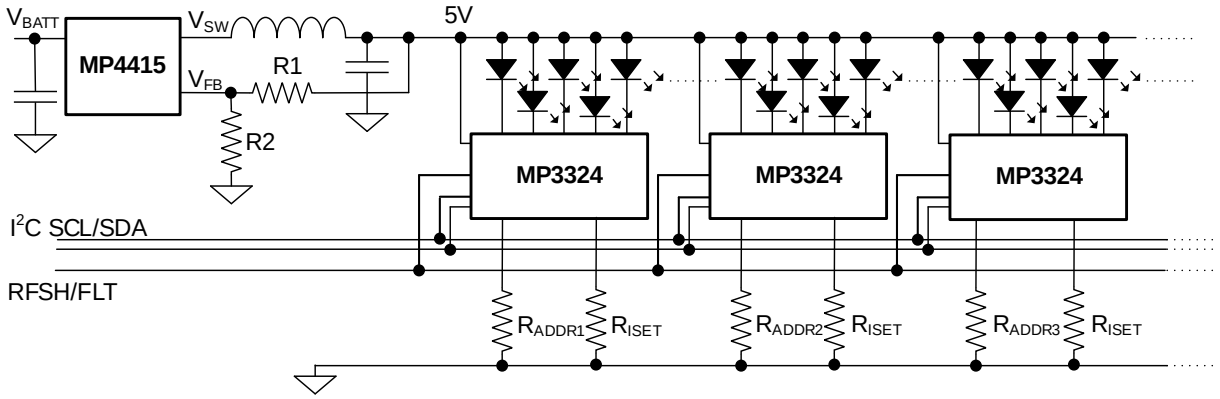
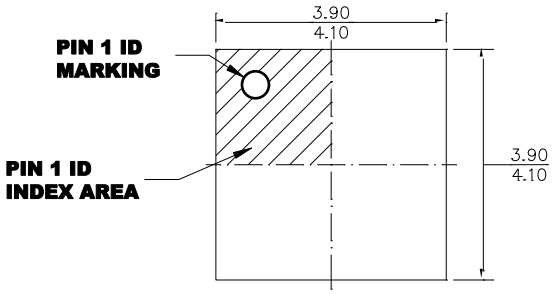


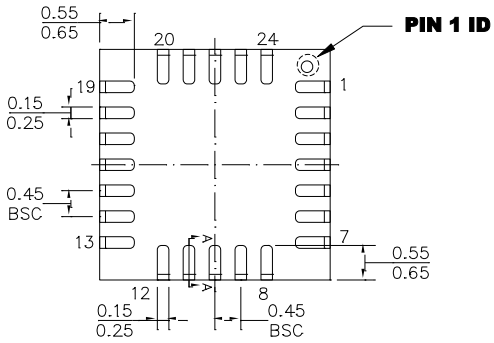
Figure 8: Typical System Application Circuit

PACKAGE INFORMATION

QFN-24 (4mmx4mm)
Wettable Flank

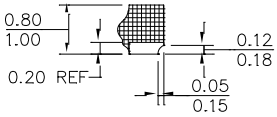


TOP VIEW

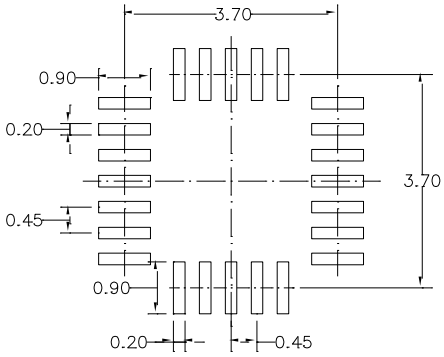


BOTTOM VIEW

SIDE VIEW



SECTION A-A

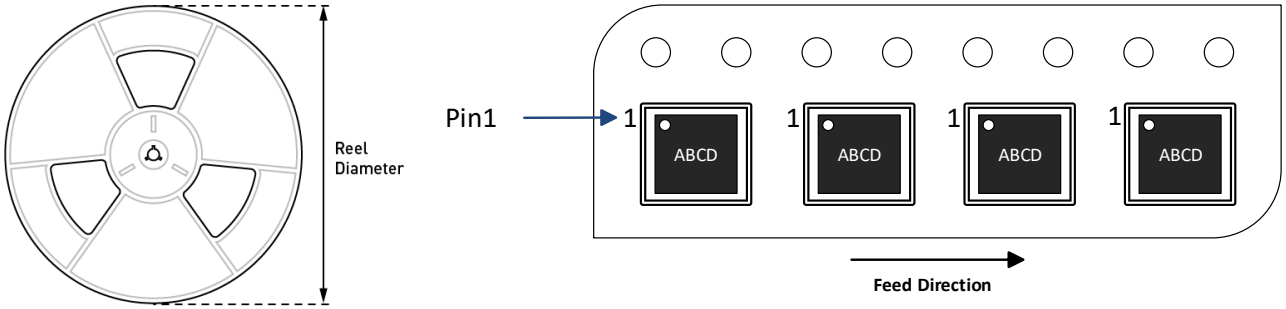


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3324GRE-Z	QFN-24 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/20/2022	Initial Release	-

Mouser Electronics

Authorized Distributor

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Monolithic Power Systems (MPS):

MP3324GRE-P MP3324GRE-Z