MP2723A

3A, I²C-Controlled SW Charger with NVDC Power Path, USB OTG, and Enhanced ADC

DESCRIPTION

The MP2723A is a 3A, highly integrated, switch-mode battery charge management device for single-cell Li-ion or Li-polymer batteries. This device works with narrow-voltage DC (NVDC) system power path management, and is suitable for a variety of applications, such as smartphones, tablets, wireless cameras, and other portable devices. Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The I²C serial interface allows the device to be flexibly controlled via adjustable charging and system settings.

The MP2723A supports 5V input sources, including standard USB host ports, USB charging ports, and USB-compliant wall adapters. The device provides USB input type detection via the DP/DM pins. It supports USB On-the-Go (OTG) operation by supplying 5V on the input bus with an output current limit up to 1.5A.

The MP2723A also initiates and completes charging cycles without software control. The device automatically detects the battery voltage and charges the battery in different stages. The charger automatically terminates when it detects that the battery is fully charged. If the battery drops below its recharge threshold, the charger initiates another charging cycle.

The charger provides various safety features for battery charging and system operations, including a charging safety timer, battery temperature monitoring, over-voltage protection (OVP), and over-current protection (OCP). If a fault occurs, the charger asserts INT to the host. The device provides disabled battery FET (BATFET) control to enter shipping mode, as well as system reset functionality via the DISC pin.

The MP2723A is available in a QFN-26 (3.5mmx3.5mm) package.

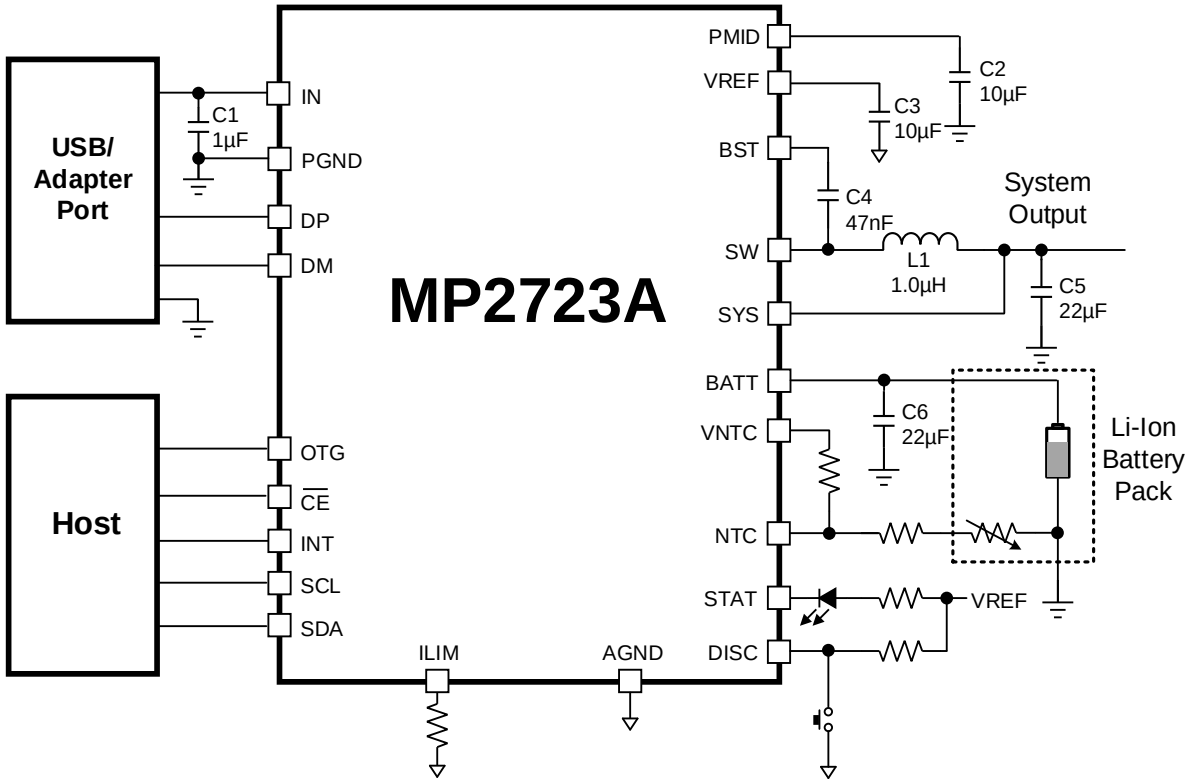
FEATURES

- 3.7V to 5.5V Operating Input Voltage Range
- Up to 22V Sustainable Voltage
- **High-Efficiency, 3A, 1.35MHz Buck Charger:**
  - Up to 92% Charge Efficiency at 3A Charge Current
  - Auto-Detection for USB SDP, CDP, DCP, and Non-Standard Adapters
- USB OTG with 4.8V to 5.5V Adjustable Output: Up to 1.5A Output with Up to 93% Efficiency
- **NVDC Power Path Management:**
  - Instant On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- High Battery Discharge Efficiency with 14mΩ BATFET up to 8.5A
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Fully Integrated Power MOSFETs and Current Sensing
- Dedicated DISC Pin to Control Ship Mode and System Reset
- 13μA Low Battery Leakage Current in Shipping Mode
- Integrated ADC for Monitoring Input Voltage, Input Current, Battery Voltage, Charge Current, System Voltage, and Battery Temperature
- Charging Status Indicator
- Safety Features: Configurable JEITA for Battery Temperature Protection, Battery Charging Safety Timer, Thermal Regulation and Shutdown, Watchdog Monitoring I²C Operation, and Input/System OVP

APPLICATIONS

- Tablet PCs
- Smartphones
- Wireless Cameras
- Other Portable Devices

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2723AGQC-xxxx**	QFN-26 (3.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2723AGQC-xxxx-Z).

** "-xxxx" is the register setting option. The factory default is "-0000." This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "-xxxx" value.

TOP MARKING

BTCYW

LLLLL

BTC: Product code
Y: Year code
W: Week code
LLLLL: Lot number

EVALUATION KIT EVKT-MP2723A

EVKT-MP2723A kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2723A-QC-00A	MP2723A evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

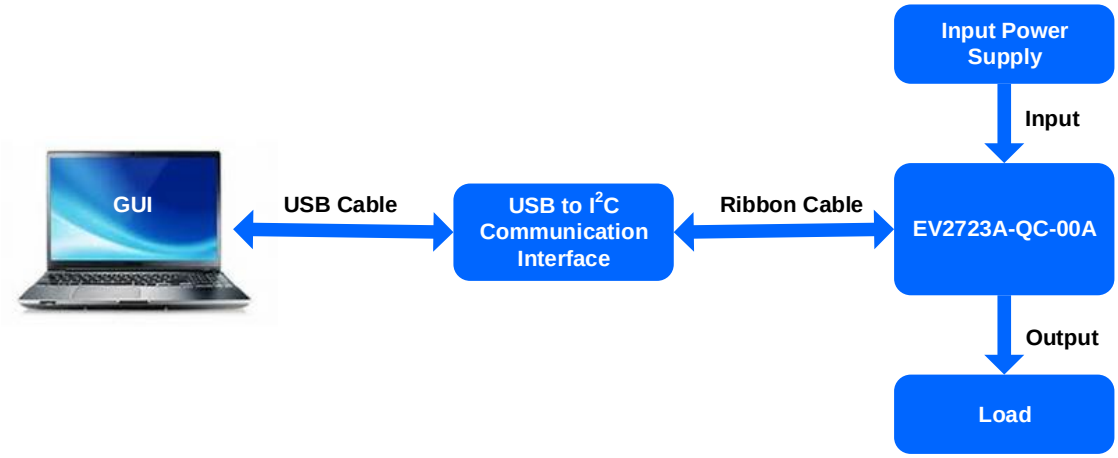
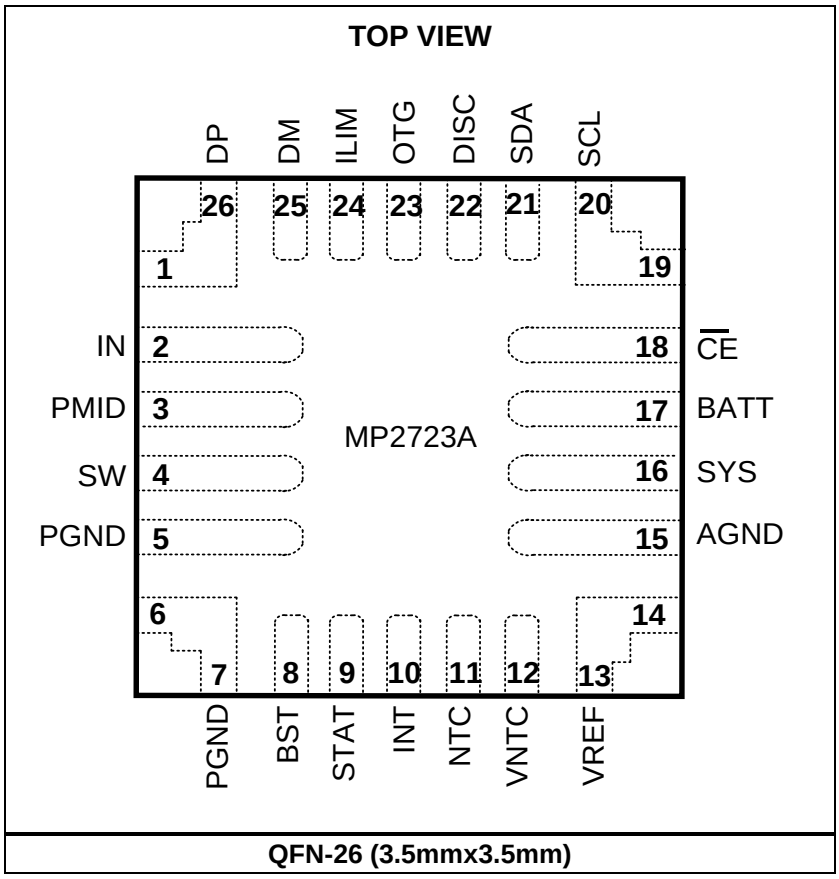


Figure 1: EVKT-MP2723A Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-26 (3.5mmx3.5mm)

PIN FUNCTIONS

Pin #	Name	Type (1)	Description
26	DP	AIO	**Positive pin of the USB data line pair.**
2	IN	P	**Power input of the IC.** Connect a 1µF ceramic capacitor from IN to PGND, placed as close as possible to the IC.
3	PMID	P	**Internal power pin.** Connect PMID to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET. Bypass PMID with a 10µF capacitor from PMID to PGND, placed as close as possible to the IC.
4	SW	P	**Switching node.**
5, 6, 7	PGND	P	**Power ground.**
8	BST	P	**Bootstrap pin**. Connect a 47nF bootstrap capacitor between the BST and SW pins to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
9	STAT	DO	**Open-drain charge status output to indicate various charger operations.** Connect STAT to VREF using a resistor.
10	INT	DO	**Open-drain interrupt output**. The INT pin can send charging status and fault interrupt (INT) signals to the host.
11	NTC	AI	**Temperature-sense input**. Connect a negative temperature coefficient (NTC) thermistor to the NTC pin. Configure the hot and cold temperature window with a resistor divider connected from VNTC to NTC to AGND. Charging is suspended when the NTC pin is out of range.
12	VNTC	P	**Pull-up voltage bias.** The VNTC pin is the pull-up voltage bias of the NTC comparator's resistor divider.
13, 14	VREF	P	**PWM low-side driver output.** Connect a 10µF ceramic capacitor from VREF to AGND, placed as close as possible to the IC.
15	AGND	P	**Analog ground.**
16	SYS	P	**System output.** Connect a 22µF ceramic capacitor from SYS to PGND, placed as close as possible to the IC.
17	BATT	P	**Battery positive terminal.** Connect a 22µF ceramic capacitor from BATT to PGND, placed as close as possible to the IC.
18	$\overline{CE}$	DI	**Active low charge enable pin.** Battery charging is enabled when the corresponding register is set to active, and the $\overline{CE}$ pin is low.
19, 20	SCL	DI	**I²C clock interface.** Connect SCL to the logic rail through a 10kΩ resistor.
21	SDA	DIO	**I²C data interface.** Connect SDA to the logic rail through a 10kΩ resistor.
22	DISC	DI	**Battery disconnection control pin.** The DISC pin can be used for ship mode and to reset the system.
23	OTG	DI	**Boost mode enable control pin.** The On-the-Go (OTG) function is enabled through the I²C. During boost operation, the OTG pin can go low to suspend boost operation.
24	ILIM	AI	**Configurable input current limit.** To set the maximum input current limit, connect a resistor from ILIM to ground. The actual input current limit is the lower value between what is set by the ILIM pin and the I²C.
25	DM	AIO	**Negative pin of the USB data line pair.**

Note:

1) AI = analog input, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output, P = power

ABSOLUTE MAXIMUM RATINGS (2)

IN, PMID to GND ..... -0.3V to +22V
SW to GND.....-0.3V (-2V for 20ns) to +22V
BST to GND..... SW to SW + 5V
BATT, SYS to GND..... .-0.3V to +6V
All other pins to GND ..... -0.3V to +5V
STAT, INT sink current 10mA
Continuous power dissipation (T_A = 25°C) (3)
.....2.6W
Junction temperature.....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM).....±2kV
Charged device model (CDM)..... ±500V

Recommended Operating Conditions (4)

V_{IN} to GND ..... 3.7V to 5.5V
I_{IN} ..... Up to 3.25A
I_{SYS} ..... Up to 4.5A
I_{CHG} ..... Up to 3A
V_{BATT} ..... Up to 4.67V
$I_{DISCHARGE}$ (continuous)..... Up to 8.5A
$I_{DISCHARGE}$ (pulse) ..... Up to 9A
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-26 (3.5mmx3.5mm)	48	11... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Step-Down Converter						
Input voltage range	V_{IN}		3.7		5.5	V
Input suspend current	I_{IN_SUS}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, suspended mode, EN_HIZ = 1		1	1.5	mA
Input quiescent current	I_{IN_Q}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, V_{BATT} = 3.6V, converter switching, I_{SYS} = 0A		4		
Input under-voltage lockout threshold	V_{IN_UVLO}	V_{IN} falling		3	3.2	V
Input under-voltage lockout threshold hysteresis		V_{IN} rising		200		mV
Input vs. battery voltage headroom	V_{HDRM}	V_{IN} rising	230	300	370	mV
		V_{IN} falling	120	190	260	mV
Input over-voltage protection threshold	V_{IN_OVLO}	V_{IN} rising	5.8	6	6.3	V
Input over-voltage protection threshold hysteresis		V_{IN} falling		380		mV
Internal reverse-blocking MOSFET on resistance	R_{ON_Q1}	Measured from IN to PMID		20		mΩ
High-side MOSFET on resistance	R_{ON_Q2}	Measured from PMID to SW		37		mΩ
Low-side MOSFET on resistance	R_{ON_Q3}	Measured from SW to PGND		37		mΩ
Switching frequency	f_{SW}	V_{BATT} = 3.7V, I_{CHG} = 2A, REG0Ah, bit[7] = 0	1.1	1.35	1.6	MHz
SYS Output						
Minimum system regulation voltage (I²C)	$V_{SYS\_REG\_MIN}$	V_{SYS_MIN} + V_{TRACK}, I_{SYS} = 0A, V_{BATT} = 3.4V, REG04h, bit[0] = 1, REG04h, bits[3:1] = 110		3.82		V
Battery track voltage	V_{TRACK}	REG04h, bit[0] = 0		100		mV
		REG04h, bit[0] = 1		150		mV
Ideal diode forward voltage in supplement mode	V_{FWD}	10mA discharge current		20		mV
SYS vs. BATT comparator	$V_{SYS\_GT\_BATT}$	VSYS falling to enter ideal diode mode		-20		mV
SYS vs. BATT comparator hysteresis		VSYS rising to exit ideal diode mode		50		mV
Battery good comparator (threshold compared with V_{SYS_MIN})	V_{BATT_GD}	V_{BATT} rising to the battery FET being turned on fully		60		mV
Battery good comparator hysteresis		V_{BATT} falling		100		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery charge voltage regulation (I²C)	V_{BATT_REG}	Depends on the I²C setting	3.4		4.67	V
Battery charge voltage regulation accuracy	$V_{BATT\_REG\_ACC}$	REG07h, bits[7:1] = 1010000 (4.2V)	-0.5		+0.5	%
		REG07h, bits[7:1] = 1011111 (4.35V)				
		REG07h, bits[7:1] = 1100100 (4.4V)				
Fast charge current (I²C)	I_{CC}	Depends on the I²C setting	320		3000	mA
Fast charge current accuracy	I_{CC_ACC}	REG05h, bits[5:0] = 000100, V_{BATT} = 3.8V	462	530	598	mA
		REG05h, bits[5:0] = 100110, V_{BATT} = 3.8V	1849	1950	2071	mA
		REG05h, bits[5:0] = 111111, V_{BATT} = 3.8V	2859	3000	3151	mA
Pre-charge to fast charge threshold (I²C)	V_{BATT_PRE}	V_{BATT} rising, REG05h, bit[7] = 1	2.8	3.0	3.1	V
Pre-charge to fast charge hysteresis		V_{BATT} falling		160		mV
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2.0	2.1	V
Trickle charge to pre-charge threshold hysteresis		V_{BATT} falling		50		mV
Trickle-charge current	I_{TC}	V_{BATT} = 1.8V, I_{PRE}[0] = 1		185		mA
		V_{BATT} = 1.8V, I_{PRE}[0] = 0		145		
Pre-charge current (I²C)	I_{PRE}	Depends on the I²C setting	150		750	mA
Pre-charge current accuracy		V_{BATT} = 2.6V, REG06h, bits[7:4] = 0010	182	225	268	mA
Charge termination current threshold (I²C)	I_{TERM}	Determined by the I²C setting	120		720	mA
Termination current accuracy		V_{BATT_REG} = 4.2V, REG06h, bits[3:0] = 0110	298	360	422	mA
Charge termination deglitch time	t_{TERM_DGL}			200		ms
Auto-recharge voltage threshold below V_{BATT_REG}	V_{RECH}	REG07h, bit[0] = 0		110		mV
Auto-recharge deglitch time	t_{RECH_DGL}			200		ms
BATFET on resistance	R_{ON_Q4}	V_{BATT} = 3.8V		14		mΩ
Battery discharge current limit	I_{DSCHG_LMT}	V_{IN} = 0V, V_{BATT} = 3.8V, OTG disabled, I_{SYS} rising	8.5			A
Battery discharge function controlled by the DISC pin	t_{DISC}	DISC pin pulls low lasting time to turn off BATFET, REG0Ah, bits[1:0] = 00		8		s
		DISC pin pull low time or BATFET off time to reset BATFET, REG0Ah, bits[3:2] = 00		0.5		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Input Current Regulation						
Input minimum voltage regulation (I²C)	V_{IN_MIN}		3.7		5.2	V
Input minimum voltage regulation accuracy	$V_{IN\_MIN\_ACC}$	REG01h, bits[3:0] = 0110, V_{IN_MIN} = 4.3V	-3		+3	%
Input current limit	I_{IN_LIM}	USB500	400	450	500	mA
		USB900	750	825	900	
		1A	840	920	1000	
		CDP or 1.5A	1270	1400	1500	
		DCP	1570	1690	1800	
		2A	1750	1880	2000	
		2.1A	1840	1970	2100	
		2.4A	2050	2240	2400	
		3A	2640	2800	3000	
Protection						
Battery over-voltage protection threshold	V_{BATT_OVP}	Rising, compared to V_{BATT_REG}		103.5		%
Battery over-voltage protection threshold hysteresis		Compared to V_{BATT_REG}		1.5		%
Thermal regulation	T_{J_REG}	T_{J_REG}, bits[1:0] = 11		112		°C
Thermal shutdown threshold (6)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (6)				20		°C
NTC float threshold	V_{FLT}	As a percentage of V_{NTC}		95		%
NTC float threshold hysteresis		As a percentage of V_{NTC}		3.6		%
NTC low temp rising threshold	V_{COLD}	As a percentage of V_{NTC}	71	72	73	%
NTC low temp rising threshold hysteresis		As a percentage of V_{NTC}		1.3		%
NTC cool temp rising threshold	V_{COOL}	As a percentage of V_{NTC}	59	60	61	%
NTC cool temp rising threshold hysteresis		As a percentage of V_{NTC}		1.3		%
NTC warm temp falling threshold	V_{WARM}	As a percentage of V_{NTC}	39.3	40.3	41.3	%
NTC warm temp falling threshold hysteresis		As a percentage of V_{NTC}		1.5		%
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{NTC}	35.3	36.3	37.3	%
NTC hot temp falling threshold hysteresis		As a percentage of V_{NTC}		1.5		%

Note:

6) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREF LDO						
VREF LDO output voltage	V_{REF}	V_{IN} = 5V, I_{VREF} = 20mA		3.6		V
VREF LDO current limit	I_{REF_LMT}	V_{VREF} = 3.3V	40			mA
Battery Discharge Operation						
Battery operating range	V_{BATT}		2.6		4.75	V
Battery current in shipping mode	I_{BATT_SP}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATFET off		13	16	µA
Battery quiescent current	I_{BATT_Q}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATFET on, OTG is disabled		40	47	µA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATFET on, OTG is disabled, ADC enabled		2		mA
		V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, BATFET on, OTG is enabled		5.0		mA
OTG output voltage	V_{IN_DSCHG}	REG03h, bits[5:3] = 011 (5.1V), I_{OTG} = 0A		5.07		V
OTG output voltage accuracy		As percentage of V_{IN_OTG}, I_{OTG} = 0A	-2		+2	%
Battery operation UVLO	V_{BATT_UVLO}	V_{BATT} falling	2.35	2.45	2.55	V
		V_{BATT} rising	2.68	2.8	2.92	V
Battery operation UVLO for OTG	$V_{BATT\_UVLO\_OTG}$	V_{BATT} falling	2.45	2.55	2.65	V
		V_{BATT} rising		3.0		V
OTG output voltage protection threshold	V_{INOVP_DSCHG}	V_{BATT} = 3.7V, OTG is enabled, force a voltage at IN pin until switching is off		6.15		V
OTG output voltage protection threshold hysteresis				330		mV
OTG output current limit (I²C)	I_{IN_DSCHG}	REG03h, bits[1:0] = 00, V_{BATT} = 3.7V	0.5	0.6	0.7	A
		REG03h, bits[1:0] = 11, V_{BATT} = 3.7V	1.5	1.65	1.8	
Analog-to-Digital Converter (ADC)						
Resolution	RES			8		bits
Input voltage range	V_{IN}		3.6		7.62	V
Input voltage LSB	V_{IN_RES}			60		mV
Input voltage accuracy	V_{IN_ACC}	V_{IN} = 5V		2		LSB
Battery voltage range	V_{BATT}		0		5.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

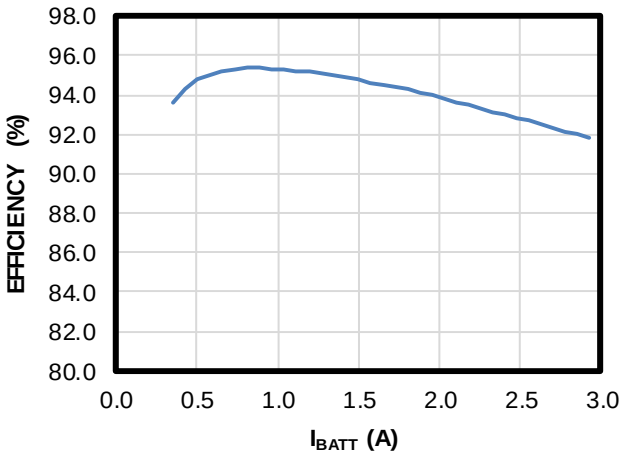
Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery voltage LSB	V_{BATT_RES}			20		mV
Battery voltage accuracy	V_{BATT_ACC}	V_{BATT} = 3.8V		2		LSB
Charge current LSB	I_{CHG_RES}			17.5		mA
Charge current accuracy	I_{CHG_ACC}	I_{CHG} = 1.92A		3		LSB
System voltage range	V_{SYS}		0		5.1	V
System voltage LSB	V_{SYS_RES}			20		mV
System voltage accuracy	V_{SYS_ACC}	V_{SYS} = 3.8V		2		LSB
Input current range	I_{IN}		0		3.39	A
Input current LSB	I_{IN_RES}			13.3		mA
Input current accuracy	I_{IN_ACC}	I_{IN} = 500mA		4		LSB
NTC voltage range	V_{NTC}		0		100	%
NTC voltage LSB	V_{NTC_RES}			0.392		%
NTC voltage accuracy	V_{NTC_ACC}	V_{NTC} = 50%		2		LSB
DP/DM USB Detection						
DP DCD current source	I_{DP_SRC}		7	10	14	µA
DM pull-down resistance	R_{DM_DOWN}		14.3	20	24.8	kΩ
Data detect voltage	V_{DAT_REF}		0.25	0.325	0.4	V
DP/DM comparator threshold (2.9V)	V_{TH_2P9}		2.8	2.9	3.0	V
DP/DM comparator threshold (2.4V)	V_{TH_2P4}		2.3	2.4	2.5	V
DP/DM comparator threshold (2.2V)	V_{TH_2P2}		2.1	2.2	2.3	V
DP/DM comparator threshold (1.7V)	V_{TH_1V7}		1.6	1.7	1.8	V
DP voltage source	V_{DP_SRC}		0.5	0.6	0.7	V
DM voltage source	V_{DM_SRC}		0.5	0.6	0.7	V
DP sink current	I_{DP_SINK}		70	100	130	µA
DM sink current	I_{DM_SINK}		70	100	130	µA
Leakage current input DP/DM pin	I_{DP_LKG}		-1		+1	µA
	I_{DM_LKG}		-1		+1	µA
Logic I/O Pin Characteristics (STAT, INT, OTG, /CE, DISC)						
Low logic voltage threshold	V_{IL}				0.4	V
High logic voltage threshold	V_{IH}		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level	V_{IH}	$V_{PULL\ UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock frequency	f_{CLK}			5		MHz
Watchdog timer	t_{WDT}	REG08h, bits[5:4] = 11		160		s

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1.92A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

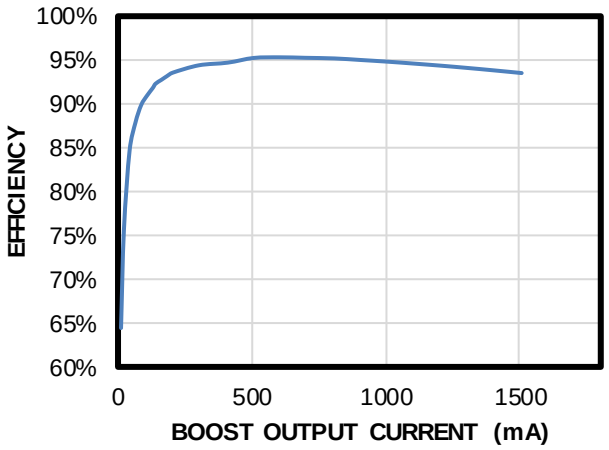
Charge Efficiency

V_{BATT} = 3.8V

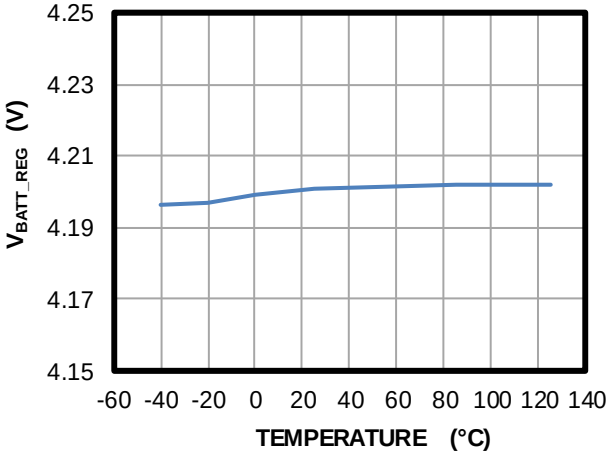


Boost Efficiency

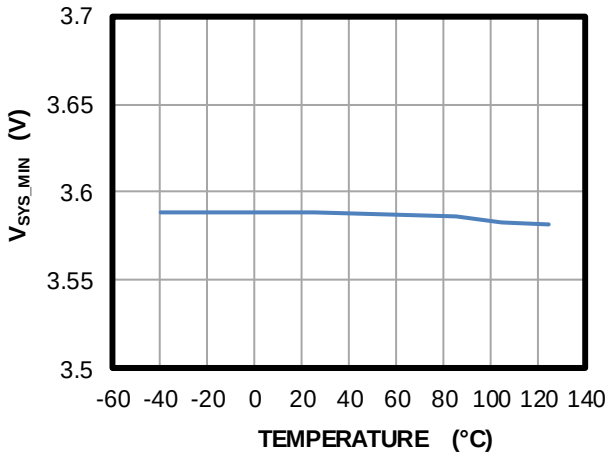
V_{BATT} = 3.8V



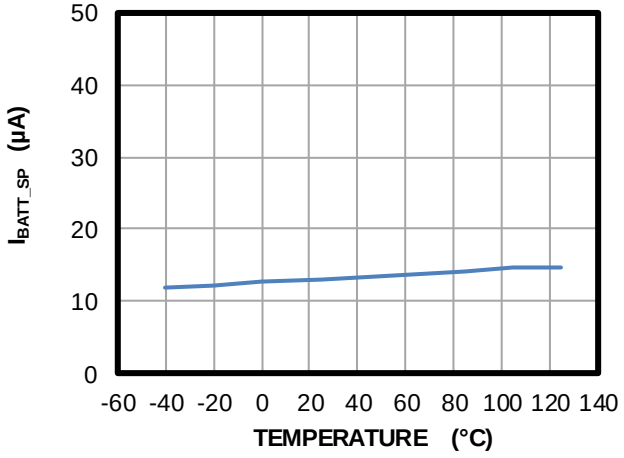
Battery Regulation Voltage vs. Temperature



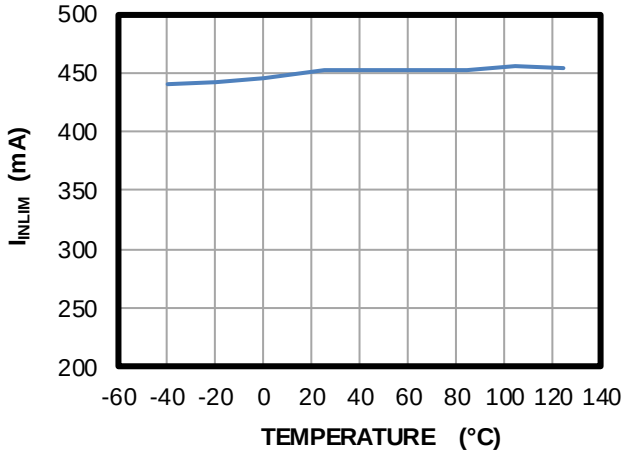
System Minimum Voltage vs. Temperature



Battery Current in Shipping Mode vs. Temperature



500mA Input Current Limit vs. Temperature

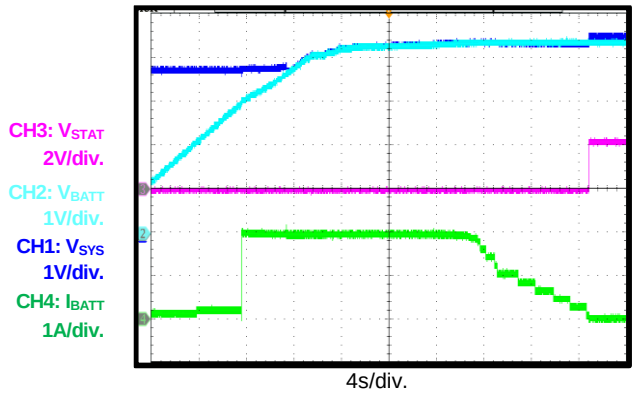


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1.92A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

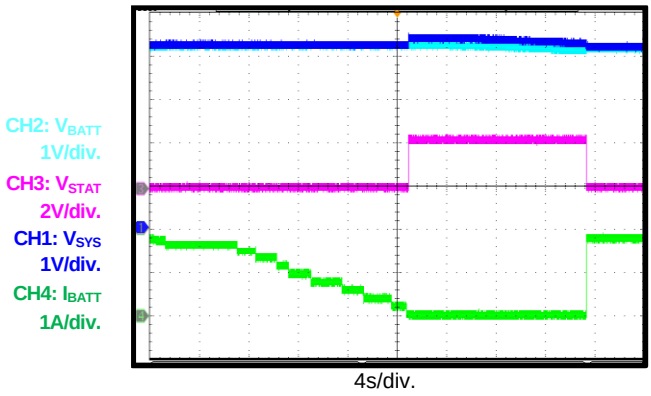
Battery Charge Curve

V_{IN} = 5V, V_{BATT_REG} = 4.35V, I_{SYS} = 0A



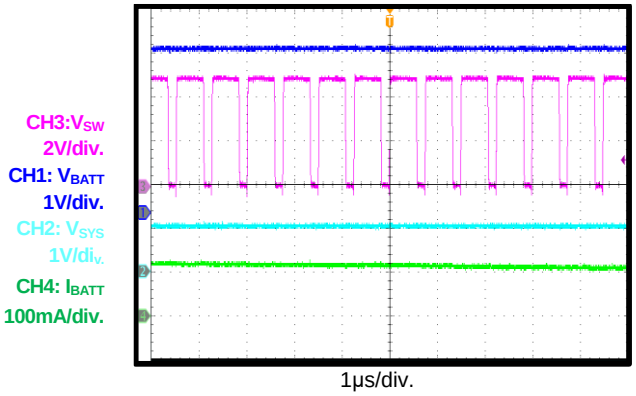
Auto-Recharge

V_{IN} = 5V, V_{BATT_REG} = 4.2V, I_{SYS} = 0A



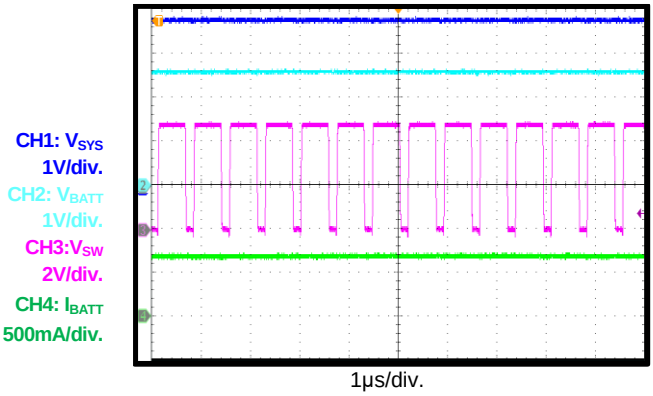
Trickle Charge

V_{IN} = 5V, V_{BATT} = 1.0V, I_{TC} = 145mA



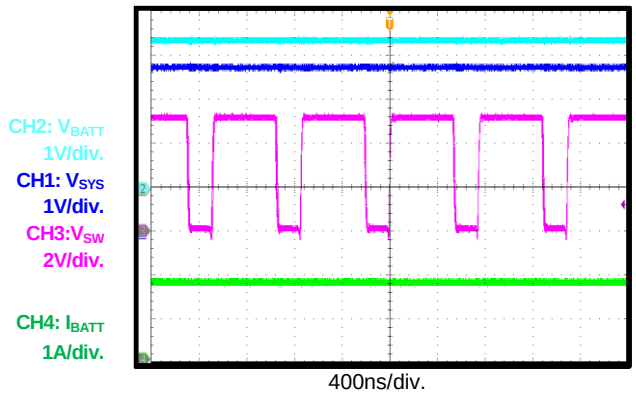
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2.5V, I_{PRE} = 680mA



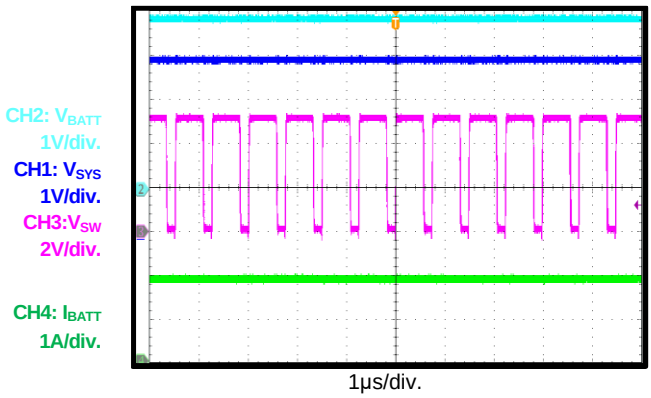
Constant Current Charge

V_{IN} = 5V, V_{BATT} = 3.3V



Constant Current Charge

V_{IN} = 5V, V_{BATT} = 3.8V

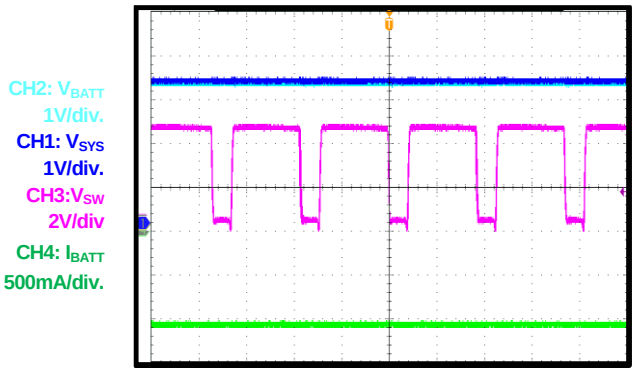


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1.92A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

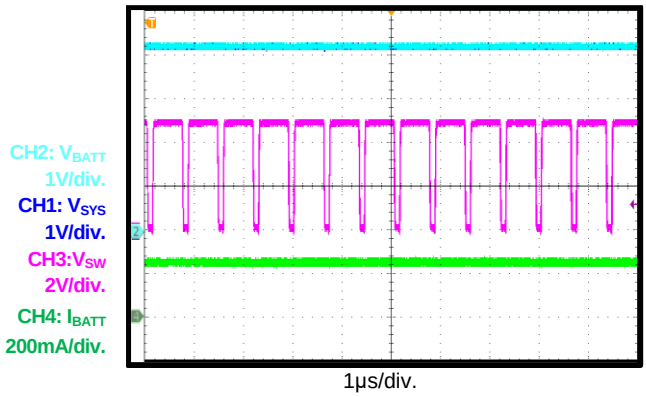
Battery Supplement Mode

V_{IN} = 5V, V_{BATT} = 3.8V, I_{SYS} = 4.5A



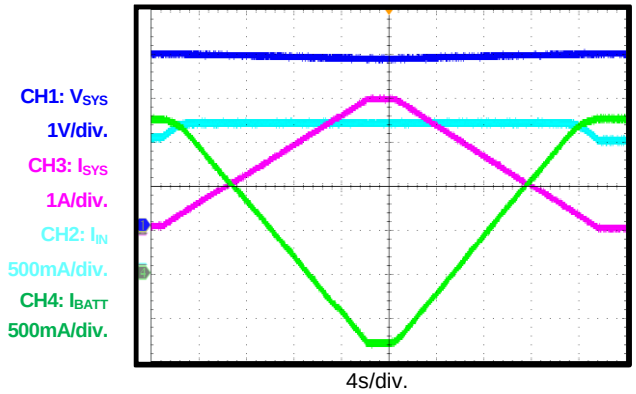
Constant Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.2V, I_{SYS} = 0A



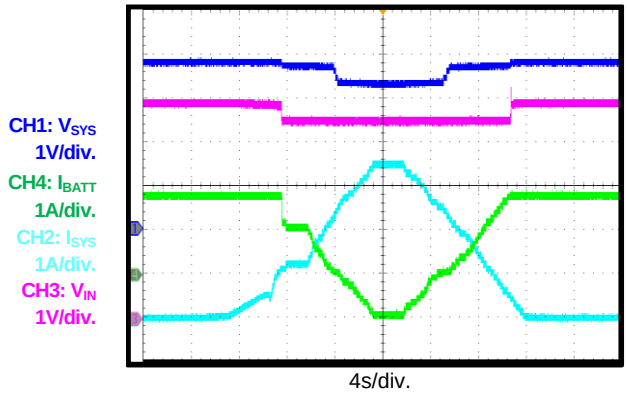
Input Current Limit

V_{IN} = 5V, V_{BATT} = 3.8V, I_{IN_LIM} = 1800mA



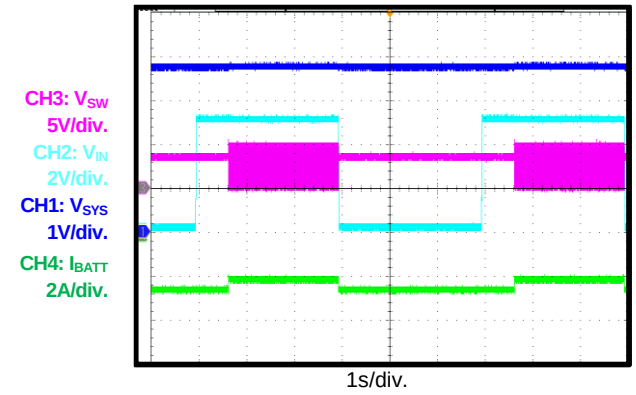
Input Voltage Limit

V_{IN} = 5V (2A), V_{BATT} = 3.3V, V_{IN_MIN} = 4.6V



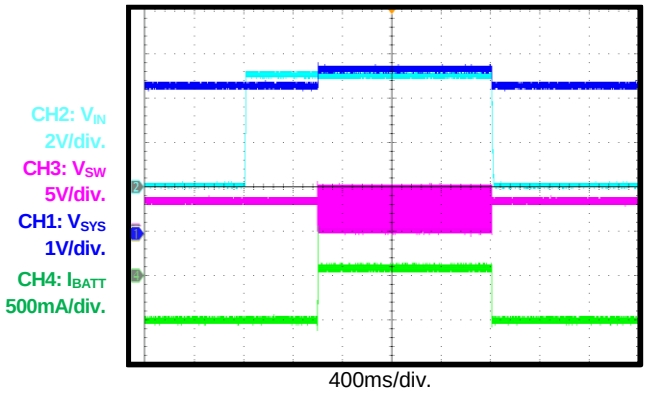
Power-On/Off Waveform

V_{IN} = 5V, V_{BATT} = 3.8V, I_{SYS} = 2.5A, default mode



Power-On/Off Waveform

V_{IN} = 5V, V_{BATT} = 3.3, I_{SYS} = 0.5A, default mode

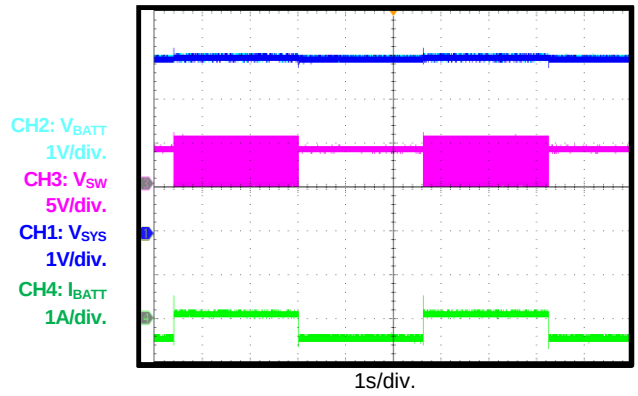


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1.92A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

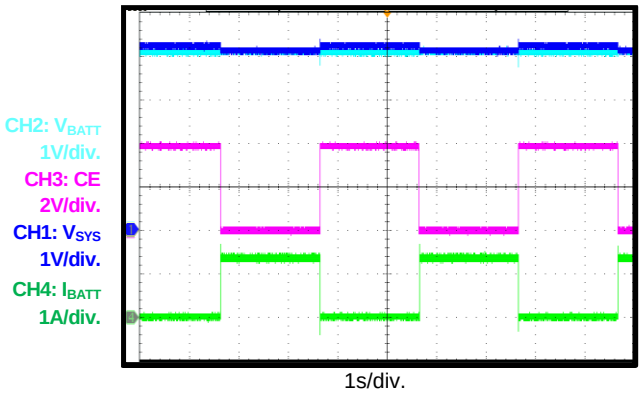
Suspend Mode On/Off

V_{IN} = 5V, V_{BATT} = 4.0V, I_{SYS} = 0.5A, default mode



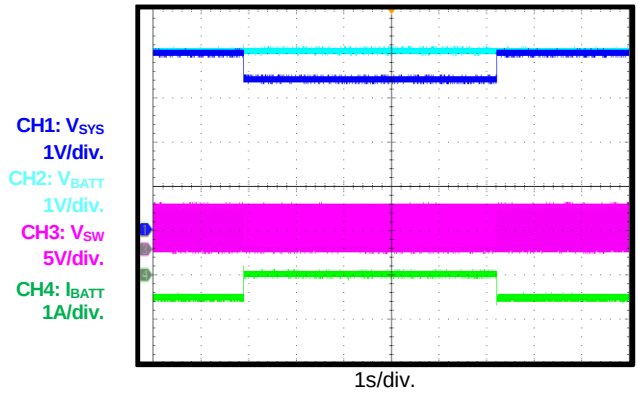
Charge On/Off

V_{IN} = 5V, V_{BATT} = 4.0V, I_{SYS} = 0A



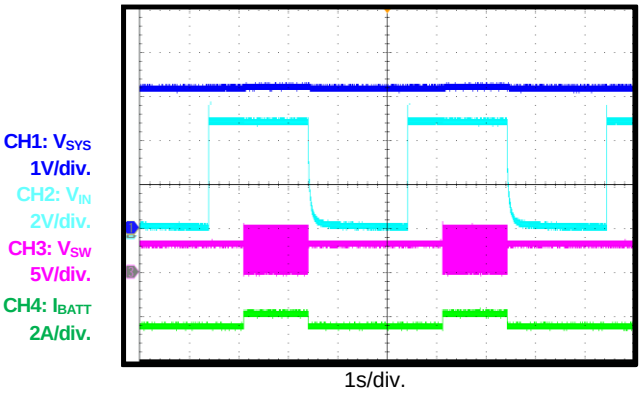
BATFET On/Off

V_{IN} = 5V, V_{BATT} = 4.0V, I_{SYS} = 4A



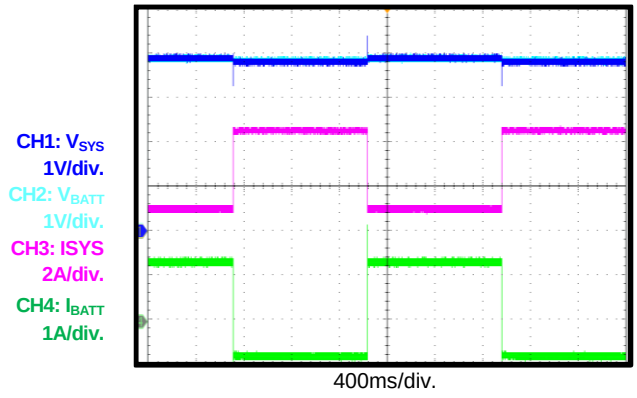
VIN Hot Insertion/Removal

V_{IN} = 5V, V_{BATT} = 3.3V, I_{SYS} = 4.5A, default mode



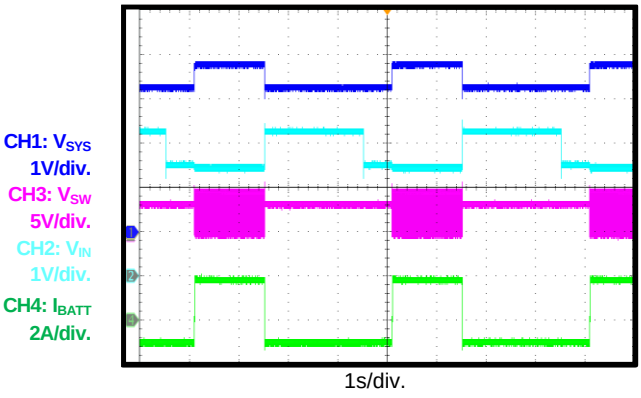
SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.8V, I_{SYS} = 1A to 4.5A, transient



VIN OVP Test

V_{IN} = 5V to 6.5V transient, V_{BATT} = 3.3V, I_{SYS} = 1A

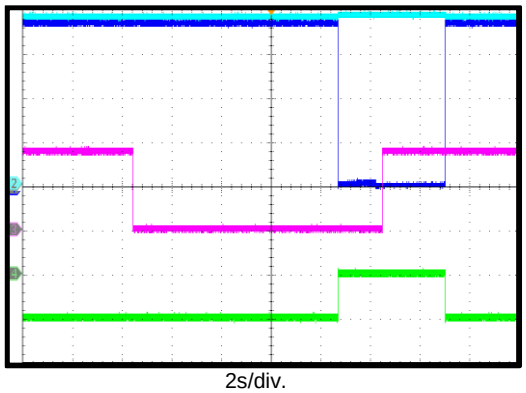


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I²C-controlled, I_{CC} = 1.92A, I_{IN_LIM} = 3.0A, V_{IN_MIN} = 4.3V, L = 1.0µH (DCR = 14.9mΩ), T_A = 25°C, unless otherwise noted.

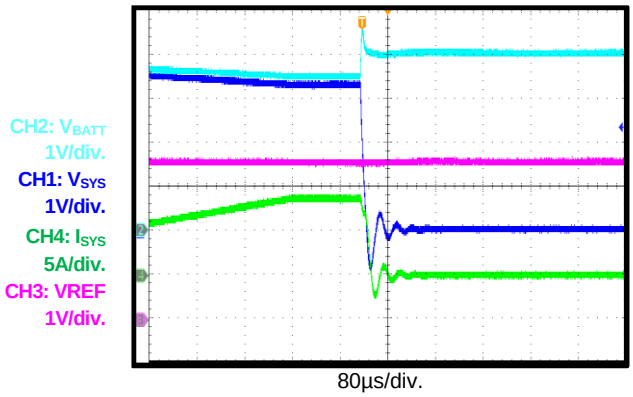
System Reset Mode

V_{IN} = float, V_{BATT} = 3.8V, I_{SYS} = 2A



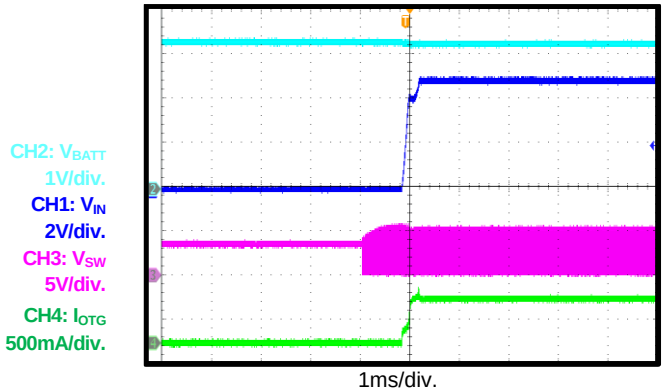
Battery Discharge Current

V_{IN} = float, V_{BATT} = 4.0V, I_{SYS} = up to 9A



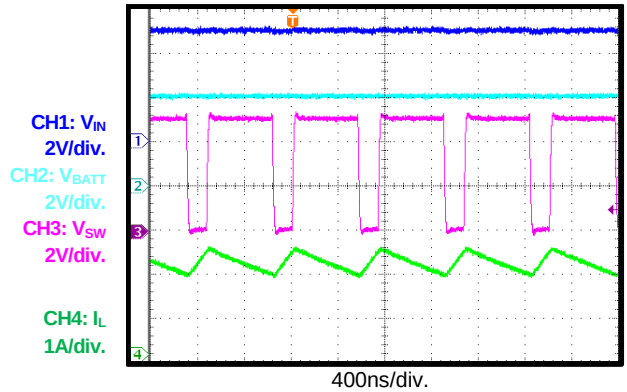
OTG Mode Start-Up

V_{IN} = float, OTG mode, V_{BATT} = 3.3V, I_{IN_DSCHG} = 0.5A, I_{OTG} = 0.5A



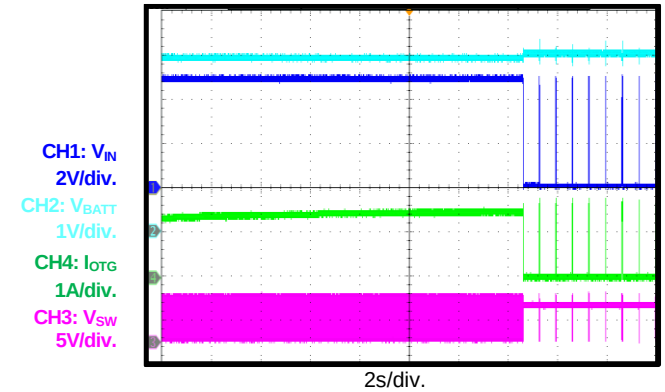
OTG Steady State Operation

V_{IN} = float, OTG mode, V_{BATT} = 4.0V, I_{IN_DSCHG} = 1.5A, I_{OTG} = 1.5A



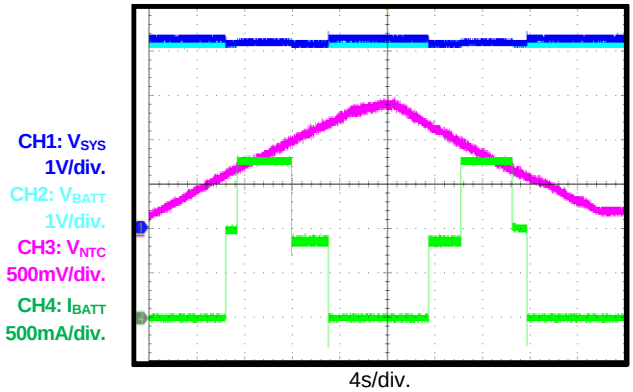
OTG Voltage Regulation

V_{IN} = float, OTG mode, V_{BATT} = 4.0V, I_{IN_DSCHG} = 1.5A, I_{OTG} = 0A to 1.5A



NTC JIETA Operation

V_{IN} = 5V, V_{BATT} = 4.1V, I_{SYS} = 0A, J_{EITA_VSET} = -100mV, J_{EITA_ISET} = 50%



FUNCTIONAL BLOCK DIAGRAM

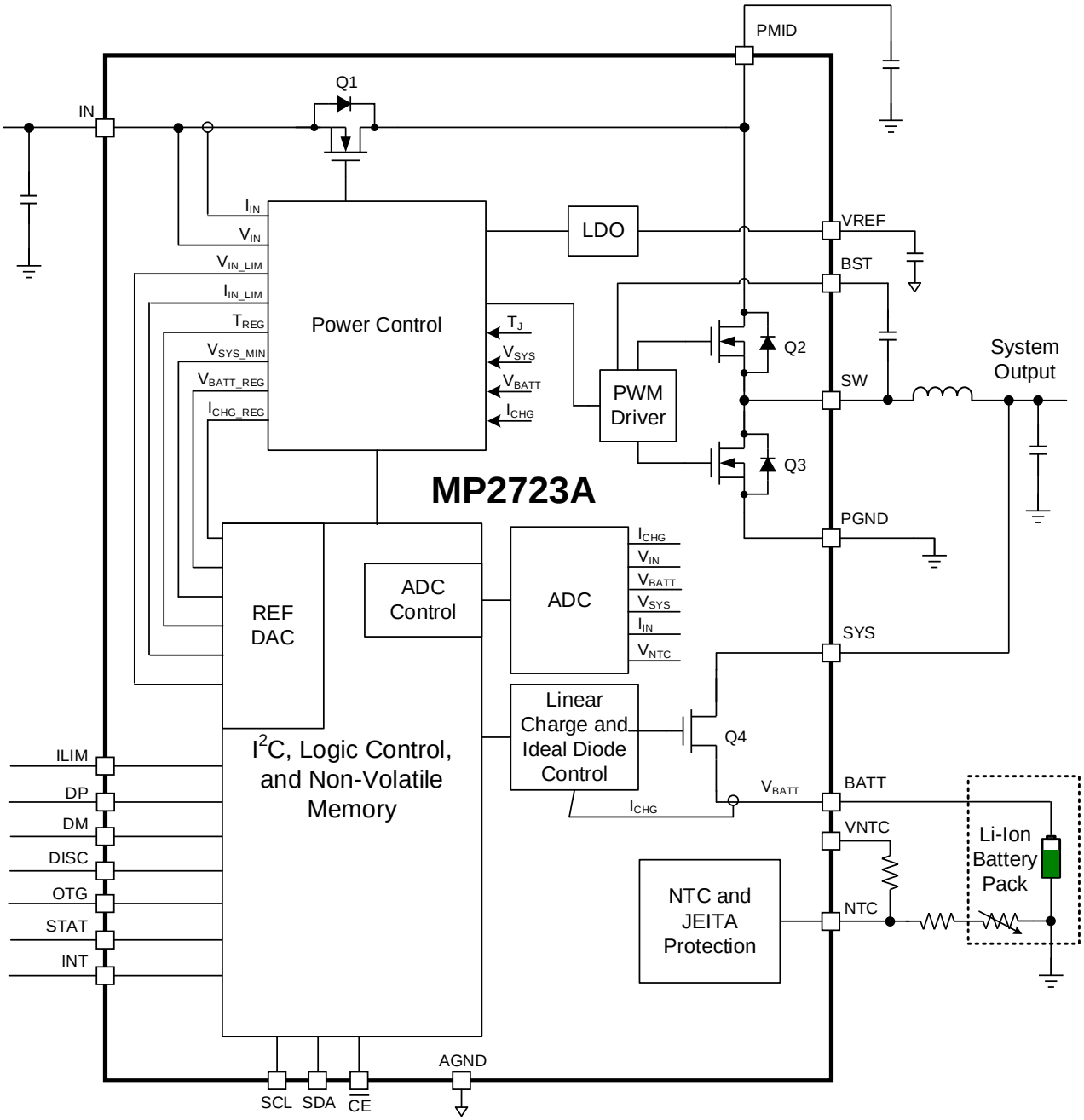


Figure 2: Functional Block Diagram

OPERATION

The MP2723A is a highly integrated, 3A, switch-mode battery charger IC with NVDC power path management for single-cell Li-ion or Li-polymer battery applications. The device integrates a reverse blocking FET (Q1), high-side switching FET (Q2), low-side switching FET (Q3), and battery FET (Q4) between the SYS and BATT pins.

Power Supply

The VREF pin's voltage supplies the internal bias circuits as well as the high-side and low-side MOSFET gate drivers. The STAT pull-up rail can also be connected to VREF. The VREF pin has an internal LDO, which has two inputs. One input is from IN, and the other is from a battery. VIN and the battery voltage are connected to the input of the LDO via a P-channel MOSFET.

Figure 3 shows the VREF power supply circuit.

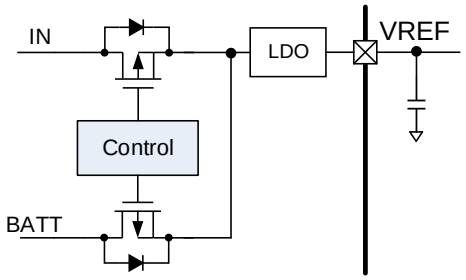


Figure 3: VREF Power Supply Circuit

Device Start-Up from an Input Source

When an input source is plugged in, the MP2723A checks the input source before start-up. The input source must meet the following requirements:

1. $V_{IN} > V_{BATT} + V_{HDRM}$
2. $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$

If the input power source meets the conditions above, a good input is detected, and the device asserts an INT signal to the host. Then the device detects the input source type via the DP/DM pins. When DP/DM detection completes, the status register bits (VIN_STAT) changes, and an INT pulse is sent to the host. Then the device starts up the step-down converter.

NVDC Power Path Management

The MP2723A employs a narrow-voltage DC (NVDC) power structure with the battery FET, decoupling the system from the battery and thus allowing separate controls between the system and the battery. The system is a priority during start-up, even if the battery is deeply discharged or missing. If the input power is available with a depleted battery, the system voltage is regulated at the minimum system voltage ($V_{SYS\_REG\_MIN}$).

Figure 4 shows the NVDC power structure, which is comprised of a front-end, step-down DC/DC converter, and a battery FET placed between the SYS and BATT pins.

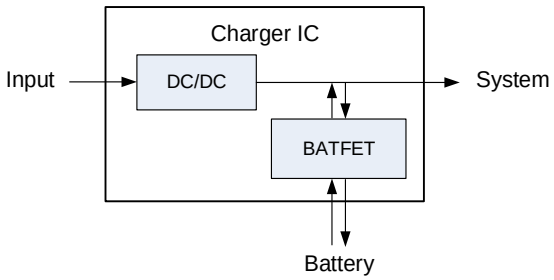


Figure 4: NVDC Power Path Management Structure

The DC/DC converter is a 1.35MHz step-down switching regulator, which drives the system load directly, and charges the battery through the battery FET.

The system regulates the voltage in the following ways:

1. If the battery voltage drops below V_{SYS_MIN}, the system voltage is regulated at a minimum system voltage ($V_{SYS\_REG\_MIN}$), which exceeds V_{SYS_MIN} by V_{TRACK}. The battery FET works linearly to charge the battery via trickle charge, pre-charge, or fast charge current, depending on the battery voltage. V_{SYS_MIN} can be set via register REG04h, bits[3:1], and V_{TRACK} can be set via REG04h, bit[0].
2. When the battery voltage exceeds V_{SYS_MIN} + V_{BATT_GD} (60mV), the battery FET fully turns on, and the voltage difference between the system and the battery is the V_{DS} of BATFET. The charge current loop is implemented by the PWM control of the DC/DC converter.
3. If charging is suspended or completed (the battery FET is off), the system voltage is

always regulated at its maximum value, (V_{SYS_MIN}, V_{BATT}) + V_{TRACK}.

Figure 5 shows how the voltage is regulated.

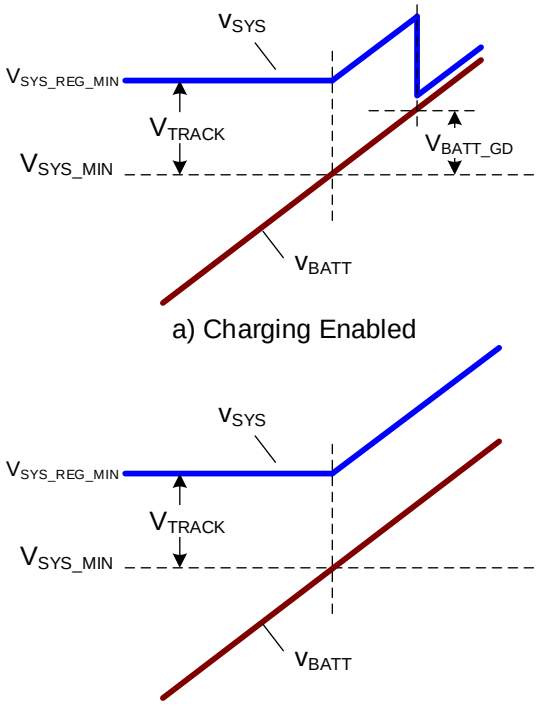


Figure 5: V_{SYS} Variation with V_{BATT}

Dynamic Power Management

To meet the maximum current limit in USB specifications and avoid overloading the adapter, the MP2723A features dynamic power management (DPM), and continuously monitors the input current and input voltage. The total input current limit is configurable to prevent the input source from being overloaded. If the input current increases and reaches the input current limit, the charge current is reduced to prioritize the system power.

If the preset input current limit exceeds the adapter's rating, the additional minimum input voltage regulation loop activates to prevent the input power source from being overloaded. When the input voltage falls below the input voltage regulation threshold due to a heavy load, the charge current is reduced to prevent the input voltage from dropping further.

Power path management can operate in two ways:

1. If V_{BATT} < V_{SYS_MIN} + V_{BATT_GD}, the system voltage is regulated at $V_{SYS\_REG\_MIN}$. If the input current or voltage regulation threshold is reached, the input current loop or input voltage loop controls the DC/DC converter, the system voltage drops, and the battery FET driver is pulled down to decrease the charge current. This prioritizes the system power requirement.
2. The second scenario occurs if the battery is directly connected to the system, and V_{BATT} > V_{SYS_MIN} + V_{BATT_GD}. Due to the free transition between each control loop, the charge decreases automatically when the input current limit or voltage regulation threshold is reached.

Battery Supplement Mode

If the device reaches the input current limit or input voltage threshold, the charge current decreases. If the input source is still overloaded when the charge current decreases to zero, the system voltage starts to decrease. If the system voltage drops below the battery voltage, the MP2723A enters battery supplement mode, in which the battery simultaneously powers the system and the DC/DC converter.

The MP2723A offers ideal diode mode to optimize the control transition between the battery FET and the DC/DC converter. The battery FET enters ideal diode mode under either of the following conditions:

a) V_{IN} start-up from the battery supply system

b) V_{BATT} < V_{SYS_MIN}, and the system voltage drops below the battery voltage

During ideal diode mode, the battery FET operates as an ideal diode, and regulates the battery FET's gate drive. The battery FET V_{DS} stays at about 20mV. As the discharge current increases, the battery FET's gate drive increases, and its R_{DS} decreases until the battery FET is fully on.

Battery Charge Profile

If V_{IN} powers on, CHG_CONFIG bit = 01, and the $\overline{CE}$ pin is low, the device completes a charging cycle without host involvement. However, the host can set different charging parameters to optimize the charge profile by writing to the corresponding registers via the I²C.

A new charge cycle starts when all of the following conditions are valid:

- Good input power is inserted
- Battery charging is enabled by the I²C, and $\overline{CE}$ is forced to a low logic
- There is no thermistor fault on the NTC pin
- There is no safety timer fault
- BATFET is not forced to turn off

The MP2723A provides four main charging phases: trickle charge, pre-charge, constant current charge, and constant voltage charge, described below:

Phase 1 (trickle charge): When the input power qualifies as a good power supply, the MP2723A checks the battery voltage to decide if trickle charge is required. If the battery voltage is below V_{BATT_TC} (2.0V), a trickle-charge current is applied on the battery, which helps reset the protection circuit in the battery pack. The trickle-charge current can be set via REG06h, bit[4]. If REG06h, bit[4] is set to 1, the trickle-charge current is 185mA. If REG06h, bit[4] is set to 0, the trickle-charge current is 145mA.

Phase 2 (pre-charge): If the battery voltage exceeds V_{BATT_TC}, the MP2723A starts to safely pre-charge the depleted battery until the battery voltage reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle ends and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via I²C register REG06h, bits[7:4], and can be set between 150mA and 750mA.

Phase 3 (constant current charge): If the battery voltage exceeds V_{BATT_PRE} (set via REG05h, bit[7]), the MP2723A enters a constant current charge (fast charge) phase. The fast-charge current can be configured to as high as to 3A via REG05h, bits[5:0].

There are two stages during fast charge. First, the battery FET works linearly to charge the battery with a fast charge current. Once the battery voltage exceeds V_{SYS_MIN} + V_{BATT_GD}, the battery FET is fully turned on. The charge current loop is implemented by the PWM control of the buck converter.

Phase 4 (constant voltage charge): When the battery voltage rises to the configurable float voltage (V_{BATT_REG}) set via REG07h, bits[7:1], the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the battery termination threshold (I_{TERM}) set via REG06h, bits[3:0] after a 200ms termination deglitch time (assuming that the termination function is enabled if REG08h, bit[7] is set to 1). If I_{TERM} is not reached before the safety charge timer expires, the charge cycle ends, and a corresponding timeout fault signal is asserted (see the Safety Timer section on page 24).

Figure 6 shows the charge profile.

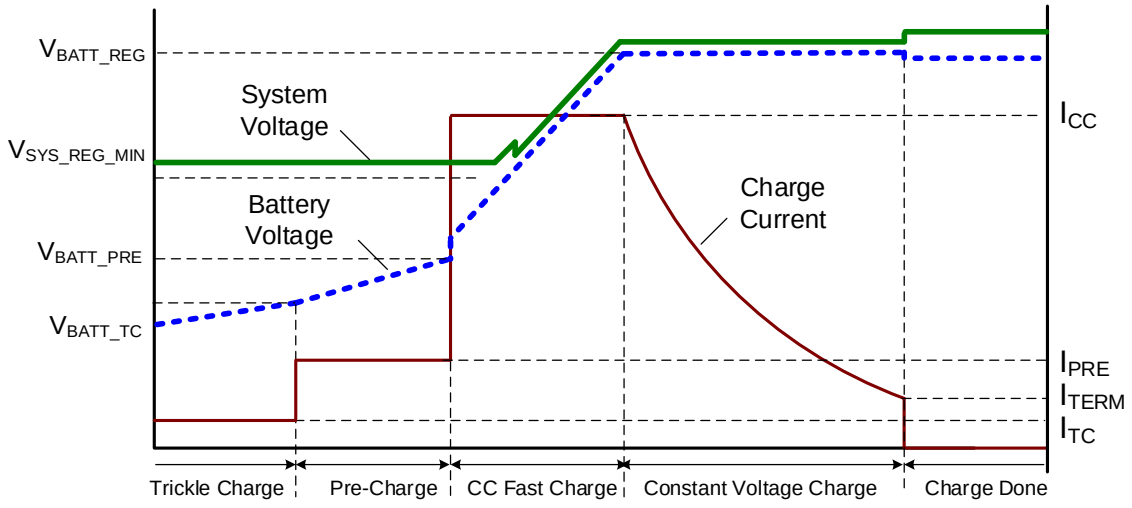


Figure 6: Battery Charge Profile

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, like dynamic power management (DPM) regulation (input current limit or input voltage regulation loop), or thermal regulation. Thermal regulation reduces the charge current so that the IC junction temperature does not exceed the preset limit. The multiple thermal regulation thresholds (from 60°C to 120°C) help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via REG02h, bits[3:2].

Automatic Recharge

When the battery is done charging, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold after a 200ms automatic recharge deglitch time, the MP2723A automatically starts a new charging cycle.

CE Control

$\overline{CE}$ is a logic input pin that enables/disables battery charging, or restarts a new charging cycle. Battery charging is enabled when CHG_CONFIG (REG04h, bits[5:4]) is set to 01 and the $\overline{CE}$ pin is pulled to logic low.

Battery Over-Voltage Protection (OVP)

The MP2723A is designed with built-in battery over-voltage protection (OVP). When the battery voltage exceeds 103.5% of V_{BATT_REG}, the MP2723A immediately suspends charging and asserts a fault. When battery OVP occurs, only the charging is disabled, and the DC/DC converter keeps operating.

System Over-Voltage Protection (OVP)

The MP2723A monitors the voltage at the SYS pin. When an over-voltage condition (V_{SYS} > V_{BATT_REG} + 0.4V) is detected, the DC/DC converter turns off and the system is powered by the battery via the BATFET.

Automatic Input Current Optimizer

The device provides an optimized input current limit without overloading the input source. This function can be enabled or disabled by configuring the AICO_EN bit, which is disabled by default. If AICO is enabled, I_{IN_LIM} is set to a larger current, and the input voltage drops to V_{IN_MIN}, the AICO function is triggered. This function decreases I_{IN_LIM} step by step, until the input voltage exits V_{IN_MIN} control. The input current limit remains optimized and does not automatically run the AICO function unless another V_{IN_MIN} event occurs.

The actual input current limit is reported in the I_{IN_DPM} register when the AICO function is enabled (AICO_EN = 1). If the AICO function is disabled (AICO_EN = 0), the input current limit is set by the I_{IN_LIM} register. Any write to I_{IN_LIM} can reset I_{IN_DPM} to the same value of I_{IN_LIM} when the AICO function is enabled.

Input Source Type Detection

The MP2723A features input source detection that is compatible with USB Battery Charging Specification 1.2 (BC1.2) and nonstandard adapters. The user can force DP/DM detection in host mode by writing 1 to the USB_DET_EN (REG0Bh, bit[5]).

When the input voltage is first applied, and a good input source is detected, the BC1.2 detection starts first with data content detection (DCD). If DCD is effective, the standard downstream port (SDP), charging downstream port (CDP), and dedicated charging port (DCP) can be distinguished. If the 500ms DCD timer expires, then the MP2723A proceeds with nonstandard adapter detection.

DCD uses a current source to detect when the data pins have made contact during an attach event. The protocol for DCD is as follows:

- The portable device (PD) detects V_{IN} assertion
- The PD turns on DP (I_{DP_SRC}) and the DM pull-down resistor
- The PD waits for the DP line to be low
- If the DP line is detected to be low for 10ms, the PD starts primary detection
- If data contact is not detected, the DCD timer (500ms) expires

After the DCD timer expires, the PD turns off I_{DP_SRC} and the DM pull-down resistor. Then the 50ms timer starts, and the PD can detect a special adapter. If a special adapter is detected, an INT is sent to the host. Otherwise, the PD

starts primary detection after the 50ms timer expires.

Primary detection is used to distinguish between USB hosts (or the SDP) and different types of charging ports.

During primary detection, the IC turns on V_{DP_SRC} on DP, and I_{DM_SINK} on DM. If the portable device is attached to a USB host, the DM pin pulls low. Then SDP is detected, and sends an INT signal to the host.

If the DM pin is high, the IC goes into secondary detection, which distinguishes between a CDP and a DCP.

During secondary detection, the IC turns on V_{DM_SRC} on DM, and I_{DP_SINK} on DP. If the input source is a CDP and DP is low, then the CDP is detected and an INT signal is sent to the host. If DP is high, the DCP source is detected, and an INT is sent to the host.

Table 1 lists input current limits that are compatible with the USB specifications and BC1.2.

Table 1: Input Current Limit vs. USB Type

DP/DM Detection	I_{IN_LIM} (A)	V_{IN_OVP} (V)	V_{IN_MIN} (V)
Apple 1.0A	1	6	3.7 to 5.2
Apple 2.1A	2.1	6	3.7 to 5.2
Apple 2.4A	2.4	6	3.7 to 5.2
SDP	0.5	6	3.7 to 5.2
CDP	1.5	6	3.7 to 5.2
DCP	1.8	6	3.7 to 5.2

USB detection is independent of the charge enable status. After DP/DM detection is complete, the MP2723A indicates the USB port type in status register VIN_STAT (REG0Ch, bits[7:5]), and asserts an INT signal to the host. The host can revise the input current limit according to VIN_STAT.

Input Current Limit Setting via ILIM

For safe operation, the MP2723A has an additional hardware pin (ILIM) to adjust the maximum input current limit. The limit can be set by connecting a resistor from ILIM to GND. The actual input current limit is the lower value between what is set by the ILIM pin and the value set by the I²C.

The current limit set by the ILIM pin can be calculated with Equation (1):

$$I_{IN\_LIM}=\frac{120}{R_{ILIM}(k\Omega)}(A) \quad (1)$$

Battery Temperature Monitoring in Charge Mode

The MP2723A continuously monitors the battery's temperature by measuring the voltage at the NTC pin. This value is typically determined by a negative temperature coefficient (NTC) thermistor and external voltage dividers. For the NTC thermistor, a hotter ambient temperature corresponds with a lower resistance and voltage ratio, and vice versa.

Figure 7 shows an NTC protection circuit. The external resistor dividers and the internal reference resistor series are pulled up to the VNTC pin. The voltage ratios between the internal and external dividers are compared to determine if an NTC protection has been triggered. The VNTC voltage (1.7V) is regulated by an LDO that is powered from VREF. The VNTC pin is available in both charge mode and OTG mode.

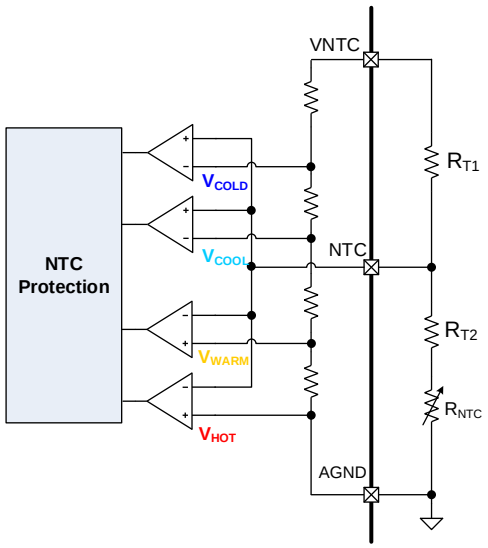


Figure 7: NTC Protection Circuit

The MP2723A provides standard and JEITA battery temperature monitoring, which can be selected by the NTC_TYPE bit. If the standard type is selected, and the external voltage ratio transitions from the high temperature threshold (V_{HOT}) to the low temperature threshold (V_{COLD}), this means that the battery temperature is out of the cold-to-hot range. The IC suspends charging and reports the NTC fault.

Charging resumes automatically after the battery temperature is within the cold-to-hot temperature range again.

If the JEITA type is selected, the MP2723A monitors four temperature thresholds: the cold temperature threshold (T_{NTC} < 0°C, default), the cool temperature threshold (0°C < T_{NTC} < 15°C, default), the warm temperature threshold (45°C < T_{NTC} < 55°C, default), and the hot temperature threshold (T_{NTC} > 55°C, default).

For a given NTC thermistor, these temperatures correspond to the values for V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}. These voltage thresholds can be configured via REG16h, bits[5:0] to set different temperature ranges.

If V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, the charging and timers are suspended. If V_{HOT} < V_{NTC} < V_{WARM}, the battery regulation voltage (V_{BATT_REG}) is reduced by 200mV, which can be configured via REG16h, bit[7]. If V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to 16.7%, which can be configured via REG16h, bit[6]. Figure 8 shows JEITA control.

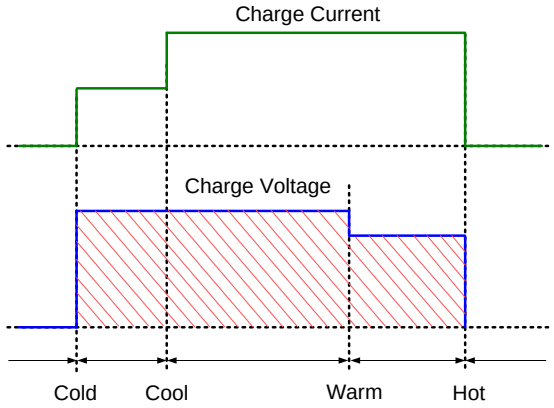


Figure 8: NTC Window

The MP2723A provides PCB over-temperature monitoring. The PCB over-temperature response is selected by the NTC_OPT bit (REG02h, bit[1]). If this bit is set to 1, PCB over-temperature protection is enabled. If this bit is set to 0 (the default setting), the battery temperature monitoring and corresponding protection features mentioned above are utilized instead.

While monitoring over-temperature conditions in the PCB, the IC continuously monitors the PCB temperature at the NTC pin. If the NTC pin voltage is below the threshold that reuses V_{HOT}, the DC/DC converter and battery FET turn off. Operation resumes once the NTC pin voltage goes back to the normal value.

If the NTC thermistor is removed, NTC is pulled up to VNTC (see Figure 7 on page 22). If the MP2723A detects an NTC voltage exceeding 95% of VNTC, then the NTC thermistor float is detected. The MP2723A sends an INT signal to the host, and the RNTC_FLOAT_STAT bit is set to 1.

Battery Temperature Monitoring in OTG Boost Mode

In boost mode, the device monitors the battery temperature to be between the V_{COLD} and V_{HOT} thresholds if boost mode temperature is enabled by setting EN_OTG NTC (REG02h, bit[5]) to 1. When the temperature is outside the temperature thresholds, boost mode is suspended. Once the temperature is within the thresholds, boost mode resumes.

Charging STAT Indication

The MP2723A indicates the charging state on the open drain of the STAT pin (see Table 2). The STAT pin can be disabled by setting the STAT_EN bit to 0.

Table 2: Operation Indications

Charging State	STAT
In charging	Low
Charging done, charging disabled, input OVP, battery discharge mode	High
Charging suspended (battery OVP, system OVP, timer fault, NTC fault, NTC float)	Blinking at 1Hz

Interrupt to Host (INT)

The MP2723A has an alert mechanism that can output an interrupt signal via the INT pin to notify the system of the operation by outputting a 256μs low-state INT pulse. The events that can trigger an INT output are listed below:

- Good input source detected
- DP/DM USB detection completed
- Input removed
- Charge completed
- NTC float is detected
- V_{INPPM} or I_{INPPM} is reached
- Any fault in REG0Dh (watchdog timer fault, OTG fault, thermal shutdown, safety timer fault, battery OVP fault, or NTC fault)

If a fault occurs, the charger device sends an INT signal. The fault is not latched, and always reports the current conditions.

Safety Timer

The MP2723A provides both a pre-charge and a complete charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 1 hour when the battery voltage is below V_{BATT_PRE}. The complete charge safety timer starts when the battery enters constant current charge. The user can configure the constant current charge safety timer via the CHG_TMR bit (REG08h, bits[2:1]) through the I²C. If the safety timer function is not used, it can be disabled by EN_TIMER (REG08h, bit[0]) via the I²C while the charger configuration is initialized.

The safety timer is reset at the beginning of a new charging cycle. Before the safety timer expires, any of the actions listed below can reset the safety timer:

- A new charge cycle begins by either input insertion or automatic recharge
- Toggle the $\overline{CE}$ pin low to high to low (charge enabled)
- Write CHG_CONFIG (REG04h, bits[5:4]) from 00 to 01 (charge enabled)
- Write EN_TIMER (REG08h, bit[0]) from 0 to 1 (safety timer enabled)

When the safety timer expires, the safety timer fault bit (REG17h, bit[7]) is set to 1, and an INT is asserted to the host. Writing BG_EN (REG09h, bit[3]) from 1 to 0 or re-inserting the input re-enables the input detection, clears the safety timer fault, and restarts the safety timer.

The MP2723A automatically adjusts or suspends the timer if any fault occurs. The timer is suspended under any condition listed below:

- Battery OVP occurs
- NTC hot or cold fault
- NTC float

The MP2723A stops counting the timer if EN_TIMER (REG08h, bit[0]) is set from 1 to 0 (timer is disabled) or charge full termination is detected.

The MP2723A can double the remaining time left on the timer, which is enabled by the TMR2X_EN bit. If the input current limit, input voltage regulation, or thermal regulation threshold is reached, the remaining time on the timer is doubled when TMR2X_EN is enabled. Once the device is cleared of the above conditions, the remaining time returns to the original setting.

The safety timer does not operate in USB OTG mode.

Watchdog Timer

The MP2723A is host-controlled device, but it can operate in default mode without host control. In default mode, all the registers are at their default settings, and WATCHDOG_FAULT is 0.

In host-controlled mode, all the parameters can be configured by the host. To keep the device in host mode, the host has to periodically reset the watchdog by setting the WATCHDOG_TIMER_RESET bit (REG08h, bit[3]) to 1 before the watchdog timer expires. If the watchdog timer expires, some of the registers are reset to their default values.

The following actions reset the watchdog timer and force the IC to recover from a watchdog timer fault:

- Write 1 to the WATCHDOG_TIMER_RESET bit (REG08h, bit[3])
- Toggling the watchdog timer enable bit (disable first, then enable)

Thermal Regulation and Thermal Shutdown

The MP2723A continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the thermal regulation threshold (which is set by the T_{J_REG} bit), the MP2723A starts to reduce the charge current to prevent higher power dissipation. During thermal regulation, the THERM_STAT bit is set to 1.

If the junction temperature reaches the thermal shutdown threshold (T_{J_SHDN}, about 150°C), the MP2723A turns off the PWM step-down converter and BATFET. The THERMAL_SHUTDOWN bit in the fault register is set to 1, and an INT signal is asserted to the host. The step-down converter and BATFET

recover to normal operation when the junction temperature drops below the T_{J_SHDN} hysteresis (20°C).

Battery Discharge Mode

If only the battery is connected to the device and V_{BATT} exceeds the V_{BATT_UVLO} threshold, the battery FET turns on and connects the battery to the system. The 14mΩ battery FET minimizes the conduction loss during discharge. The MP2723A's quiescent current is as low as 40μA. The low on resistance and low quiescent current help extend the battery's runtime.

There is an over-current limit designed in the MP2723A to avoid system over-current conditions while the battery discharges. If the discharge current exceeds this limit (I_{DSCHG_LMT}) for a 50μs blanking time, the discharge FET turns off and enters hiccup mode. After a 600ms recovery time, the discharge FET turns on again. If the discharge current goes high to reach an internal fast-off current limit (14A), the battery FET turns off immediately and initiates hiccup mode.

Battery Disconnect Function

In applications where the battery is not removable, disconnect the battery from the system for shipping mode or reset the system's power. The MP2723A provides both shipping mode and system reset mode for different applications.

The MP2723A can enter and exit shipping mode through the I²C control of the BATFET_DIS bit (REG0Ah, bit[5]). Writing 1 to BATFET_DIS turns off BATFET after a 10s delay if REG02h, bit[7] is set to 1. If this bit is set to 0, the battery FET immediately turns off when BATFET_DIS is set to 1. Writing 0 to BATFET_DIS turns the battery FET on again.

If an application requires the system's power to be reset, the MP2723A uses a dedicated DISC pin to cut off the path from the battery to the system.

The system has two reset functions that can be selected via the SYSRST_SEL bit (REG0Ah, bit[4]). If SYSRST_SEL is set to 1, and the logic at DISC is pulled low for more than 8s (which can be configured by the t_{DISC_L} bits (REG0Ah, bits[1:0])), the system is disconnected from the battery by turning off the battery FET. After the 4s low period (which can be configured by the t_{DISC_H} bits (REG0Ah, bits[3:2])), the BATFET automatically turns on (see Figure 9).

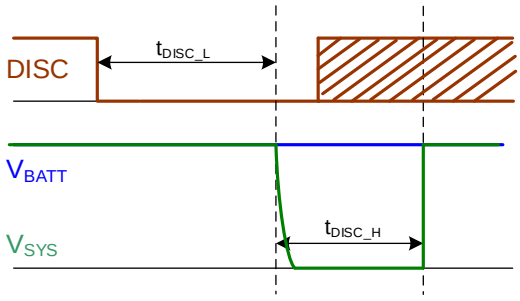


Figure 9: System Software Reset (SYSRST_SEL = 1)

If the SYSRST_SEL bit (REG0Ah, bit[4]) is set to 0, and the logic at DISC is pulled low for more than the time configured by the t_{DISC_L} bits, the BATFET turns off. Once the logic at DISC is pulled low again for the time specified by the t_{DISC_H} bits, the BATFET turns on (see Figure 10).

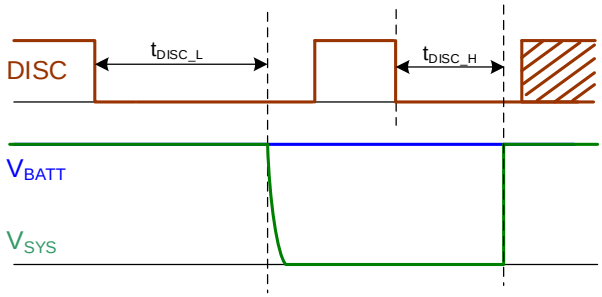


Figure 10: System Hardware Reset (SYSRST_SEL = 0)

OTG Boost Function

The MP2723A can supply a regulated 5V output at the IN pin to power the peripherals. This output is compliant with USB On-the-Go (OTG) specifications. To ensure that the battery is not drained, the MP2723A does not enter OTG mode if the battery is below the battery under-voltage lockout (UVLO) threshold. To enable OTG mode, the input voltage at the IN pin must be below 1.0V.

Boost operation can be enabled when the CHG_CONFIG bits (REG04h, bits[5:4]) are set to 11, and the OTG pin is high. The OTG output current limit can be configured by the I_{IN_DSCHG} bits (REG03h, bits[1:0]) via the I²C. During OTG mode, the status register OTG bit (REG17h, bit[5]) changes to 1.

The following conditions must be met to enable boost operation:

- V_{BATT} > $V_{BATT\_UVLO\_OTG}$ (rising 3V)
- V_{IN} < 1V
- OTG pin is high and the CHG_CONFIG bits (REG04h, bits[5:4]) are set to 11
- Boost mode enabled after 200ms delay

Once OTG is enabled, the MP2723A boosts the PMID to the value set by REG03h, bits[5:3], the default value is 5V. Then the block FET (Q1) is linearly regulated with a 3A output current limit. When V_{IN} is charged above 4.4V within 6ms, the block FET fully turns on. Otherwise, the block FET turns off and the part goes into hiccup mode. After a 600ms off period, PMID tries to charge V_{IN} again.

The MP2723A provides OTG output short protection. If V_{IN} falls below 4.0V, the block FET and boost mode turn off, and the part enters hiccup mode. After a 600ms recovery time, OTG starts up again. When the OTG output is short, the fault register's OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host. The device also provides OTG output voltage protection. Once V_{IN} exceeds V_{INOVP_DSCHG}, the MP2723A stops switching, the fault register OTG_FAULT bit (REG0Dh, bit[6]) is set to 1, and an INT signal is sent to the host.

In boost mode, the MP2723A employs a fixed 1.35MHz PWM step-up switching regulator. It switches from PWM operation to pulse-skip operation at light-load.

Analog-to-Digital Converter (ADC)

The MP2723A integrates an 8-bit analog-to-digital converter (ADC). A 6-channel multiplexer is used to measure voltage, current, and battery temperature alternately.

In charge mode, the ADC monitors the input voltage, input current, system voltage, battery voltage, charge current and NTC voltage alternately. In OTG mode, the ADC monitors the battery voltage, system voltage, NTC voltage, OTG output voltage, and OTG output current. In battery discharge mode, the ADC monitors the battery voltage, system voltage, and NTC voltage.

ADC operation has two modes, which can be selected by ADC_RATE. If ADC_RATE is 0, ADC acts once after enabling ADC_START. If ADC_RATE is 1, the ADC always acts in a round-robin manner. In battery discharge mode, ADC must be enabled by setting EN_ADC_DSG (REG08h, bit[6]) to 1 first, then the ADC can be controlled by ADC_START and ADC_RATE.

Series Interface

The IC uses an I²C compatible interface to set flexible charging parameters and instantaneously report the device status . The I²C is a two-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are open drains that must be connected to the positive voltage supply via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device, such as a microcontroller (MCU). The SCL is always driven by the master device. The I²C interface supports both standard mode (up to 100kbit/s), and fast mode (up to 400kbit/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. Start and stop conditions are always generated by the master. A start condition is defined as a high-to-low transition on the SDA line while SCL is high. A stop condition is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 11).

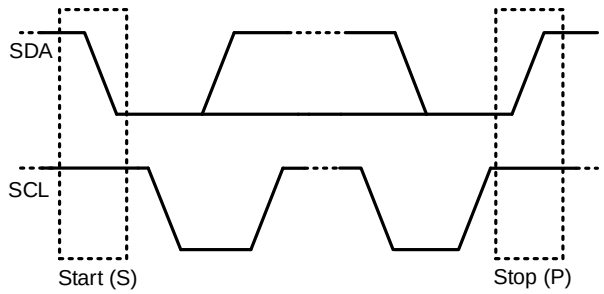


Figure 11: Start and Stop Conditions

For data validity, the data on the SDA must be stable during the high period of the clock. The high or low state of the SDA can only change when the clock signal on the SCL is low (see Figure 12). Every byte on the SDA must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB).

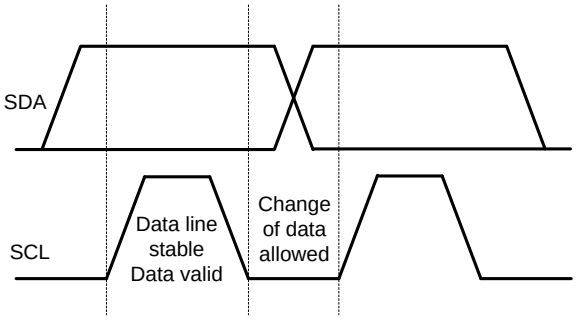


Figure 12: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal occurs when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low. The SDA line stays low during the high period of the ninth clock.

If the SDA line is high during the ninth clock, this is defined as a not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start (Sr) condition to start a new transfer.

After the start condition, a slave address is sent. This address is 7 bits long, followed by the 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 12 shows the address bit arrangement.

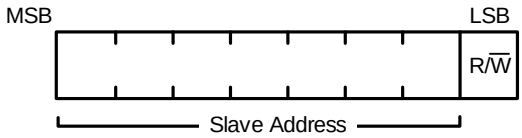


Figure 13: 7-Bit Address

For detailed sequences, see Figure 14, Figure 15, Figure 16, Figure 17 (on page 28), and Figure 18 (on page 28).

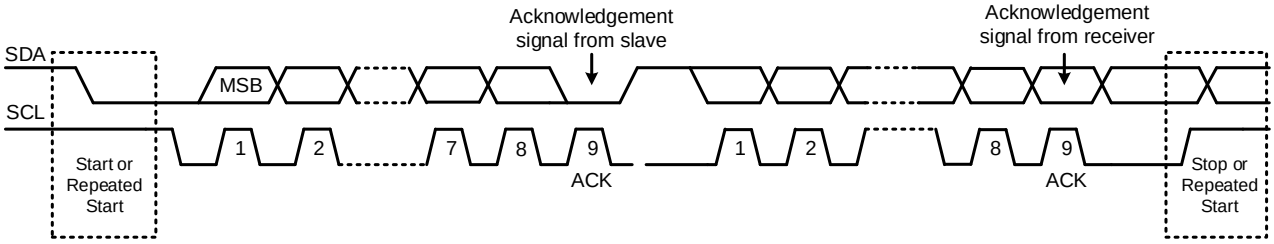


Figure 14: Data Transfer on the I²C Bus

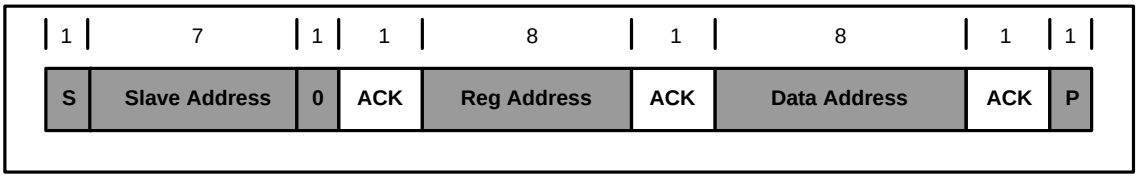


Figure 15: Single Write

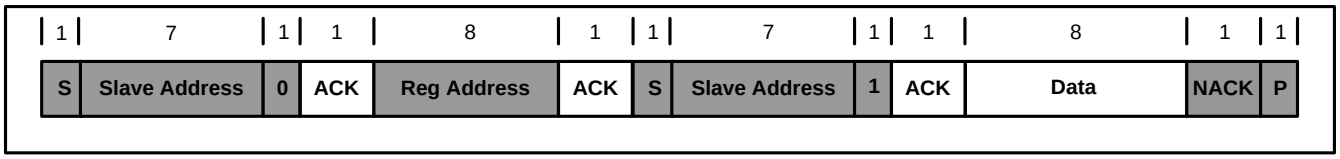


Figure 16: Single Read

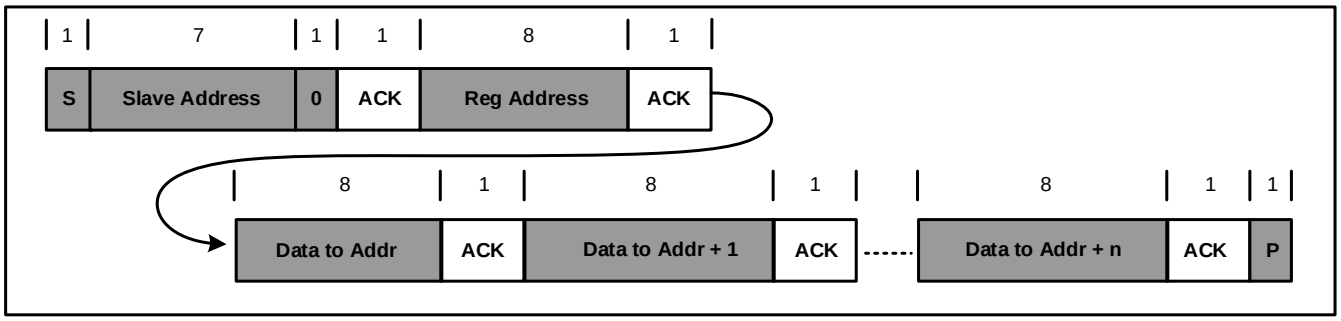


Figure 17: Multi-Write

Figure 18: Multi-Read

I²C REGISTER MAP

IC Address 4Bh Register Name	Address	R/W	Description
REG00h	0x00	R/W	Input current limit.
REG01h	0x01	R/W	Input voltage regulation.
REG02h	0x02	R/W	NTC configuration and thermal regulation.
REG03h	0x03	R/W	ADC control and OTG configuration.
REG04h	0x04	R/W	Charge control and V_{SYS} configuration.
REG05h	0x05	R/W	Charge current configuration.
REG06h	0x06	R/W	Pre-charge and termination current.
REG07h	0x07	R/W	Charge regulation voltage.
REG08h	0x08	R/W	Timer configuration.
REG09h	0x09	R/W	Bandgap.
REG0Ah	0x0A	R/W	BATFET configuration.
REG0Bh	0x0B	R/W	INT MASK and USB detection.
REG0Ch	0x0C	R	Status.
REG0Dh	0x0D	R	Fault.
REG0Eh	0x0E	R	ADC of the battery voltage.
REG0Fh	0x0F	R	ADC of the system voltage.
REG10h	0x10	R	ADC of the NTC voltage.
REG11h	0x11	R	ADC of the input voltage or OTG output voltage.
REG12h	0x12	R	ADC of the charge current.
REG13h	0x13	R	ADC of the input current or OTG output current.
REG14h	0x14	R	Power management status.
REG15h	0x15	R/W	DPM mask.
REG16h	0x16	R/W	JEITA configuration.
REG17h	0x17	R	Safety timer and OTG status.

REG00h: Input Current Limit

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_HIZ	0	Y	Y	R/W	0: Disabled 1: Enabled	Default : 0 (Disabled) Enables Hi-Z mode. This bit only turns off the DC/DC converter.
6	EN_LIM	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables the ILIM pin. The charger input current limit is the lower value between the IIN_LIM register setting and ILIM pin setting.
5	I_{IN_LIM}[5]	0	Y	N	R/W	1600mA	Default: 500mA Offset: 100mA Range: 100mA to 3250mA These bits set the input current limit threshold via the one-time programmable (OTP) memory. V_{IN} POR can reset I_{IN_LIM} to the default OTP threshold.
4	I_{IN_LIM}[4]	0	Y	N	R/W	800mA	
3	I_{IN_LIM}[3]	1	Y	N	R/W	400mA	
2	I_{IN_LIM}[2]	0	Y	N	R/W	200mA	
1	I_{IN_LIM}[1]	0	Y	N	R/W	100mA	
0	I_{IN_LIM}[0]	0	Y	N	R/W	50mA	

REG01h: Input Voltage Regulation

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	REGISTER_ RESET	0	Y	N	R/W	0: Keep current setting 1: Reset	Default: 0 (Keep current setting)
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	V_{IN_MIN}[3]	0	Y	N	R/W	800mV	Default: 0110 (4.3V) Offset: 3.7V Range: 3.7V to 5.2V These bits set the input voltage limit threshold. V_{IN} POR can reset V_{IN_MIN} to its default value via the OTP.
2	V_{IN_MIN}[2]	1	Y	N	R/W	400mV	
1	V_{IN_MIN}[1]	1	Y	N	R/W	200mV	
0	V_{IN_MIN}[0]	0	Y	N	R/W	100mV	

REG02h: NTC Configuration and Thermal Regulation

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	t_{SM_DLY}	1	Y	Y	R/W	0: No delay 1: 10s delay	Default: 1 (10s delay) Sets the shipping mode entry delay time.
6	NTC_TYPE	1	Y	Y	R/W	0: Standard 1: JEITA	Default: 1 (JEITA)
5	EN_OTG_NTC	0	Y	Y	R/W	0: Disabled 1: Enabled	Default: 0 (Disabled) Enables OTG NTC.
4	EN_CHG_NTC	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Charge NTC enable bit.
3	T_{J_REG}[1]	1	Y	Y	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Default: 11 (120°C) Sets the thermal regulation threshold.
2	T_{J_REG}[0]	1	Y	Y	R/W		
1	NTC_OPT	0	Y	Y	R/W	0: Battery over-temperature protection (OTP) 1: PCB OTP	Default: 0 (Battery OTP) Selects the NTC OTP.
0	AICO_EN	0	Y	N	R/W	0: Disabled 1: Enabled	Default: 0 (Disable AICO) Enables automatic input current optimization (AICO).

REG03h: ADC Control and OTG Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ADC_START	0	Y	Y	R/W	0: Disabled 1: Enabled	Default: 0 (Disabled) Enables the ADC. This bit is read-only when ADC_RATE is set to 1. This bit stays high during ADC conversion.
6	ADC_RATE	0	Y	Y	R/W	0: One-shot conversion 1: Start continuous conversion	Default: 0 (One-shot conversion) Sets the ADC conversion rate.
5	V_{IN_DSCHG}[2]	0	Y	Y	R/W	400mV	Default: 010 (5V) Offset: 4.8V Range: 4.8V to 5.5V Set the OTG voltage.
4	V_{IN_DSCHG}[1]	1	Y	Y	R/W	200mV	
3	V_{IN_DSCHG}[0]	0	Y	Y	R/W	100mV	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	I_{IN_DSCHG}[1]	0	Y	Y	R/W	00: 0.5A 01: 0.8A 10: 1.1A 11: 1.5A	Default: 00 (0.8A) Sets the OTG current limit.
0	I_{IN_DSCHG}[0]	0	Y	Y	R/W		

REG04h: Charge Control and VSYS Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	BAT_LOAD_EN	0	Y	Y	R/W	0: Disable $I_{BATLOAD}$ 1: Enable $I_{BATLOAD}$	Default: 0 (Disable $I_{BATLOAD}$) Enables the battery load.
6	STAT_EN	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables the STAT pin.
5	CHG_ CONFIG[1]	0	Y	Y	R/W	00: Charge disabled 01: Charge enabled 10: Reserved 11: OTG	Default: 01 (Charge enabled) Configures the charging mode.
4	CHG_ CONFIG[0]	1	Y	Y	R/W		
3	V_{SYS_MIN}[2]	1	Y	N	R/W	000: 3V 001: 3.15V 010: 3.3V 011: 3.45V 100: 3.525V 101: 3.6V 110: 3.675V 111: 3.75V	Default: 101 (3.6V) Offset: 3V Range: 3.75V Sets the minimum system voltage.
2	V_{SYS_MIN}[1]	0	Y	N	R/W		
1	V_{SYS_MIN}[0]	1	Y	N	R/W		
0	V_{TRACK}[0]	1	Y	N	R/W	0: 100mV 1: 150mV	Default: 1 (150mV) Sets the battery track voltage.

REG05h: Charge Current Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_PRE}	1	Y	Y	R/W	0: 2.8V 1: 3V	Default: 1 (3V) Sets the pre-charge to fast charge threshold.
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	I_{CC}[5]	1	Y	Y	R/W	1344mA	Default: 100110 (1916mA) Offset: 320mA Range: 320mA to 2966mA Sets the fast charge current.
4	I_{CC}[4]	0	Y	Y	R/W	672mA	
3	I_{CC}[3]	0	Y	Y	R/W	336mA	
2	I_{CC}[2]	1	Y	Y	R/W	168mA	
1	I_{CC}[1]	1	Y	Y	R/W	84mA	
0	I_{CC}[0]	0	Y	Y	R/W	42mA	

REG06h: Pre-Charge and Termination Current

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{PRE}[3]	0	Y	Y	R/W	320mA	Default: 0010 (230mA) Offset: 150mA Range: 150mA to 750mA Sets the pre-charge current.
6	I_{PRE}[2]	0	Y	Y	R/W	160mA	
5	I_{PRE}[1]	1	Y	Y	R/W	80mA	
4	I_{PRE}[0]	0	Y	Y	R/W	40mA	
3	I_{TERM}[3]	0	Y	Y	R/W	320mA	Default: 0010 (200mA) Offset: 120mA Range: 120mA to 720mA Sets the termination current.
2	I_{TERM}[2]	0	Y	Y	R/W	160mA	
1	I_{TERM}[1]	1	Y	Y	R/W	80mA	
0	I_{TERM}[0]	0	Y	Y	R/W	40mA	

REG07h: Charge Regulation Voltage

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG}[5]	1	Y	Y	R/W	640mV	Default: 1010000 (4.2V) Offset: 3.4V Range: 3.4V to 4.67V Sets the battery regulation voltage.
6	V_{BATT_REG}[5]	0	Y	Y	R/W	320mV	
5	V_{BATT_REG}[4]	1	Y	Y	R/W	160mV	
4	V_{BATT_REG}[3]	0	Y	Y	R/W	80mV	
3	V_{BATT_REG}[2]	0	Y	Y	R/W	40mV	
2	V_{BATT_REG}[1]	0	Y	Y	R/W	20mV	
1	V_{BATT_REG}[0]	0	Y	Y	R/W	10mV	
0	V_{RECH}	0	Y	Y	R/W	0: 100mV 1: 200mV	Default: 0 (100mV) Sets the battery recharge threshold (below V_{BATT_REG}).

REG08h: Timer Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_TERM	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables the charge termination function.
6	EN_ADC_DSG	0	Y	N	R/W	0: Disabled 1: Enabled	Default: 0 (Disabled) Enables the ADC in battery discharge mode. Note that this bit is only valid in battery discharge mode.
5	WATCHDOG[1]	0	Y	N	R/W	00: Disable timer 01: 40s 10: 80s 11: 160s	Default: 01 (40s) Sets the I²C watchdog timer limit. The watchdog function is not available when only a battery is present in OTG mode.
4	WATCHDOG[0]	1	Y	N	R/W		
3	WATCHDOG_ TIMER_RESET	0	Y	Y	R/W	0: Normal 1: Reset	Default: 0 (Normal) This bit returns to 0 after the watchdog timer resets.
2	CHG_TMR[1]	1	Y	Y	R/W	00: 5hrs 01: 8hrs 10: 12hrs 11: 20hrs	Default: 10 (12hrs) Sets the constant current charge timer. These bits are set via the OTP.
1	CHG_TMR[2]	0	Y	Y	R/W		
0	EN_TIMER	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables the safety timer.

REG09h: Bandgap

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	BG_EN	0	Y	Y	R/W	0: Enabled 1: Disabled	Default: 0 (Enabled) Setting this bit from 1 to 0 resets the input plug-in detection and safety timer.
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG0Ah: BATFET Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	SW_FREQ	0	Y	Y	R/W	0: 1.35MHz 1: 1MHz	Default: 0 (1.35MHz) Sets the switching frequency.
6	TMR2X_EN	1	Y	Y	R/W	0: Disabled 1: Enabled	Default: 1 (Enabled) Enables the 2x timer enable bit.
5	BATFET_DIS	0	N	N	R/W	0: Allow the BATFET to turn on 1: Force the BATFET off	Default: 0 (Allow BATFET to turn on)
4	SYSRST_SEL	1	Y	N	R/W	0: Hardware reset 1: Software reset	Default: 1 (Software reset) Selects the system reset function. If this bit is set to 1, the DISC pin is pulled from high to low for a time set by bits[1:0] of this command to turn off the BATFET for a time set by bits[3:2] of this command. If this bit is set to 0, the DISC pin must be pulled high to low for the time set by bits[1:0] of this command to turn off the BATFET. Then the DISC pin must be pulled high to low for the time set by bits[3:2] of this command to turn on the BATFET again.
3	t_{DISC_H}[1]	1	Y	Y	R/W	00: 0.5s 01: 2s 10: 4s 11: 8s	Default: 10 (4s) Sets the time during which to pull DISC low to either turn off the BATFET or reset it.
2	t_{DISC_H}[0]	0	Y	Y	R/W		
1	t_{DISC_L}[1]	0	Y	Y	R/W	00: 8s 01: 10s 10: 12s 11: 16s	Default: 00 (8s) Sets the time during which to pull the DISC pin low to turn off the BATFET.
0	t_{DISC_L}[0]	0	Y	Y	R/W		

REG0Bh: INT Mask and USB Detection

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	INT_MASK[1]	1	Y	Y	R/W	0: No INT during thermal shutdown (TSD) and safety timer fault 1: INT during TSD and safety timer fault	Default: 1 (INT during TSD and safety timer fault)
6	INT_MASK[0]	1	Y	Y	R/W	0: No INT signal during BAT_FAULT 1: INT signal during BAT_FAULT	Default: 1 (INT signal during BAT_FAULT)
5	USB_DET_EN	0	Y	Y	R/W	0: No DP/DM detection 1: Forced DP/DM detection	Default: 0 (No DP/DM detection) Enables USB DP/DM detection.
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG0Ch: Status

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VIN_STAT[2]	0	N	N	R	D+/D- version 000: No input 001: Unknown adapter 010: Apple 1.0A 011: Apple 2.1A 100: Apple 2.4A 101: SDP 110: CDP 111: DCP	These bits select the input source. It is set to 000 by default. V_{IN} POR resets V_{IN_STAT}.
6	VIN_STAT[1]	0	N	N	R		
5	VIN_STAT[0]	0	N	N	R		
4	CHG_STAT[1]	0	N	N	R	00: Not charging 01: Trickle charge 10: Constant current charge 11: Charging complete	Default: 00 (Not charging)
3	CHG_STAT[0]	0	N	N	R		
2	RNTC_FLOAT_STAT	0	N	N	R	0: No NTC float 1: NTC float	Default: 0 (No NTC float)
1	THERM_STAT	0	N	N	R	0: Normal 1: Thermal regulation	Default: 0 (Normal)
0	VSYS_STAT	1	N	N	R	0: In VSYSMIN regulation (BAT < V_{SYSMIN}) 1: Not in VSYSMIN regulation (BAT > V_{SYSMIN})	Default: 1 (Not in VSYSMIN regulation (BAT > V_{SYSMIN}))

REG0Dh: Fault

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG_ FAULT	0	N	N	R	0: Normal 1: Watchdog timer expiration	Default: 0 (Normal)
6	OTG_FAULT	0	N	N	R	0: Normal 1: V_{IN} overloaded, or V_{IN} over-voltage protection (OVP), or battery is under-voltage	Default: 0 (Normal)
5	INPUT_FAULT	0	N	N	R	0: Normal 1: Input over-voltage protection (OVP) or no input	Default: 0 (Normal)
4	THERMAL_ SHUTDOWN	0	N	N	R	0: Normal 1: Thermal shutdown	Default: 0 (Normal)
3	BAT_FAULT	0	N	N	R	0: Normal 1: Battery over-voltage protection (OVP)	Default: 0 (Normal)
2	NTC_FAULT[2]	0	N	N	R	Buck mode: 000: Normal 010: NTC warm 011: NTC cool 101: NTC cold 110: NTC hot Boost mode: 000: Normal 101: NTC cold 110: NTC hot	Default: 000 (Normal)
1	NTC_FAULT[1]	0	N	N	R		
0	NTC_FAULT[0]	0	N	N	R		

REG0Eh: ADC of Battery Voltage

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT[7]	0	N	N	R	2560mV	Offset: 0V Range: 0V to 5.1V Selects the ADC conversion for the battery cell voltage.
6	VBATT[6]	0	N	N	R	1280mV	
5	VBATT[5]	0	N	N	R	640mV	
4	VBATT[4]	0	N	N	R	320mV	
3	VBATT[3]	0	N	N	R	160mV	
2	VBATT[2]	0	N	N	R	80mV	
1	VBATT[1]	0	N	N	R	40mV	
0	VBATT[0]	0	N	N	R	20mV	

REG0Fh: ADC of System Voltage

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VSYS[7]	0	N	N	R	2560mV	Offset: 0V Range: 0V to 5.1V Sets the ADC conversion for the system voltage.
6	VSYS[6]	0	N	N	R	1280mV	
5	VSYS[5]	0	N	N	R	640mV	
4	VSYS[4]	0	N	N	R	320mV	
3	VSYS[3]	0	N	N	R	160mV	
2	VSYS[2]	0	N	N	R	80mV	
1	VSYS[1]	0	N	N	R	40mV	
0	VSYS[0]	0	N	N	R	20mV	

REG10h: ADC of NTC Voltage

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	NTC[7]	0	N	N	R	50.176%	Offset: 0% Range: 0% to 99.96% Sets the ADC conversion for the NTC voltage.
6	NTC[6]	0	N	N	R	25.088%	
5	NTC[5]	0	N	N	R	12.544%	
4	NTC[4]	0	N	N	R	6.272%	
3	NTC[3]	0	N	N	R	3.136%	
2	NTC[2]	0	N	N	R	1.568%	
1	NTC[1]	0	N	N	R	0.784%	
0	NTC[0]	0	N	N	R	0.392%	

REG11h: ADC of Input Voltage or OTG Output Voltage

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
6	VIN[6]	0	N	N	R	3840mV	Offset: 0V Range: 3.6V to 7.62V Sets the ADC conversion for the input voltage in charge mode. In OTG mode, these bits set the ADC conversion for the OTG output voltage.
5	VIN[5]	0	N	N	R	1920mV	
4	VIN[4]	0	N	N	R	960mV	
3	VIN[3]	0	N	N	R	480mV	
2	VIN[2]	0	N	N	R	240mV	
1	VIN[1]	0	N	N	R	120mV	
0	VIN[0]	0	N	N	R	60mV	

REG12h: ADC of Charge Current

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	ICHG[7]	0	N	N	R	2240mA	Offset: 0A Range: 0A to 4.4625A Sets the ADC conversion for the charge current.
6	ICHG[6]	0	N	N	R	1120mA	
5	ICHG[5]	0	N	N	R	560mA	
4	ICHG[4]	0	N	N	R	280mA	
3	ICHG[3]	0	N	N	R	140mA	
2	ICHG[2]	0	N	N	R	70mA	
1	ICHG[1]	0	N	N	R	35mA	
0	ICHG[0]	0	N	N	R	17.5mA	

REG13h: ADC of Input Current or OTG Output Current

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IIN[7]	0	N	N	R	1702.4mA	Offset: 0A Range: 0A to 3.39A Sets the ADC conversion for the input current in charge mode. In OTG mode, these bits set the ADC conversion for the OTG output current.
6	IIN[6]	0	N	N	R	851.2mA	
5	IIN[5]	0	N	N	R	425.6mA	
4	IIN[4]	0	N	N	R	212.8mA	
3	IIN[3]	0	N	N	R	106.4mA	
2	IIN[2]	0	N	N	R	53.2mA	
1	IIN[1]	0	N	N	R	26.6mA	
0	IIN[0]	0	N	N	R	13.3mA	

REG14h: Power Management Status

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VINPPM_STAT	0	N	N	R	0: No PPM 1: V_{INPPM}	Default: 0 (No PPM)
6	IINPPM_STAT	0	N	N	R	0: No PPM 1: I_{INPPM}	Default: 0 (No PPM)
5	I_{IN_DPM}[5]	0	N	N	R	1600mA	Default: 001000 (500mA) Offset: 100mA Range: 100mA to 3.25A
4	I_{IN_DPM}[4]	0	N	N	R	800mA	
3	I_{IN_DPM}[3]	1	N	N	R	400mA	
2	I_{IN_DPM}[2]	0	N	N	R	200mA	
1	I_{IN_DPM}[1]	0	N	N	R	100mA	
0	I_{IN_DPM}[0]	0	N	N	R	50mA	

REG15h: DPM Mask

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	AICO_STAT	0	N	N	R	0: No operation 1: AICO action	Default: 0 (No operation) Indicates the AICO status.
6	VINPPM_INT_MASK[1]	1	Y	Y	R/W	0: No INT during VINPPM 1: INT in V_{INPPM}	Default: 1 (INT in V_{INPPM})
5	IINPPM_INT_MASK[1]	1	Y	Y	R/W	0: No INT during IINPPM 1: INT in I_{INPPM}	Default: 1 (INT in I_{INPPM})
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG16h: JEITA Configuration

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	JEITA_VSET	1	Y	Y	R/W	0: V_{BATT_REG} minus 100mV 1: V_{BATT_REG} minus 200mV	Default: 1 (V_{BATT_REG} minus 200mV)
6	JEITA_ISET	1	Y	Y	R/W	0: 50% of I_{CHG} 1: 16.7% of I_{CHG}	Default: 1 (16.7% of I_{CHG})
5	V_{HOT}	1	Y	Y	R/W	0: 34.0% (60°C) 1: 36.0% (55°C)	Default: 1 (36.0% (55°C)) Sets the hot threshold. The thermistor is 103AT. These values are percentages of V_{NTC}.
4	V_{WARM}[1]	0	Y	Y	R/W	00: 43.0% (40°C) 01: 40.0% (45°C) 10: 38.0% (50°C) 11: 36.0% (55°C)	Default: 01 (40.0% (45°C)) Sets the warm threshold. The thermistor is 103AT. These values are percentages of V_{NTC}.
3	V_{WARM}[0]	1	Y	Y	R/W		
2	V_{COOL}[1]	1	Y	Y	R/W	00: 72.0% (0°C) 01: 68.0% (5°C) 10: 64.0% (10°C) 11: 60.0% (15°C)	Default: 11 (60.0% (15°C)) This bit sets the cool threshold. The thermistor is 103AT. These values are percentages of V_{NTC}.
1	V_{COOL}[0]	1	Y	Y	R/W		
0	V_{COLD}	0	Y	Y	R/W	0: 72.0% (0°C) 1: 68.0% (5°C)	Default: 0 (72.0% (0°C)) Sets the cold threshold. The thermistor is 103AT. These values are percentages of V_{NTC}.

REG17h: Safety Timer and OTG Status

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	SAFETY_ TIMER	0	N	N	R	0: Normal 1: Safety timer expiration	Default: 0 (Normal)
6	RESERVED	N/A	N/A	N/A	N/A		
5	OTG	0	N	N	R	0: Normal 1: OTG	Default: 0 (Normal)
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

REG18h (8)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IINLIM/VINMIN_ RESET_EN	0	N	N	N	0: I_{IN_LIM} and V_{IN_MIN} are not reset when V_{IN} POR 1: I_{IN_LIM} and V_{IN_MIN} reset when V_{IN} POR	Default: 0 (I_{IN_LIM} and V_{IN_MIN} are not reset when V_{IN} POR)
6	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
3	RESERVED	N/A	N/A	N/A	N/A	Reserved.	
2	ADDRESS	0	N/A	N/A	N/A	0: 4Bh 1: 21h	Default: 0 (4Bh)
1	PFM_EN	0	N/A	N/A	N/A	0: Enabled 1: Disabled	Default: 0 (Enabled) Enables PFM when charging is disabled.
0	RESERVED	N/A	N/A	N/A	N/A	Reserved.	

Note:

8) This register is for the one-time programmable (OTP) memory. It is not accessible.

OTP MAP

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h	N/A		I_{IN_LIM} (100mA to 3250mA/50mA step)					
01h	N/A				V_{IN_MIN} (3.7V to 5.2V/100mV step)			
05h	N/A		I_{CC} (320mA to 2966mA/42mA step)					
07h	V_{BATT_REG} (3.4V to 4.67V/10mV step)							N/A
08h	N/A					CHG_TMR		N/A
18h	IINLIM/ VINMIN_ RESET_EN	N/A	N/A	N/A	N/A	ADDRESS	PFM_EN	N/A

OTP DEFAULT

OTP Settings	Default
I_{IN_LIM}	500mA
V_{IN_MIN}	4.3V
I_{CC}	1.92A
V_{BATT_REG}	4.2V
CHG_TMR	12hrs
INLIM/VINMIN_RESET_EN	I_{IN_LIM} and V_{IN_MIN} do not reset when V_{IN} POR
ADDRESS	4Bh
PFM_EN	Enabled

APPLICATION INFORMATION

Setting the Input Current Limit

The input current limit is set according to the input power source. The input current limit can be set through the I²C using the MP2723A's GUI. To set a current limit that is not selectable via the I²C, use the ILIM pin. Connect a resistor from the ILIM pin to AGND to configure the input current limit. The MP2723A selects the lower limit between the I²C setting and the resistor setting (see the Input Current Limit Setting via ILIM section on page 22 for more details).

See Table 2 on page 23 to determine how to set the input current limit for USB inputs.

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A smaller-value inductor is physically small, but results in higher ripple current, magnetic hysteretic loss, and an output capacitor with a higher capacitance. A larger-value inductor provides lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

For the best results, the inductor ripple current should not exceed 30% of the maximum load current under the worst-case conditions. For the MP2723A to operate with a typical 5V input voltage, the maximum inductor current ripple occurs at the corner point between pre-charge and CC charge. The inductance (L) can be estimated with Equation (2):

$$L=\frac{V_{IN}-V_{SYS}}{\Delta I_{L\_MAX}}\frac{V_{SYS}}{V_{IN}\times f_{SW}(MHz)}(\mu H) \quad (2)$$

Where V_{IN} is the input voltage, V_{SYS} is the system voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum inductor ripple current, which is usually 30% of the CC charge current. I_{PEAK} can be calculated with Equation (3):

$$I_{PEAK}=I_{LOAD(MAX)}\times(1+\frac{\%ripple}{2})(A) \quad (3)$$

The maximum charge current can be set to 3A, but the real charge current may reach the input current limit. To support most typical applications and to provide a sufficient margin to avoid reaching the peak current limit of the high-side switch, the maximum inductor current ripple is set to 0.5A with a 5V input voltage, and the inductance is 1.5µH. Select a 1.0µH inductor for low-profile operation. To optimize efficiency, chose an inductor with a low DC resistance.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are sufficient. Choose ceramic capacitors with X5R or X7R dielectrics.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{SYS}}{V_{IN}}\times\left(1-\frac{V_{SYS}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs when V_{IN} = 2 x V_{SYS}, and I_{CIN} = I_{SYS} / 2. For simplification, choose the input capacitor with an RMS current rating that exceeds half of the maximum load current.

For the MP2723A, the RMS current in the input capacitor flows from PMID to GND. This means a small, high-quality ceramic capacitor (e.g. 10µF) should be placed from VPMID to PGND, and as close to the IC as possible. The remaining capacitor should be from VIN to GND.

With ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge that prevents excessive voltage ripple at the input.

Selecting the Output Capacitor

In the typical application circuit, the output capacitor (C_{SYS}) is in parallel with the SYS load. C_{SYS} absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be below that of the system load to ensure that it properly absorbs the ripple current.

Use a ceramic capacitor since its low ESR and small size allows the output capacitor's ESR to be ignored.

The output voltage ripple can be calculated with Equation (5):

$$\Delta R = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times C_{SYS} \times f_{SW}^{2} \times L}\% \quad (5)$$

To guarantee the ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g. 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

The output capacitor can be calculated with Equation (6):

$$C_{SYS} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times f_{SW}^{2} \times L \times \Delta R} \quad (6)$$

For example, if V_{IN} = 5V, V_{SYS} = 3.7V, L = 1µH, f_{SW} = 1.35MHz, and ΔR = 0.1%, choose a 22µF ceramic capacitor.

Selecting the NTC Resistor

Figure 7 on page 22 shows an external resistor divider reference circuit that limits the high-temperature threshold (V_{HOT}) and low-temperature threshold (V_{COLD}). For a given NTC thermistor, select the appropriate R_{T2} and R_{T1} to set the NTC window, calculated with Equation (7) and Equation (8), respectively:

$$R_{T2} = \frac{R_{NTC\_HOT} \times V_{COLD} \times (1-V_{HOT}) - R_{NTC\_COLD} \times V_{HOT} \times (1-V_{COLD})}{V_{HOT} - V_{COLD}} \quad (7)$$

$$R_{T1} = \frac{(1-V_{COLD}) \times (R_{NTC\_COLD} + R_{T2})}{V_{COLD}} \quad (8)$$

R_{NTC_HOT} is the value of the NTC resistor at the high temperature of the required temperature operation range, and R_{NTC_COLD} is the value of the NTC resistor at the low temperature.

R_{T1} and R_{T2} allow the high-temperature limit and low-temperature limit to be configured independently. With this feature, the MP2723A can operate with most NTC and temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of the NTC resistor. For example, for the 103AT thermistor, it has the following electrical characteristics:

- At 0°C, R_{NTC_COLD} = 27.28kΩ
- At 60°C, R_{NTC_HOT} = 3.02kΩ

V_{HOT} is set to 34% of V_{NTC}, and V_{COLD} is set to 72% of V_{NTC} via the REG16h register. Using Equation (7) and Equation (8), R_{T1} = 11.8kΩ and R_{T2} = 3.06kΩ.

PCB Layout Guidelines

Careful PCB layout is critical to meet specified noise rejection requirements and efficiency. For the best results, follow the guidelines below:

1. Route the power stage adjacent to their grounds.
2. Minimize the high-side switching node (SW and the inductor), the trace lengths in the high-current paths, and the current-sense resistor trace.
3. Keep the switching node short and route it away from all small control signals, especially the feedback network.
4. Place the input capacitor as close as possible to the PMID and PGND pins.
5. Place the output inductor close to the IC. and
6. Connect the output capacitor between the output inductor and PGND.
7. For high-current applications, the pins for the power pads (IN, SW, SYS, BATT, and PGND) should be connected to as much copper in the board as possible. This improves thermal performance by conducting heat away from the IC.
8. Connect a ground plane directly to the return of all components through via holes. It is also recommended to
9. Put via holes inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components separated minimizes coupling between signals and stability requirements.
10. Pull the connection wire from the MCU (I^2C) far from the SW mode and cooper regions.
11. SCL and SDA should be in close parallel.

TYPICAL APPLICATION CIRCUIT

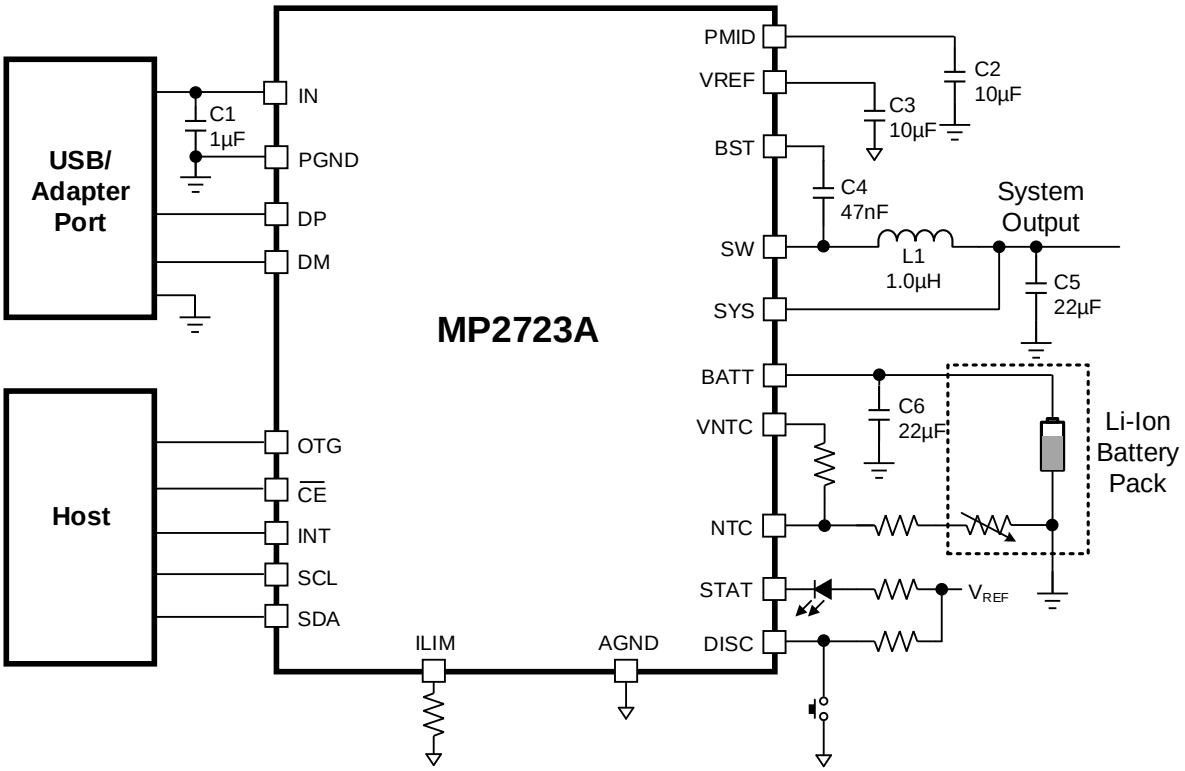


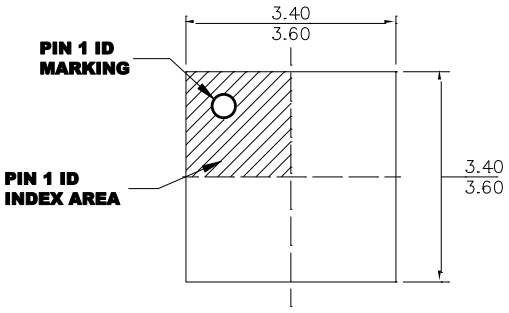
Figure 19: MP2723A Typical Application Circuit

Table 3: Key BOM for Typical Application Circuit

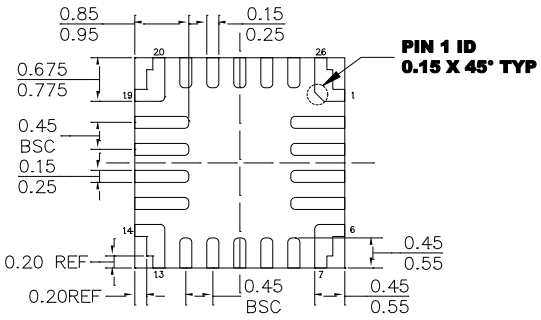
Qty	Ref	Value	Description	Package	Manufacturer
1	C1	1µF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C2	10µF	Ceramic capacitor, 50V, X5R or X7R	0603	Any
1	C3	10µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C4	47nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C5	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C6	22µF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	L1	1.0µH	>9.6A		Any

PACKAGE INFORMATION

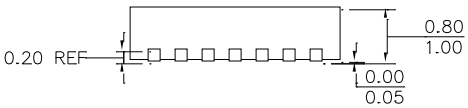
QFN-26 (3.5mmx3.5mm)



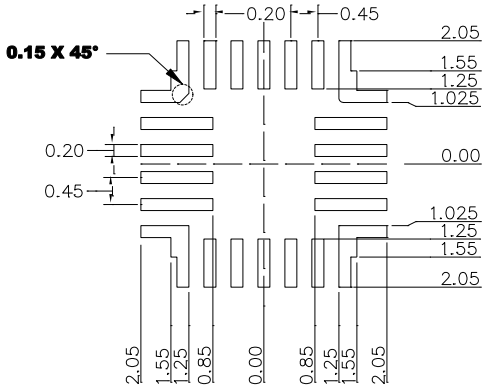
TOP VIEW



BOTTOM VIEW



SIDE VIEW

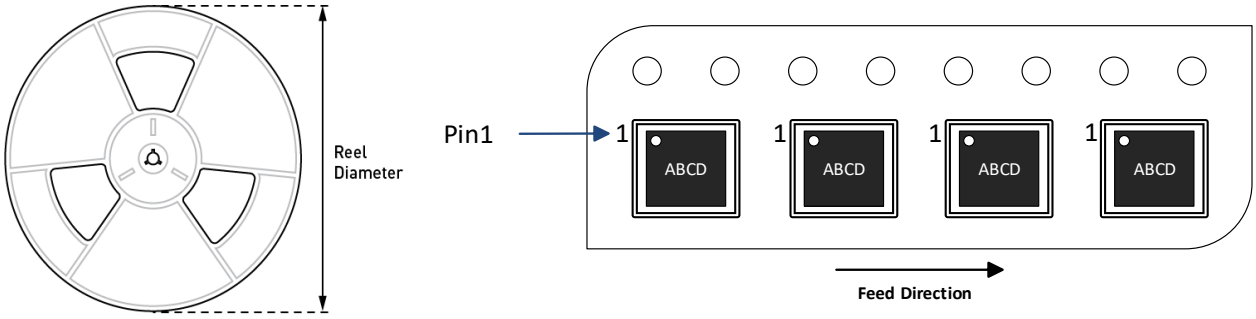


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch	Trailer Leader/ Reel
MP2723AGQC-xxxx-Z	QFN-26 (3.5mmx 3.5mm)	5000	N/A	N/A	13in	12mm	8mm	125&125

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	10/25/2021	Initial Release	-

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