MP2624A

4.5A, I²C-Controlled, Single-Cell USB/Adaptor Charger with Narrow VDC Power-Path Management USB OTG and SYS Reset Function

The Future of Analog IC Technology

DESCRIPTION

The MP2624A is a 4.5A, highly integrated, switching-mode, battery charger IC for single-cell Li-ion or Li-polymer batteries. The MP2624A supports NVDC architecture with power path management and is suitable for various portable applications. Its low impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The I²C serial interface with charging and system settings allows the device to be controlled flexibly.

The MP2624A supports a wide range of input sources, including standard USB host ports and wall adapters. The MP2624A detects the input source type according to the USB Battery Charging Spec 1.2 (*BC1.2*) and then informs the host to set the proper input current limit. In addition, the MP2624A supports USB On-The-Go operation by supplying 5.0V with current up to1.3A.

The power-path management regulates the system voltage slightly above the set maximum voltage between the battery voltage and the I²C programmable lowest voltage level. With this feature, the system is able to operate even when the battery is depleted completely or removed. When the input source current or voltage limit is reached, power path management reduces the charge current automatically to meet the priority of the system power requirement. If the system current continues increasing, even when the charge current is reduced to zero, the supplement mode allows the battery to power the system together with the input power supply simultaneously.

The MP2624A is available in a QFN-22 (3mmx4mm) package.

FEATURES

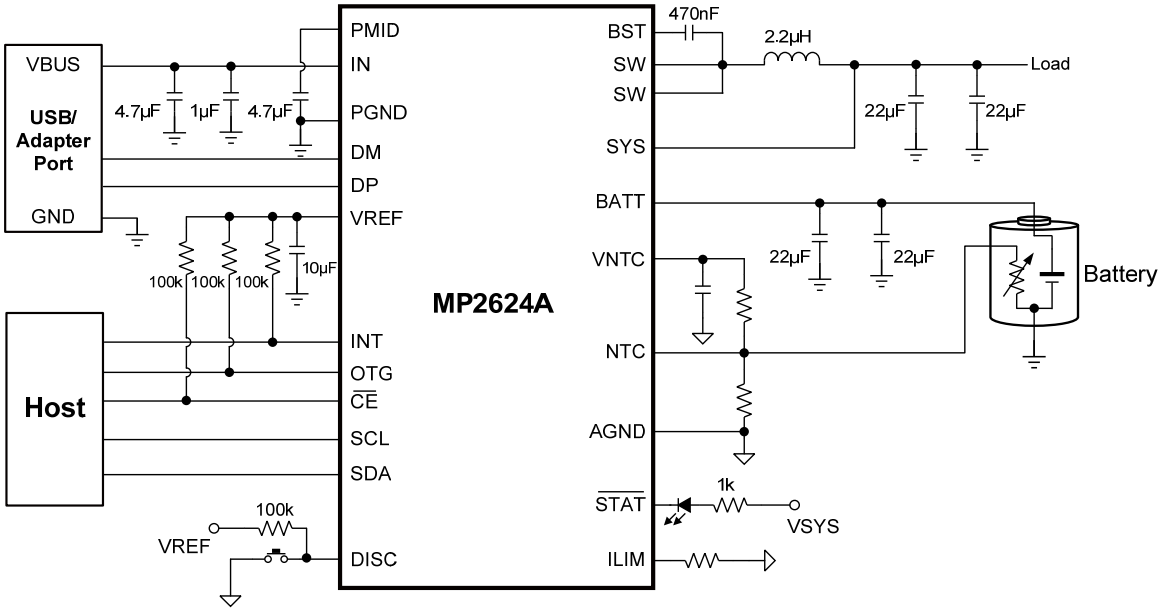
- High-Efficiency 4.5A 1.7MHz Buck Charger and 1.7MHz 1.3A Boost Mode to Support OTG
  - 94% Efficiency at 2A Charge Current
  - Fast Charge Time By Battery Path Impedance Compensation
  - 94% Efficiency at 5V, 1.2A OTG
  - Selectable OTG Current Outputs
- 3.9V to 7.0V Operating Input Voltage Range
- Highest Battery Discharge Efficiency with 10mΩ Battery Discharge MOSFET up to 9A
- Narrow System Bus Voltage Power Path Management
  - Instant On Works with No Battery or Deeply Discharged Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Constant-Off-Time Control to Reduce Charging Time under Lower Input Voltages
- High Accuracy of Charging Parameter
- I²C Port for Flexible System Parameter Setting and Status Reporting
- Full DISC Control to Support System Refresh
- I²C Control and DISC Control to Support Shipping Mode
- High Integration
  - Fully Integrated Power Switches
  - Built-In Robust Charging Protection
  - Built-In Battery Disconnection Function
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±5% Charge Current Regulation
  - ±5% Input Current Regulation
  - ±2% Output Regulation in Boost Mode
- Safety
  - Battery Temperature Sensing for Charge Mode
  - Battery Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Battery System Over-Voltage Protection
  - MOSFET Over-Current Protection
- Charging Operation Indicator

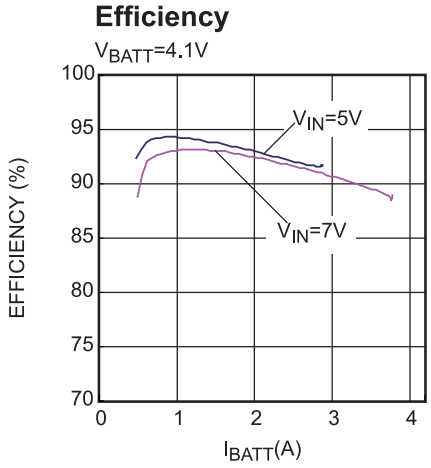
- Thermal Limiting Regulation on Chip

APPLICATIONS

- Tablet PCs
- Smart Phones
- Tiny QFN-22 (3mmx4mm) Package
- Mobile Internet Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2624AGL	QFN-22 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2624AGL–Z)

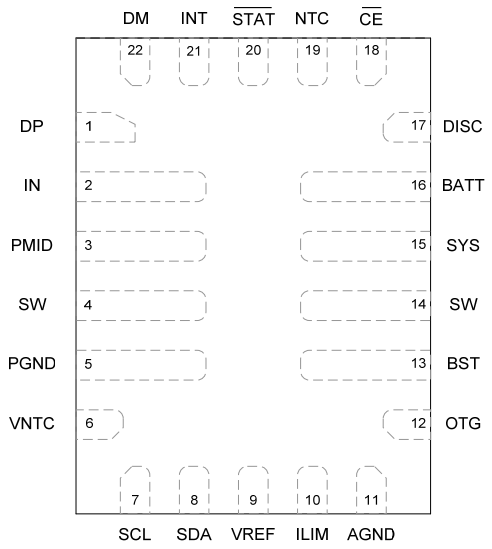
TOP MARKING

MPYW
2624
ALLL

MP: MPS prefix
Y: Year code
W: Week code
2624A: Product code of MP2624AGL
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-22 (3mmx4mm)

PIN FUNCTIONS

Package Pin #	Name	Type	Description
1	DP	I	**Positive pin of the USB data line pair.** DP and DM achieve USB host/charging port detection automatically.
2	IN	Power	**Power input of the IC from the adapter or USB.** Place a 1µF ceramic capacitor from IN to PGND as close to the IC as possible.
3	PMID	Power	**Internal power**. Connect PMID to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET. Bypass with a 4.7µF capacitor from PMID to PGND as close to the IC as possible.
4, 14	SW	Power	**Switching node.**
5	PGND	Power	**Power ground.**
6	VNTC	O	**Voltage source for NTC.** VNTC is the pull-up voltage bias of the NTC comparator resistive divider for both the feedback and the reference.
7	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
8	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
9	VREF	P	**PWM low-side driver output.** Connect a 10µF ceramic capacitor from VREF to AGND as close to the IC as possible.
10	ILIM	I	**Programmable input current limit.** A resistor is connected from ILIM to ground to set the minimum input current limit. The actual input current limit is the lowest setting by ILIM and I²C.
11	AGND	I/O	**Analog ground.**
12	OTG	I	**OTG mode enable control or input current limiting selection.** On-The-Go is enabled through the I²C. During OTG operation, OTG low suspends boost operation while OTG high enable the operation again. If the input is detected as the USB host, OTG is used as the input current limiting selection pin. When OTG is high, I_{IN_LMT} is 500mA. When OTG is low, I_{IN_LMT} is 100mA.
13	BST	P	**Bootstrap.** Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the power switch driver to drive the power switch gate above the supply voltage.
15	SYS	P	**System output.** Connect a 2x22µF ceramic capacitor from SYS to PGND as close to the IC as possible.
16	BATT	P	**Battery positive terminal.** Connect a 2x22µF ceramic capacitor from BATT to PGND as close as possible to the IC.
17	DISC	I	**Battery disconnection control.** Do not leave this pin float.
18	$\overline{CE}$	I	**Active low charge enable.** Battery charging is enabled when the corresponding register is set to active and $\overline{CE}$ is low.
19	NTC	I	**Temperature sense input.** Connect NTC to a negative temperature coefficient thermistor. Program the hot and cold temperature windows with a resistor divider from VNTC to NTC to AGND. The charge is suspended when VNTC is out of range.
20	$\overline{STAT}$	O	**Indicator for charging operation.**
21	INT	O	**Open-drain interrupt output.** INT sends the charging status, and the fault interrupts the host.
22	DM	I	**Negative pin of the USB date line pair.** DM and DP achieve USB host/charging port detection automatically.

ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, $\overline{\text{STAT}}$ to GND.....-0.3V to +20V
SW to GND .....-0.3V (-2V for 20ns) to +20V
BST to GND…….. .....SW to +6V
BATT, SYS to GND……...-0.3V to +6V
All other pins to GND .....-0.3V to +6V
STAT, INT sink current 10mA
Continuous power dissipation (T_A = +25°C)**(2)**
.....2.6W
Junction temperature….. .....150°C
Lead temperature (solder) .....260°C
Storage temperature….. .....-65°C to +150°C

Recommended Operating Conditions (3)

V_{IN} to GND…….....3.9V to 7.0V**(4)**
I_{IN} ..... Up to 3A
I_{SYS} ..... Up to 4.5A
I_{CHG} ..... Up to 4.5A
V_{BATT} ..... Up to 4.425V
I_{DCHG}.....(Continuous) up to 6A
I_{DCHG}..... (Pulse) up to 9A
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance **(5)** θ_{JA} θ_{JC}

QFN-22 (3mmx4mm).....48.....11 ...°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The inherent switching noise voltage should not exceed the absolute maximum rating on either BST or SW. A tight layout minimizes switching loss.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Step-Down Converter						
Input voltage range	V_{IN}		3.9		7.0	V
Input shutdown current		V_{IN} = 5V, both DC/DC and battery FET are disabled			65	μA
		V_{IN} = 7.0V, both DC/DC and battery FET are disabled			70	
Input quiescent current		V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, charge disabled, switching, SYS float		3	5	mA
		V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, charge enabled, switching BATT and SYS float		3	5	
Input under-voltage lockout	V_{IN_UVLO}	V_{IN} rising		3.45	3.6	V
V_{IN_UVLO} hysteresis		V_{IN} falling		200		mV
V_{IN} vs V_{BATT} headroom		V_{IN} rising	200	250	300	mV
		V_{IN} falling	65	90	115	mV
Internal reverse-blocking MOSFET on resistance	$R_{IN\ to\ PMID}$	Measure from IN to PMID		25	35	mΩ
High-side NMOS on resistance	R_{H_DS}	Measure from PMID to SW		25	35	mΩ
Low-side NMOS on resistance	R_{L_DS}	Measure from SW to PGND		28	35	mΩ
High-side NMOS peak current limit				7.5		A
Low-side NMOS peak current limit				7		A
Switching frequency		V_{BATT} = 4.2V, I_{CHG} = 2A	1.4	1.7	2.0	MHz
SYS Output						
Minimum system regulation voltage [I²C]	V_{SYS_MIN}	I_{SYS} = 0, V_{BATT} = 3.4V, POR default, REG01 Bit[2:0] = 110		3.6		V
System regulation voltage	V_{SYS_MAX}	50mV or 100mV (REG01Bit[0]) higher than V_{BATT_FULL} depends on the I²C setting	3.53		4.525	V
Ideal diode forward voltage in supplement mode	V_{F_IDD}	50mA discharge current		24		mV
SYS/BAT comparator		V_{SYS} falling		40		mV
Battery good comparator (threshold compared with V_{SYS_MIN})		V_{BATT} rising to the battery FET being turned on completely		60		mV
		V_{BATT} falling		-40		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery Charger						
Battery charge full voltage [I²C]	V_{BATT_FULL}	Depends on the I²C setting default (REG04 Bit04[7:2] = 110000): 4.2V	3.48		4.425	V
Charge voltage regulation accuracy		V_{BATT_FULL} = 4.2V	-0.5		0.5	%
Constant current charge current [I²C]		Depends on the I²C setting	0.512		4.544	A
Charge current regulation accuracy		I_{CHG} = 2A	-5		5	%
Battery pre-charge threshold [I²C]	V_{BATT_PRE}	REG04 Bit[4] = 1, V_{BATT} rising	2.8	3.0	3.1	V
Battery pre-charge hysteresis		V_{BATT} falling		220		mV
Battery short threshold	V_{BATT_SHORT}	V_{BATT} rising	2.0	2.1	2.2	V
Battery short threshold hysteresis		V_{BATT} falling		230		mV
Trickle-charge current	I_{TC}	V_{BATT} = 1.8V		128		mA
Pre-charge current [I²C]	I_{PRE}	Depends on the I²C setting	64		1024	mA
Pre-charge current accuracy		V_{BATT} = 2.6V, I_{PRE} = 256mA	-25		25	%
Termination current [I²C]	I_{BF}	Depends on the I²C setting	128		1024	mA
Termination current accuracy		V_{BATT_FULL} = 4.2V, I_{BF} = 512mA	-30		30	%
Recharge threshold below V_{BATT_FULL}	V_{RECH}	REG04 Bit[0] = 1		100		mV
Recharge threshold delay				20		ms
BATT to SYS FET on resistance	R_{BATFET}	V_{BATT} = 3.8V		10	15	mΩ
Battery discharge peak current limit	I_{DSG_LMT}	V_{IN} = 0V, V_{BATT} = 3.8V, OTG disabled, I_{SYS} rising		11(6)		A
Battery discharge function controlled by DISC	t_{DISC}	DISC pulled low, time period to turn off the battery discharge function	7.5		9.5	s
		Off time before auto-on		0.5		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage and Input Current-Based Power Path						
Input voltage regulation threshold [I²C]	V_{IN_REG}		3.9		5.1	V
Input voltage regulation accuracy		REG00 Bit[6:3] = 1011, V_{IN_REG} = 4.76V	-4		4	%
Input current limit	I_{IN_LMT}	USB100		70	100	mA
		USB150		120	150	
		USB500	400		500	
		USB900	750		900	
Input current limit accuracy		I_{IN_LMT} = 1.8A, REG00 Bit[2:0] = 101	1450		1800	mA
Protection						
Battery over-voltage protection	V_{BATT_OVP}	Rising, compared to V_{BATT_FULL}		200		mV
Battery over-voltage protection hysteresis		Compared to V_{BATT_FULL}		68		mV
Thermal shutdown rising threshold(6)	T_{J_SHDN}	T_J rising		184		°C
Thermal shutdown hysteresis (6)				20		°C
NTC low temp rising threshold	V_{COLD}	As a percentage of V_{VNTC}	70.9	71.5	72.1	%
NTC low temp rising threshold hysteresis		As a percentage of V_{VNTC}		1.4		%
NTC cool temp rising threshold	V_{COOL}	As a percentage of V_{VNTC}	68.6	69.2	69.8	%
NTC cool temp rising threshold hysteresis		As a percentage of V_{VNTC}		1.3		%
NTC warm temp falling threshold	V_{WARM}	As a percentage of V_{VNTC}	55.9	56.5	57.1	%
NTC warm temp falling threshold hysteresis		As a percentage of V_{VNTC}		1.4		%
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{VNTC}	47.9	48.5	49.1	%
NTC hot temp falling threshold hysteresis		As a percentage of V_{VNTC}		1.3		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREF LDO						
VREF LDO output voltage		V_{IN} = 10V, I_{VREF} = 40mA	4.82	5		V
		V_{IN} = 5V, I_{VREF} = 20mA		4.8		
VREF LDO current limit		V_{VREF} = 4V	50			mA
OTG Boost Mode						
Battery operating range	V_{BATT_OTG}		2.5		4.5	V
Battery discharge current	I_{BATT_OTG}	V_{IN} < V_{IN_UVLO}, V_{BATT_OTG} = 4.2V, battery FET is off			20	µA
		V_{IN} < V_{IN_UVLO}, V_{BATT_OTG} = 4.2V, battery FET is on			35	µA
OTG output voltage	V_{IN_OTG}	I_{OTG} = 0A		5.15		V
OTG output voltage accuracy		As percentage of V_{IN_OTG}, I_{OTG} = 0A	-2		2	%
Battery operation UVLO	V_{BATT_UVLO}	V_{BATT} falling		2.5		V
Battery operation UVLO hysteresis				260		mV
OTG output voltage protection threshold	V_{OTG_OVP}	V_{BATT} = 3.7V, OTG is enabled, force a voltage at IN until switching is off		5.75		V
OTG output voltage protection threshold hysteresis				175		mV
OTG overload short-circuit threshold(6)	V_{OTG_SHORT}	Falling		V_{BATT} + 0.1		V
		Rising		4.65		
OTG output current limit [I²C]	I_{OLIM}	REG02 Bit[1:0] = 00, V_{BATT} = 3.7V	0.5	0.6	0.7	A
		REG02 Bit[1:0] = 01, V_{BATT} = 3.7V	1.3	1.5	1.7	

NOTE:

6) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

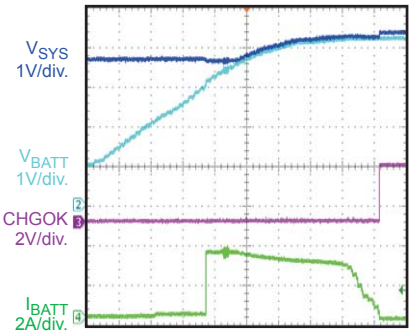
Parameter	Symbol	Condition	Min	Typ	Max	Units
DP/DM USB Detection						
DP voltage source	V_{DP_SRC}		0.5	0.6	0.7	V
Data connect detect current source	I_{DP_SRC}		7		13	µA
DM sink current	I_{DM_SINK}		50	100	150	µA
Leakage current input DP/DM	I_{DP_LKG}		-1		1	µA
	I_{DM_LKG}		-1		1	µA
Data detect voltage	V_{DAT_REF}		0.25		0.4	V
Logic low	V_{LGC_LOW}				0.8	V
Session valid to connect time for powered-up peripheral					45	mins
Logic I/O Characteristics						
Low-logic voltage threshold	V_L				0.4	V
High-logic voltage threshold	V_H		1.3			V
I²C Interface (SDA, SCL)						
Input high threshold level		$V_{PULL\ UP}$ = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock 1	F_{DIG1}	VREF LDO enabled	1400	1700	2000	kHz
Digital clock 2	F_{DIG2}			39		kHz
Watchdog timer	t_{WDT}	REG05 Bit[5:4] = 11		160		s

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = full range, I²C controlled, I_{CHG} = 4.5A, I_{IN_LMT} = 3.0A, V_{IN_REG} = 4.36V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

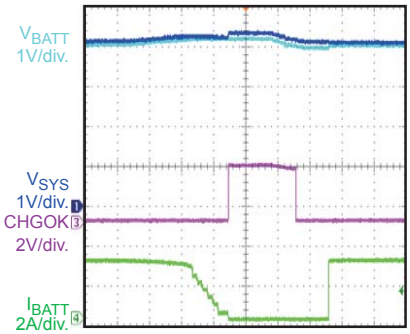
Battery Charge Curve

V_{IN}=5V, I_{SYS}=0A



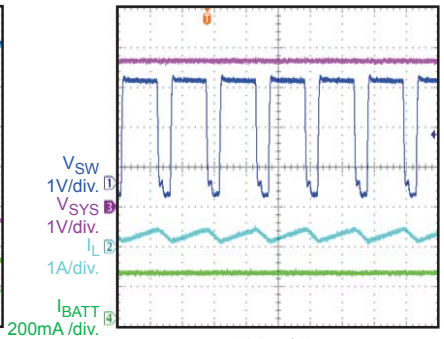
Auto Recharge

V_{IN}=5V, I_{SYS}=0A



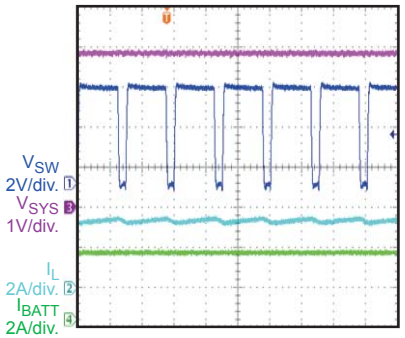
Trickle Charge Steady State

V_{IN}=5V, V_{BATT}=2.8V



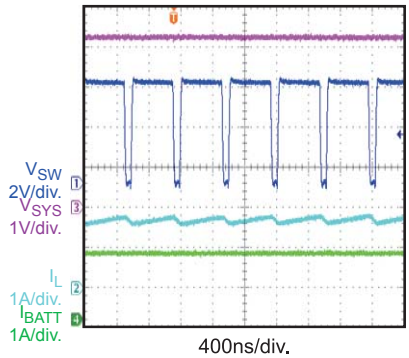
Constant Current Charge Steady State

V_{IN}=5V, V_{BATT}=3.6V



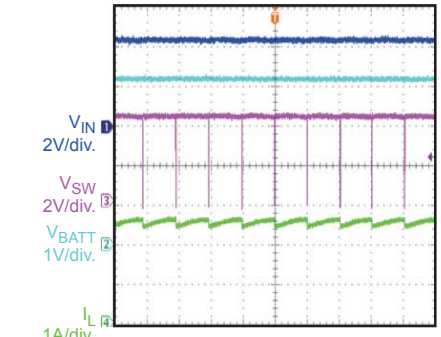
Constant Voltage Charge Steady State

V_{IN}=5V, V_{BATT}=4.2V



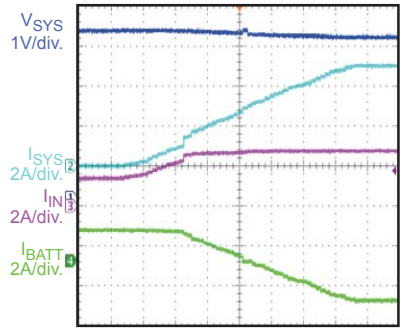
COT Operation

V_{IN}=4.5V



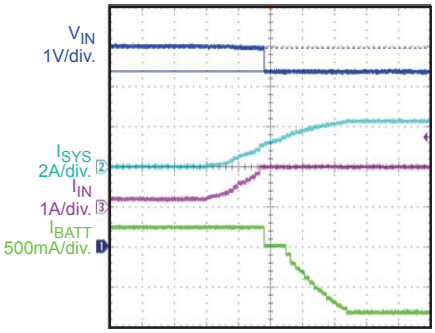
Input Current Limit

V_{IN}=5V, V_{BATT}=4.2V, I_{CHG}=3.5A



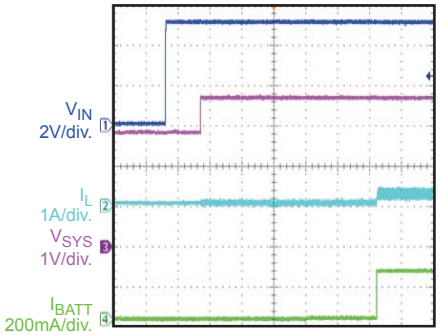
Input Voltage Limit

V_{IN}=5V/1.0A, V_{BATT}=2.8V, I_{CHG}=2A



Power On

V_{IN}=5V, V_{BATT}=3.7V

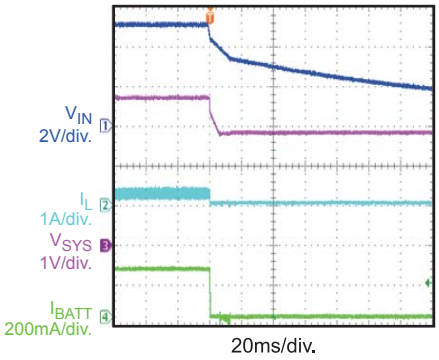


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = full range, I^2C controlled, I_{CHG} = 4.5A, I_{IN_LMT} = 3.0A, V_{IN_REG} = 4.36V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

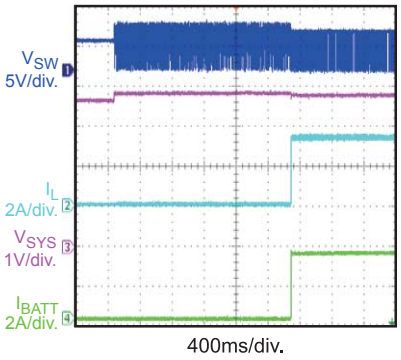
Power Off

V_{IN}=5V, V_{BATT}=3.7V



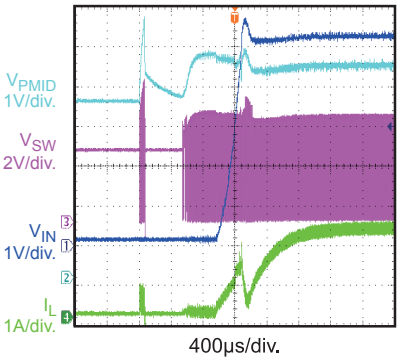
EN On

V_{IN}=5V, V_{BATT}=3.7V



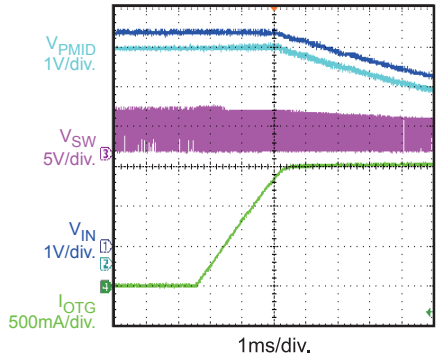
OTG Mode Start-Up

V_{IN_OTG}=5V,V_{BATT_OTG}=3.6V, I_{OTG}=1.3A



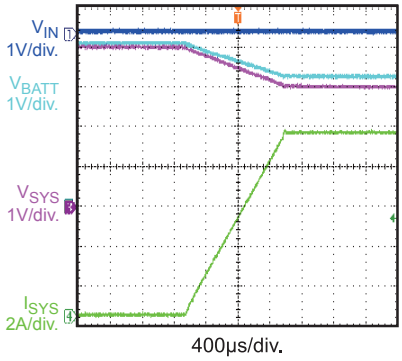
OTG Output CC Mode

V_{IN_OTG}=5V,V_{BATT_OTG}=3.6V, I_{OTG}=1.3A



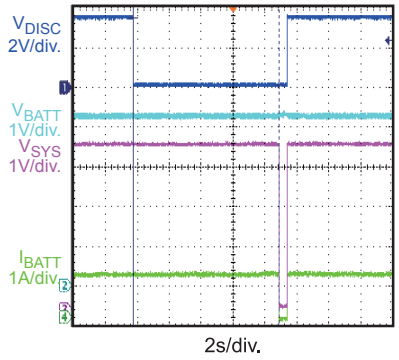
Battery Discharge Current

V_{IN}=Float, I_{SYS}=9A,V_{BATT}=4.0V



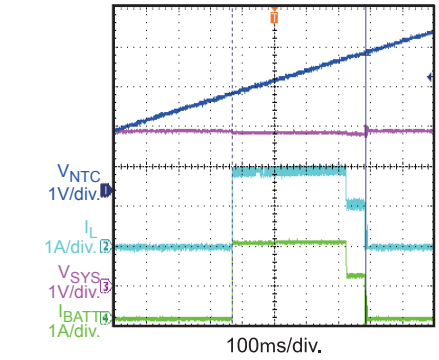
DISC Function

V_{IN}=Float, I_{SYS}=1A,V_{BATT}=4.2V



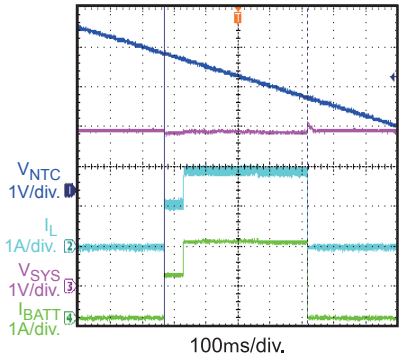
NTC Function

V_{IN}=5V,V_{BATT}=3.8V, I_{CHG}=2A



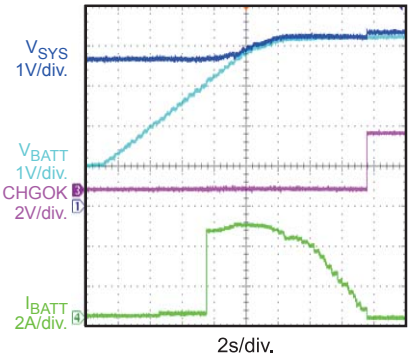
NTC Function

V_{IN}=5V,V_{BATT}=3.8V, I_{CHG}=2A



Battery Charge Curve

V_{IN}=9V, I_{SYS}=0A



BLOCK DIAGRAM

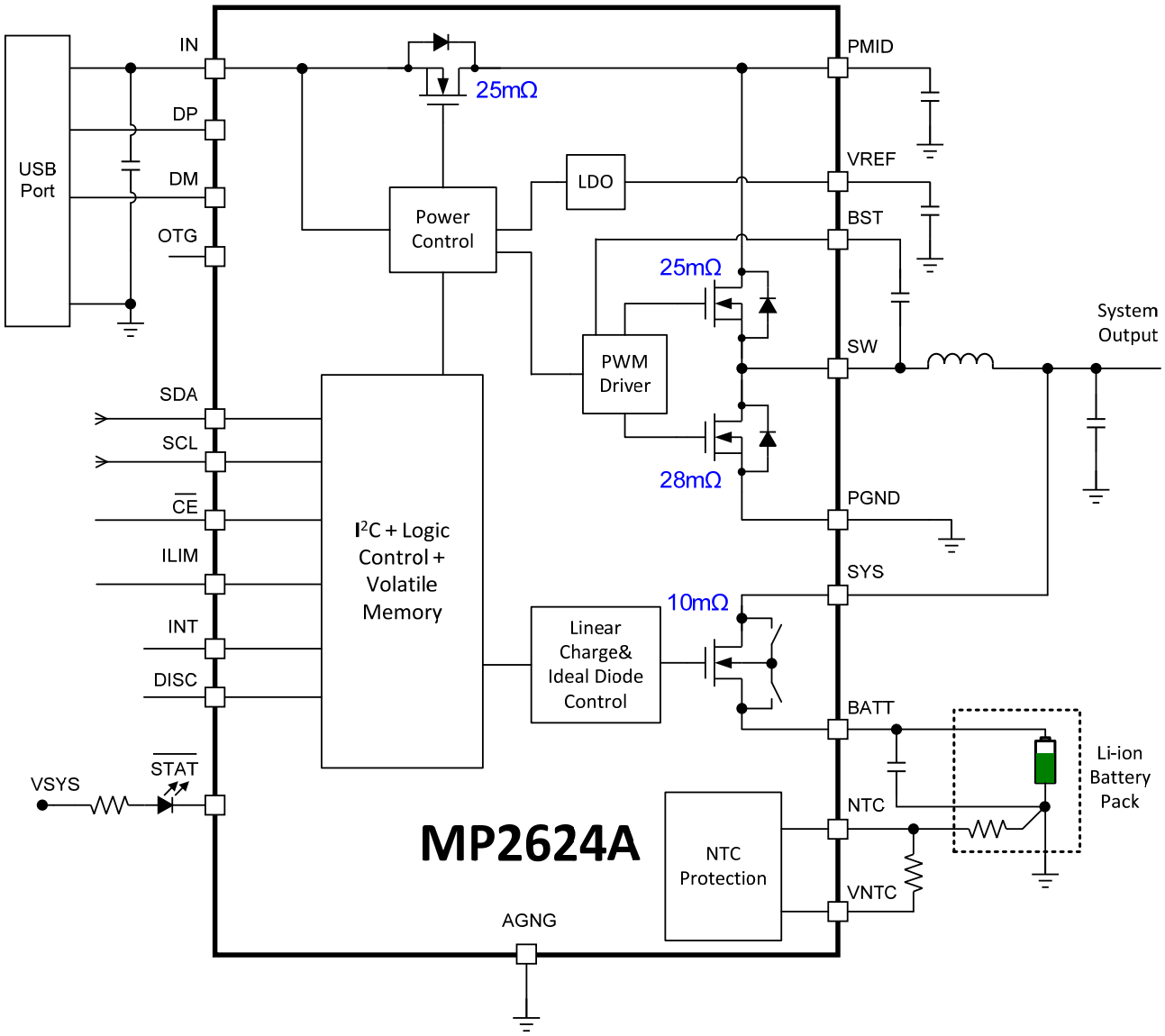


Figure 1: Functional Block Diagram

OPERATION

Introduction

The MP2624A is a highly integrated, I²C-controlled, switching-mode battery charger IC with NVDC power path management for single-cell lithium-ion or lithium-polymer battery applications. The MP2624A integrates a reverse-blocking FET, a high-side switching FET, a low-side switching FET, and a battery FET between SYS and BATT. Its low impedance and high efficiency allows higher current (4.5A) capacity for a given package size.

Power Supply

The internal bias circuit of the MP2624A is powered from the higher voltage of V_{IN} and V_{BATT}. When V_{IN} or V_{BATT} rises above the respective UVLO threshold, the sleep comparator, battery depletion comparator, and the battery FET driver are active. The I²C interface is ready for communication and all registers are reset to the default value. The host can access all registers.

Input Power Status Indication

The MP2624A qualifies the voltage and current of the input source before start-up. The input source has to meet the following requirements:

- $V_{IN} > V_{BATT} + 250mV$
- $V_{IN\_UVLO} < V_{IN}$
- OTG is not enabled by the host

Once the input power source meets the conditions above, the system status register REG08 Bit[2] asserts that the input power is good, and DP/DM detection starts if enabled. Then the step-down converter is ready to operate.

The conditions above are monitored continuously, and the charge cycle is suspended if a condition is outside one of the limits (see Figure 2).

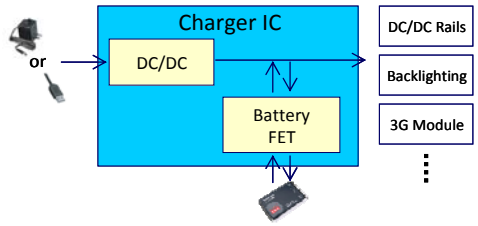


Figure 2: NVDC Power Path Management Structure

Narrow VDC Power Structure

The MP2624A employs a narrow VDC (NVDC) power structure with the battery FET decoupling the system from the battery, thus allowing separate control between the system and the battery. The system is always given priority to start-up even with a deeply-discharged or missing battery. When the input power is available (even with a depleted battery), the system voltage is always above the preset minimum system voltage (V_{SYS_MIN}) set by the I²C register REG01 Bit[3:1].

As depicted in Figure 2, the NVDC power structure is composed of a front-end, step-down, DC/DC converter and a battery FET between SYS and BATT.

The DC/DC converter is a 1.7MHz, step-down, switching regulator that adopts constant-off-time (COT) control to provide power to the system, which drives the system load directly and charges the battery through the battery FET.

System voltage control has three scenarios:

1. A minimum system voltage (V_{SYS_MIN}) can be set via the register REG01 Bit[3:1]. When the battery voltage is lower than V_{SYS_MIN} + 60mV, the system voltage is regulated at Max(V_{SYS_MIN}, V_{BATT}) + ΔV, and the battery FET works linearly to charge the battery with a trickle-charge, pre-charge, or fast-charge current through the battery FET, depending on the battery voltage. ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit[0].
2. When the battery voltage exceeds V_{SYS_MIN} + 60mV, the system voltage tracks the battery voltage with a voltage differential of ($I_{CHG} \bullet R_{BATFET}$), where R_{BATFET} is the ON resistance of the battery FET.
3. When the charging is suspended or completed, the system voltage is regulated at ΔV higher than Max(V_{SYS_MIN}, V_{BATT}). ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit[0].

V_{SYS} regulation is shown in Figure 3.

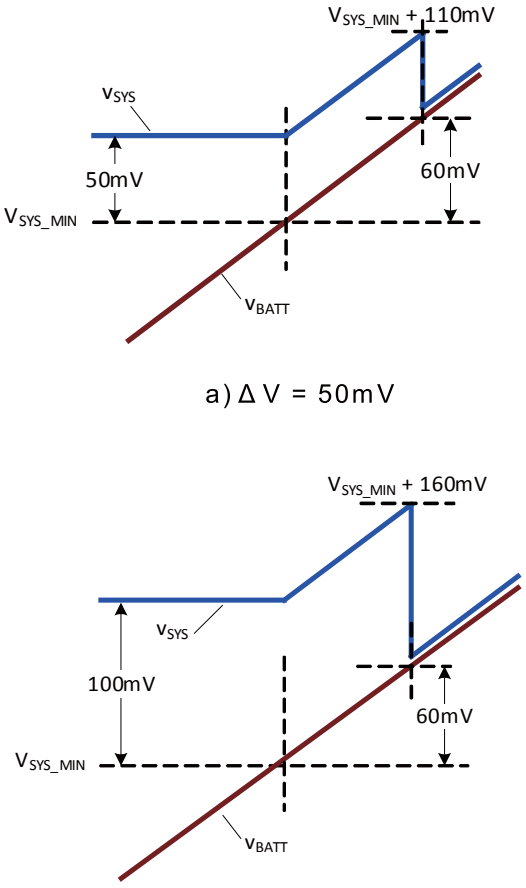


Figure 3: V_{SYS} Variation with V_{BATT}

Battery Charge Profile

The MP2624A provides four main charging phases: trickle charge, pre-charge, constant-current charge, and constant-voltage charge.

Phase 1: Trickle Charge

When the input power is qualified as a good power supply, the MP2624A checks the battery voltage to decide if trickle charge is required. If the battery voltage is lower than V_{BATT_SHORT} (2.1V), a charging current of 128mA is applied on the battery, which helps reset the protection circuit in the battery pack.

Phase 2: Pre-Charge

When the battery voltage exceeds V_{BATT_SHORT}, the MP2624A starts to pre-charge the depleted battery safely until the battery voltage reaches the "pre-charge to fast-charge threshold" (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer expires ,the charge cycle ends, and a corresponding timeout fault signal is asserted. The pre-charge current can be programmed via the I²C register REG03 Bit[7:4].

Phase 3: Constant-Current Charge

When the battery voltage exceeds V_{BATT_PRE} set via the REG04 Bit[1], the MP2624A enters a constant-current charge (fast charge) phase. The fast-charge current can be programmed as high as 4.5A via the REG02 Bit[7:2].

Phase 4: Constant-Voltage Charge

When the battery voltage rises to the pre-programmable charge-full voltage (V_{BATT_FULL}) set via REG04 Bit[7:2], the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the battery-full termination threshold (I_{BF}) set via the REG03 Bit[3:0], assuming the termination function is enabled by REG05 Bit[7] = 1. If I_{BF} is not reached before the safety charge timer expires (see the "Safety Timer" section), the charge cycle ends, and the corresponding timeout fault signal is asserted.

Figure 4 shows the battery charge profile.

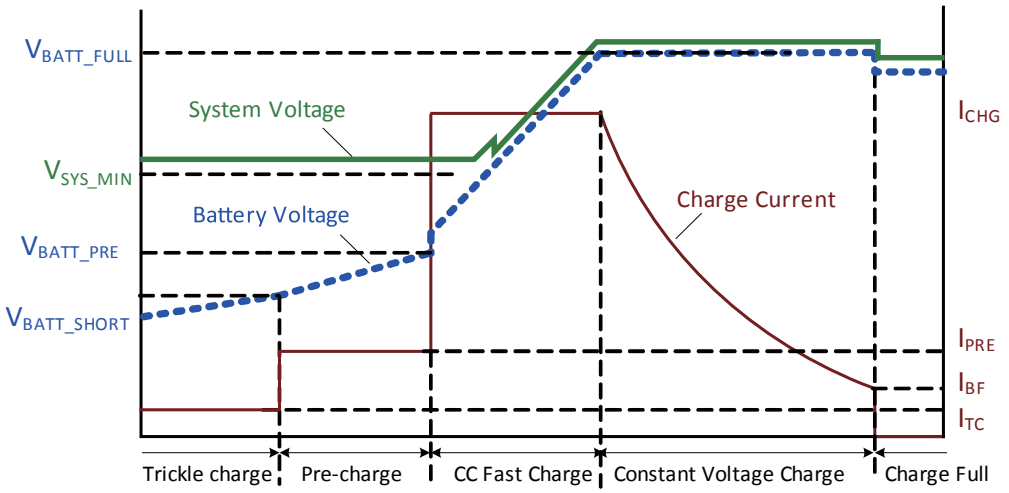


Figure 4: Battery Charge Profile

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, like dynamic power management (DPM) regulation (input current limit or input voltage regulation loop) or thermal regulation. Thermal regulation reduces the charge current, so the IC junction temperature does not exceed the preset limit. The multiple thermal regulation thresholds (from 60°C to 120°C) help system design meet thermal requirements for different applications. The junction temperature regulation threshold can be set via REG06 Bit[1:0].

A new charge cycle starts when the following conditions are valid:

- The input power is re-plugged.
- Battery charging is enabled by the I²C, and $\overline{CE}$ is forced to a low logic.
- No thermistor fault.
- No safety timer fault.
- No battery over voltage.
- The BATT FET is not forced to turn off.

Automatic Recharge

When the battery is charged full or the charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, the MP2624A starts a new charging cycle automatically.

$\overline{CE}$ Control

$\overline{CE}$ is a logic input pin for enabling or disabling battery charging functions while the DC/DC converter continues operating. The battery charging is enabled when the REG01 Bit[5:4] is set to 01 and $\overline{CE}$ is pulled to low logic.

Indication

Apart from multiple status bits designed in the I²C registers, the MP2624A also has a hardware status output pin ($\overline{STAT}$). The status of $\overline{STAT}$ in different states is shown in Table 1.

Table 1: Operation Indications

Charging State	$\overline{STAT}$
Charging	Low
Charging complete, sleep mode, charge disable	High
Charging suspended	Blinking at 1Hz

Battery Over-Voltage Protection (OVP)

The MP2624A is designed with built-in battery over-voltage protection. When the battery voltage exceeds V_{BATT_FULL} + 160mV, the MP2624A suspends the charging immediately and asserts a fault. When battery OVP occurs, only the charging is disabled, and the DC/DC converter continues operating.

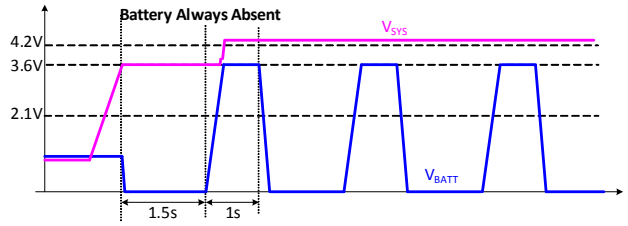
Battery Floating Detection

The MP2624A is capable of detecting whether a battery is connected or not. The following conditions initiate battery float detection:

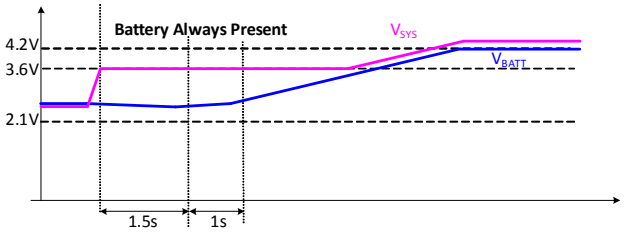
- Charging is enabled.
- Auto-recharge is triggered.
- Battery OVP recovery.

Before a charging cycle is initiated, the MP2624A implements battery floating detection (see Figure 5). Under this condition, the detection block sinks a 3mA current for 1.5 seconds to check if V_{BATT} is lower than 2.1V. If V_{BATT} is higher than 2.1V, the battery present is detected. Otherwise, the MP2624A continues to source a 3mA current and starts a 1 second timer to check when V_{BATT} exceeds 3.6V. If V_{BATT} is still lower than 3.6V when the 1 second timer expires, the battery present is asserted. The system regulation voltage is set to Max(V_{SYS_MIN}, V_{BATT}) + ΔV, and the charging begins to soft start. Before the 1 second timer expires and once V_{BATT} rises up to 3.6V, the 3mA sink current source is disabled, and the battery absent is detected. In this case, the charging is disabled, and the system regulation voltage is set to V_{BATT_FULL} + ΔV.

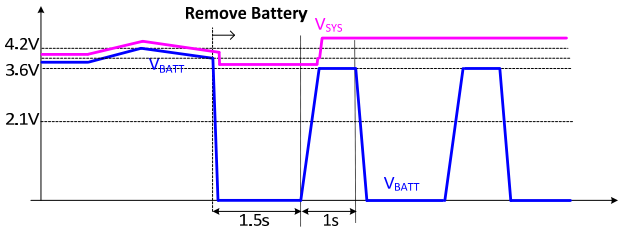
Battery floating detection flow is shown in Figure 6.



a) Charging Start-Up with Battery Absent



b) Charging Start-Up with Battery Present



c) Remove Battery during Charging

Figure 5: Battery Float Detection Examples

System Over-Voltage Protection (OVP)

The MP2624A always monitors the voltage at SYS. When system over-voltage is detected (V_{SYS} > V_{BATT_FULL} + ΔV + 100mV), the DC/DC converter is turned off, and the system is powered by the battery via the battery FET. ΔV can be set to 50mV or 100mV via the I²C register REG01 Bit[0].

During heavy system load transient, System OVP often happens when load transient from heavy to light. The timer is suspend when system OVP, so the timer may transfer between normal and suspend frequently, the timer counter will receive a fault timer clock signal, then fault timer out may happen under this condition.

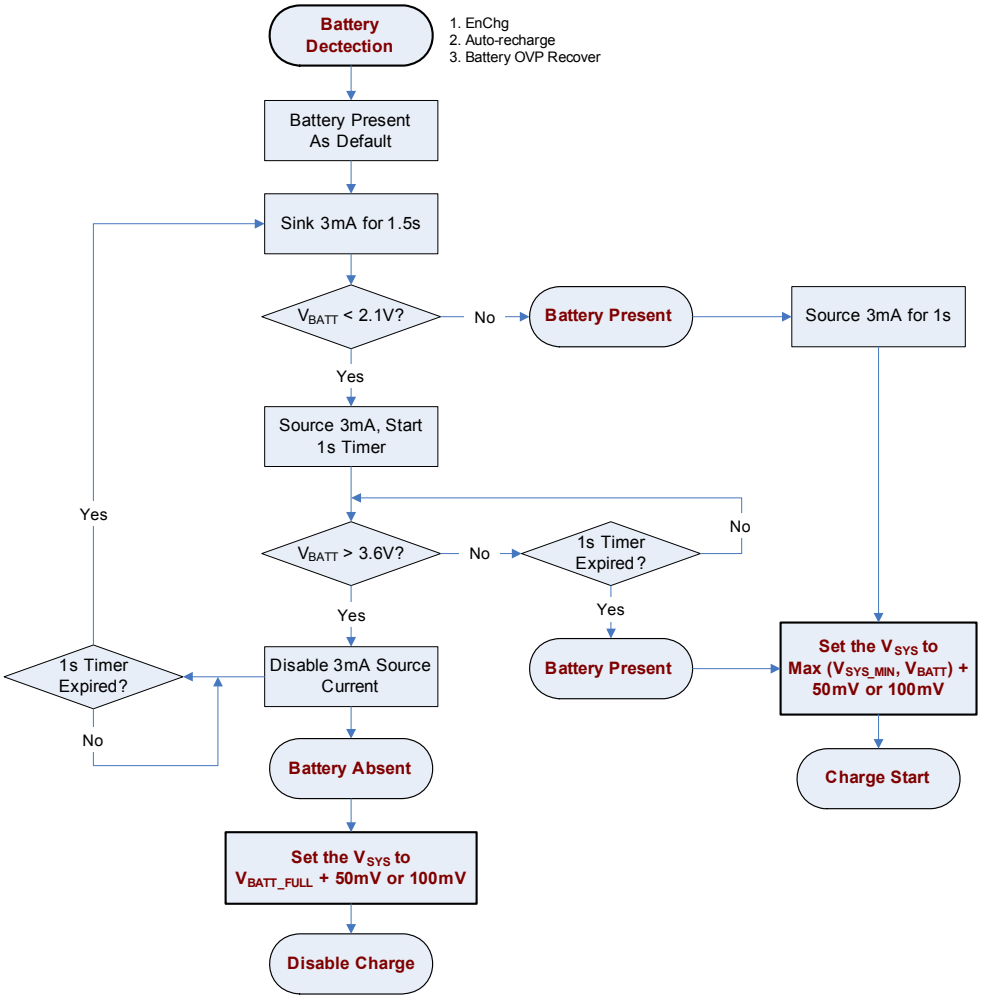


Figure 6: Battery Float Detection Flow

Input Voltage Based and Input Current Based Power Management

To meet the maximum current limit for the USB specification and avoid overloading the adapter, the MP2624A uses both input current and input voltage power management by continuously monitoring the input current and input voltage. The total input current limit is programmable to prevent the input source from being overloaded. When the input current hits the limit, the charge current tapers off to keep the input current from increasing further.

If the preset input current limit is higher than the rating of the adapter, the back-up input voltage based power management works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold due to the heavy load, the charge current is reduced to keep the input voltage from dropping further.

During CV mode, while battery voltage has been charged to the value only 100mV lower than the battery full threshold, if the power path management happens and charge current drops be lower than I_{BF}, the charge full will be fault detected.

The operation of the power path management is applied in the following two cases:

As mentioned in the "NVDC Power Structure" section,

a) When $V_{BATT} < V_{SYS\_MIN}$ + 60mV, the system voltage is regulated at Max(V_{SYS_MIN}, V_{BATT}) + ΔV. If the input current or voltage regulation threshold is reached, the system voltage loop loses control of the DC/DC converter, which causes system voltage drops. Once the system voltage drops by (2%•V_{SYS_MIN}), the charge current decreases to keep the system voltage from dropping further.

b) When $V_{BATT} > V_{SYS\_MIN}$ + 60mV (since the battery is connected to the system directly due to the free transition between each control loop), the charge current decreases automatically when the input current limit or the voltage regulation threshold is reached.

Battery Supplement Mode

During battery supplement mode, the charge current is reduced to keep the input current or input voltage from dropping when DPM occurs. If the input source is still overloaded, even when the charge current has decreased to zero, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the MP2624A enters battery supplement mode.
The battery powers the system together with the DC/DC converter simultaneously.

An ideal diode mode is designed in the MP2624A to optimize the control transition between the battery FET and DC/DC converter. The battery FET enters ideal diode mode under the following conditions:

- Charging start-up when $V_{BATT} > V_{SYS\_MIN} + \Delta V$.
- When $V_{BATT} < V_{SYS\_MIN} + \Delta V$, if the system voltage drops below the battery voltage, the battery FET enters ideal diode mode.

During ideal diode mode, the battery FET operates as an ideal diode. When the system voltage is 40mV below the battery voltage, the battery FET turns on and regulates the gate driver of the battery FET. The voltage drop (V_{DS}) of the battery FET remains around 20mV. As the discharge current increases, the battery FET obtains a stronger gate drive and a smaller on-state resistance (R_{DS}) until the battery FET is fully on.

NTC (Negative Temperature Coefficient) Thermistor

“Thermistor” is the generic name given to a thermally sensitive resistor. Generally, a negative temperature coefficient thermistor is called a thermistor. Depending on the manufacturing method and the structure, there are many thermistor shapes and characteristics for various applications. The thermistor resistance values, unless otherwise specified, are classified at a standard temperature of 25°C. The resistance of a temperature is solely a function of its absolute temperature.

The mathematical expression, which relates to the resistance and the absolute temperature of a thermistor is shown in Equation (1):

$$R_1 = R_2 \cdot e^{\beta \cdot \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (1)$$

Where R1 is the resistance at the absolute temperature T1, R2 is the resistance at the

absolute temperature T2, and β is a constant which depends on the material of the thermistor.

In charge mode, the MP2624A continuously monitors the battery's temperature by measuring the voltage at NTC. This voltage is determined by the resistive divider, whose ratio is produced by the different resistances of the NTC thermistor under different ambient temperatures of the battery.

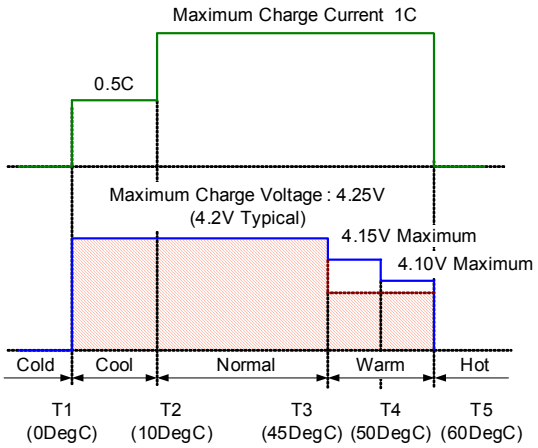


Figure 7: NTC Window

MP2624A internally sets a pre-determined upper and lower bound of the range. If the voltage at NTC goes out of this range, which means the temperature is outside the safe operating limit, the charging is ceased unless the operating temperature returns to a safe range.

To satisfy the JEITA requirement, the MP2624A monitors four temperature thresholds: the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C), and the hot battery threshold (T_{NTC} > 60°C).

For a given NTC thermistor, these temperatures correspond to V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}. When V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, the charging is suspended, and the timer is suspended, too. When V_{HOT} < V_{NTC} < V_{WARM}, the charge-full voltage (V_{BATT_FULL}) is reduced by 150mV, compared to the programmable battery-full voltage. When V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to half of the programmable charge current. Figure 7 shows the JEITA control.

Separate Pull-Up Pin VNTC for NTC Protection

As shown in Figure 8, a separate pull-up VNTC is designed as the internal pull-up terminal of the resistive divider for the NTC comparator. Both the reference divider and the feedback divider are connected together to VNTC. The VNTC is connected to VREF via an internal switch (in charge mode only).

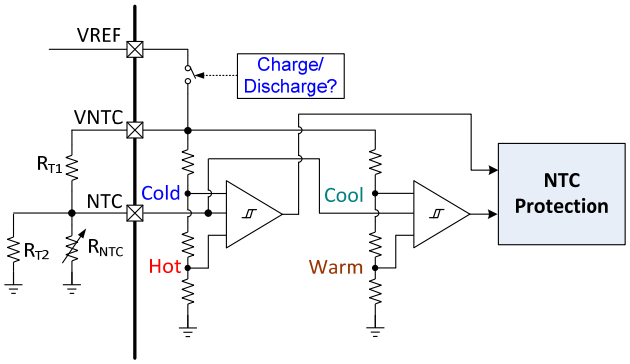


Figure 8: NTC Protection Circuit

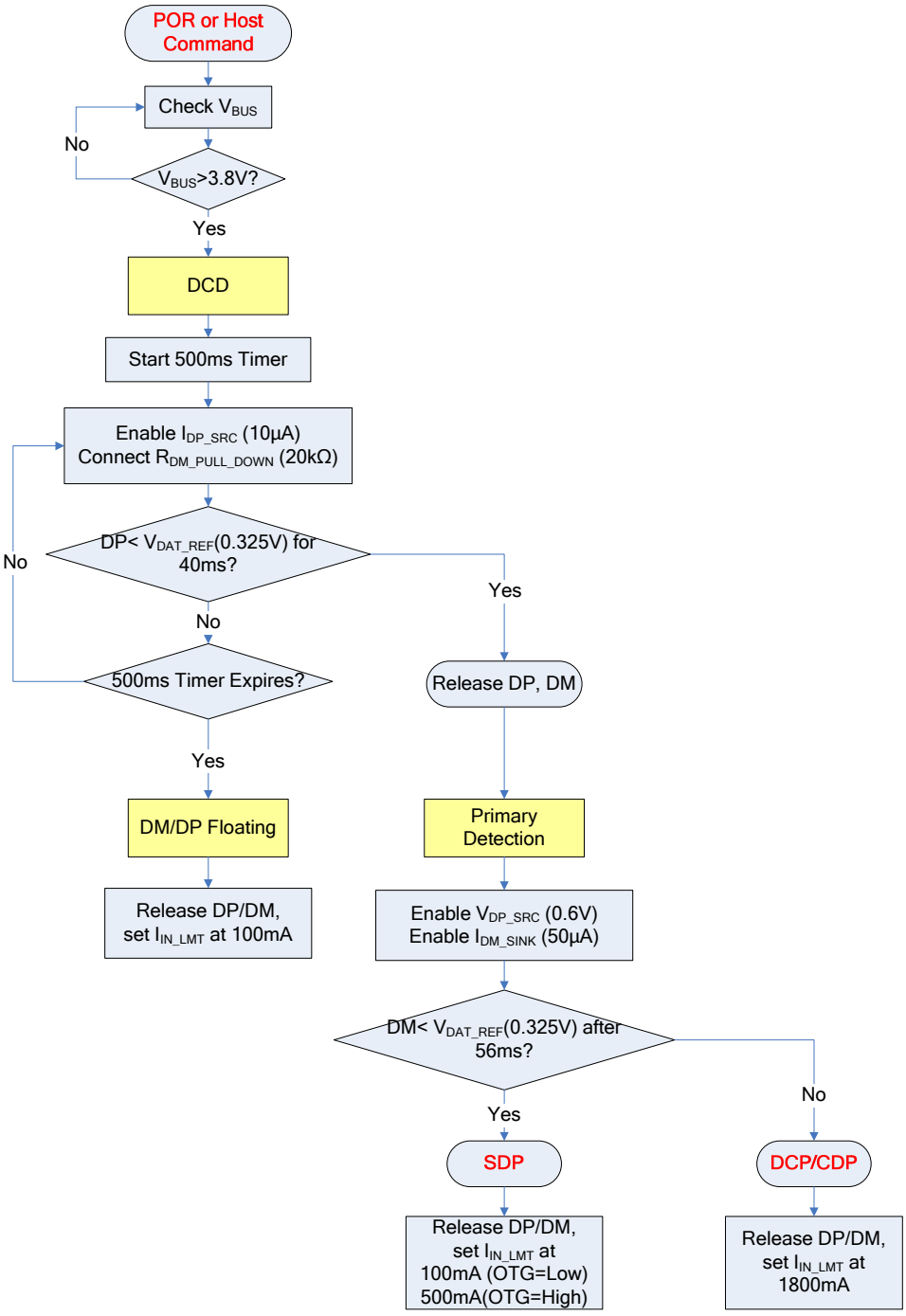


Figure 9: USB Detection Flow Chart

DM/DP USB Detection

The USB ports in personal computers are convenient places for portable devices to draw current for charging batteries. If the portable device is attached to a USB host or hub, then the USB specification requires the portable device to draw a limited current (100mA/500mA in USB2.0, and 150mA/ 900mA in USB3.0). When the device is attached to a charging port, it can draw more than 1.5A.

The MP2624A features input source detection compatible with the Battery Charging Specification Revision 1.2 (BC1.2) to program the input current limit during default mode. DP/DM detection can be forced in host mode by writing 1 to REG07 Bit[7].

When the input source is first applied, the input current limit begins with 100mA by default. If the input source passes the input source qualification, the MP2624A starts DP/DM detection. The DP/DM detection circuit is shown in Figure 10.

The DP/DM detection has two steps:

1. Data contact detection (DCD)
2. Primary detection

DCD detection uses a current source to detect when the data pins have made contact during an attach event. The protocol for data contact detection is as follows:

- The power device (PD) detects V_{IN} is asserted.
- The PD turns on DP I_{DP_SRC} and the DM pull-down resistor for 40ms.
- The PD waits for the DP line to be low.
- The PD turns off I_{DP_SRC} and the DM pull-down resistor when the DP line is detected as low or the 40ms timer expires.

DCD allows the PD to start primary detection as soon as the data pins have made contact. Once the data contact is detected, the MP2624A jumps to primary detection immediately. If the data contact is not detected, the MP2624A jumps to primary detection automatically after 300ms from the beginning of the DCD.

Primary detection is used to distinguish between the USB host (or SDP) and different types of charging ports.

During primary detection, the PD turns on the V_{DP_SRC} on DP and the I_{DM_SINK} on DM. If the portable device is attached to a USB host, DM is low.

Figure 9 shows the USB detection flow chart.

To be compatible with the USB specification and BC1.2, set the input current limit according to the values listed in Table 2.

Table 2: Input Current Limit vs USB Type

DP/DM Detection	OTG	I_{IN_LMT}	REG08 Bit[7:6]
Floating	X	100mA	00
SDP	LOW	100mA	10
SDP	HIGH	500mA	10
DCP	X	1.8A	01

The USB detection runs as soon as VIN is detected and is independent of the charge enable status. After the DP/DM detection is complete, the MP2624A sets the input current limit according to Table 2 and asserts the USB port type in REG08 Bit[7-6]. The host is able to revise the input current limit as well according to the USB port type asserted in REG08 Bit[7:6].

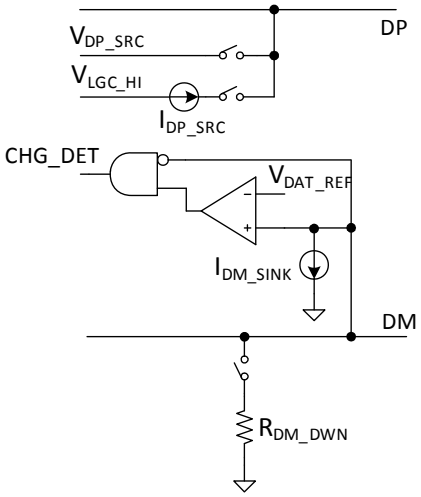


Figure 10: DP/DM Detection Circuit

When the detection algorithm is complete, the DP and DM signal lines enter a high-Z (HZ) state with an approximate 4pF capacitive load.

Input Current Limit Setting via ILIM

For safe operation, the MP2624A has an additional hardware pin (ILIM) to adjust the maximum input current limit. It can be set by a resistor connected from ILIM to GND. The actual input current limit is the lower value between the ILIM setting and the register setting value via I²C.

Interrupt to Host (INT)

The MP2624A has an alert mechanism, which can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the events below can trigger the INT output:

- Good input source detected.
- USB detection completed.
- UVLO
- Charge completed.
- Any fault in REG09 (watchdog timer fault, OTG fault, thermal fault, safety timer fault, battery OVP fault, or NTC fault).

When a fault occurs, the charge device sends out an INT signal and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device will not send a new INT signal upon new fault except for NTC faults. The NTC fault is not latched and always reports the current thermistor conditions.

In order to read the current fault status, the host must read REG09 two times consecutively. During the first reading, the host reads the fault register status from the last INT. During the second reading, the host reads the current fault register status.

Safety Timer

The MP2624A provides both a pre-charge and a complete charge safety timer to prevent the extended charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is 1 hour when the battery voltage is lower than V_{BATT_PRE}. The complete charge safety timer starts when the battery enters a constant-current charge. The constant-current charge safety timer can be programmed by I²C. The safety timer feature can be disabled via I²C. The safety timer does not operate in USB OTG mode.

The safety timer is reset at the beginning of a new charging cycle. It can also be reset by toggling $\overline{CE}$ or writing 00 and 01 to the REG01 Bit[5:4] sequentially. The following actions restart the safety timer:

- A new charge cycle begins.
- Toggling $\overline{CE}$ from low to high to low (charge enable).
- Writing REG01 Bit[5:4] from 00 to 01 (charge enable).
- Writing REG05 Bit[3] from 0 to 1 (safety timer enable).
- Writing REG01 Bit[7] from 0 to 1 (software reset).

The timer can be refreshed after timer out when one of the following thing happens:

- The input power reset.
- Toggling $\overline{CE}$ from low to high to low (charge enable).
- Writing REG01 Bit[5:4] from 00 to 01 (charge enable).

MP2624A adjusts automatically or suspends the timer when a fault occurs.

The timer is suspended during the conditions below:

- The battery is discharging.
- System OVP occurs.

NTC hot or cold fault occurs..

If the input current limit, input voltage regulation, or thermal regulation threshold is reached, the rest of the timer is doubled by enable the 2X timer in PPM function (REG07H Bit[6]=1)**. Once the PPM operation is removed, the rest of the timer returns to the original setting. This setting may cause an application issue, if the IC operates in and out of PPM frequently, the single timer period will be divided, which causes false timer out termination. The solution is to disable the 2X timer function by set REG07H Bit[6] to 0.**

VREF LDO Output

The VREF LDO supplies the internal bias circuits, as well as the high-side and low-side FET gate driver. The pull-up rail of $\overline{STAT}$ can be connected to VREF as well. The VREF LDO is enabled once OTG is enabled. In non-OTG mode, the internal VREF LDO is enabled when the following conditions are valid:

- V_{IN} > 3.3V
- No thermal shutdown

Both the internal LDO output and V_{BATT} are passed to VREF via a PMOS. The internal LDO output is delivered to VREF only when V_{IN} is greater than V_{BATT} + 250mV.

The VREF power supply circuit is shown in Figure 11.

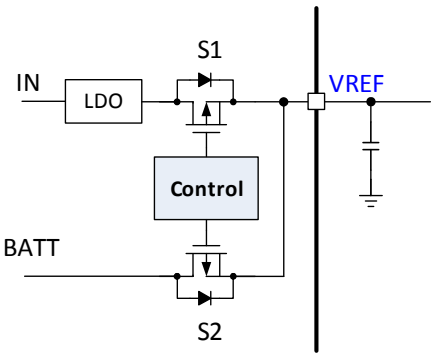


Figure 11: VREF Power Supply Circuit

Thermal Regulation and Thermal Shutdown

The MP2624A continuously monitors the internal junction temperature to maximize power delivery and prevent overheating the chip. When the internal junction temperature reaches the preset threshold, the MP2624A starts to reduce the charge current to prevent higher power dissipation.

When the junction temperature reaches 150°C, the PWM step-down converter enters shutdown mode.

Host Mode and Default Mode

The MP2624A is a host-controlled device. After the power-on reset, the MP2624A starts in the watchdog timer expiration state or default mode. All registers are in the default settings.

Any write to the MP2624A makes it transition into host mode. All device parameters are programmable by the host. To keep the device in host mode, the host must reset the watchdog timer regularly by writing 1 to REG01 Bit[6] before the watchdog timer expires. Once the watchdog timer expires, the MP2624A resumes default mode. Figure 12 shows the host mode and default mode change flow chart.

Battery Discharge Function

If only the battery is connected and the input source is absent (but the OTG function is disabled), the battery FET is turned on completely when V_{BATT} is above the V_{BATT_UVLO} threshold. The 10mΩ battery FET minimizes the conduction loss during discharge, and VREF LDO stays off. The quiescent current of the MP2624A is as low as 20μA. The low ON resistance and low quiescent current help extend the running time of the battery.

There is an over-current limit designed in the MP2624A to prevent system over current when the battery is discharging. Once the discharged current exceeds this limit (I_{DSG_LMT} in the EC table) for 20μs blanking time, the discharge FET is turned off. After a one second of recovery time, the discharge FET is turned on again.

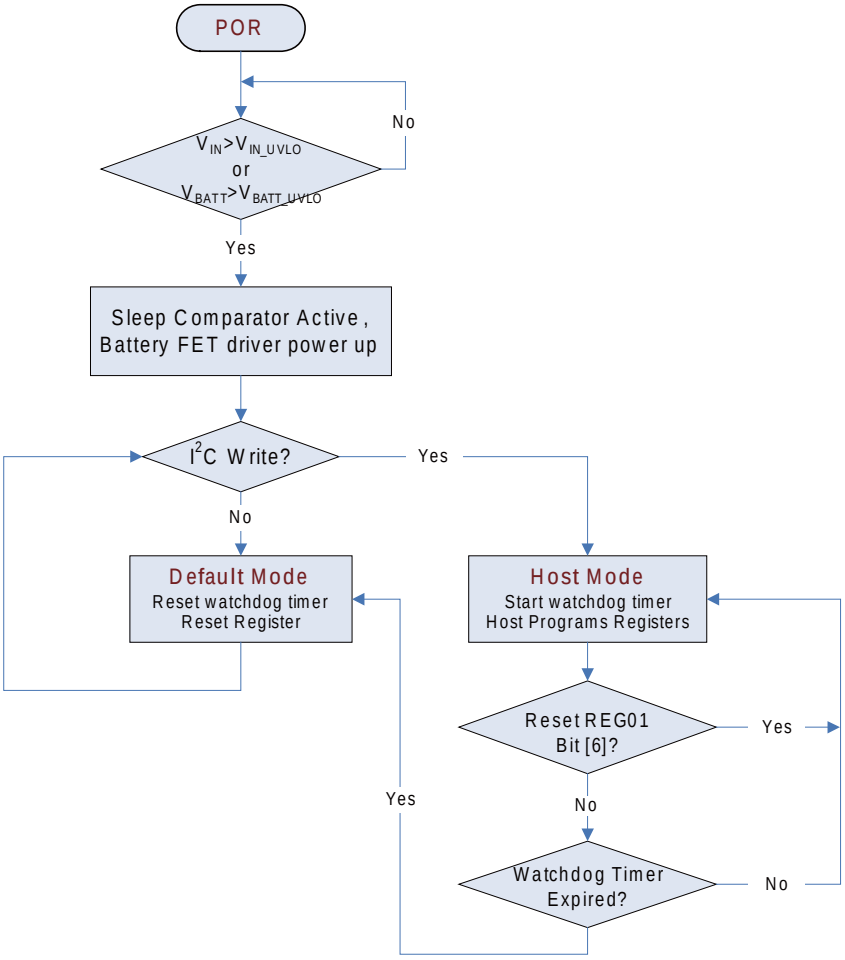


Figure 12: Host Mode and Default Mode

Battery Disconnect Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power reset. The MP2624A provides both shipping mode and system reset mode for different applications.

The MP2624A can enter and exit shipping mode through the I²C control to the REG07H Bit[5]. Writing 1 to REG07 Bit[5] turns off the battery FET immediately when in battery discharge mode. Writing 0 to REG07 Bit[5] turns the battery FET on again.

In applications where the battery is not removable, the MP2624A has a dedicated DISC pin to cut off the path from the battery to the system when the host has lost control. Once the logic at DISC is set to low for more than t_{DISC} seconds, the battery is disconnected from the system by turning off the battery FET. After a 0.5 second off period, the battery FET is softly turned on again to reset the power to the system (see Figure 13).

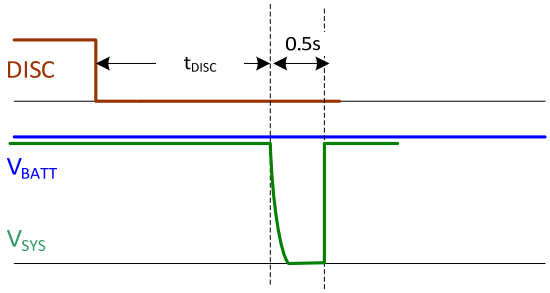


Figure 13: DISC Control Function

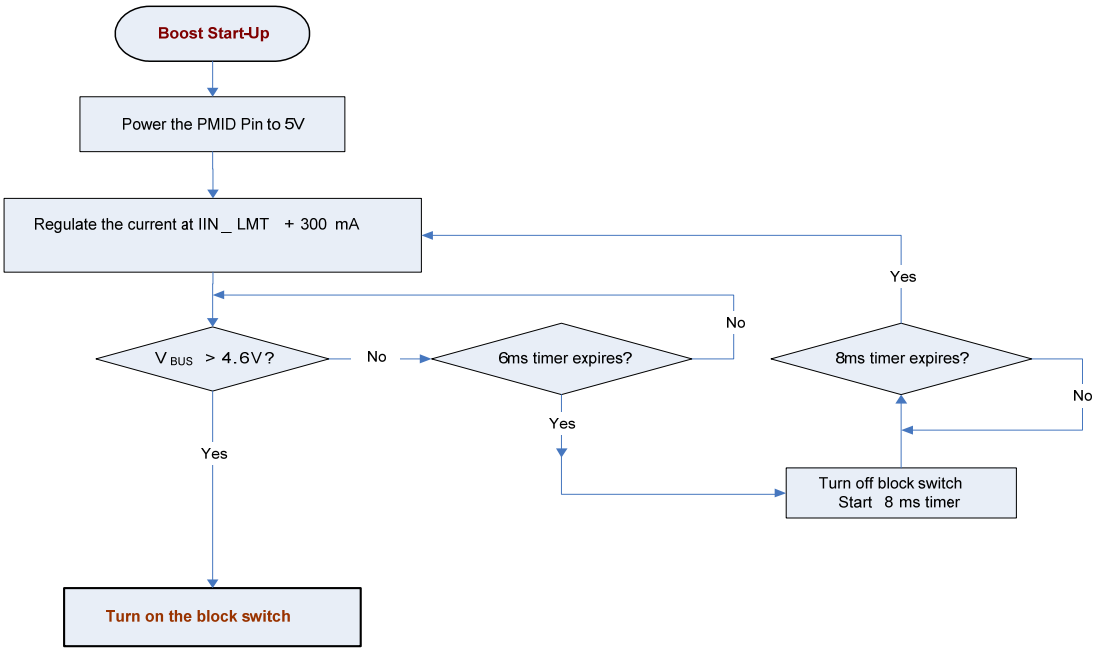


Figure 14: OTG Boost Start-Up Flow

OTG Boost Function

The MP2624A is able to supply a regulated 5V output at IN for powering the peripherals compliant with the USB On-The-Go specification. To ensure that the battery is not drained, the MP2624A will not enter OTG mode if the battery is below the battery UVLO threshold. In order to enable OTG mode, the input voltage at IN must be below 1.0V.

Boost operation can be enabled when REG01 Bit[5:4] = 10/11 and OTG is high. The OTG output current can be selected as 500mA and1.3A, o via I²C (REG02 Bit[1:0]). During boost mode, the status register REG08 Bit[7:6] is set to 11.

Boost operation is enabled only when the following conditions are met:

- V_{BATT} > V_{BATT_UVLO} (rising 2.7V).
- OTG is high and REG01 Bit[5:4] = 10/11.
- Boost mode is enabled after a 200ms delay.
- V_{IN} < 1V.

Once OTG is enabled, if the voltage at V_{IN} does not rise above the USB UVLO (4.6V) level within 6ms, the IC turns off the block switch for 8ms and regulates the switch linearly again for 6ms. The condition repeats until the OTG voltage is higher than 4.6V.

When both charging and OTG are enabled, OTG operation takes priority.

Figure 14 shows the OTG boost start-up time sequence. Once OTG is enabled, the MP2624A boosts PMID to 5.0V first. Then the block FET is regulated linearly with the current limit of I_{OLIM} + 300mA. When V_{IN_OTG} is charged higher than 4.6V within 6ms, the block FET is turned on fully. Otherwise, PMID tries to charge IN again after an 8ms off period. The condition repeats until V_{IN_OTG} is higher than 4.6V.

The MP2624A provides output short-circuit protection and output over-voltage protection. In OTG mode, if V_{IN} falls to only 100mV higher than V_{BATT}, the operation enters the 6ms linear control, turns off for 8ms, and enters hiccup mode.

The MP2624A monitors the voltage at V_{IN_OTG} in OTG boost mode continuously. Once the V_{IN} exceeds V_{OTG_OVP}, the MP2624A stops switching, and a corresponding fault register is set high to indicate the fault.

Any fault that occurs during boost operation sets the fault register REG09 Bit[6] to 1.

In OTG mode, the MP2624A employs a fixed, 1.7MHz, PWM, step-up switching regulator. It switches from PWM operation to pulse-skipping operation at light load.

OTG Output CC Mode

When in the OTG mode, the load at the V_{IN} has a current limit, which could be set up to 2A via the I²C REG02 Bit[1:0]. MP2624A could operate in CC mode when the current limit is reached, and V_{IN} does not drop to the overload or short-circuit threshold (<V_{BATT} + 100mV) as shown in Figure 15. Therefore, MP2624A not only has the CC mode during the charging process, but also has CC mode operation in OTG mode for various applications.

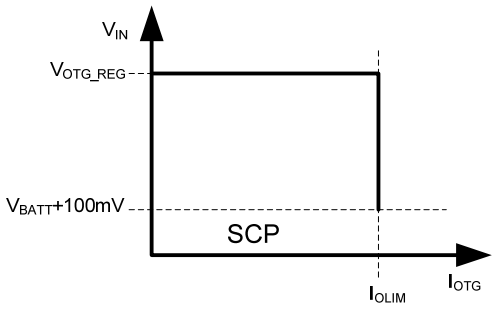


Figure 15: OTG Output U-I Curve

Impedance Compensation to Accelerate Charging

Throughout the charging cycle, the constant-voltage charging stage occupies large ratios. To accelerate the charging cycle, it is better to have the charging remain in the constant-current charge stage for as long as possible.

MP2624A allows the user to compensate the intrinsic resistance of the battery by adjusting the charge full voltage threshold, according to the charge current and internal resistance. In addition, a maximum-allowed regulated voltage is set for the sake of the safety condition. See Equation (2):

$$V_{BATT\_REG} = V_{BATT\_FULL} + Min\left(I_{CHG\_ACT} \times R_{BAT\_CMP}, V_{CLAMP}\right) \quad (2)$$

Where V_{BATT_REG} is the battery regulation voltage, V_{BATT_FULL} is the charge-full voltage set via the I²C REG04 Bit[7:2], I_{CHG_ACT} is the real-time charge current during the operation, R_{BAT_CMP} is the compensated resistor to simulate the resistor of the connection wire of the battery(it is selected through the REG06 Bit[7:5]), and V_{CLAMP} is the battery compensation voltage clamp (above V_{BATT_FULL}) selected via REG06 Bit[4:2].

Sleep Mode

When the input power source is missing and OTG is disabled, the MP2624A transitions into sleep mode. During sleep mode, the battery powers the internal circuit, and the internal VREF LDO is turned off. The system is connected to the battery through the battery FET, and IN is bridged off from SYS by the reverse blocking FET. In order to extend battery life during shipping and storage, the MP2624A can turn off the battery FET to minimize leakage.

Series Interface

The MP2624A uses I²C compatible interface for flexible parameter settings and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL).

The IC operates as a slave device with the address 4BH receiving control inputs from the master device, like a microcontroller or a digital signal processor.

The I²C interface supports both standard mode (up to 100k bits) and fast mode (up to 400k bits).

Both SDA and SCL are bidirectional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. SDA and SCL are open drain.

The Data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred (see Figure 16).

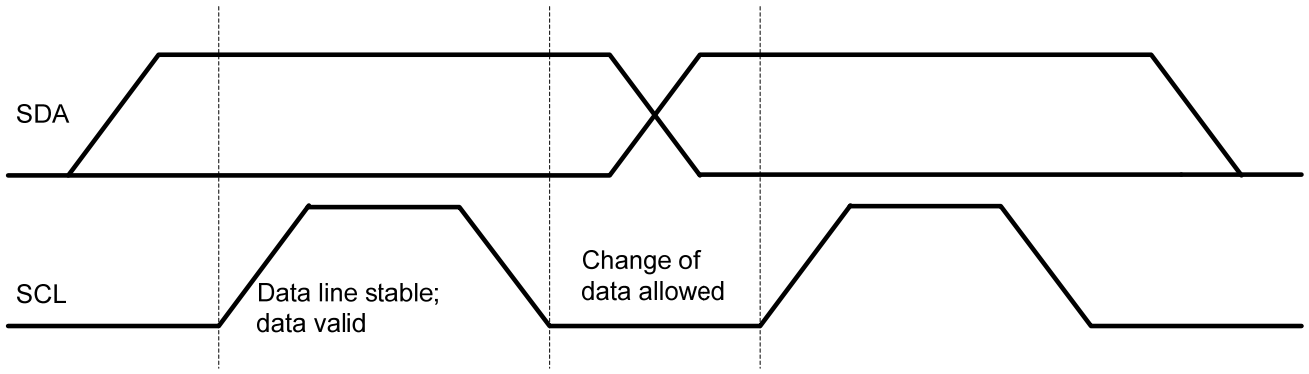


Figure 16: Bit Transfer on the I²C Bus

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH-to-LOW transition on the SDA line while the SCL line is high defines a start condition. A LOW-to-HIGH transition on the SDA line when the SCL line is high defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition; it is considered free after the STOP condition (see Figure 17).

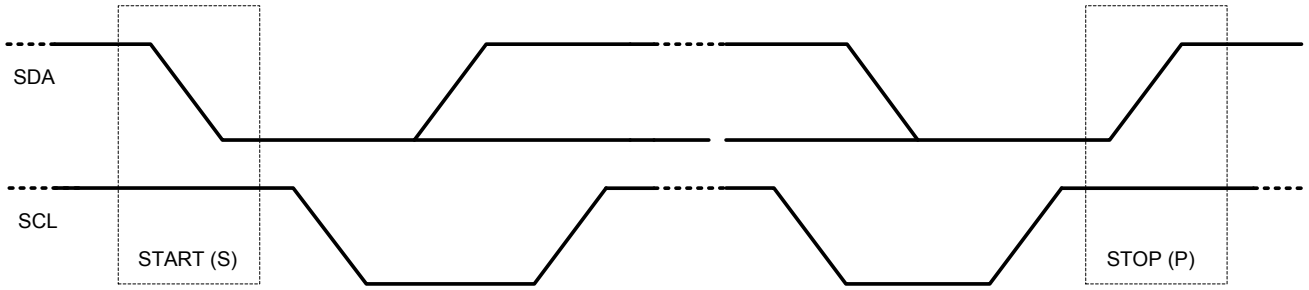


Figure 17: Start and Stop Conditions

Every byte on the SDA line must be 8 bits long. The number of bytes transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line LOW to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the SCL line (see Figure 18).

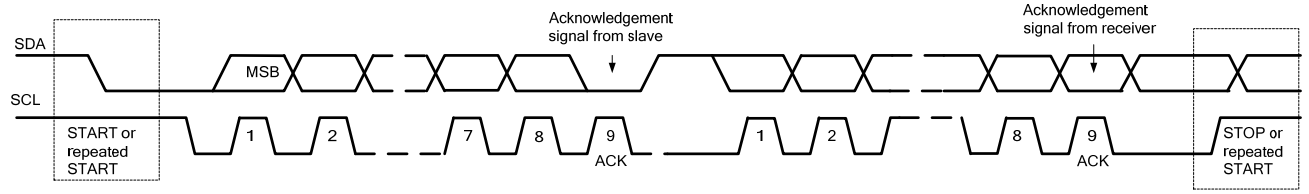


Figure 18: Data Transfer on the I²C Bus

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was received successfully and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line LOW and it remains HIGH during the 9th clock pulse. This is the “Not Acknowledge” signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

After the START, a slave address is sent. This address is 7 bits long followed by an 8th bit a data direction bit (bit R/W).

A zero indicates a transmission (WRITE), and a one indicates a request for data (READ). The complete data transfer is shown in Figure 19 though Figure 23.

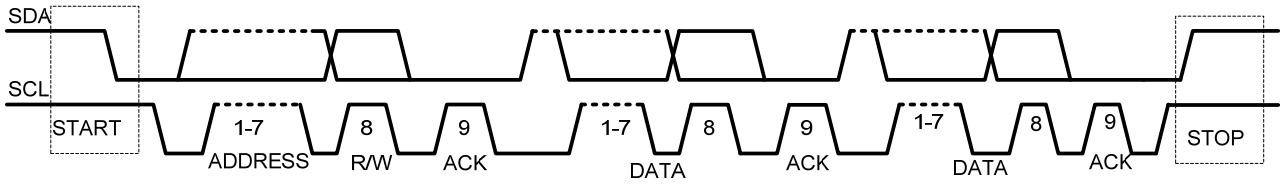


Figure 19: Complete Data Transfer

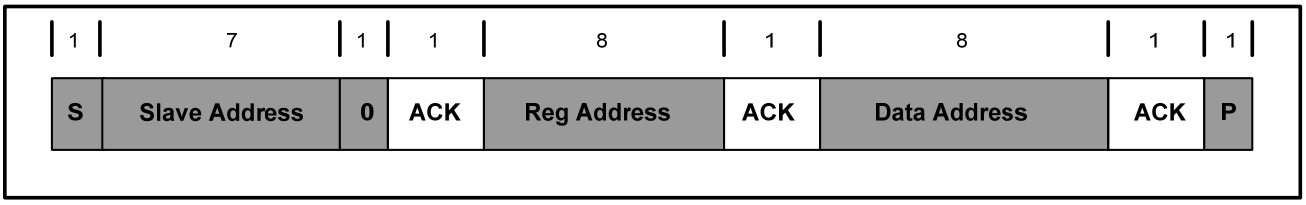


Figure 20: Single Write

Figure 21: Single Read

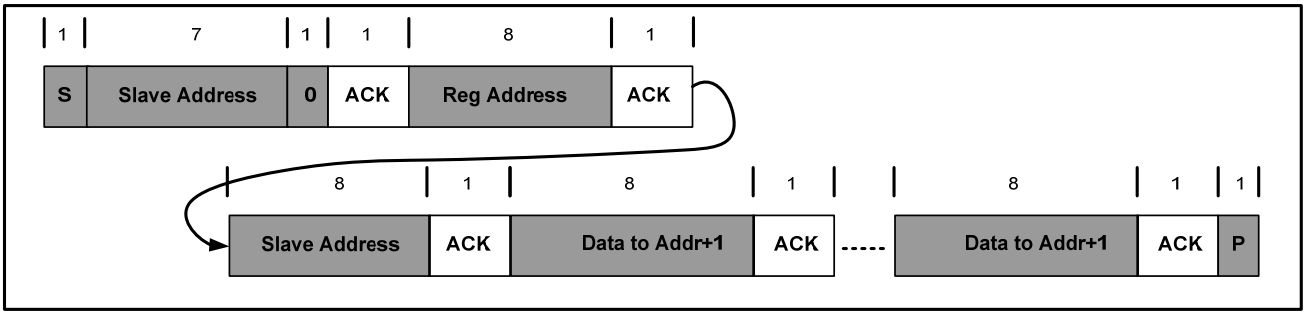


Figure 22: Multi-Write

Figure 23: Multi-Read

If the register address is not defined, the charger IC sends back NACK and returns to an idle state.

The charger device supports multi-read and multi-write on REG00 through REG08.

The fault register REG09 records the fault status in time and sends an interrupt signal (INT) to the host to read the fault status:

Case1: if the fault disappears before the host reads it, the host could read a normal status only. For example, if the system OVP fault occurs but recovers later, the fault register REG09 reports the fault when the fault occurs and clears the fault when the fault disappears. So, if the host reads REG09 after the fault disappears, it reads a normal status. Additionally, the fault register REG09 supports multi-read.

Case2: When a fault occurs, an INT is sent to host to the show that the fault occurred if host did not read REG09 in time. When the fault disappears and another fault occurs, the IC will not send INT to the host, since the host did not react to the previous interrupt, but REG09 will be written as the current fault status. For example, if there is a battery OVP fault, but it recovers immediately, then a timer-out fault occurs, and the IC does not send the INT again. But if the host reads REG09, it reads the register's current state timer-out fault.

Case3: The NTC fault is an exception to this condition. Once the NTC fault occurs, an interrupt is sent to the host by setting the REG09 status.

I²C REGISTER MAP

IC Address: 4BH

Input Source Control Register/Address: 00H (Default: 0011 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	EN_HZ(8)	0: Disable 1: Enable	Read/Write	Default: Disable (0)
Input Voltage Regulation				
Bit 6	V_{IN_REG} [3]	640mV	Read/Write	Offset: 3.88V Range:3.88V - 5.08V Default: 4.36V (0110)
Bit 5	V_{IN_REG} [2]	320mV		
Bit 4	V_{IN_REG} [1]	160mV		
Bit 3	V_{IN_REG} [0]	80mV		
Input Current Limit				
Bit 2	I_{IN_LMT} [2]	000: 100mA 001: 150mA 010: 500mA 011: 900mA 100: 1200mA 101: 1800mA 110: 2000mA 111: 3000mA	Read/Write	Default: SDP: 100mA (000) or 500mA (010) Default: DCP/CDP: 1.8A (101)
Bit 1	I_{IN_LMT} [1]			
Bit 0	I_{IN_LMT} [0]			

Power-On Configuration Register/Address: 01H (Default: 0001 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Register reset	0: Keep current setting 1: Reset	Read/Write	Keep current register setting (0)
Bit 6	I²C watchdog timer reset	0: Normal 1: Reset	Read/Write	Normal (0)
Charger Configuration				
Bit 5	Mode [1]	00: Charge disable 01: Charge battery 10/11: OTG	Read/Write	Charge battery (01)
Bit 4	Mode [0]			
Minimum System Voltage				
Bit 3	V_{SYS_MIN} [2]	0.4V	Read/Write	Offset: 3V Range: 3V - 3.7V Default: 3.6V (110)
Bit 2	V_{SYS_MIN} [1]	0.2V		
Bit 1	V_{SYS_MIN} [0]	0.1V		
System Regulation Voltage Higher than Full Battery Voltage				
Bit 0	V_{SYS_MAX} [0]	0: 50mV 1: 100mV	Read/Write	Default: 100mV (1)

NOTE:
7) This is used to turn off the DC/DC only. At this time, the system is powered by the battery.

Charge Current Control Register/Address: 02H (Default: 0010 0001)

Bit	Symbol	Description	Read/Write	Default
Bit 7	I_{CHG} [5]	2048mA	Read/Write	Offset: 512mA Range: 512mA - 4544mA Default: 1024mA (001000)
Bit 6	I_{CHG} [4]	1024mA		
Bit 5	I_{CHG} [3]	512mA		
Bit 4	I_{CHG} [2]	256mA		
Bit 3	I_{CHG} [1]	128mA		
Bit 2	I_{CHG} [0]	64mA		
USB OTG Current Limit				
Bit 1	I_{OLIM} [1]	00: 500mA 01: 1.3A	Read/Write	1.3A (01)
Bit 0	I_{OLIM} [0]			

Pre-Charge/Termination Current/Address: 03H (Default: 0011 0011)

Bit	Symbol	Description	Read/Write	Default
Pre-Charge Current				
Bit 7	I_{PRE} [3]	512mA	Read/Write	Offset: 64mA Range: 64mA - 1024mA Default: 256mA (0011)
Bit 6	I_{PRE} [2]	256mA		
Bit 5	I_{PRE} [1]	128mA		
Bit 4	I_{PRE} [0]	64mA		
Termination Current				
Bit 3	I_{BF} [3]	512mA	Read/Write	Offset: 64mA Range: 64mA - 1024mA Default: 256mA (0011)
Bit 2	I_{BF} [2]	256mA		
Bit 1	I_{BF} [1]	128mA		
Bit 0	I_{BF} [0]	64mA		

Charge Voltage Control Register/Address: 04H (Default: 1100 0011)

Bit	Symbol	Description	Read/Write	Default
Charge Full Voltage				
Bit 7	V_{BATT_FULL} [5]	480mV	Read/Write	Offset: 3.48V Range: 3.48V - 4.425V Default: 4.2V (110000)
Bit 6	V_{BATT_FULL} [4]	240mV		
Bit 5	V_{BATT_FULL} [3]	120mV		
Bit 4	V_{BATT_FULL} [2]	60mV		
Bit 3	V_{BATT_FULL} [1]	30mV		
Bit 2	V_{BATT_FULL} [0]	15mV		
Pre-Charge Threshold				
Bit 1	V_{BATT_PRE}	0: 2.8V 1: 3.0V	Read/Write	3.0V (1)
Battery Recharge Threshold (below V_{BATT_FULL})				
Bit 0	V_{RECH}	0: 200mV 1: 100mV	Read/Write	100mV (1)

Charge Termination/Timer Control Register/Address: 05H (Default: 1001 1000)

Bit	Symbol	Description	Read/Write	Default
Termination Setting				
Bit 7	EN_BF	0: Disable 1: Enable	Read/Write	Enable (1)
Termination Indicator Threshold				
Bit 6	BF_STAT	0: Match I_{BF} 1: Indicate before the actual termination on START	Read/Write	Match I_{BF} (0)
I²C Watchdog Timer Limit				
Bit 5	WATCHDOG [1]	00: Disable timer 01: 40s 10: 80s 11: 160s	Read/Write	40s (01)
Bit 4	WATCHDOG [0]			
Safety Timer Setting				
Bit 3	EN_TIMER	0: Disable 1: Enable	Read/Write	Enable timer (1)
Constant-Current Charge Timer (2x during PPM)				
Bit 2	CHG_TMR [1]	00: 5hrs 01: 8hrs 10: 12hrs 11: 20hrs	Read/Write	5hrs (00)
Bit 1	CHG_TMR [2]			
Bit 0	Reserved		Read/Write	(0)

Compensation/Thermal Regulation Control Register/Address: 06H (Default: 0000 0011)

Bit	Symbol	Description	Read/ Write	Default
Bit 7	R_{BAT_CMP} [2]	40mΩ	Read/Write	Range: 0 - 70mΩ Default: 0mΩ (000)
Bit 6	R_{BAT_CMP} [1]	20mΩ		
Bit 5	R_{BAT_CMP} [0]	10mΩ		
Battery Compensation Voltage Clamp (above V_{BATT_FULL})				
Bit 4	V_{CLAMP} [2]	64mV	Read/Write	Range: 0 - 112mV Default: 0mV (000)
Bit 3	V_{CLAMP} [1]	32mV		
Bit 2	V_{CLAMP} [0]	16mV		
Thermal Regulation Threshold				
Bit 1	T_{REG} [1]	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Read/Write	Default: 120°C (11)
Bit 0	T_{REG} [0]			

Miscellaneous Operation Control Register/Address: 07H (Default: 0101 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	USB_DET_EN	0: Not in DP/DM detection 1: Force DP/DM detection	Read/Write	Not in DP/DM detection (0)
Bit 6	TMR2X_EN	0: Disable 2x extended safety timer 1: Enable 2x extended safety timer	Read/Write	Enable (1)
Bit 5	BATFET_DIS	0: Enable 1: Turn off	Read/Write	Enable (0)
Bit 4	Reserved		Read/Write	(0)
Bit 3	EN_NTC	0: Disable 1: Enable	Read/Write	Enable (1)
Bit 2	BATUVLO_DIS	0: Enable 1: Disable	Read/Write	(0)
Bit 1	INT_MASK [1]	0: No INT in CHG_FAULT 1: INT in CHG_FAULT	Read/Write	INT in CHG_FAULT (1)
Bit 0	INT_MAST [0]	0: No INT in BAT_FAULT 1: INT in BAT_FAULT	Read/Write	INT in BAT_FAULT (1)

System Status Register/Address: 08H (Default: 0000 0001)

Bit	Symbol	Description	Read/Write	Default
Bit 7	V_{BUS_STAT} [1]	00: Unknown 01: Adaptor port 10: USB host 11: OTG	Read only	Unknown (00) (including no input or DPDM detection incomplete)
Bit 6	V_{BUS_STAT} [0]			
Bit 5	CHG_STAT [1]	00: Not charging 01: Trickle charge 10: Constant-current charge 11: Charge done	Read only	Not charging (00)
Bit 4	CHG_STAT [0]			
Bit 3	PPM_STAT	0: No PPM 1: VINPPM or IINPPM	Read only	No PPM (0) (no power path management occurs)
Bit 2	PG_STAT	0: No power good 1: Power good	Read only	No power good (0)
Bit 1	THERM_STAT	0: Normal 1: Thermal regulation	Read only	Normal (0)
Bit 0	VSYS_STAT	0: In VSYSMIN regulation 1: Not in VSYSMIN regulation	Read only	Not in VSYSMIN regulation (1)

Fault Register/Address: 09H (Default: 0000 0000)

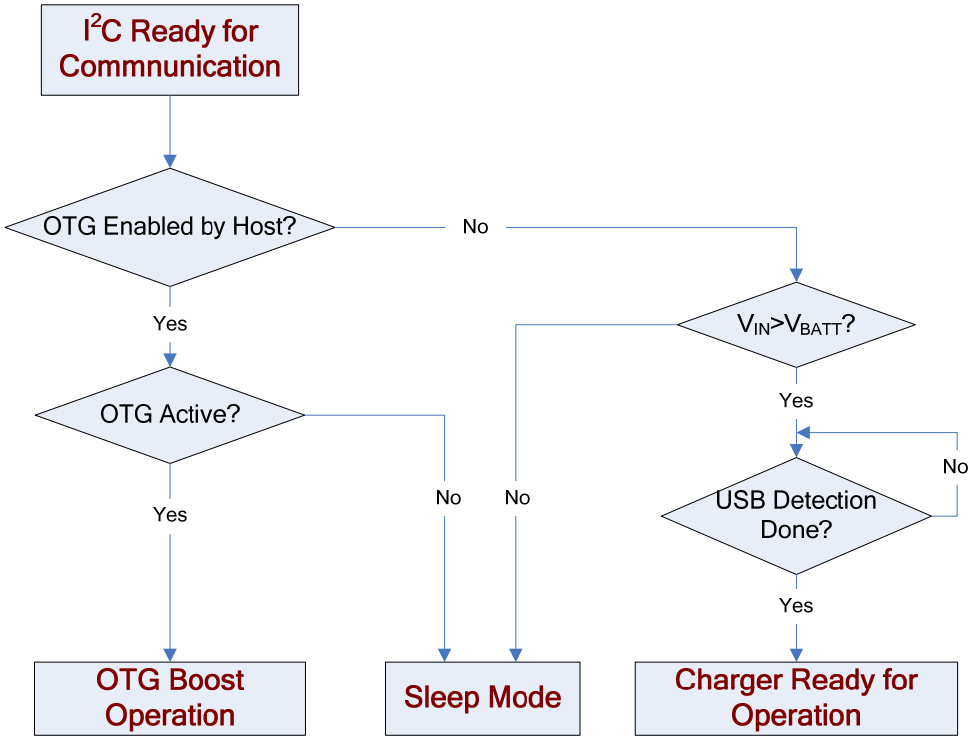
Bit	Symbol	Description	Read/Write	Default
Bit 7	WATCHDOG_FAULT	0: Normal 1: Watchdog timer expiration	Read only	Normal (0)
Bit 6	OTG_FAULT	0: Normal 1: VBUS overloaded, VBUS OVP, or battery under-voltage	Read only	Normal (0)
Bit 5	CHG_FAULT [1]	00: Normal 01: Input fault (OVP or bad source) 00: Thermal shutdown 11: Safety timer expiration	Read only	Normal (00)
Bit 4	CHG_FAULT [0]			
Bit 3	BAT_FAULT	0: Normal 1: Battery OVP	Read only	Normal (0)
Bit 2	NTC_FAULT [2]	000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot	Read only	Normal (000)
Bit 1	NTC_FAULT [1]			
Bit 0	NTC_FAULT [0]			

Vender/Part/Reversion Status Register/Address: 0AH (Default: 0000 0100)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved		Read only	(0)
Bit 6	Reserved		Read only	(0)
Part Number				
Bit 5	PN [2]	MP2624A (000)	Read only	(000)
Bit 4	PN [1]			
Bit 3	PN [0]			
Bit 2	NTC_TYPE	0: Standard 1: JEITA	Read only	(1)
Revision				
Bit 1	Rev [1]		Read only	(00)
Bit 0	Rev [0]			

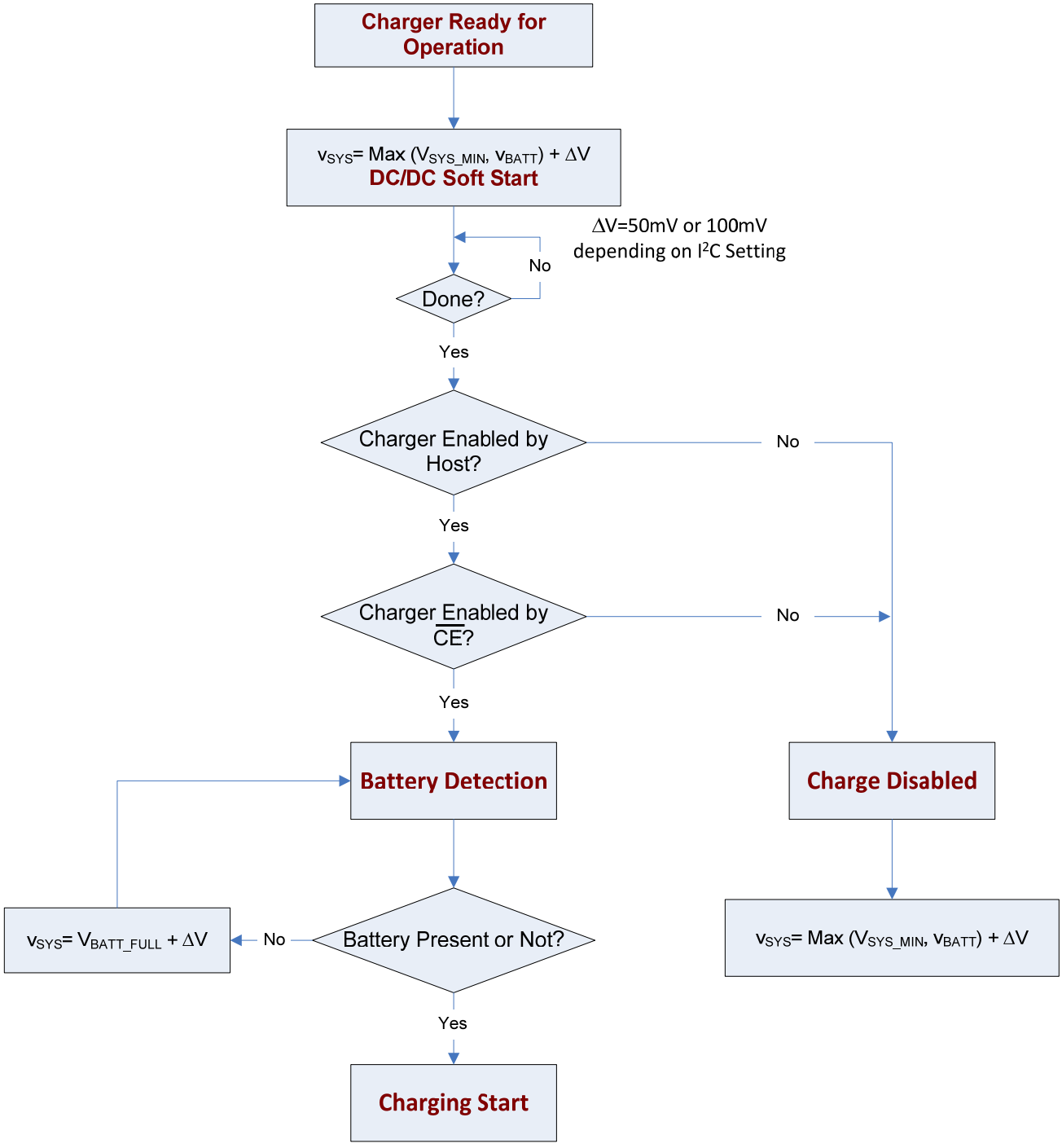
CONTROL FLOW CHART

Different Operations in Host Mode



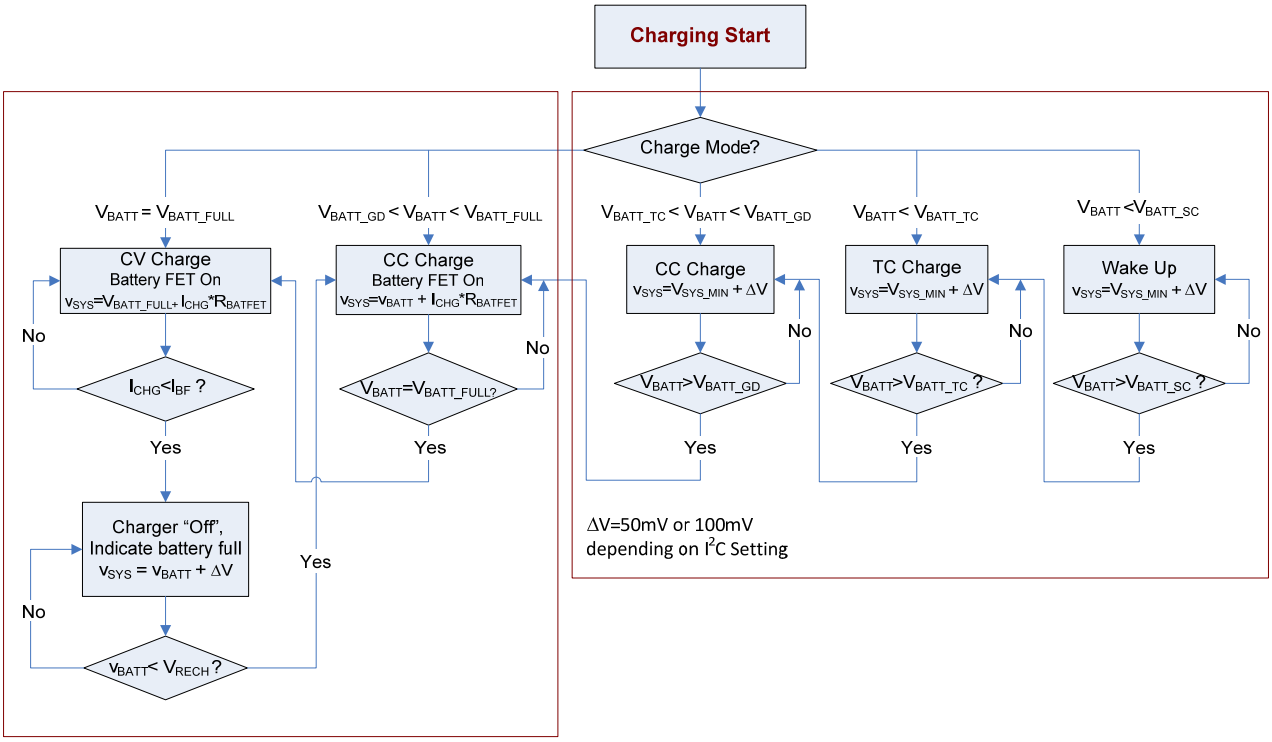
CONTROL FLOW CHART *(continued)*

Charging Process



CONTROL FLOW CHART *(continued)*

Charging Process



APPLICATION INFORMATION

Setting the Input Current Limit

The input current limit setting is set according to the input power source. For an adapter input, the input current limit can be set through I²C by the GUI. To set a value that is not provided by the I²C, the input current limit can be set through ILIM. Connect a resistor from ILIM to AGND to program the input current limit. The relationship can be calculated using Equation (3):

$$I_{IN\_LMT} = \frac{48.48}{R_{ILIM}(k)}(A) \quad (3)$$

The MP2624A selects the smaller one of the I²C and resistor settings for its input current limit setting. For resistor setting, use 1% accuracy resistor.

For a USB input, the input current limit is set according to Table 2.

Selecting the Inductor

Inductor selection is a trade-off between cost, size, and efficiency. A lower inductance value corresponds with a smaller size, but it results in a higher ripple current, a higher magnetic hysteretic loss, and a higher output capacitance. Choosing a higher inductance value provides a lower ripple current and smaller output filter capacitors, but it may result in higher inductor DC resistance (DCR) loss and larger size.

From a practical standpoint, the inductor ripple current should not exceed 30% of the maximum load current under worst-case conditions. When operating with a typical 5V input voltage, the maximum inductor current ripple occurs at the corner point between the trickle charge and the CC charge (V_{BATT} = 3V). Estimate the required inductance with Equation (4) and Equation (5):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L\_MAX}} \frac{V_{BATT}}{V_{IN} \times f_S(MHz)}(\mu H) \quad (4)$$

$$I_{PEAK} = I_{LOAD(MAX)} \times (1 + \frac{\%ripple}{2})(A) \quad (5)$$

Where V_{IN} is the typical input voltage, V_{BATT} is the battery voltage, f_S is the switching frequency, and ΔI_{L_MAX} is the maximum inductor ripple current, which is usually 30% of the CC charge current.

Although the maximum charge current can be set to a high 4.5A, the real charge current cannot reach this value as the input current limit. For most applications, allow for a large enough margin to avoid reaching the peak current limit of the high-side switch (7A, typically). The maximum inductor current ripple is set to 1.0A with $5V_{IN}$ (30% of the max load- about 3.5A considering the input current limit); the inductor is 0.75μH. Select 1.0μH in the application with the saturation current over 4.5A

Choose a larger inductance such as 2.2μH is good for the EMI consideration with smaller current ripple, while the size may be larger.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors are also sufficient. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C_{IN}} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

Where V_{OUT} is V_{SYS}.

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = I_{LOAD}/2 \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

For the MP2624A, the RMS current in the input capacitor comes from PMID to GND, so a small, high-quality, ceramic capacitor (e.g.: 4.7μF), should be placed as close to the IC as possible from VPMID to PGND. The remaining capacitor should be placed from VIN to GND.

When using ceramic capacitors, ensure they have enough capacitance to provide a sufficient

charge to prevent excessive voltage ripple at the input.

Selecting the Output Capacitor

The output capacitor (C_{SYS}) from the typical application circuit is in parallel with the SYS load. C_{SYS} absorbs the high-frequency switching ripple current and smooths the output voltage. Its impedance must be much less than the system load to ensure it properly absorbs the ripple current.

Ceramic capacitors are recommended because they have a lower ESR and a smaller size. This allows the ESR of the output capacitor to be ignored. Thus, the output voltage ripple is given with Equation (8):

$$\Delta r = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1 - \frac{V_{SYS}}{V_{IN}}}{8 \times C_{SYS} \times f_S^2 \times L}\% \quad (8)$$

To guarantee ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g.: 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

For V_{IN} = 7V, V_{SYS_MIN} = 3.6V, L = 2.2μH, f_S = 1.6MHz, and Δr = 0.1%. The output capacitor can be calculated as 11μF using Equation (9):

$$C_{SYS} = \frac{1 - \frac{V_{SYS\_MIN}}{V_{IN}}}{8 \times f_S^2 \times L \times \Delta r} \quad (9)$$

Then choose a 22μF ceramic capacitor.

Resistor Selection for the NTC Sensor

Figure 8 shows an internal resistor divider reference circuit that limits both the high and low temperature thresholds at V_{TH_High} and V_{TH_Low}, respectively. For a given NTC thermistor, select an appropriate R_{T1} and R_{T2} to set the NTC window using Equation (10) and Equation (11):

$$\frac{R_{T2} // R_{NTC\_Cold}}{R_{T1} + R_{T2} // R_{NTC\_Cold}} = \frac{V_{COLD}}{V_{NTC}} \quad (10)$$

$$\frac{R_{T2} // R_{NTC\_Hot}}{R_{T1} + R_{T2} // R_{NTC\_Hot}} = \frac{V_{HOT}}{VCC} \quad (11)$$

R_{NTC_Hot} is the value of the NTC resistor at a high temperature (within the required temperature operating range), and R_{NTC_Cold} is the value of the NTC resistor at a low temperature.

The two resistors (R_{T1} and R_{T2}) allow the high and low temperature limits to be programmed independently. With this feature, the MP2624A can fit most types of NTC resistors and different temperature operating range requirements.

The R_{T1} and R_{T2} values depend on the type of NTC resistor selected. For example, for a 103AT thermistor, the thermistor has the following electrical characteristics: at 0°C, R_{NTC_Cold} = 27.28kΩ, and at 60°C, R_{NTC_Hot} = 3.02kΩ.

The following equation calculations are derived assuming that the NTC window is between 0°C and 50°C. According to Equation (10) and Equation (11), use $\frac{V_{COLD}}{V_{NTC}}$ and $\frac{V_{HOT}}{V_{NTC}}$ from the EC table to calculate R_{T1} = 2.27kΩ and R_{T2} = 6.86kΩ.

PCB Layout Guidelines

Efficient PCB layout is critical for meeting specified noise rejection requirements and improving efficiency. For best results, follow the guidelines below.

1. Route the power stage adjacent to the grounds.
2. Minimize the high-side switching node (SW, inductor) trace lengths in the high-current paths and the current sense resistor trace.
3. Keep the switching node short and away from all small control signals, especially the feedback network.
4. Place the input capacitor as close to PMID and PGND as possible.
5. Place the output inductor close to the IC.
6. Connect the output capacitor between the inductor and PGND of the IC.
7. Connect the pins for the power pads (IN, SW, SYS, BATT, and PGND) to as much copper on the board as possible for high-current applications.

   This improves thermal performance because the board conducts heat away from the IC.
8. Connect the PCB ground plane directly to the return of all components. It is recommended to place it inside the PGND pads for the IC, if possible.

   Typically, a star ground design approach is used to keep the circuit block currents isolated (high-power/low-power small signals), which reduces noise coupling and ground-bounce issues. A single ground plane for this design produces good results. With this small layout and a single ground plane, there is no ground-bounce issue. Segregating the components minimizes coupling between the signals and stability requirements.
9. Pull the connection wire from the MCU (I²C) far away from the SW mode and copper regions.
10. Keep SCL and SDA close in parallel.

TYPICAL APPLICATION CIRCUITS

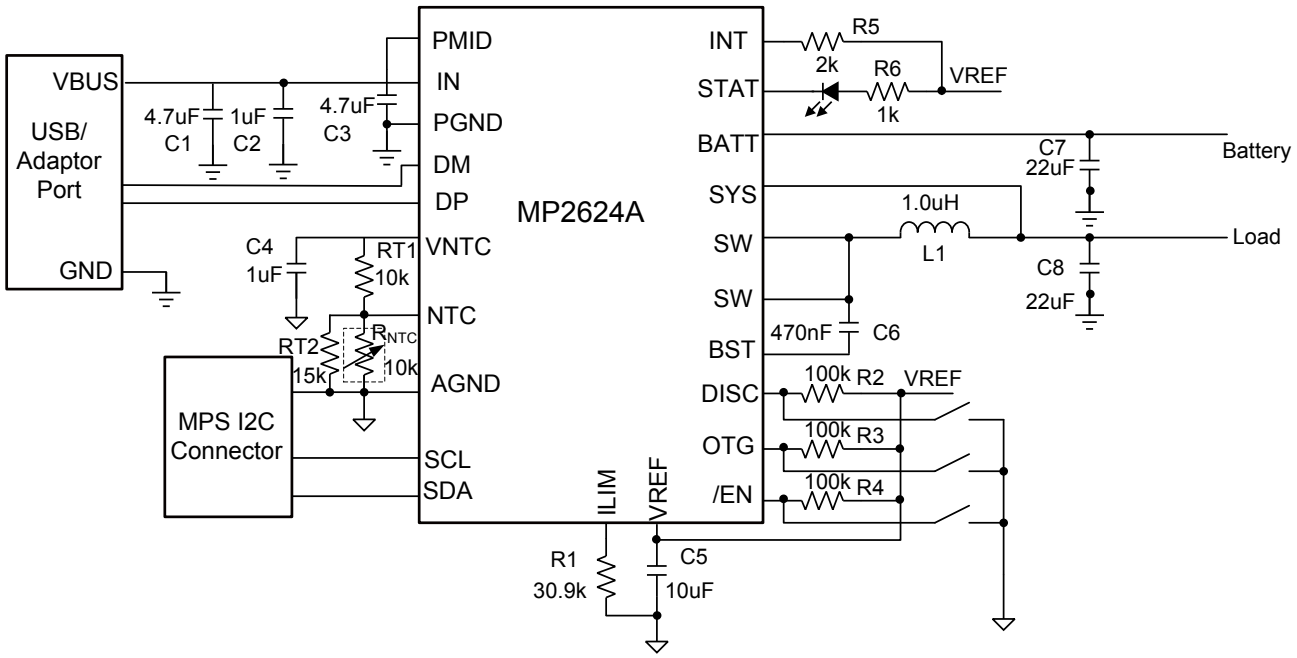


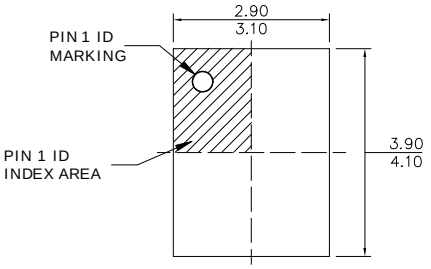
Figure 24: Typical Application Circuit of MP2624A with 5VIN

Table 3. The BOM of the Key Components

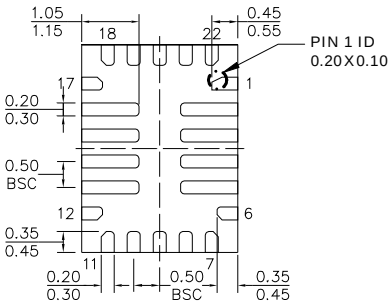
Qty	Ref	Value	Description	Package	Manufacture
1	C1	4.7μF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	C2	1μF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
1	C3	4.7μF	Ceramic Capacitor;10V; X5R or X7R	0805	Any
1	C4	1μF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	C5	10μF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	C6	470nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
2	C7,C8	22μF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	RT1	10k	Film Resistor;1%	0603	Any
1	RT2	15k	Film Resistor;1%;	0603	Any
1	L1	1.0μH	Inductor;1.0μH;Low DCR;I_{SAT}>5A	SMD	Any

PACKAGE INFORMATION

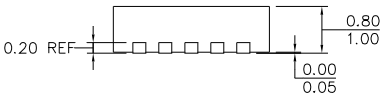
QFN-22 (3mmx4mm)



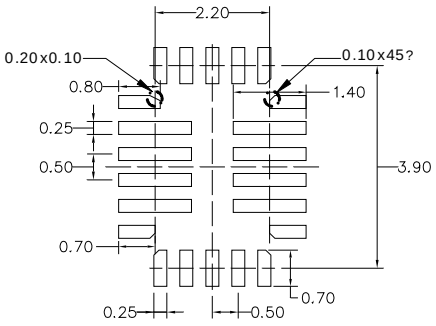
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX
4) JEDEC REFERENCE IS MO220.
5) DRAWING IS NOT TO SCALE

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