MP100

Offline Inductor-less Regulator For Low Power Applications

The Future of Analog IC Technology

DESCRIPTION

The MP100 is a compact, inductor-less, good-efficiency, off-line regulator. It steps down the AC line voltage to an adjustable DC output. It is a simple solution to provide a bias voltage to ICs in off-line applications. Its integrated smart-control system uses AC line power only when necessary, thus minimizing device losses to achieve good efficiency. This device can help system designs meet new standby power specifications.

The MP100 provides various protections, such as over-current protection, short-circuit protection, VD over-voltage protection, VD under-voltage lockout, and thermal shutdown.

The MP100 is available in a SOIC8E package.

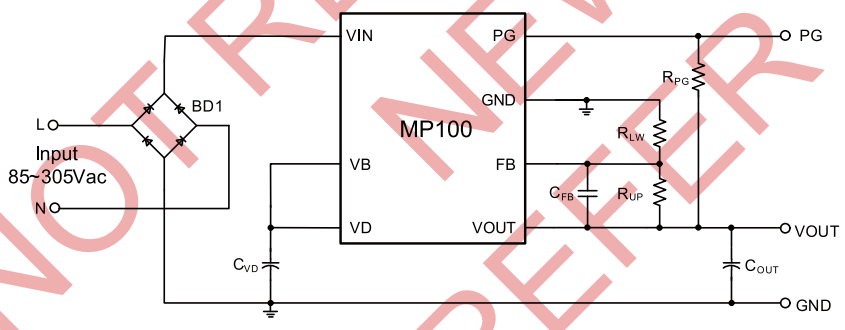
FEATURES

- Universal AC Input (85VAC-to-305VAC)
- Smart Control to Maximize Efficiency
- Adjustable Output Voltage from 1.5V to 15V
- Low Component Count and Cost
- Thermal Shutdown Protection
- Short-Circuit Protection
- Provide Power-Good Signal
- No Bulk Capacitor Required

APPLICATIONS

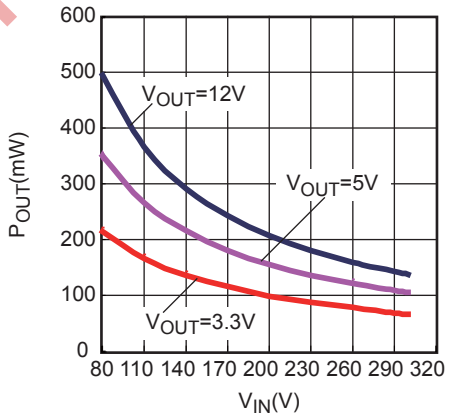
- Wall Switches and Dimmers
- AC/DC Power Supply for Wireless System, like ZigBee,Z-Wave and so on
- Standby Power for General Off-Line Applications

TYPICAL APPLICATION



Output Power vs. VIN

Full Bridge Rectifier

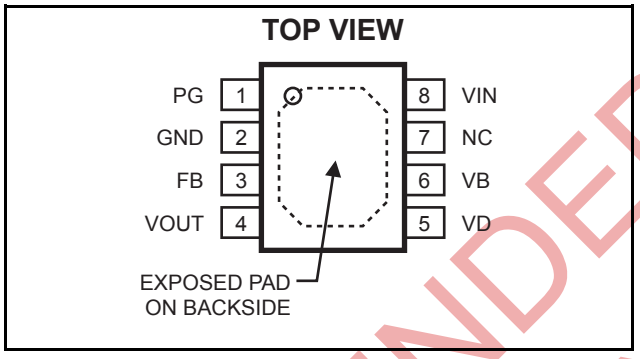


ORDERING INFORMATION

Part Number *	Package	Top Marking
MP100GN	SOIC8E	MP100

* For Tape & Reel, add suffix –Z (e.g. MP100GN–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -1V to 750V
VOUT ..... -0.3V to 30V
VB,VD ..... -0.3V to 35V
FB ..... -0.3V to 6.5V
PG ..... -0.3V to 14V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8E..... 2.5W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... -55°C to +150°C

Recommended Operating Conditions (3)

50/60Hz AC RMS Voltage ..... 85V to 305V
VB ,VD ..... 8V to 30V
Operating Junction Temp. (T_J) -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
SOIC8E	50	10 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Supply (Pin VIN)						
Input Voltage	VIN				700	V
Input Supply Quiescent Current	I_{INQS}	VD=30V, VIN=60V,No Load			20	μA
Input Voltage Threshold Fast	$V_{THVINFAST}$		32		38	V
Input Voltage Threshold Fast Hysteresis	$V_{THVINFASTHYS}$			3.5		V
Input Voltage Threshold Slow	$V_{THVINSLOW}$		27		32	V
Input Voltage Threshold Slow Hysteresis	$V_{THVINSLOWHYS}$			2		V
MOSFET ON Resistance	R_{dson}	VIN=20V		9.5		Ω
Energy Store Section (Pin VD)						
VD Peak-Voltage Limit	VD_{LMT}		27		32.5	V
VD UVLO	VD_{UVLO}		6.3		7.4	V
Output Enable VD Threshold	VD_{THOUT}		13.2		17.5	V
Active Bleeder VD Threshold off	$VD_{THBLEEDER}$		13.2		17.5	V
Hysteresis	$VD_{THOUTHYS}$			1.3		V
Bleeder Current	I_{BLEED}			240		μA
Adjustable Output Voltage (Pin VOUT)						
Vo Regulated Voltage	Vo	VD=30V,Io=40mA	11.5	12	12.4	V
Output Current Limit	I_{OLMT}		120		270	mA
Line Regulation[5]		VD=15V to 30V, Io=100μA		0.06		%
Load Regulation[6]		VD=30V, Io=100μA to 40mA		0.08		%
Dropout Voltage[7]	V_{DROP}	Io=40mA		0.75		V
Ground Pin Current	I_G	Io=40mA		1.069		mA
Power-Supply Ripple Rejection[8]	PSRR	f=10Hz to 60kHz, VD=20V,C_{VD}=1μF, C_{OUT}=4.7μF		<60		dB
Over-Temperature–Protection Threshold	T_{OTP}			160		°C
Over-Temperature–Protection Threshold Hysteresis	T_{HYS}			20		°C
Output Voltage Feedback (Pin FB)						
Reference Voltage	V_{REF}		1.204	1.235	1.266	V
Power-Good Signal (Pin PG)						
Power-Good Pull Down Current	I_{PG}			1.77		mA
Power-Good Threshold	V_{THPG}		1		1.239	V
Power-Good Hysteresis	V_{HYSPG}			65		mV
Power-Good Delay	$\tau_{DELAYPG}$		170	235	280	μs

Notes:

5) Line Regulation = $\frac{\left|V_{OUT\left[V_{IN(MAX)}\right]} - V_{OUT\left[V_{IN(MIN)}\right]}\right|}{V_{OUT(NORM)}} \times 100(\%)$

6) Load Regulation = $\frac{\left|V_{OUT\left[I_{OUT(MAX)}\right]} - V_{OUT\left[I_{OUT(MIN)}\right]}\right|}{V_{OUT(NORM)}} \times 100(\%)$

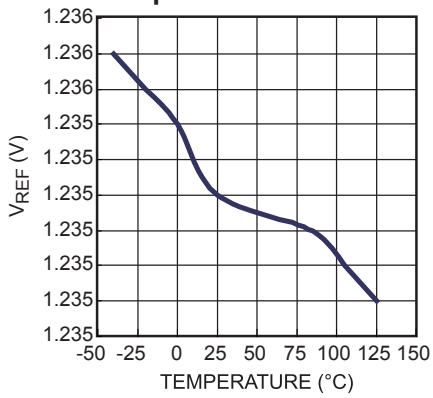
7) The dropout voltage is defined as V_{IN}-V_{OUT}

8) Guarantee by design

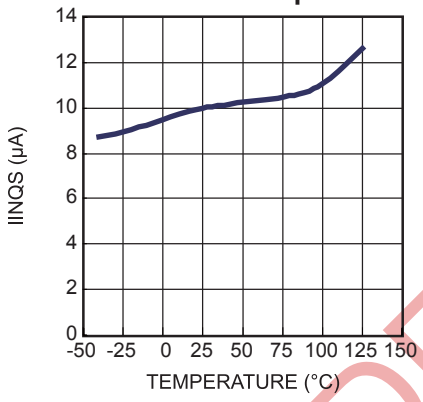
TYPICAL CHARACTERISTICS

VIN=230VAC, VOUT=12V, I_{OUT}=10mA, C_{VD}=220µF/35V, T_A=+25°C, unless otherwise noted.

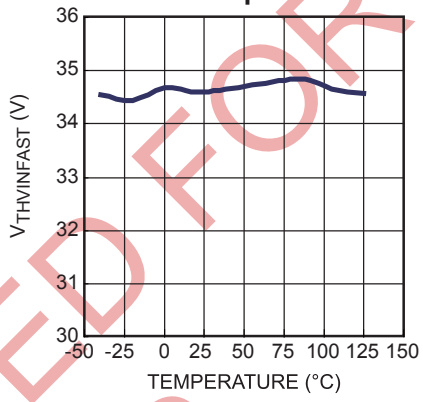
Reference Voltage vs. Temperature



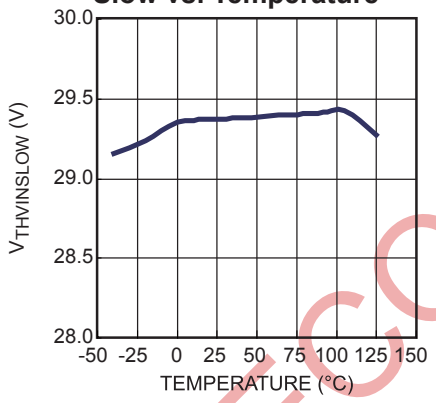
Input Supply Quiescent Current vs. Temperature



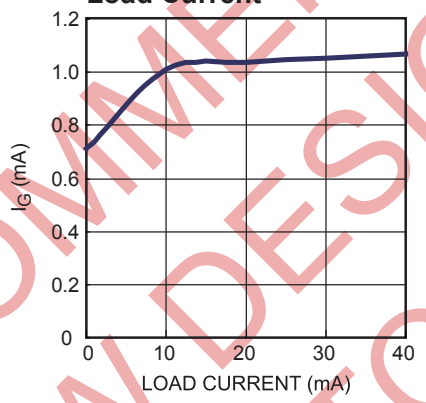
Input Voltage Threshold Fast vs. Temperature



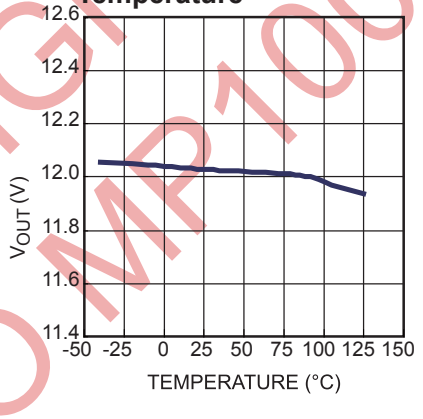
Input Voltage Threshold Slow vs. Temperature



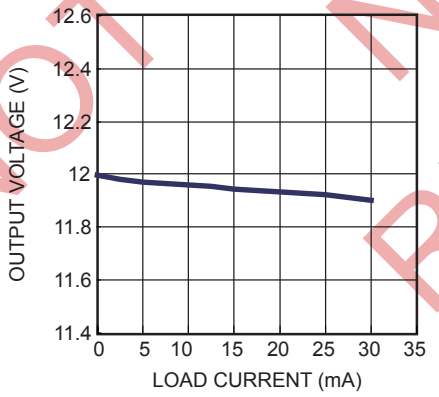
Ground Pin Current vs. Load Current



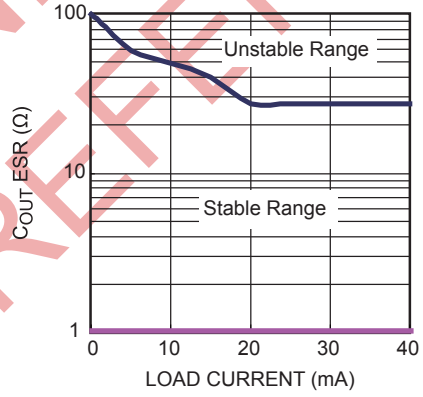
Output Voltage vs. Temperature



Output Voltage vs. Output Load

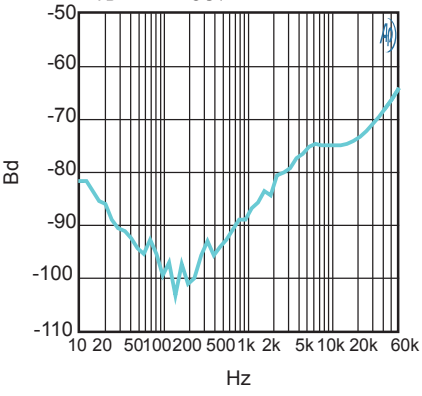


Region of Stable Cout ESR vs. Load Current



PSRR Test

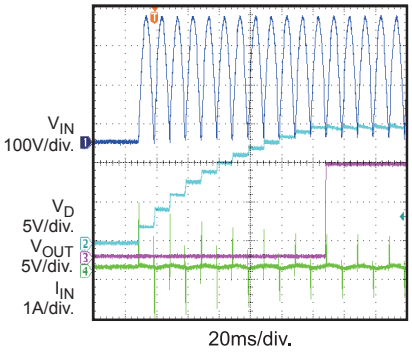
VD=20V, V_{OUT}=5V, I_{OUT}=0mA,
C_{VD}=1µF, C_{OUT}=4.7µF



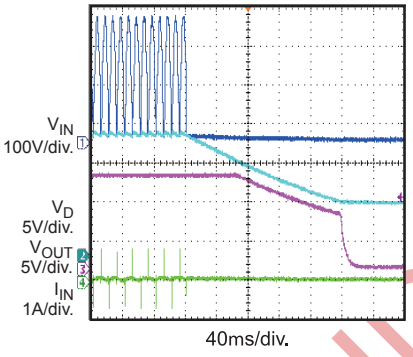
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. VIN=230VAC, VOUT=12V, I_{OUT}=10mA, C_{VD}=220μF/35V, T_A=+25°C, unless otherwise noted.

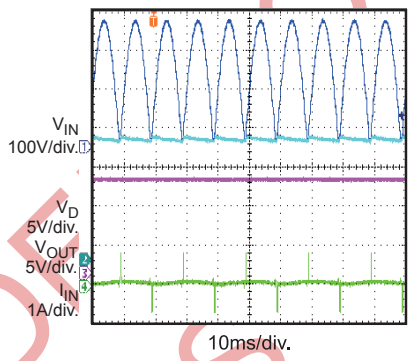
Input Power Start up



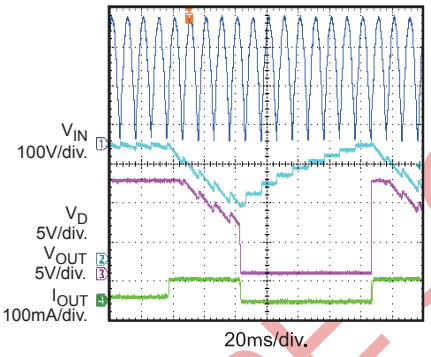
Input Power Shut down



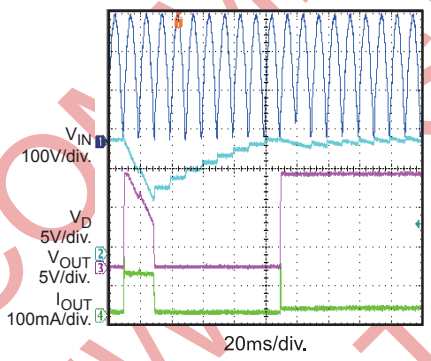
Steady State



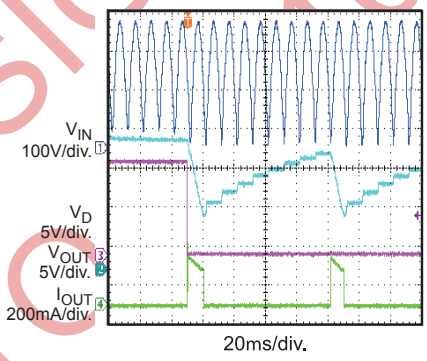
Over Current Protection Entry



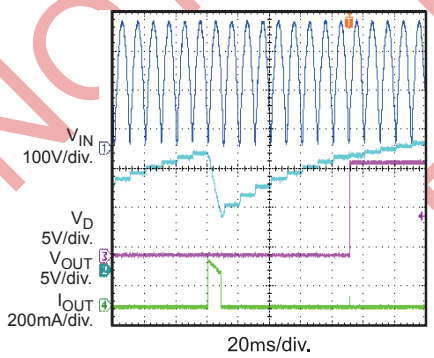
Over Current Protection Recovery



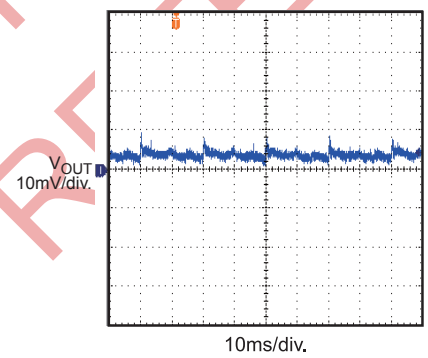
Short Circuit Protection Entry



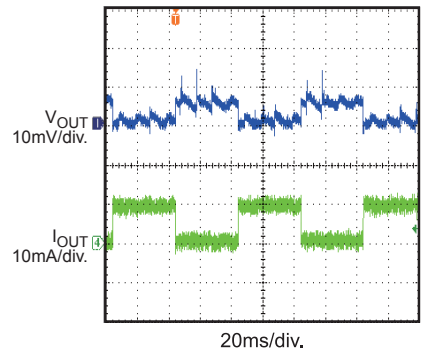
Short Circuit Protection Recovery



Output Voltage Ripple



Load Transient



PIN FUNCTIONS

Pin #	Name	Description
1	PG	Power Good. Requires an external pull-up resistor because it is an open drain. When VOUT reaches 80% of its normal output voltage, PG goes high after a 200μs delay.
2	GND	Ground.
3	FB	Output Voltage Feedback. Connect to a capacitor to VOUT to improve low dropout stability. Connect to the tap of a resistor divider to adjust the output voltage.
4	VOUT	Output Voltage.
5	VD	Energy Storage. Connect to GND with a capacitor to buffer energy for the low drop-out stage.
6	VB	Connect with VD directly.
7	NC	Not Connected.
8	VIN	Input Voltage Supply. Provides energy when the voltage falls within the charging window.
Exposed Pad		Not Connected. Connect to a large copper surface connected to GND to enhance thermal dissipation.

BLOCK DIAGRAM

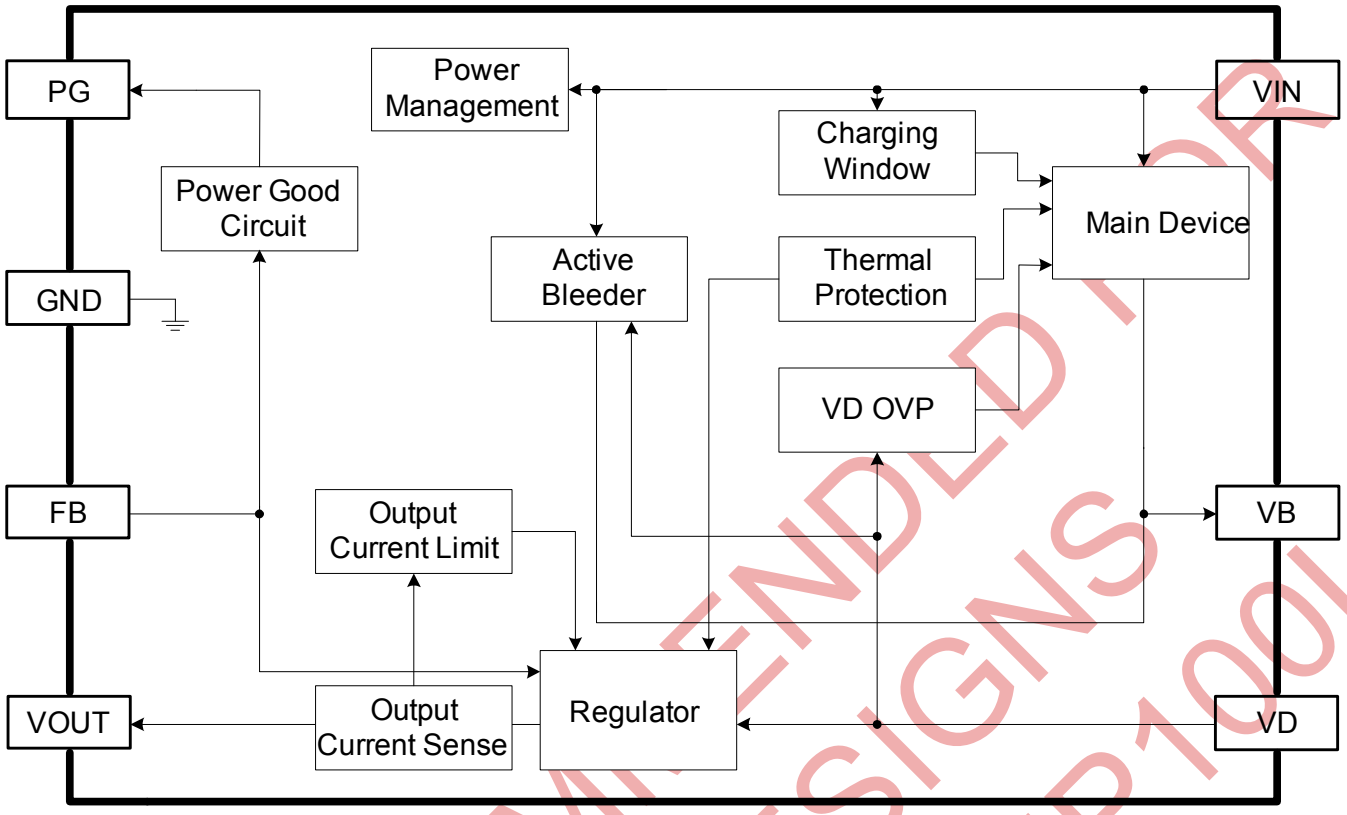


Figure 1: Functional Block Diagram

OPERATION

MP100 employs a smart inductor-less regulator design (patent pending) to charge the VD capacitor (C1 in Figure 4) from the offline AC input, and then to deliver the stored energy to the load with a stable output voltage. When VIN is less than its 35V threshold, VD can be charged up by up to 1.8A input current. An internal LDO regulates VOUT to 12V and can supply up to 10mA load when VIN is between 85VAC and 305VAC. The proprietary design allows the universal AC input to efficiently power the IC directly.

Startup

During the startup, the internal switch connected between VIN and VB turns on when the input voltage is within its charging window (typically below 35V), thus gradually charging the VD voltage. The LDO will not resume with a soft-start until the VD voltage reaches 15.3V.

Active Bleeder Circuit

The input voltage may not enter its charging window during normal operation due to parasitic capacitance from VIN to GND. An active bleeder circuit is enabled to pull down the VIN voltage whenever the VD voltage falls below 14V to guarantee that the output gets enough energy from the input ports. In addition, when the power supply shuts down, the active bleeder circuit discharges the energy stored in the parasitic capacitor to ensure that the circuit can restart easily.

VD Over-Voltage Protection

The VD capacitor provides energy for the output load. If the voltage of VD exceeds 30V, the internal switch between VIN and VB turns off immediately to prevent the VD voltage from rising too high, which can damage the LDO stage.

Short-Circuit Protection

The output current is limited to 150mA if the output is shorted to ground, which also decreases the VD voltage. When VD drops below 6.8V, LDO turns off. The input voltage then gradually charges VD up to 15.3V to enable the LDO. When LDO turns on, the output current drops the VD voltage to 6.8V again. This process will continue until the output short condition ceases.

Over-Current Protection

The VD and VOUT voltages will drop simultaneously if the output current exceeds its normal value. When the VD voltage falls to 6.8V, the second stage LDO shuts down immediately. Then the input voltage charges VD to 15.3V to enable the LDO. Due to the output current limit circuit, the maximum current is typically limited to 150mA.

Thermal Shutdown Protection

Accurate temperature protection prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the whole chip shuts down. When the temperature falls below its lower threshold of 140°C, the chip is enabled again.

Power-Good

The MP100 integrates a power-good circuit to signal that the output meets the controller IC's requirements. It is an open drain structure and requires a pull-up resistor to VOUT. During start up, the VOUT voltage rises smoothly. When it reaches 80% of its normal value, the power-good signal goes high after a 200μs delay to indicate a normal output.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set to 12V by internal large feedback resistors. Adjust VOUT by choosing appropriate external feedback resistors. The recommended output voltage is between 1.5V and 15V. If PG is used, then the maximum output voltage must be limited to 14V due to the maximum rating of PG. Defining the upper and lower feedback resistors as R_{UP} and R_{LW} respectively (refer to the picture in Typical Application section):

$$R_{UP} = R_{LW} \times (\frac{VOUT}{1.235} - 1)$$

For the external resistors to dominate over the internal resistors, select relatively small values of R_{UP} and R_{LW} compared to the internal resistors. However, to minimize the load consumption, avoid very small external resistors. For most applications, choose R_{LW}=10.2kΩ. To accurately set the output voltage, select an R_{UP} that can counter the internal upper-feedback resistor value of 1MΩ. The table below lists typical resistor values for different output voltages:

Table 1: Resistors Selecting vs. Output Voltage Setting

VOUT(V)	R_{UP}(kΩ)	R_{LW}(kΩ)
1.5	2.21(1%)	10.2(1%)
3.3	16.9(1%)	10.2(1%)
5	30.9(1%)	10.2(1%)
15	121(1%)	10.2(1%)

Selection of VD Capacitor

The bypass capacitor on the VD pin needs to be sufficiently large to provide a stable current. Calculate the capacitance (in μF) based on the following equation:

$$C_{VD} = \frac{I_{load} \times \tau_s}{V_{ripple}}$$

Where, I_{load} is the output current (mA); τ_s is based on the type of input rectifier—for example, τ_s is 20ms for a half-wave rectifier, and 10ms for a full-bridge rectifier, V_{ripple} is the voltage ripple on the VD capacitor—normally the ripple is limited to 2V to 3V. For best results, use a small ceramic capacitor and a large aluminum capacitor in parallel.

Output Power Capability

The maximum input power to the VD capacitor is limited by the fixed charging window. Considering the LDO power loss, the MP100 has a limited maximum output power.

The following factors influence the MP100's maximum output power: the input rectifier (full bridge or half-wave); the VD capacitor connected between VD and GND; the output voltage; and the MP100's temperature-rise requirement, which is relative to the different application environments.

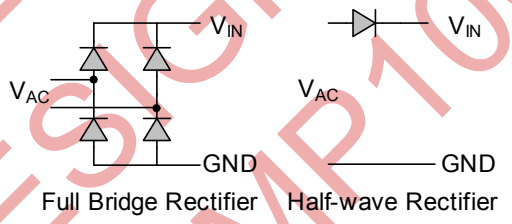


Figure 2 depicts the relationship between the maximum output power and the VIN voltage when the output voltage is 12V, 5V and 3.3V, respectively. The plots account for both full bridge and half-wave rectifiers, The temperature rise of MP100 is less than 60°C on the test board in 25°C room temperature test.

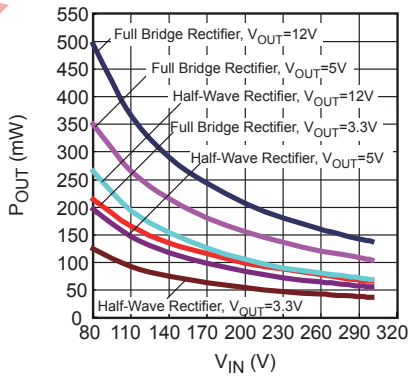


Figure 2: Output Power vs. Input Voltage

The maximum output capability can be roughly estimated by following equation:

$$P_{o\_max} = \frac{2 \times C_{VD} \times I_{peak} \times f_{line} \times (V_{THVIN} - V_{DMIN}) \times V_o}{I_{peak} + \sqrt{2} \times 2\pi \times C_{vd} \times V_{in} \times f_{line}}$$

Where,

C_{VD} (F) is the capacitance connected to VD;

I_{peak} (A) is the input peak current at full load, which can be estimated by following equation:

$$I_{peak} = 1.25 - 0.036 \times V_{DMIN};$$

f_{line} (Hz) is the rectified line frequency;

V_{THVIN} (V) is the input voltage threshold to shut down the internal switch connected between VIN and VB, typically it is 35V;

V_{DMIN} (V) is the minimum voltage of VD to maintain the output voltage, usually; it can be got by following equation:

$$V_{DMIN} = \begin{cases} V_o + 1 & \text{if } V_{DMIN} > 6.8V \\ 6.8V & \text{if } V_{DMIN} \le 6.8V \end{cases}$$

V_o (V) is the output voltage;

V_{in} (V) is the RMS value of input voltage;

To get more output power, MP100 can be paralleled. Figure 6 shows how it is implemented. More MP100 can be paralleled in the same way to get the output power need.

Another way to get more output power is using an external MOSFET to charge the capacitor connected between VD and GND. Figure 7 shows an example. To prevent the thermal damage of external MOS when VD is shorted to GND directly, PTC (Positive Temperature Coefficient) is used which should be placed as close as to the external MOS to detect the temperature. When the temperature of external MOS reaches certain value, the resistor of PTC will increase sharply to pull down the gate voltage and shut down the external MOS. To guarantee its normal start up and steady state operation, R3/R2 should be more than 4.5. At the same time, R3/R2 should not be too high to get better thermal protection; generally it should be less than 10. R1 can be used to adjust the switch speed of external MOS.

Line Transformer

MP100 can work well when connected to AC line or programmable AC source. But when using an isolation transformer or a variable transformer as source, because of the high inductance of the transformer (usually in the mH's), high voltage spikes occur when MP100 turns off the internal switch connected between VIN and VB, which may damage the IC. An X- capacitor must be installed before the rectifier to guarantee the reliability of the system.

EMI

An appropriate X-capacitor should be connected between the input ports to guarantee the circuit can meet EMI requirements. Figure 3 shows the recommended X-capacitor values to pass EMI in different applications.

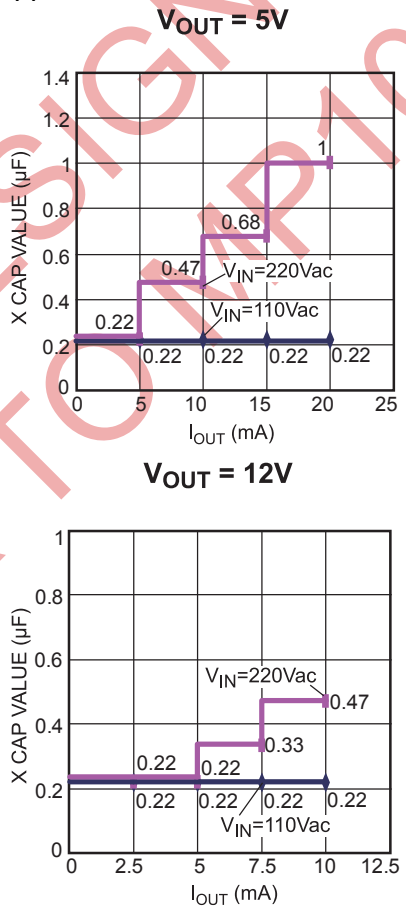


Figure 3: X Cap Value Required in Different Application

Surge

Since there is no capacitor to absorb AC line transients, MOV should be used to protect the IC to survive the transient test.

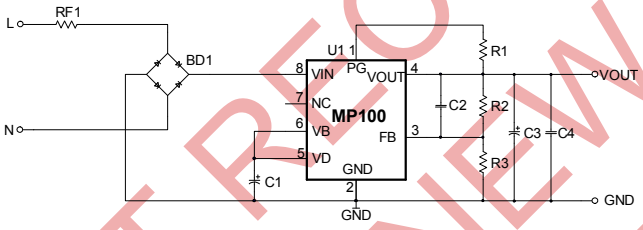
With 750V switch integrated, MP100 can pass 1kV surge test with an appropriate MOV connected between the line input ports.

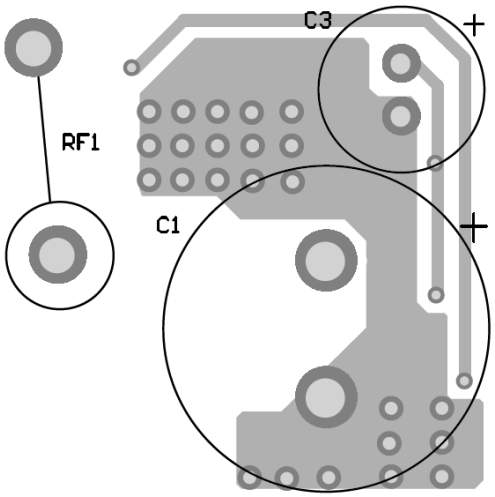
PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

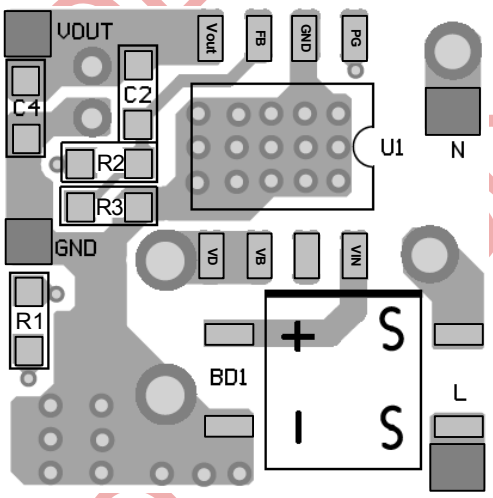
If change is necessary, please follow these guidelines and take Figure 4 for reference.

1) Minimize the loop area formed by positive output of rectifier, VIN, VB and GND.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Output capacitor should be put close to the output terminal.
4) Connect the exposed pad with GND to a large copper area to improve thermal performance and long-term reliability





Top Layer



Bottom Layer

Figure 4: PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	85V to 305V
V_{OUT}	12V
I_{OUT}	10mA

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device application, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

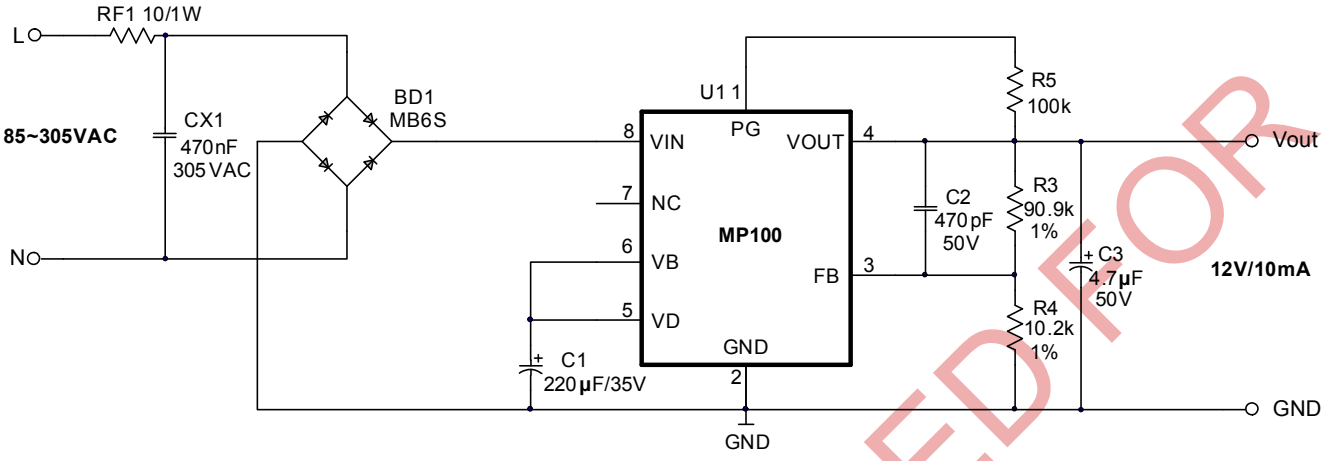


Figure 5: Typical Application

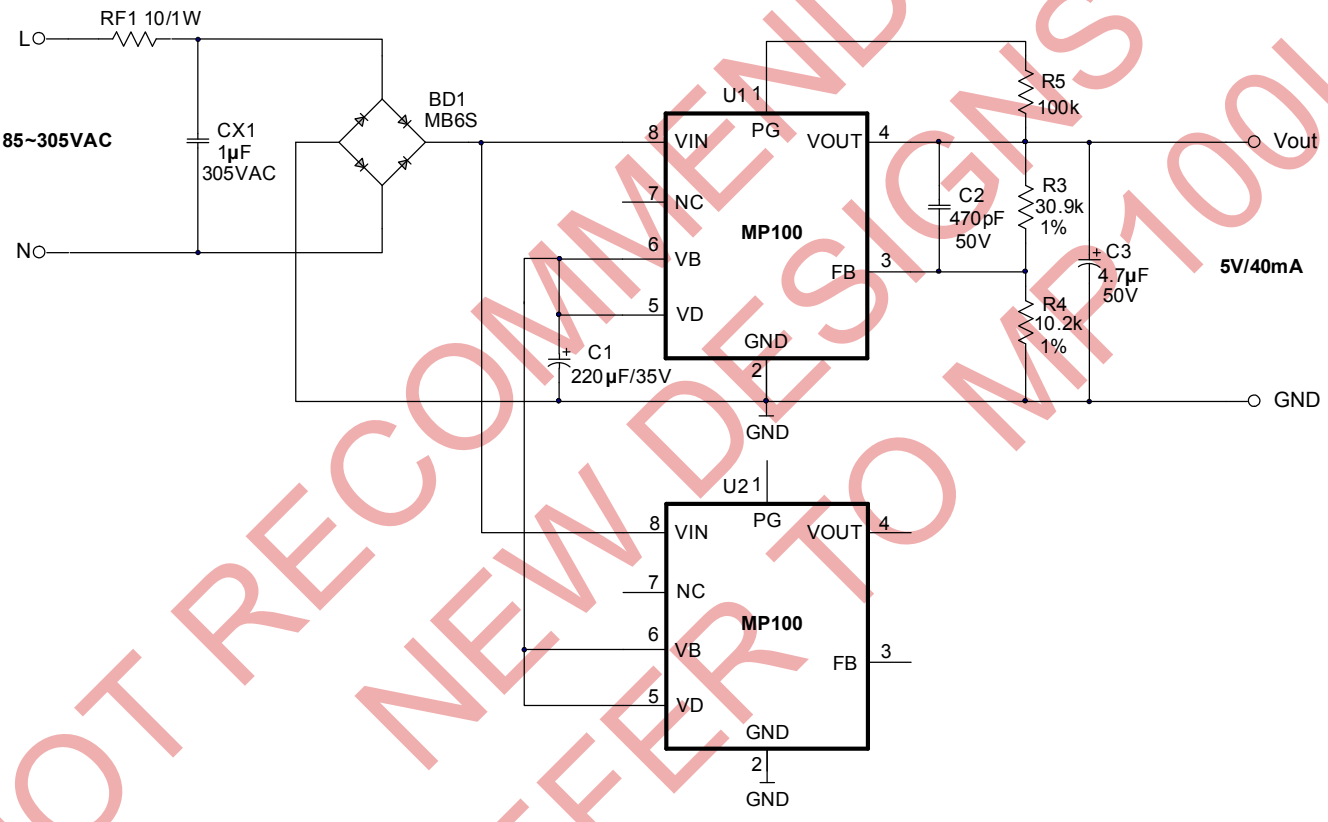


Figure 6: Paralleled Application

TYPICAL APPLICATION CIRCUITS *(continued)*

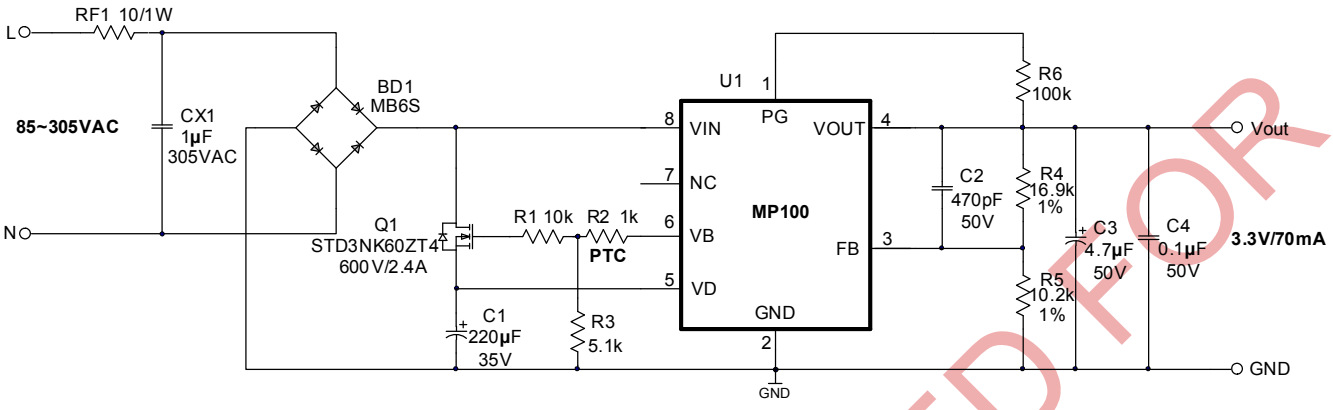
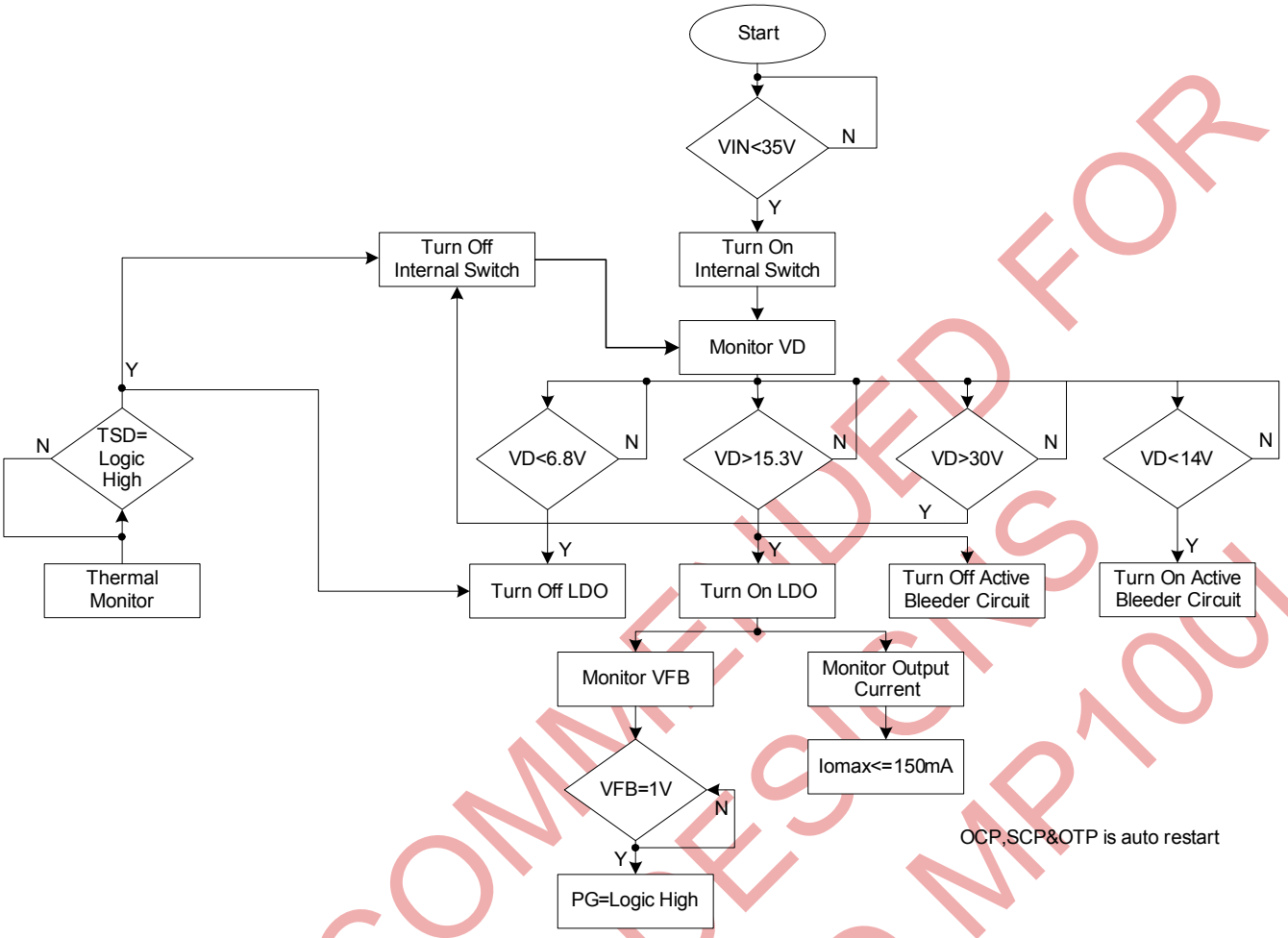
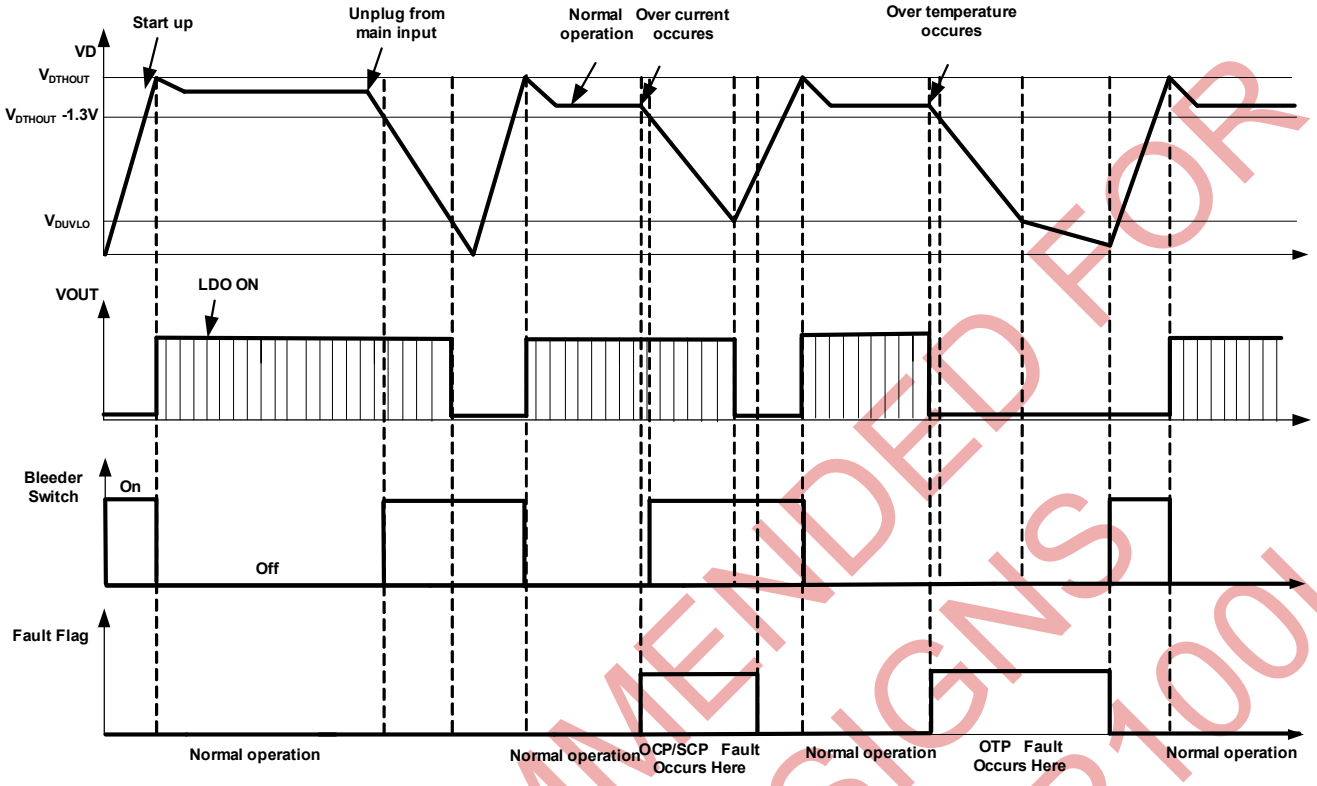


Figure 7: External MOSFET Connected Application

FLOW CHART

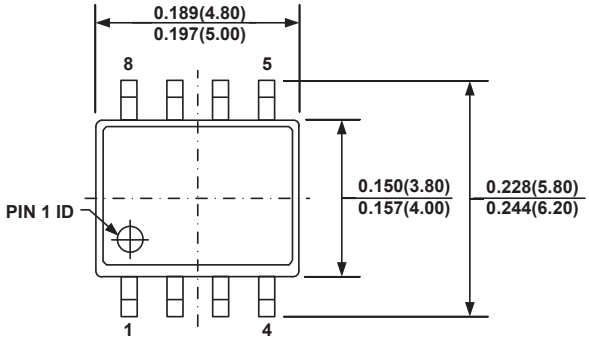


SIGNAL EVOLUTION IN THE PRESENCE OF FAULTS

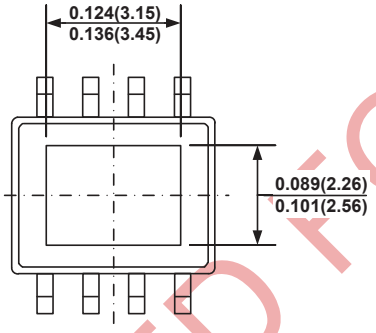


PACKAGE INFORMATION

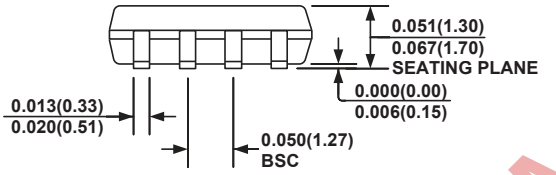
SOIC8E



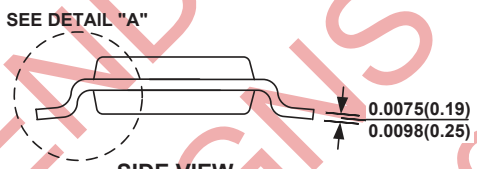
TOP VIEW



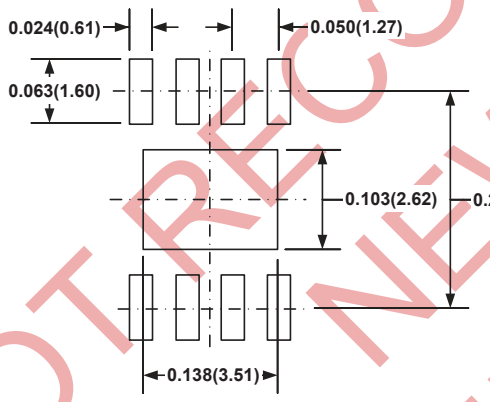
BOTTOM VIEW



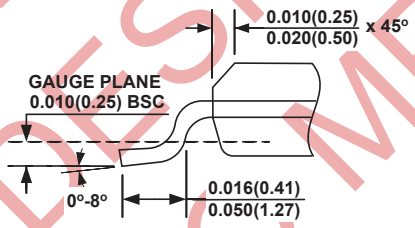
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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