HF500-7

Fixed-Frequency Flyback Regulator with Self-Supply, Multi-Mode Control and Over-Power Line Compensation

The Future of Analog IC Technology®

DESCRIPTION

The HF500-7 is a fixed-frequency, current-mode regulator with built-in slope compensation. The HF500-7 combines a 700V MOSFET and a full-featured controller into one chip for a low-power, offline, flyback, switch-mode power supply.

At medium and heavy loads, the regulator works in a fixed frequency with frequency jittering, which helps spread energy out in a conducted mode. During a light-load condition, the regulator freezes the peak current and reduces its switching frequency to $f_{OSC(min)}$ to offer excellent efficiency at light load. At very light loads, the regulator enters burst mode to achieve low standby power consumption.

Full protection features include thermal shutdown, brown-in and brown-out, VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), input and output over-voltage protection (OVP), and over-temperature protection (OTP).

The HF500-7 features timer-based fault detection and over-power compensation to ensure that the overload protection point is independent of the input voltage. The HF500-7 can also be self-supplied without any auxiliary winding to save BOM cost.

The HF500-7 is available in a SOIC8-7B package.

Maximum Output Power (1)				
Vcc external supplied	230Vac±15%		85Vac~265Vac	
	Adapter (2)	Open Frame (3)	Adapter (2)	Open Frame (3)
	6.5W	7W	6W	6.5W
Vcc self-supplied	115Vac±15%		230Vac±15%	
	5W		2W	

NOTES:

1) The junction temperature can limit the maximum output power.
2) Maximum continuous power in a non-ventilated enclosed adapter measured at 50° C ambient temperature.
3) Maximum continuous power in an open frame design at 50°C ambient temperature.

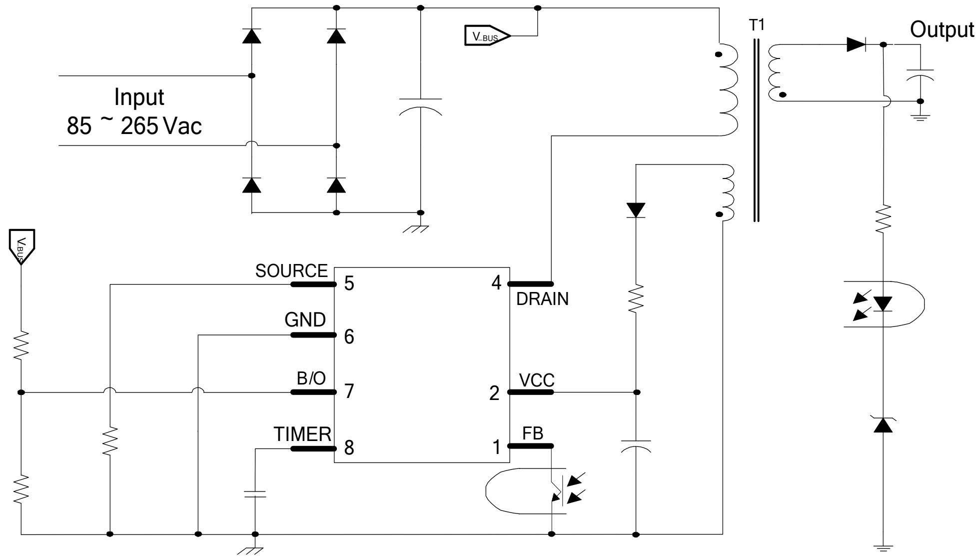
FEATURES

- 700V/12Ω Integrated MOSFET
- Fixed-Frequency Current-Mode Control Operation with Built-In Slope Compensation
- Frequency Foldback Down to $f_{OSC(min)}$ at Light Load
- Burst Mode for Low Standby Power Consumption
- Frequency Jittering for a Reduced EMI Signature
- Over-Power Compensation
- Internal High-Voltage Current Source
- Self-Supplied without Auxiliary Winding
- VCC Under-Voltage Lockout (UVLO) with Hysteresis
- Programmable Input B/O and Over-Voltage Protection (OVP)
- Overload Protection (OLP) with a Programmable Delay
- Latch-Off Protection on TIMER
- Thermal Shutdown (Auto-Restart with Hysteresis)
- Short-Circuit Protection (SCP)
- Programmable Soft Start (SS)
- Available in a SOIC8-7B Package

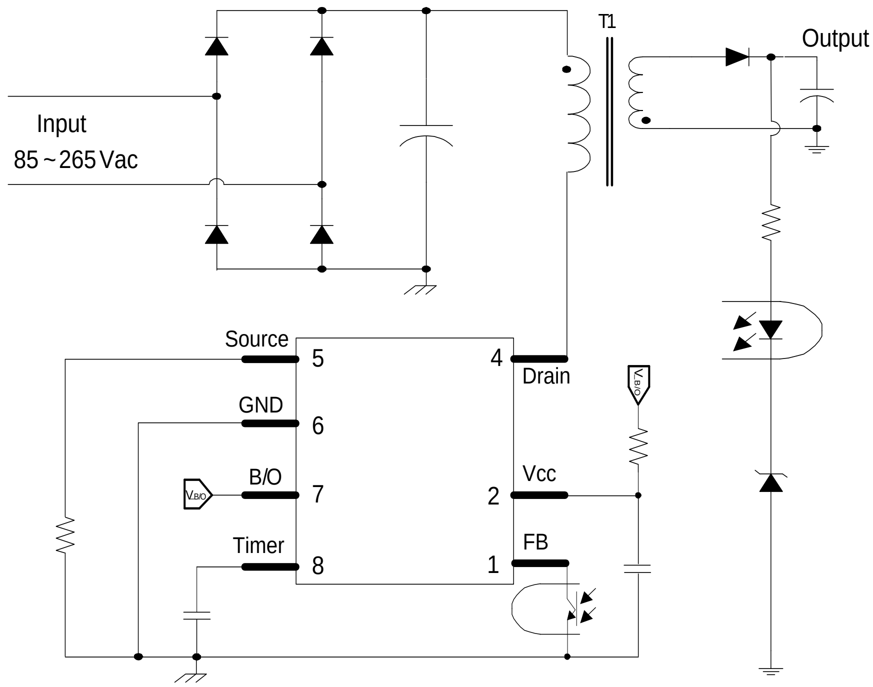
APPLICATIONS

- Power Supplies for Home Appliances
- Standby and Auxiliary Power
- Adapters

TYPICAL APPLICATION



VCC Supplied by Auxiliary Winding and Adopted Brown-In/-Out Function



VCC Self-Supplied and Disabled Brown-In/-Out Function

ORDERING INFORMATION

Part Number*	Package	Top Marking
HF500GS-7	SOIC8-7B	*See Below*

* For Tape & Reel, add suffix –Z (e.g. HF500GS-7–Z)

TOP MARKING

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 HF500-7
LLLLLLLL
  MPSYWW
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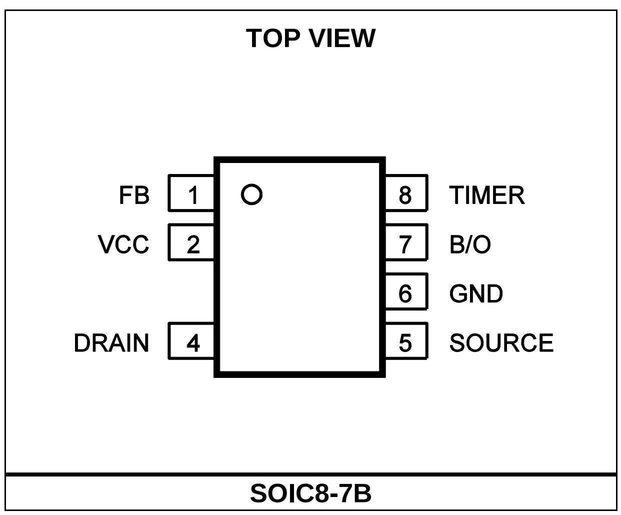
HF500-7: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS [1]

DRAIN breakdown voltage........... -0.3V to 700V
VCC to GND .... -0.3V to 30V
FB, TIMER, SOURCE, B/O to GND ....
.... -0.3V to 7V
Continuous power dissipation (T_A = +25°C) **[2]**
....1.5W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -60°C to +150°C
ESD capability human body model (all pins except DRAIN)...4.0kV
ESD capability machine model 200V

Recommended Operating Conditions [3]

Operating junction temp. (T_J) ... -40°C to +125°C
Operating VCC range .... 12.5V to 24V

Thermal Resistance [4] *θ_{JA}* *θ_{JC}*

SOIC8-7B............................. 85....... 40 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

For typical value, VCC = 16V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-Up Current Source (DRAIN)						
Supply current from DRAIN	I_{Drain_0}	VCC = 0V, V_{DRAIN} = 120V/400V	1.4	3.6	6.2	mA
	I_{Drain_11}	VCC = 11V, V_{DRAIN} = 120V/400V	1.4	5	7.8	
Leakage current from DRAIN	I_{LK}	VCC = 10V, V_{DRAIN} = 400V		4.5	10.5	μA
Breakdown voltage	V_{BR}	T_J = 25°C	700			V
Internal MOSFET (DRAIN)						
On-state resistance	R_{DS_ON}	VCC = 10.5V, I_D = 0.1A, T_J = 25°C		12	15.5	Ω
Supply Voltage Management (VCC)						
VCC level (increasing) where the internal regulator stops	VCC_{OFF}		11	12	13	V
VCC level (decreasing) where the IC shuts down and the internal regulator turns on	VCC_{UVLO}		6	7	8	V
VCC level (decreasing) where the internal regulator turns on	VCC_{ON}		10.4	11.5	12.6	V
VCC regulator on and off hysteresis	V_{HYS}		400	500		mV
VCC UVLO hysteresis	VCC_{OFF} - VCC_{UVLO}		4	4.8		V
VCC recharge level when protection occurs	VCC_{PRO}		4.7	5.3	5.9	V
VCC decreasing level where the latch-off phase ends	VCC_{LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 3V, VCC = 12V		0.9	1.2	mA
Internal IC consumption, latch-off phase	$I_{CCLATCH}$	VCC = 12V, T_J = 25°C		700	900	μA
Voltage on VCC (upper limit) where the regulator latches off (OVP)	V_{OVP}		25	27	29	V
Blanking duration on the OVP comparator	T_{OVP}			60		ms
Oscillator						
Oscillator frequency	f_{OSC}	V_{FB} > 1.85V, T_J = 25°C	62	65	68	kHz
Frequency jittering amplitude in percentage of f_{OSC}	A_{jitter}	V_{FB} > 1.85V, T_J = 25°C	±5	±6.5	±8	%
Frequency jittering entry level	V_{FB_JITTER}				1.95	V
Frequency jittering modulation period	T_{jitter}	C_{TIMER} = 47nF		3.7		ms

ELECTRICAL CHARACTERISTICS (5) *(continued)*

For typical value, VCC = 16V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Protections (B/O)						
Brown-in threshold voltage on B/O	V_{B/O_IN}	$V_{B/O}$ increasing	0.95	1	1.05	V
Brownout threshold voltage on B/O	V_{B/O_OUT}	$V_{B/O}$ decreasing	0.85	0.9	0.95	V
Brown-in/-out hysteresis	$\Delta V_{B/O}$		0.065	0.1	0.14	V
Timer duration for line cycle dropout	$T_{B/O}$	C_{TIMER} = 47nF	34	55		ms
Input OVP threshold on B/O	$OVP_{B/O}$		4.2	4.5	4.8	V
Input OVP delay time	$T_{OVPB/O}$			90		µs
Voltage on B/O to disable B/O and input OVP function	V_{DIS}		5.4	6	6.6	V
Clamp voltage on B/O	V_{B/O_Cla}		7			V
Input impedance	$R_{B/O}$		1.2			MΩ
Current Sense (SOURCE)						
Current-limit point	V_{ILIM}		0.93	1	1.07	V
Short-circuit protection point	V_{SCP}		1.3	1.5	1.7	V
Current limitation during frequency foldback	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limitation when entering burst	V_{IBURL}	V_{FB} = 0.7V		0.18		V
Current limitation when exiting burst	V_{IBURH}	V_{FB} = 0.8V		0.23		V
Leading-edge blanking for V_{ILIM}	T_{LEB1}			350		ns
Leading-edge blanking for V_{SCP}	T_{LEB2}			270		ns
Slope of the compensation ramp	S_{RAMP}		18	25	31	mV/µs
Feedback (FB)						
Internal pull-up resistor	R_{FB}	T_J = 25°C	12	13.5	15	kΩ
Internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current-set point division ratio	K_{FB1}	V_{FB} = 2V	2.5	2.8	3.1	
V_{FB} to current-set point division ratio	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	
FB level (decreasing) where the regulator enters burst mode	V_{BURL}		0.63	0.7	0.77	V
FB level (increasing) where the regulator exits burst mode	V_{BURH}		0.72	0.8	0.88	V
Overload Protection (FB)						
FB level where the regulator enters OLP after a dedicated time	V_{OLP}			3.7		V
Time duration before OLP when FB reaches the protection point	T_{OLP}	C_{TIMER} = 47nF	32			ms

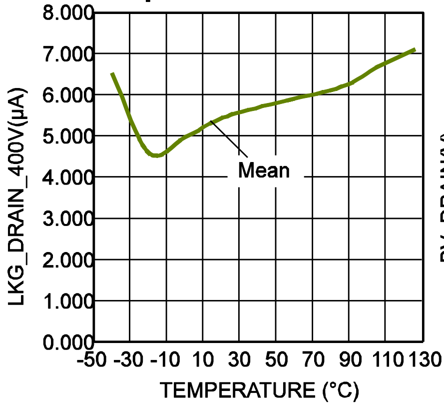
ELECTRICAL CHARACTERISTICS (5) *(continued)*

For typical value, VCC = 16V, T_J = -40°C to 125°C, unless otherwise noted.

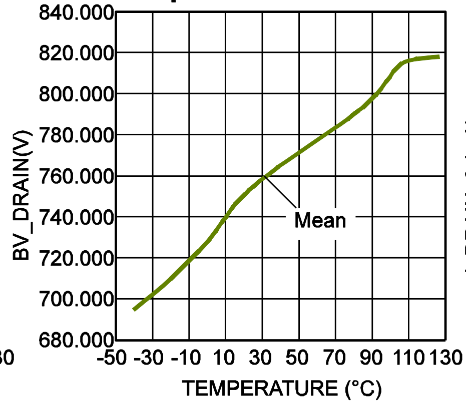
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Over-Power Compensation (B/O)						
Compensation voltage	V_{OPC}	$V_{B/O}$ = 1.1V, V_{FB} = 2.5V, T_J = 25°C		0		mV
		$V_{B/O}$ = 1.3V, V_{FB} = 2.5V, T_J = 25°C		19		
		$V_{B/O}$ = 2.9V, V_{FB} = 2.5V, T_J = 25°C	153	200	247	
		$V_{B/O}$ = 3.5V, V_{FB} = 2.5V, T_J = 25°C	205	270	335	
		$V_{B/O}$ > V_{DIS}, T_J = 25°C		0		
FB voltage (lower limit) when compensation is removed	$V_{OPC(OFF)}$		0.55			V
FB voltage (upper limit) when compensation is fully applied	$V_{OPC(ON)}$				2.5	V
Frequency Foldback						
FB voltage (lower threshold) when frequency foldback starts	$V_{FB(FOLD)}$			1.8		V
Minimum switching frequency	$f_{OSC(min)}$	T_J = 25°C	20.5	25	30	kHz
FB voltage (lower threshold) when frequency foldback ends	$V_{FB(FOLDE)}$			1		V
Latch-Off Input (Integration in TIMER)						
Lower threshold when the regulator is latched	$V_{TIMER(LATCH)}$		0.7	1	1.2	V
Blanking duration on latch detection	T_{LATCH}			42		µs
Thermal Shutdown						
Thermal shutdown threshold	T_{TSD}			150		°C
Thermal shutdown hysteresis	$T_{TSD(HYS)}$			25		°C

TYPICAL CHARACTERISTICS

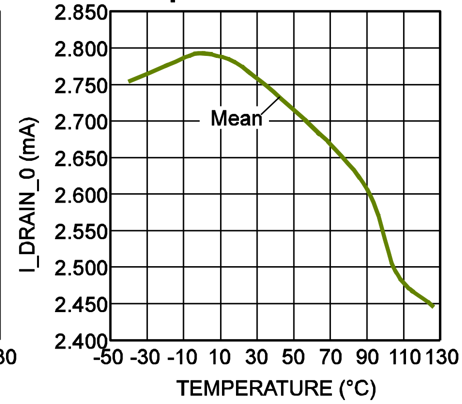
LKG_Drain_400V vs. Temperature Chart



BV_Drain vs. Temperature Chart

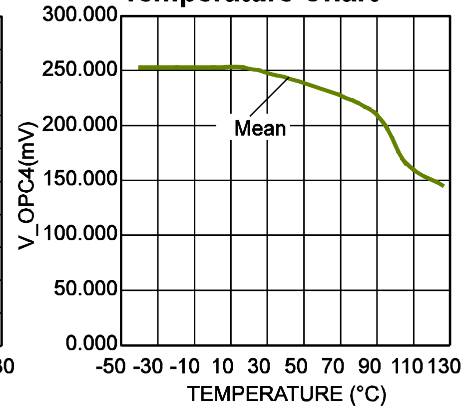


I_DRAIN_0 vs. Temperature Chart

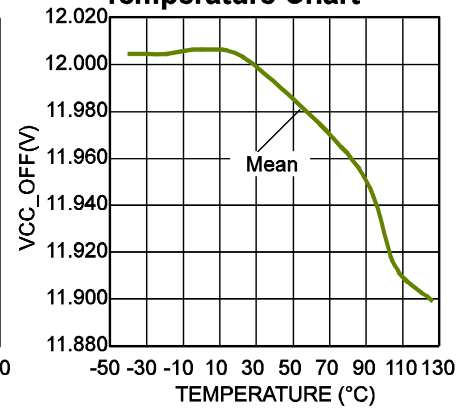


I_DRAIN_11 vs. Temperature Chart

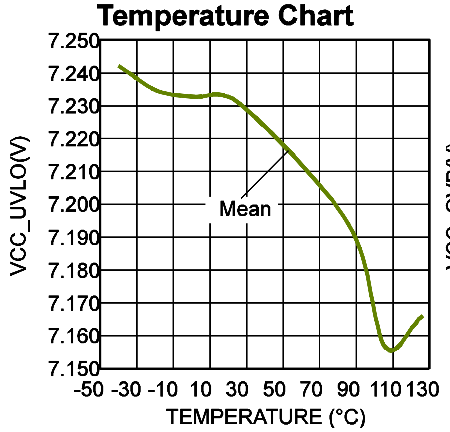
V_OPC4 vs. Temperature Chart



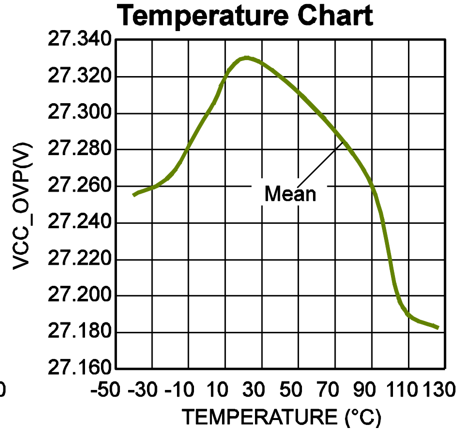
VCC_OFF vs. Temperature Chart



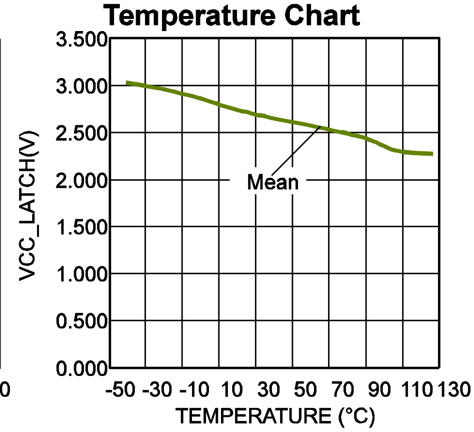
VCC_UVLO vs. Temperature Chart



VCC_OVP vs. Temperature Chart

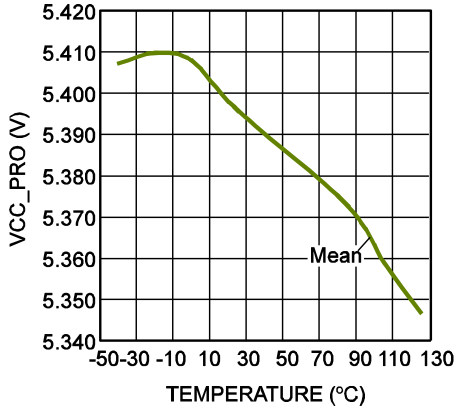


VCC_Latch vs. Temperature Chart

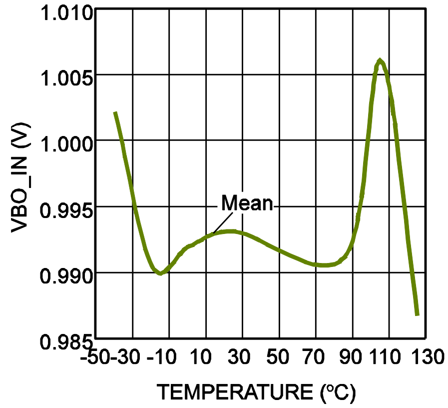


TYPICAL CHARACTERISTICS *(continued)*

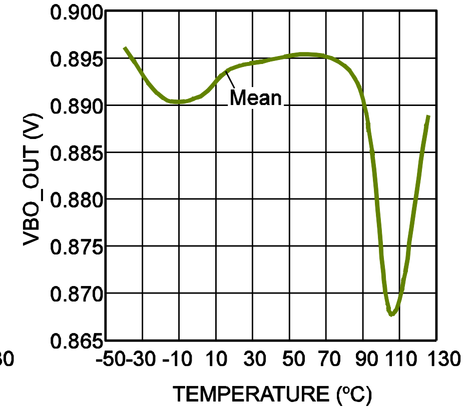
VCC_PRO vs. Temperature



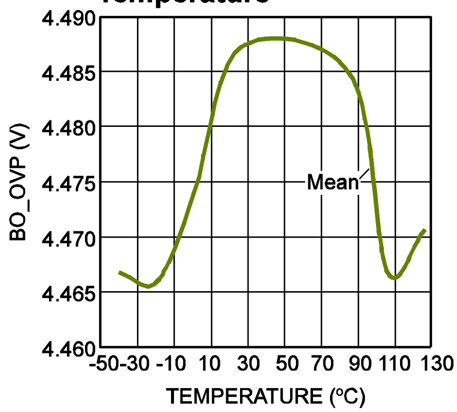
VBO_IN vs. Temperature



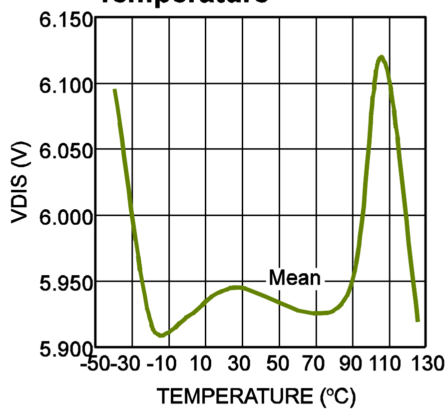
VBO_OUT vs. Temperature



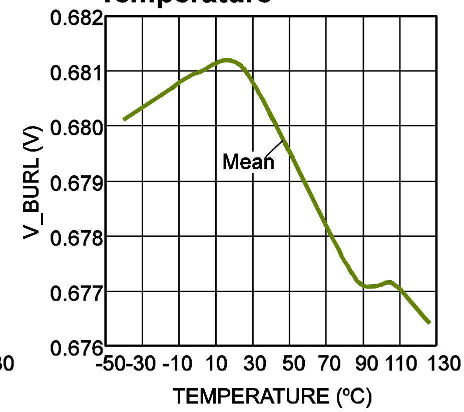
BO_OVP vs. Temperature



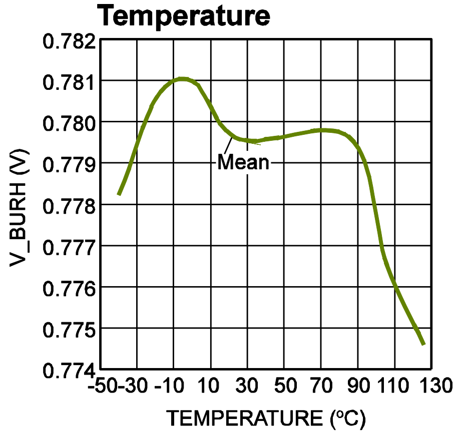
VDIS vs. Temperature



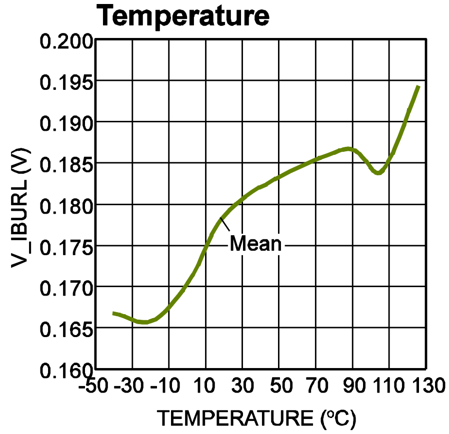
V_BURL vs. Temperature



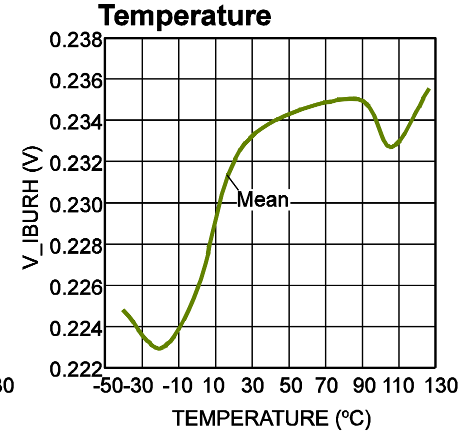
V_BURH vs. Temperature



V_IBURL vs. Temperature

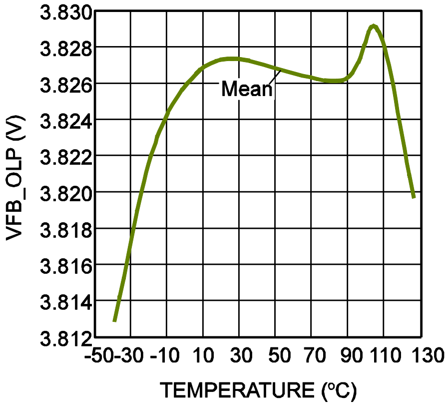


V_IBURH vs. Temperature

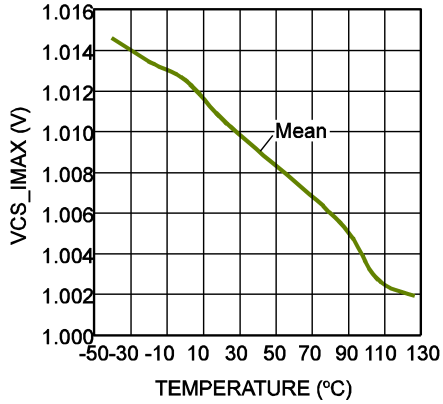


TYPICAL CHARACTERISTICS *(continued)*

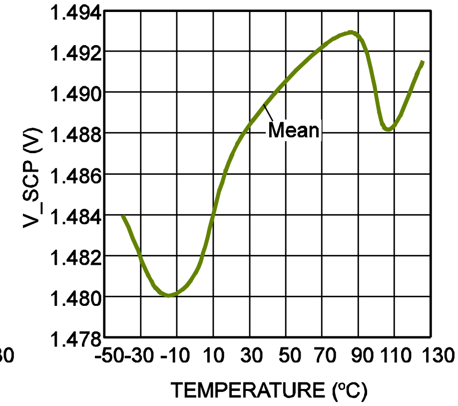
VFB_OLP vs. Temperature



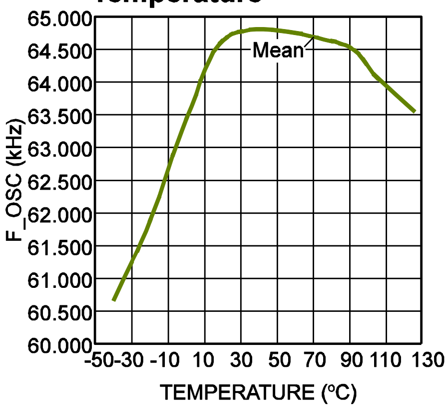
VCS_MAX vs. Temperature



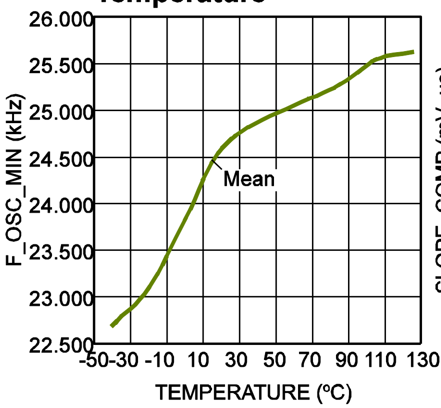
V_SCP vs. Temperature



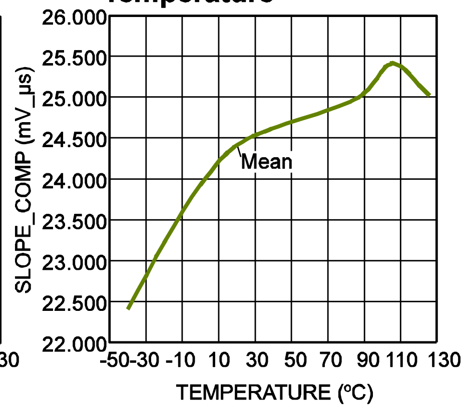
F_OSC vs. Temperature



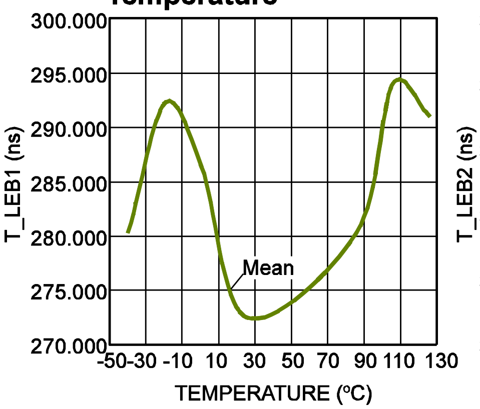
F_OSC_MIN vs. Temperature



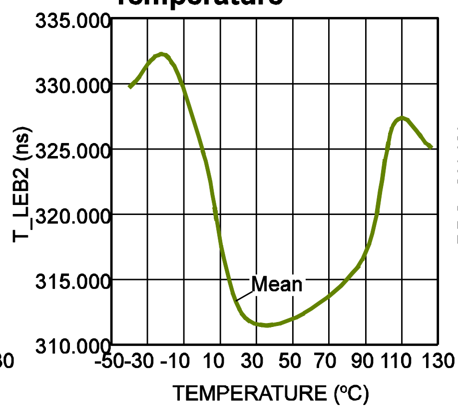
Slope_Comp vs. Temperature



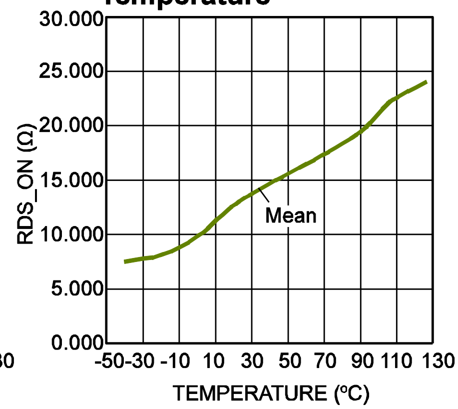
T_LEB1 vs. Temperature



T_LEB2_LOW vs. Temperature



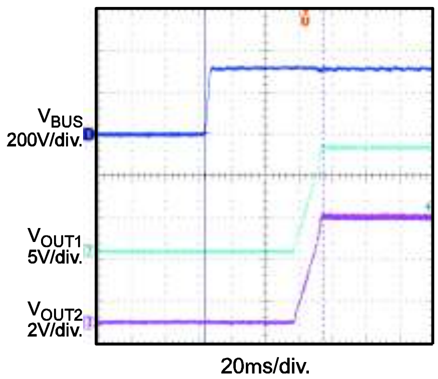
RDS_ON vs. Temperature



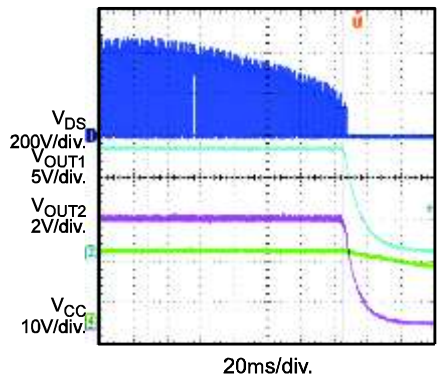
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 230V_{AC}, V_{OUT1}/V_{OUT2} = 12V/5V, I_{OUT1}/I_{OUT2} = 0.3A/0.3A, unless otherwise noted.

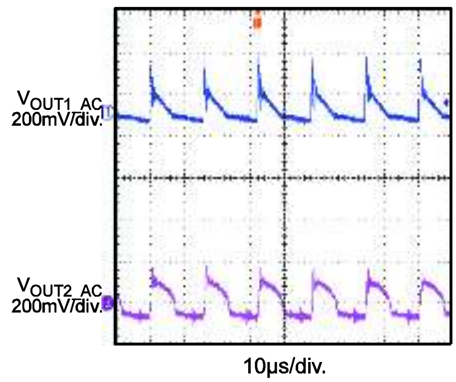
Input Power On



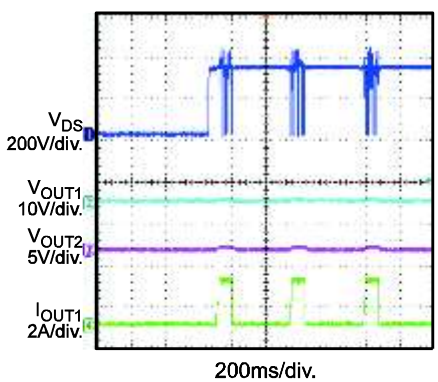
Input Power Off



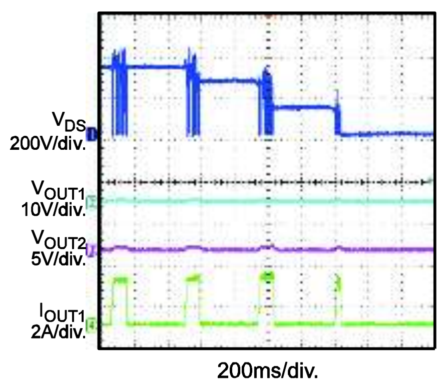
Output Ripple



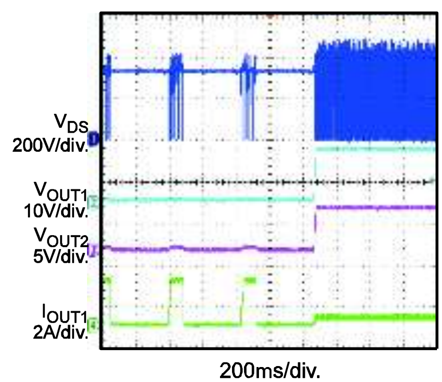
SCP Power On



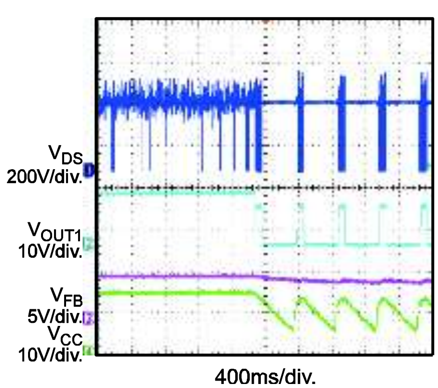
SCP Power Off



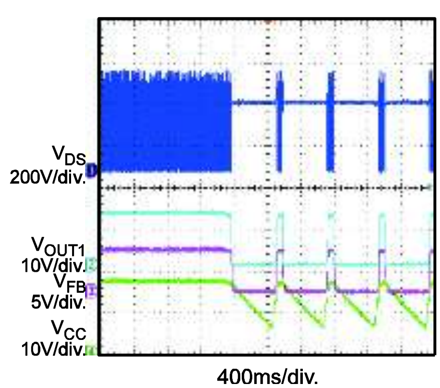
SCP Release



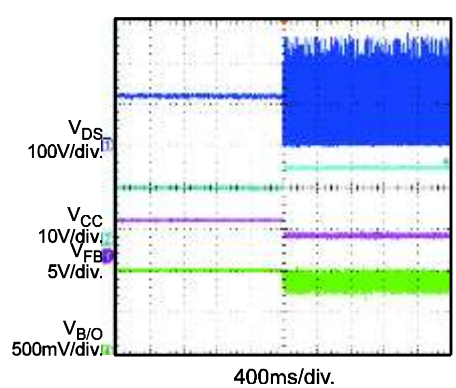
OLP Entry, No Load



OLP Entry, Full Load



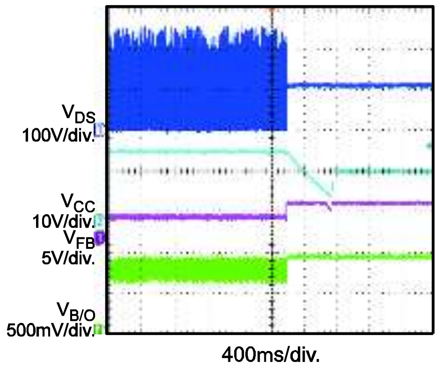
Brown In, Full Load



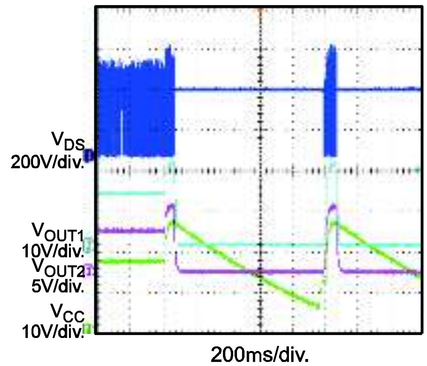
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 230V_{AC}, V_{OUT1}/V_{OUT2} = 12V/5V, I_{OUT1}/I_{OUT2} = 0.3A/0.3A, unless otherwise noted.

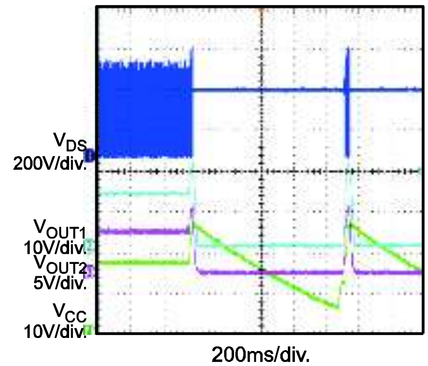
Brown Out, Full Load



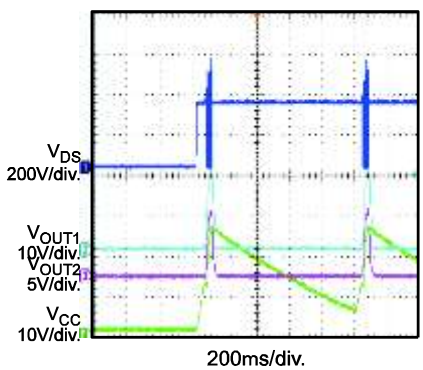
OVP Entry, No Load



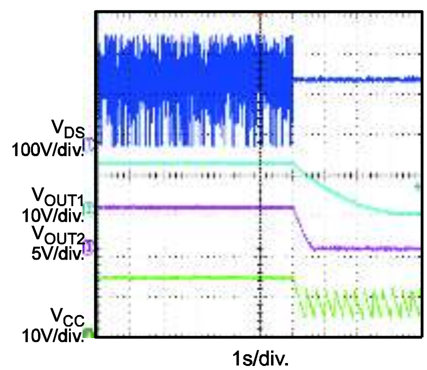
OVP Reccovery, No Load



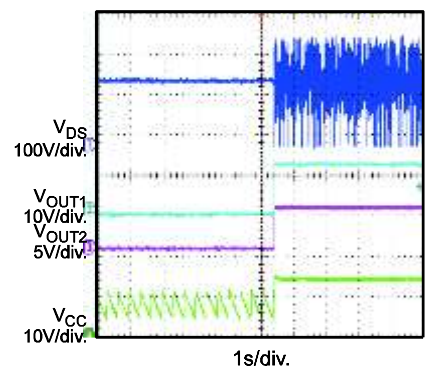
OVP Power On, No Load



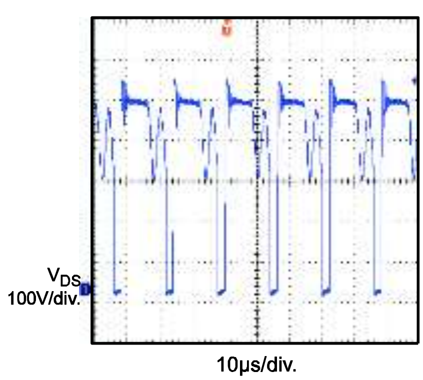
OTP Entry



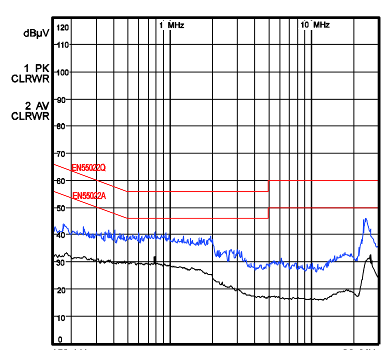
OTP Recovery



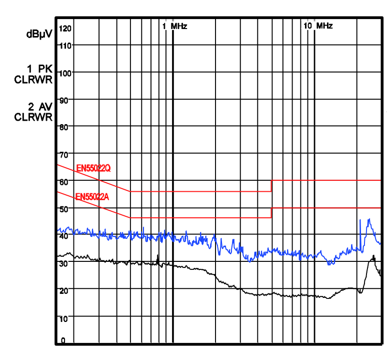
Stress



Conducted EMI, L



Conducted EMI, N



PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback.** A pull-down optocoupler controls the output regulation.
2	VCC	**Power supply of the IC.** VCC enters over-voltage protection (OVP) if the VCC voltage rises above V_{OVP}.
4	DRAIN	**Drain of the internal MOSFET.** DRAIN is the input for the start-up, high-voltage current source.
5	SOURCE	**Source of the internal MOSFET.** SOURCE is the input of the primary current-sense signal.
6	GND	**Ground.**
7	B/O	**Brown-in/-out, input OVP, and over-power compensation detection.** Brown-in/-out, input OVP, and over-power compensation are achieved by detecting the voltage on B/O. All functions are disabled when B/O is pulled higher than V_{DIS}.
8	TIMER	**Combined soft start, frequency jittering, and timer functions for overload protection (OLP) and brown-out protection.** The IC is latched by pulling TIMER down. TIMER allows for external OVP and over-temperature protection (OTP) detection.

BLOCK DIAGRAM

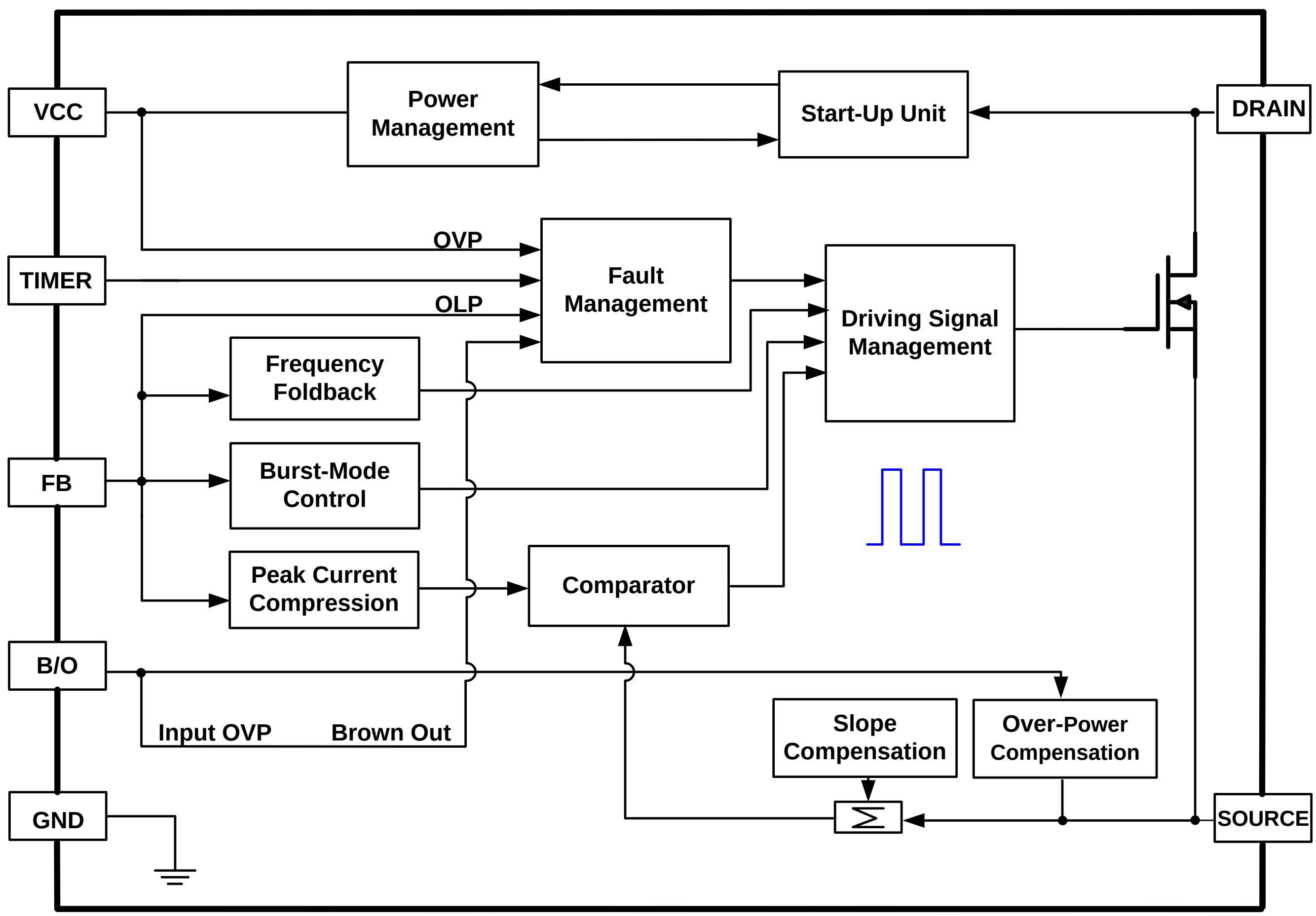


Figure 1: Functional Block Diagram

OPERATION

The HF500-7 is a fixed-frequency, current-mode regulator with built-in slope compensation that incorporates all of the necessary features to build a reliable switch-mode power supply. In light-load conditions, the regulator freezes the peak current and reduces its switching frequency to 25kHz to minimize switching loss. When the output power falls below a given level, the regulator enters burst mode. The HF500-7 uses frequency jittering to improve EMI performance.

Fixed Frequency with Jittering

Frequency jittering reduces EMI by spreading out the energy (see Figure 2).

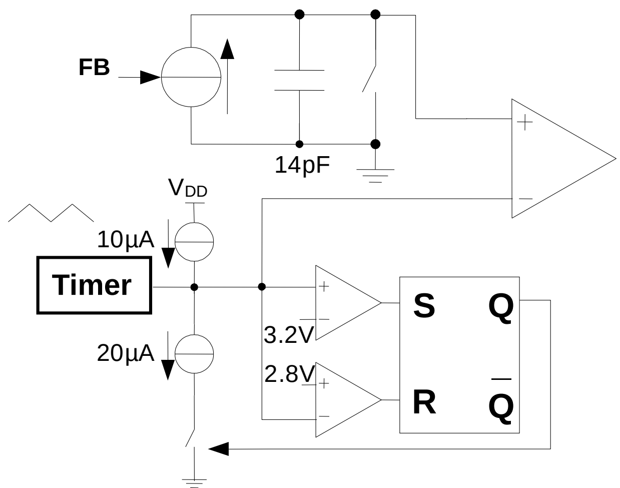


Figure 2: Frequency Jitter Circuit

An internal capacitor is charged with a controlled current source, which is fixed when FB is greater than 2V, and its voltage is compared with the TIMER voltage (V_{TIMER}). V_{TIMER} is a triangular wave between 2.8V and 3.2V with a charging/discharging current (see Figure 3). The switching frequency can be calculated using Equation (1):

$$f_s = \frac{1 \cdot 10^6}{5.28 \cdot V_{TIMER} / V + 0.2} Hz \qquad (1)$$

T_{jitter} can be calculated using Equation (2):

$$T_{jitter} = 8 \cdot C_{TIMER} / nF \cdot 10^{-5} s \qquad (2)$$

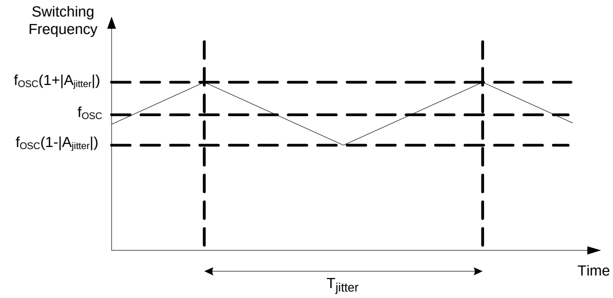


Figure 3: Frequency Jittering

Frequency Foldback

To achieve high efficiency during all load conditions, the HF500-7 implements frequency foldback during light-load conditions.

When the load decreases to a given level, the regulator freezes the V_{FOLD} peak current and reduces the charging current, dropping its switching frequency down to 25kHz and reducing switching loss. If the load continues to decrease, the peak current decreases with a 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency and peak current vs. FB.

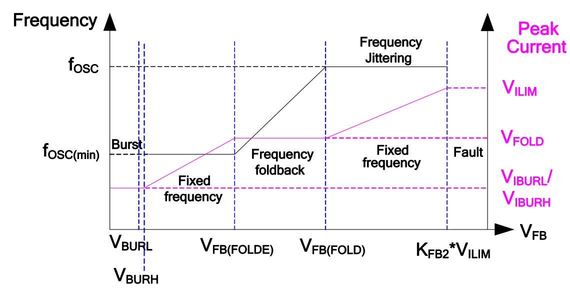


Figure 4: Frequency and Peak Current vs. FB

Current-Mode Operation with Slope Compensation

The primary peak current is controlled by the FB voltage (V_{FB}). When the peak current reaches the level determined by FB, the MOSFET turns off. The regulator can also operate in continuous conduction mode (CCM) with a wide input voltage range. Its internal synchronous slope compensation (S_{RAMP}) helps avoid subharmonic oscillation when the duty cycle is larger than 50% at CCM.

High-Voltage Start-Up Current Source

Initially, the IC is self supplied by the internal high-voltage current source, which is drawn from DRAIN. The IC turns off the current source once VCC reaches VCC_{OFF}. If VCC falls below VCC_{ON}, the high-voltage current source turns on again.

The lower threshold of VCC is pulled down from VCC_{UVLO} to VCC_{PRO} when a fault condition occurs, such as overload protection (OLP), short-circuit protection (SCP), brown-out, over-voltage protection (OVP), and over-temperature protection (OTP), etc.

Self-Power Supply

The IC can be self-supplied by the internal high-voltage current source. The IC starts switching and the internal high-voltage current source turns off once the VCC voltage reaches VCC_{OFF} (typically 12V). Then the VCC voltage decreases. The internal high-voltage current source turns on again to charge the external VCC capacitor when the VCC voltage decreases below VCC_{ON} (typically 11.5V) (see Figure 5). A small capacitor (several μF) is enough to hold the VCC voltage. The self-supply function can lower the total BOM cost by removing auxiliary winding and decreasing the capacitance of the VCC capacitor.

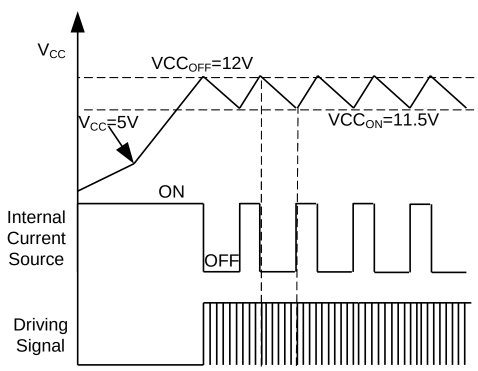


Figure 5: Self-Power Supply

Self-power supply leads to higher no-load power consumption. If tough no-load power consumption performance is required, the self-supply function should be disabled.

Soft Start (SS)

To reduce the stress on the power components and smoothly establish the output voltage, the TIMER voltage increases from 1V to 1.75V with a 1/4 charge current during normal operation during every start-up. The TIMER voltage increases the peak current from 0.25V to 1V gradually. The switching frequency also increases gradually. Figure 6 shows the typical waveform of a soft start.

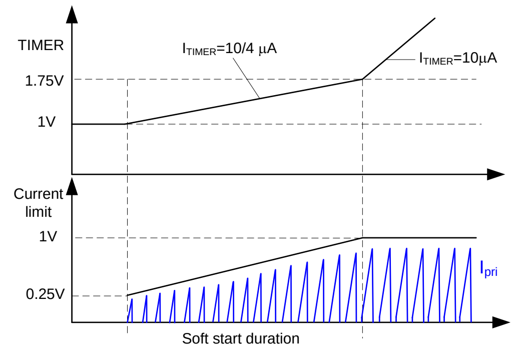


Figure 6: Soft Start

The start-up duration can be adjusted by the capacitor connected to TIMER. The TIMER capacitor determines the start-up duration, shown in Equation (3):

$$T_{Soft-start} = 0.3 \cdot C_{TIMER} / nF \cdot 10^{-3} s \qquad (3)$$

Burst Operation

The HF500-7 uses burst-mode operation to minimize the power dissipation in no-load or light-load conditions. As the load decreases, V_{FB} decreases. The IC stops the switching cycle when V_{FB} drops below the lower threshold (V_{BURL}). V_{FB} increases again once the output voltage drops, and switching resumes once V_{FB} exceeds the threshold (V_{BURH}). V_{FB} then falls and rises repeatedly. Burst-mode operation alternately enables and disables the switching cycle of the MOSFET, thereby reducing switching loss at no-load or light-load conditions.

Over-Power Compensation (OPC)

An offset voltage proportional to the B/O voltage is added to the sensing voltage. The B/O voltage is proportional to the input voltage. Figure 7 shows the compensation in relation to the voltage on FB and B/O. The over-power compensation (OPC) voltage (V_{OPC}) can be calculated using Equation (4):

$$V_{OPC} = 0.094 \cdot (V_{B/O} - 1.1V) \qquad (4)$$

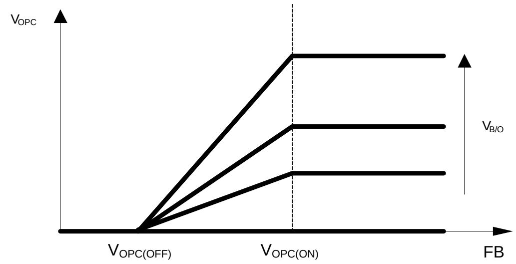


Figure 7: Compensation Current vs. FB and B/O Voltage

Timer-Based Overload Protection (OLP)

If the switching frequency is fixed in a flyback converter, the maximum output power is limited by the peak current. When the output consumes more than the limited power, the output voltage drops below the set value. The current flowing through the primary and secondary optocoupler is reduced, and V_{FB} is pulled high (see Figure 8).

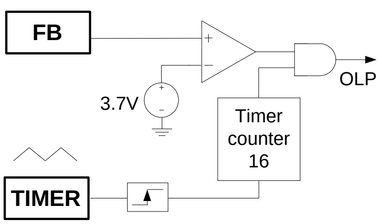


Figure 8: Overload Protection Block

FB rising higher than V_{OLP} is considered to be an error flag and causes the timer to start counting the rising edge of V_Q. When the error flag is removed, the timer resets. When the timer completes after it has counted to 16, the HR500-7 enters OLP. This timer duration does not trigger the OLP function when the power supply is starting up or during a load transition phase (see Figure 9).

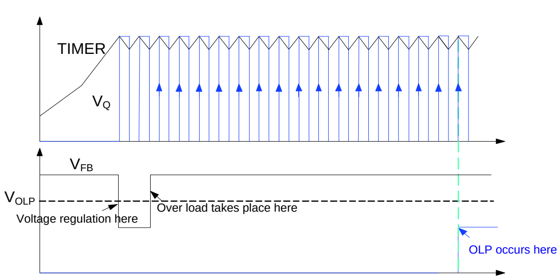


Figure 9: Overload Protection Function

Input Brown-Out and Input OVP

The input brown-out and input OVP are performed by B/O. If the B/O voltage is higher than V_{B/O_IN} during the input voltage rising period, the IC begins operating. If the B/O voltage is lower than V_{B/O_OUT} for $T_{B/O}$ (C_{TIMER} = 47nF), the IC stops operation. If the voltage on B/O is higher than $OVP_{B/O}$ for $T_{OVPB/O}$, the IC stops operating, achieving input OVP. If the voltage on B/O is higher than V_{DIS}, input brown-out and input OVP are disabled. To simplify the external circuit, connect B/O to VCC through a resistor if input brown-out, over-power compensation, and input OVP are not needed.

Short-Circuit Protection (SCP)

The HF500-7 features a short-circuit protection (SCP) that senses the SOURCE voltage and stops switching if V_{SOURCE} reaches V_{SCP} after a reduced leading-edge blanking time (T_{LEB2}). Once the fault disappears, the power supply resumes operation.

Thermal Shutdown

The HF500-7 uses thermal shutdown to turn off the switching cycle when the inner temperature exceeds T_{OTP}. Once the inner temperature drops below $T_{OTP(HYS)}$, the power supply resumes operation. During thermal shutdown, the VCC UVLO lower threshold is pulled down from VCC_{UVLO} to VCC_{PRO}.

V_{CC} Over-Voltage Protection (OVP)

The HF500-7 enters a latched fault condition if the VCC voltage rises above V_{OVP} for T_{OVP}. The regulator remains fully latched until VCC drops below VCC_{LATCH}, such as when the power supply is unplugged from the main input and plugged back in. Usually, this situation occurs when the optocoupler fails, resulting in the loss of the output voltage regulation.

TIMER Protection

The HF500-7 is latched off by pulling TIMER below $V_{TIMER(LATCH)}$ for T_{LATCH}. This allows TIMER to be used for external OVP and OTP functions by adding an external compact circuit.

Leading-Edge Blanking (LEB)

An internal leading-edge blanking (LEB) unit containing two LEB times is placed between SOURCE and the current comparator input to avoid premature switching pulse termination due to parasitic capacitances. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET (see Figure 10).

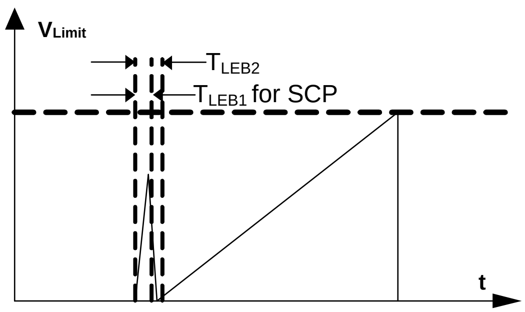


Figure 10: Leading-Edge Blanking

APPLICATION INFORMATION

VCC Capacitor Selection

When the input voltage is supplied, the VCC capacitor is charged up by the IC internal high-voltage current source. Due to the self-supply function, the start-up period is not affected by the VCC capacitor selection. The main concern is that the self-supply function should always be disabled during burst mode if VCC is supplied by the auxiliary winding. The value for the VCC capacitor can be estimated with Equation (5):

$$C_{VCC} > \frac{I_{CC} * T_{burst}}{VCC_{OFF} - VCC_{ON}} \quad (5)$$

Where I_{CC} is the internal consumption, and T_{burst} is the interval during the burst period.

Primary-Side Inductor Design (L_m)

The HF500-7 uses an internal slope compensation to support CCM when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude vs. the peak current value to $0 < K_P \leq 1$, where $K_P = 1$ for discontinuous conduction mode (DCM) (see Figure 11). A larger inductor leads to a smaller K_P, which reduces the RMS current but increases transformer size. An optimal K_P value is between 0.7 and 0.8 for the universal input range and under CrCM or under DCM for the 230V_{AC} input range.

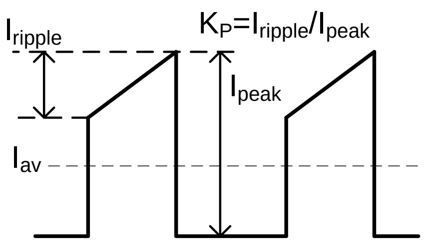


Figure 11: Typical Primary Current Waveform

The input power (P_{in}) at the minimum input can be estimated with Equation (6):

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \quad (6)$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency, typically between 0.75 and 0.85 depending on the input range and output voltage.

For CCM at a minimum input, calculate the converter duty cycle with Equation (7):

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \quad (7)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turn ratio, and $V_{in(min)}$ is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time is calculated with Equation (8):

$$T_{on} = D \cdot T_s \quad (8)$$

Where T_s is the frequency jitter's dominant switching period, and $\frac{1}{T_s} = f_s = 65kHz$.

The average value of the primary current can be calculated with Equation (9):

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \quad (9)$$

The peak value of the primary current can be calculated with Equation (10):

$$I_{peak} = \frac{I_{av}}{(1 - \frac{K_P}{2}) \cdot D} \quad (10)$$

The ripple value of the primary current can be calculated with Equation (11):

$$I_{ripple} = K_P \cdot I_{peak} \quad (11)$$

The valley value of the primary current can be calculated with Equation (12):

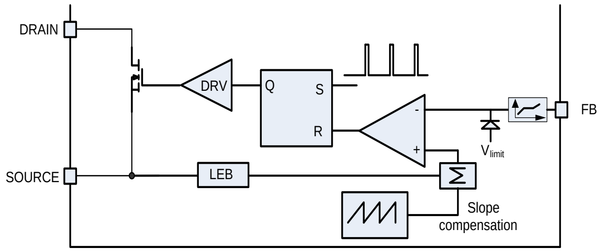
$$I_{valley} = (1 - K_P) \cdot I_{peak} \quad (12)$$

L_m can be calculated with Equation (13):

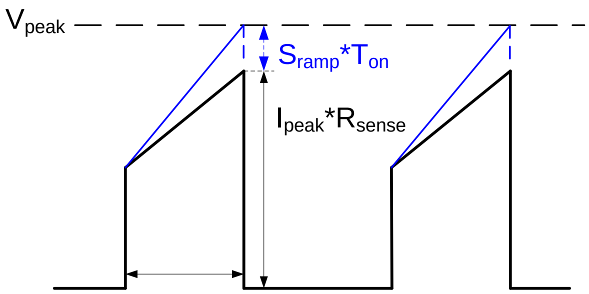
$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripple}} \quad (13)$$

Current-Sense Resistor

Figure 12 shows the peak current comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes high to reset the RS flip-flop, and the MOSFET is turned off.



Peak Current Comparator Circuit



Typical Waveform
Figure 12: Peak Current Comparator

The maximum current limit is V_{ILIM}. The ramp of the slope compensator is S_{ramp}. Given a certain margin, use 0.95 x V_{ILIM} as V_{peak} at full load. Calculate the voltage on the sensing resistor with Equation (14):

$$V_{sense} = 95\% \cdot V_{ILIM} - S_{ramp} \cdot T_{on} \qquad (14)$$

The value of the sense resistor is then calculated with Equation (15):

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \qquad (15)$$

Select a current-sense resistor with an appropriate power rating. Estimate the sense resistor power loss with Equation (16):

$$P = \left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \left(I_{peak} - I_{valley} \right)^2 \right] \cdot D \cdot R_{sense} \qquad (16)$$

Jitter Period

Frequency jitter is used as an effective method for reducing EMI by dissipating energy. The n_{th} order harmonic noise bandwidth is B_{Tn} = n · (2 · Δf + f_{jitter}), where Δf is the frequency jitter amplitude. If B_{Tn} exceeds the resolution bandwidth (R_{BW}) of the spectrum analyzer (200Hz for noise frequency less than 150kHz, 9kHz for noise frequency between 150kHz and 30MHz), the spectrum analyzer receives less noise energy.

The TIMER capacitor determines the frequency jitter period . A 10µA current source charges the capacitor when the TIMER voltage reaches 3.2V, and another 10µA current source discharges the capacitor to 2.8V. This charging and discharging cycle is repeated.

Equation (2) describes the jitter period in theory. A smaller f_{jitter} is more effective for EMI reduction. However, the measurement bandwidth requires f_{jitter} to be large compared to the spectrum analyzer R_{BW} for effective EMI reduction. f_{jitter} should also be less than the control loop gain crossover frequency to avoid disturbing the output voltage regulation.

The TIMER capacitor must be selected carefully. A capacitor that is too large may cause the start-up to fail at full load because of the long, soft start-up duration, shown in Equation (3). However, a TIMER capacitor that is too small causes the timer period to decrease, which overloads the timer count capability and may cause logic problems. For most applications, an f_{jitter} value between 200Hz and 400Hz is recommended.

Ramp Compensation

In peak current control, subharmonic oscillation occurs when D is greater than 0.5 in CCM. The HF500-7 solves this problem with internal ramp compensation. Calculate α with Equation (17):

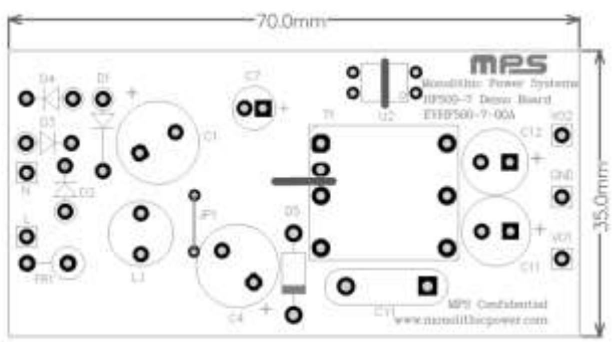
$$\alpha = \frac{\dfrac{D_{max} \cdot V_{in(min)}}{(1\text{-}D_{max}) \cdot L_m} \cdot R_{sense} - m_a}{\dfrac{V_{in(min)}}{L_m} \cdot R_{sense} + m_a} \qquad (17)$$

Where m_a = 20mV/µs is the minimum internal slope value of the compensation ramp, and $\frac{V_{in(min)}}{L_m} \cdot R_{sense}$ and $\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense}$ are the slew rates of the primary-side and equivalent secondary-side voltages sensed by the current-sensing resistor respectively. For stable operation, α must be less than 1.

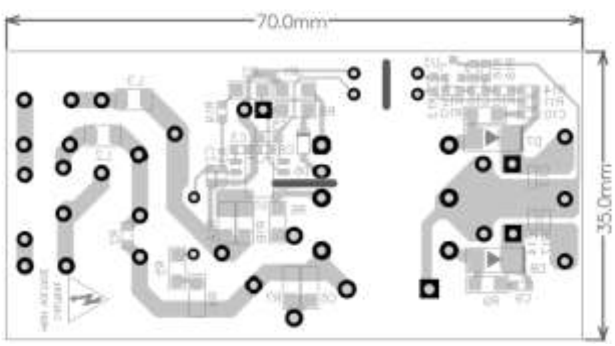
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI performance, and good thermal performance. For best results refer to Figure 13 and follow the guidelines below:

1. Minimize the power stage loop area for better EMI performance. This includes the input loop (C4 - T1 - U1 - R1A/R1B - C4), the auxiliary winding loop (T1 - D6 - R8 - C7 - T1), the output loop (T1 - D7 - C12 - T1, T1 – D8 - C11 - T1), and the RCD snubber loop (T1 - R6 - D5 - R7/C6 - T1).
2. Keep the input loop GND and the control circuit GND separate and only connect them at C4. Otherwise, the IC operation may be influenced by noise.
3. Place one ceramic capacitor close to the sensitive IC pin (such as those for FB, B/O, and VCC) to decouple noise effectively.
4. Place a larger source area around the IC to improve thermal performance, if needed.



Top



Bottom

Figure 13: Recommended PCB Layout

Design Example

Table 1 shows a design example of the HF500-7 for power adapter applications.

Table 1: Design Example

V_{IN}	85 to 265VAC
V_{OUT1}/ V_{OUT2}	12V/5V
I_{OUT1}/ I_{OUT2}	0.3A/0.3A

TYPICAL APPLICATION CIRCUITS

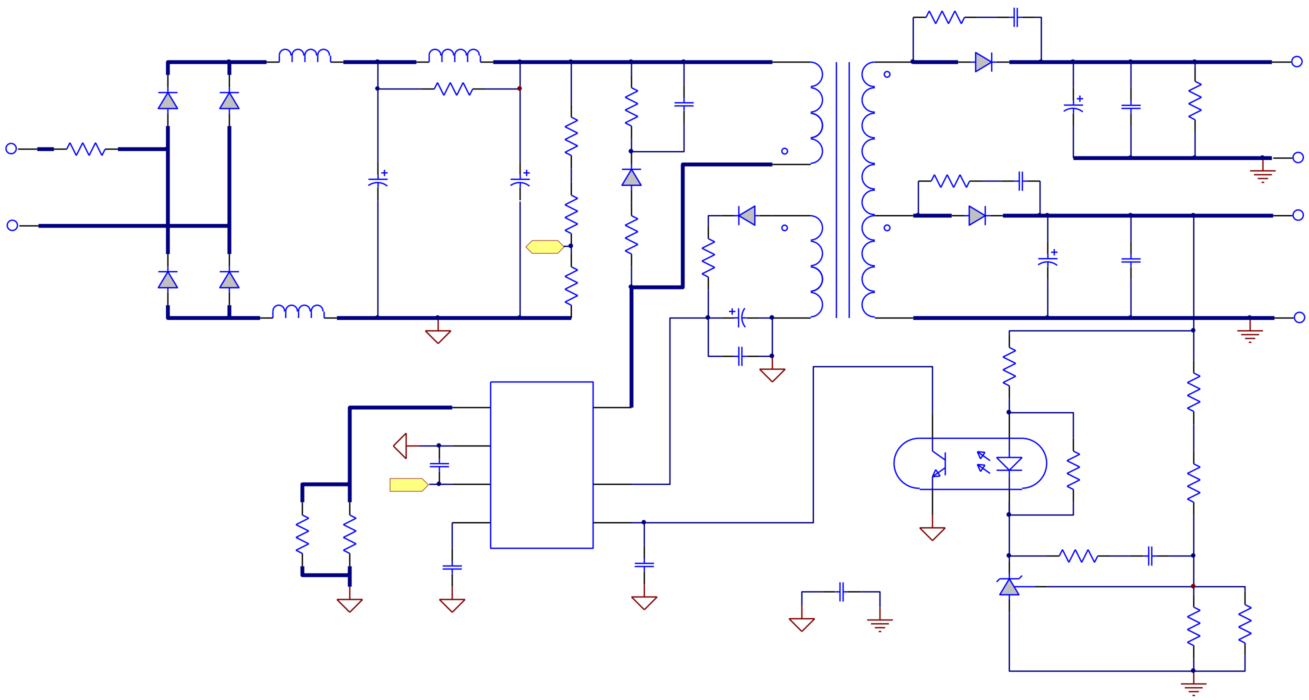
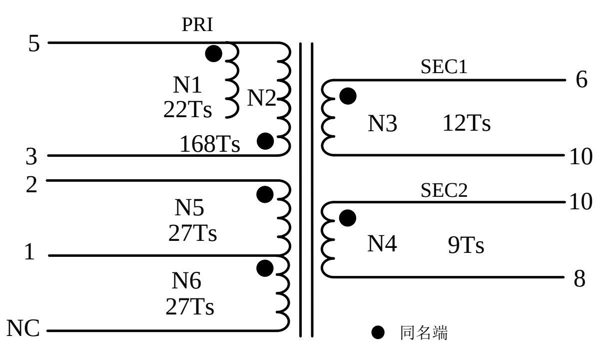
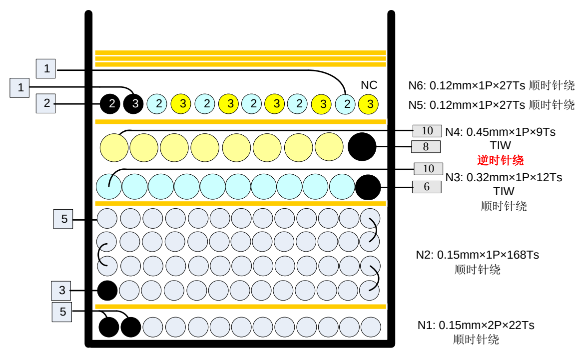


Figure 14: Example of a Typical Application



Connection Diagram



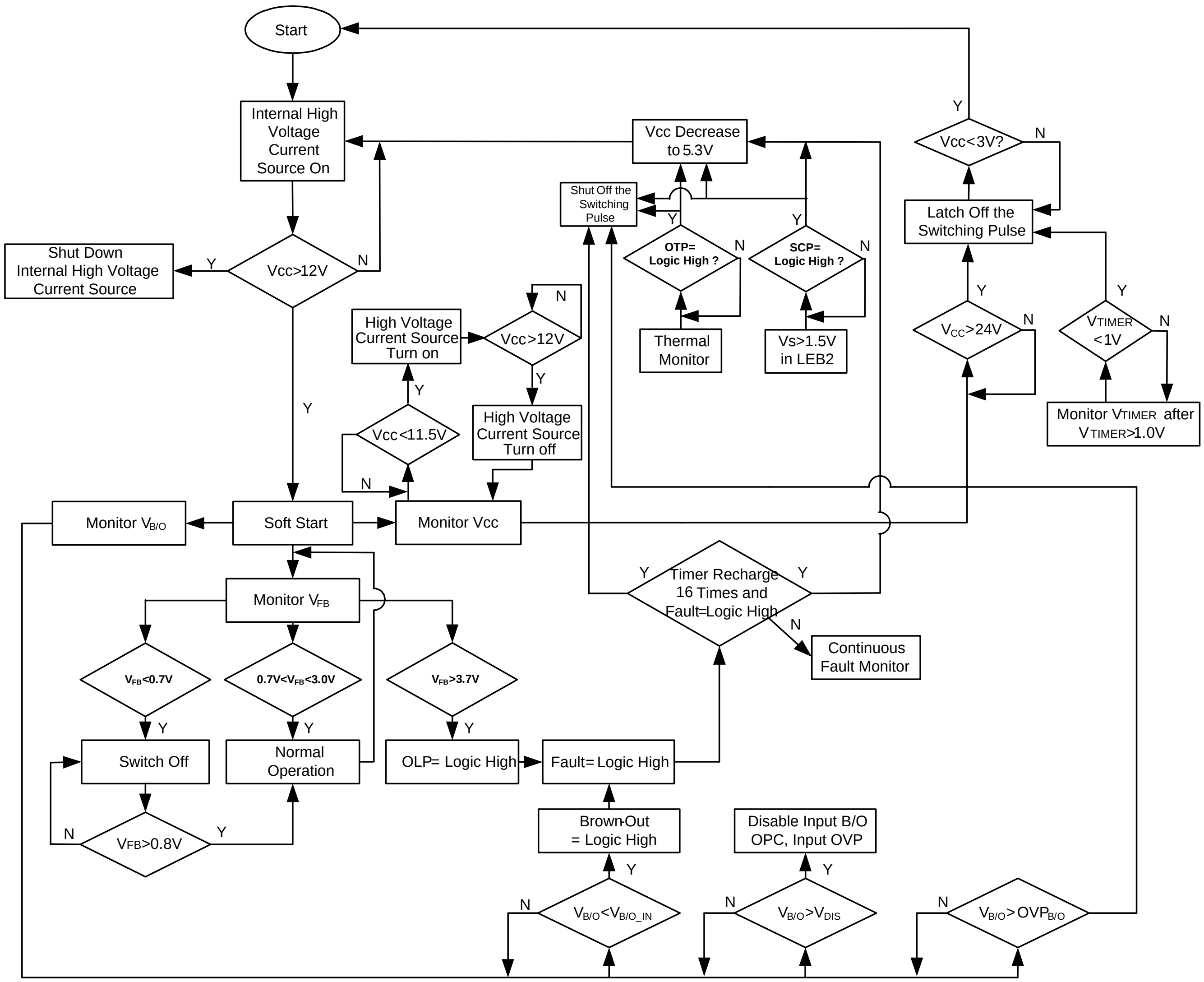
Winding Diagram

Figure 15: Transformer Structure

Table 2: Winding Order

Tape (T)	Winding	Start-End	Wire Size (Φ)	Turns (T)	Tube
0	N1	5 → NC Clockwise	0.15*2	22	None
1	N2	3 → 5 Clockwise	0.15*1	168	None
1	N3	6 → 10 Clockwise	0.32*1 TIW	12	None
1	N4	8 → 10 Anticlockwise	0.45*1 TIW	9	None
3	N5 N6	2 → 1 1 → NC Clockwise	0.12*1 0.12*1	27 27	None

FLOW CHART

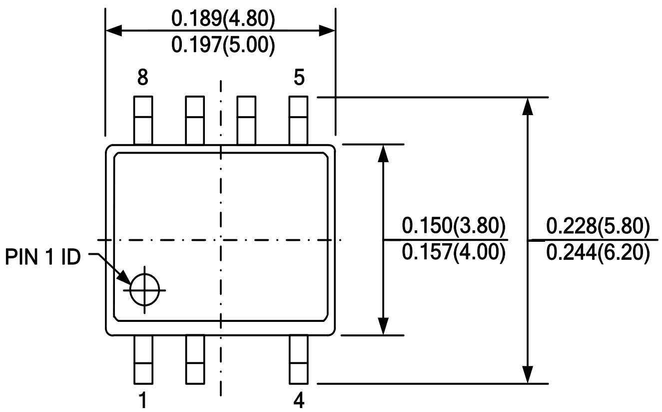


UVLO, brown-out, OTP & OLP are auto restart; OVP on VCC, and latch-off on TIMER are latch mode.
To release from the latch condition, unplug from the main input.

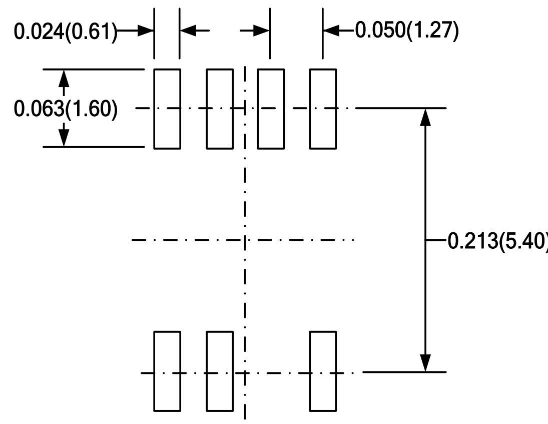
Figure 16: Control Flow Chart

PACKAGE INFORMATION

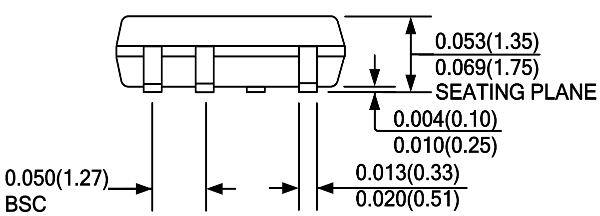
SOIC8-7B



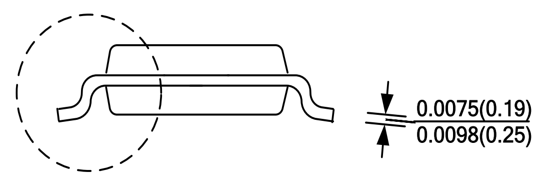
TOP VIEW



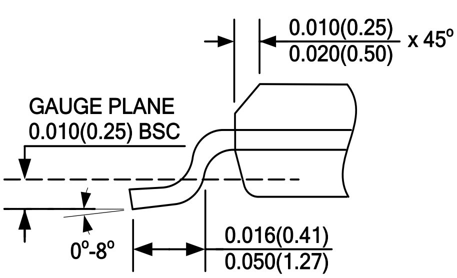
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.