



EVQ4323C-RH-00A

36V, 3A, Low- I_Q , Synchronous Step-Down Converter in a QFN-14 Package Evaluation Board, AEC-Q100 Qualified

DESCRIPTION

The EVQ4323C-RH-00A evaluation board is designed to demonstrate the capabilities of the MPQ4323C, a configurable-frequency (350kHz to 2.5MHz), synchronous, step-down switching regulator with integrated, internal high-side MOSFETs (HS-FETs) and low-side MOSFETs (LS-FETs).

The MPQ4323C provides 3A of highly efficient output current (I_{OUT}) with peak current control mode. The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance accommodates a variety of step-down applications in automotive input environments. A 1 μ A quiescent current (I_Q) in shutdown mode allows the device to be used in battery-powered applications.

An open-drain power good (PG) signal indicates whether the output is within 94.5% to 105.5% of its nominal voltage.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. A high duty cycle and low-dropout (LDO) mode are provided for automotive cold-crank conditions.

The EVQ4323C-RH-00A is fully assembled and tested. The MPQ4323C is available in a QFN-14 (2.5mmx3.5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		3.3V to 36V
Output voltage (V_{OUT})	$V_{IN} = 6\text{V to } 36\text{V}$, $I_{OUT} = 0\text{A to } 3\text{A}$	$V_{OUT} = 5\text{V}$
Maximum output current (I_{OUT})	$V_{IN} = 3.3\text{V to } 36\text{V}$	3A
Typical efficiency	$V_{IN} = 12\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 3\text{A}$	92.6%
Peak efficiency	$V_{IN} = 8\text{V}$, $V_{OUT} = 5\text{V}$, $I_{OUT} = 1\text{A}$	95.3%
Switching frequency (f_{sw})		2.2MHz

EVQ4323C-RH-00A EVALUATION BOARD



LxWxH (8.3cmx8.3cmx1cm)

Board Number	MPS IC Number
EVQ4323C-RH-00A	MPQ4323CGRHE-AEC1

QUICK START GUIDE

The EVQ4323C-RH-00A evaluation board is easy to set up and use to evaluate the MPQ4323C's performance. For proper measurement equipment set-up, refer to Figure 2 on page 4 and follow the steps below:

1. Preset the power supply between 6V and 36V, then turn off the power supply .
2. Set load current between 0A and 3A. Electronic loads represent a negative impedance to the regulator, and setting a current too high triggers hiccup mode.
3. If longer cables are used between the source and the evaluation board ($>0.5\text{m}$ total), place a damping capacitor at the input terminals, especially when $V_{IN} \geq 24\text{V}$.
4. Connect the power supply terminals to:
 - a. Positive (+): VEMI
 - b. Negative (-): GND
5. Connect the load terminals to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
6. After making the connections, turn on the power supply.
7. To use the enable function, apply a digital input to the EN pin. Drive EN above 1.02V to turn the regulator on; drive EN below 0.85V to turn the regulator off. If the enable function is not used, EN can also be connected directly to V_{IN} .
8. Connect a resistor between the FREQ and GND pins to set the internal switching frequency (f_{SW}).
9. The external resistor divider sets the output voltage (V_{OUT}).

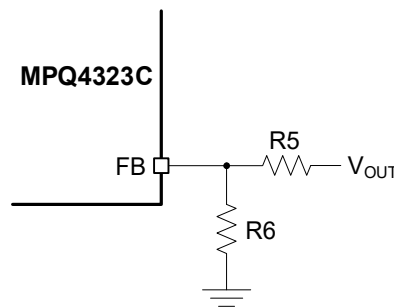


Figure 1: Feedback Divider Network with Adjustable Output

R5 is selected to be 100k Ω . R6 can then be calculated using Equation (1):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.8V} - 1} \quad (1)$$

Refer to the Application Information section in the MPQ4323C datasheet to calculate the inductance and output capacitance for different V_{OUT} values.

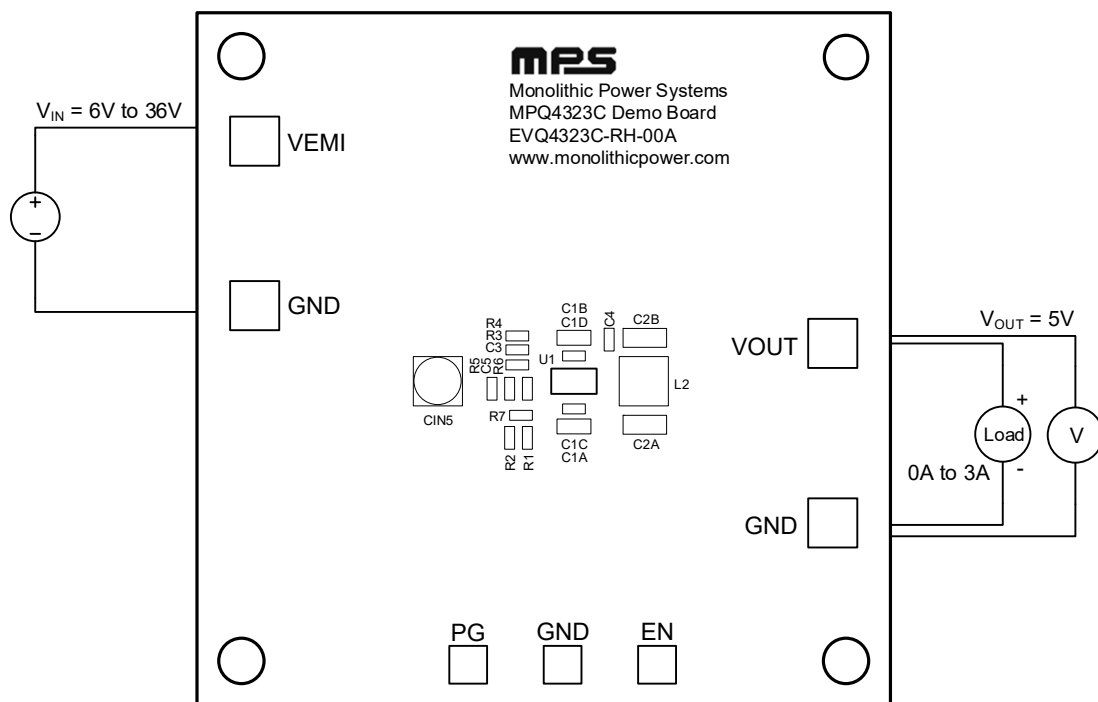


Figure 2: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

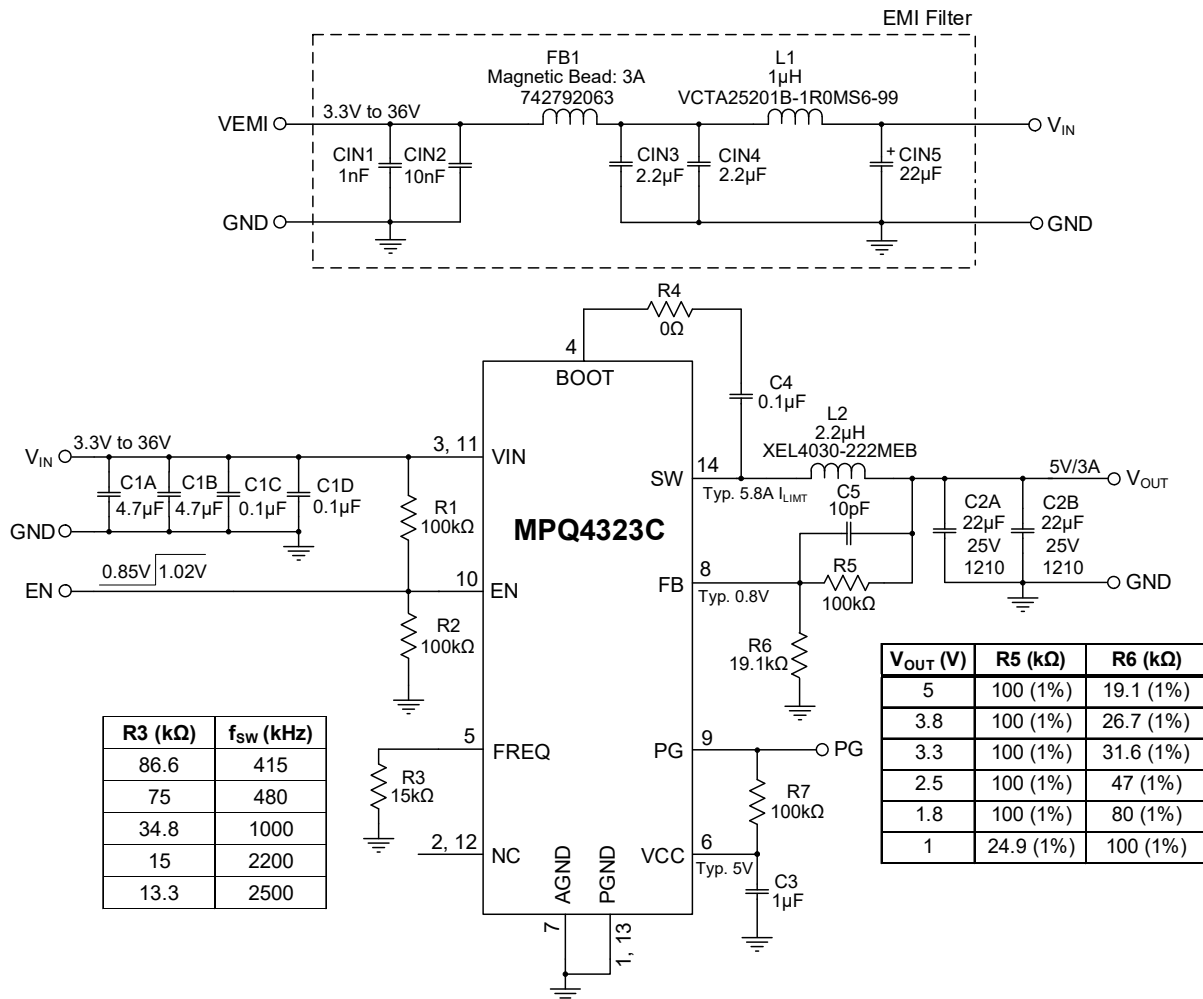
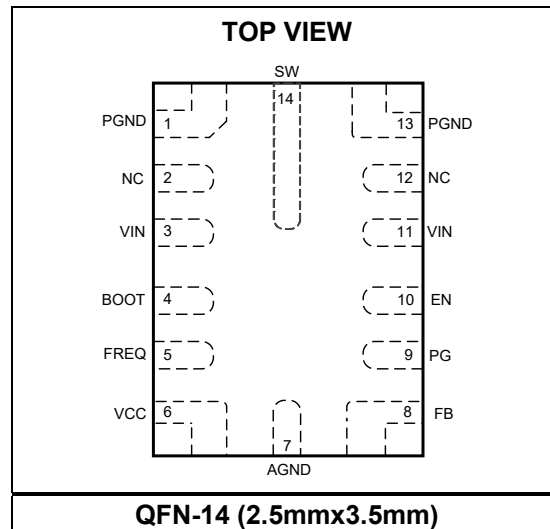


Figure 3: Evaluation Board Schematic

PACKAGE REFERENCE

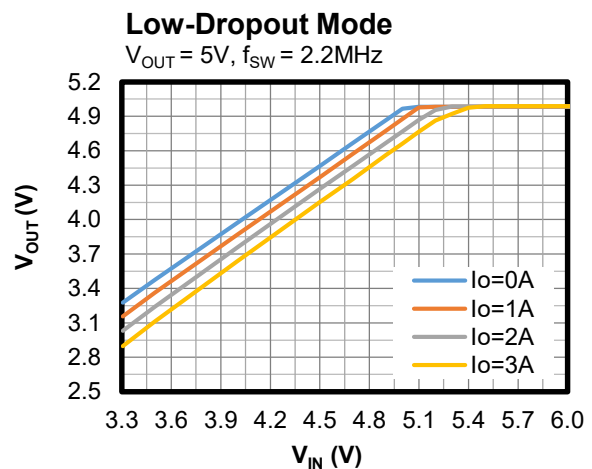
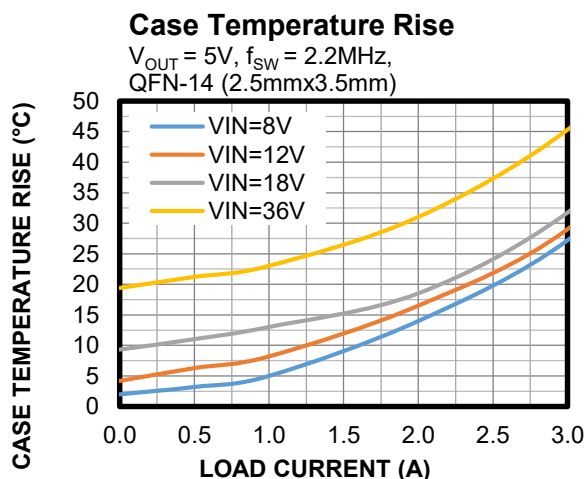
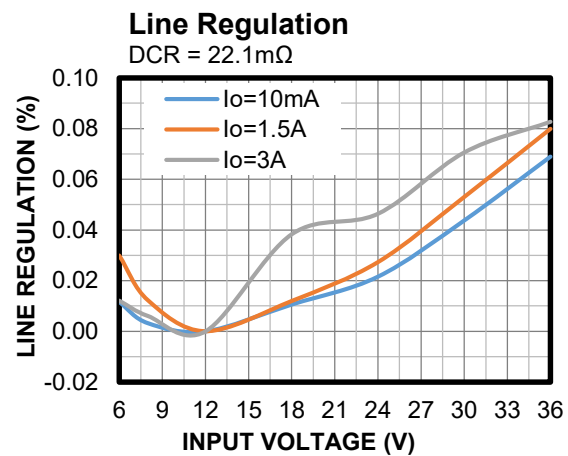
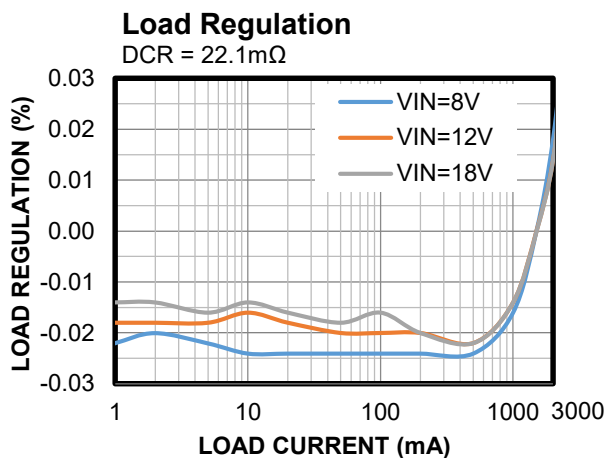
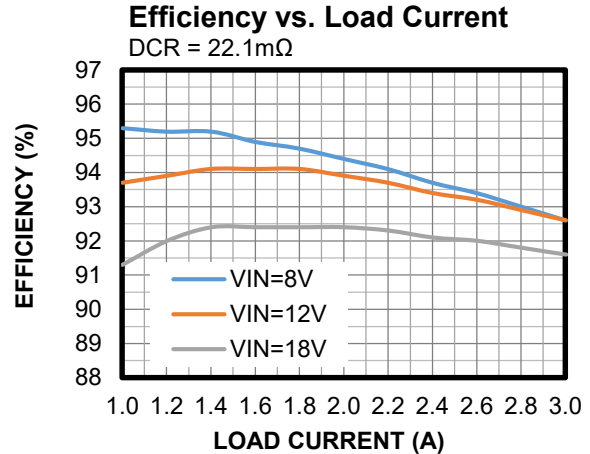
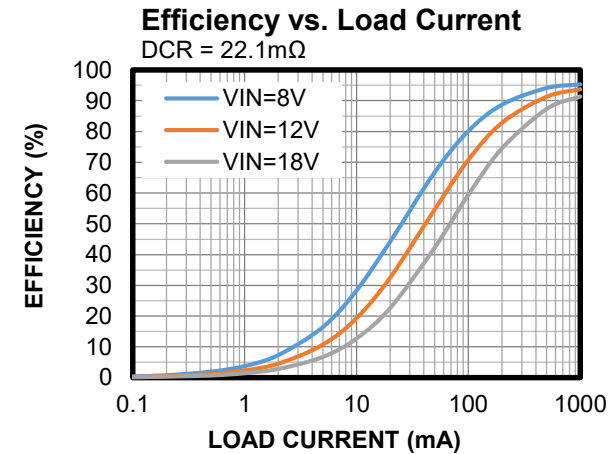


EVQ4323C-RH-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	CIN1	1nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM216R71H102KA01
1	CIN2	10nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H103KA01D
2	CIN3, CIN4	2.2 μ F	Ceramic capacitor, 50V, X7R	0805	TDK	CGA4J3X7R1H225KT000N
1	CIN5	22 μ F	Aluminum polymer capacitor, 50V	SMD	Panasonic	EEHZC1H220P
2	C1A, C1B	4.7 μ F	Ceramic capacitor, 50V, X7S	1206	Murata	GRM31CR71H475KA12L
3	C1C, C1D, C4	100nF	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
2	C2A, C2B	22 μ F	Ceramic capacitor, 25V, X7R	1210	Murata	GRM32ER71E226KE15L
1	C5	10pF	Ceramic capacitor, 50V, NP0	0603	Würth	885012006051
1	C3	1 μ F	Ceramic capacitor, 25V, X7R	0603	Murata	GCM188R71E105KA64D
1	FB1	3A	Magnetic bead	0805	Würth	742792063
1	L1	1 μ H	Inductor, 35m Ω , 3.8A	SMD	Cyntec	VCTA25201B-1R0MS6-99
1	L2	2.2 μ H	Inductor, 22.1m Ω , 5.8A	SMD	Coilcraft	XEL4030-222MEB
4	R1, R5, R7, R2	100k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R6	19.1k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0719K1L
1	R3	15k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0715KL
1	R4	0 Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
1	U1	MPQ4323C	42V load dump, 3A, sync step-down converter, AEC-Q100	QFN-14 (2.5mmx3.5mm)	MPS	MPQ4323CGRHE-AEC1

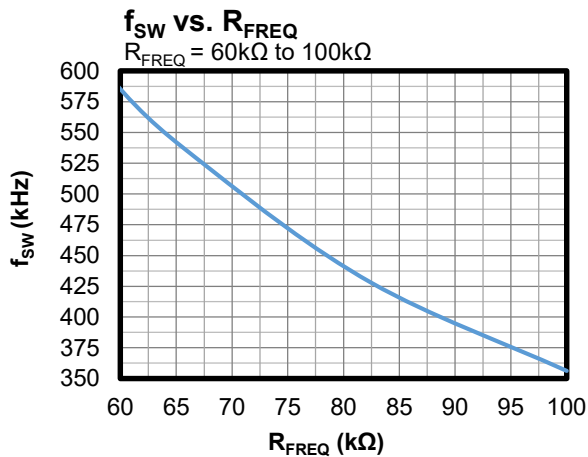
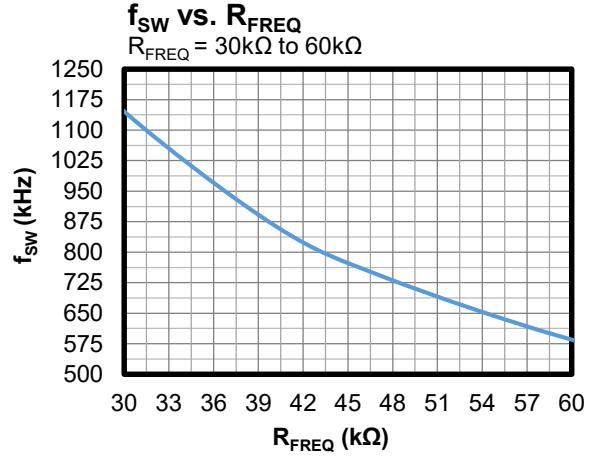
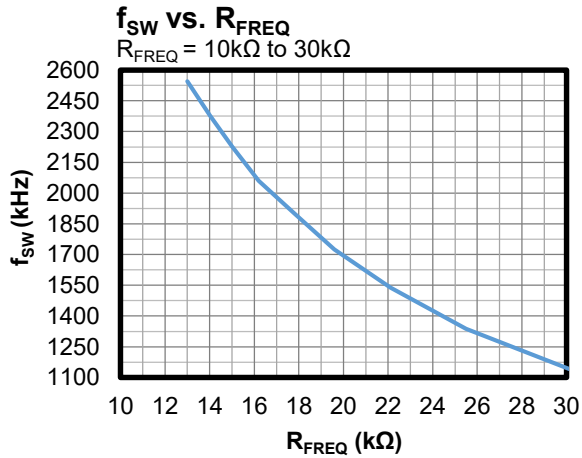
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.



EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

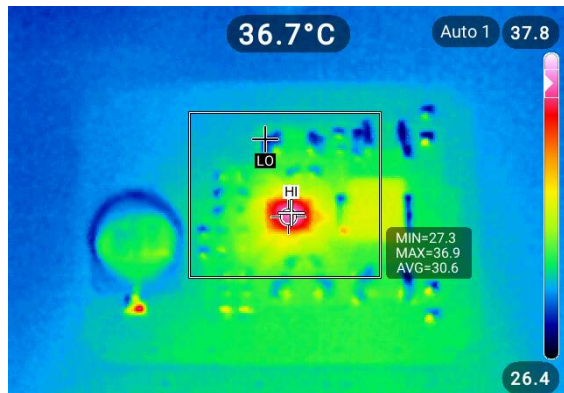


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

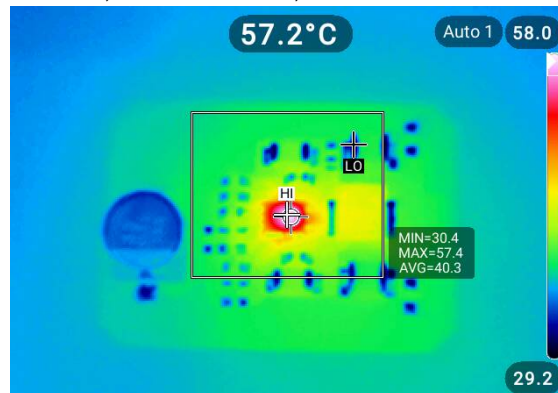
Thermal Performance

$I_{OUT} = 1.5A$, no forced airflow, $T_{CASE} = 36.7^\circ C$



Thermal Performance

$I_{OUT} = 3A$, no forced airflow, $T_{CASE} = 57.2^\circ C$

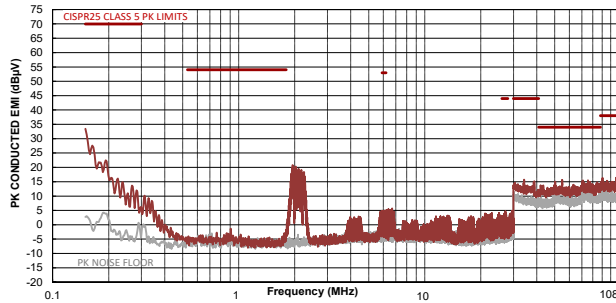


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

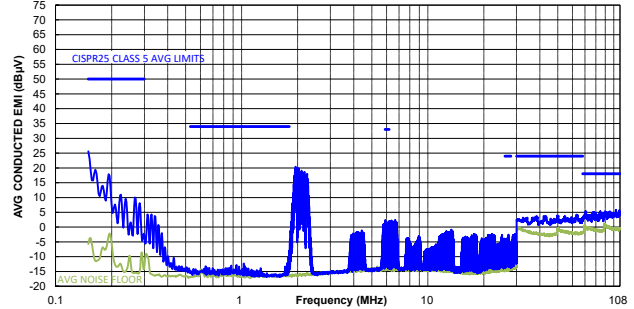
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



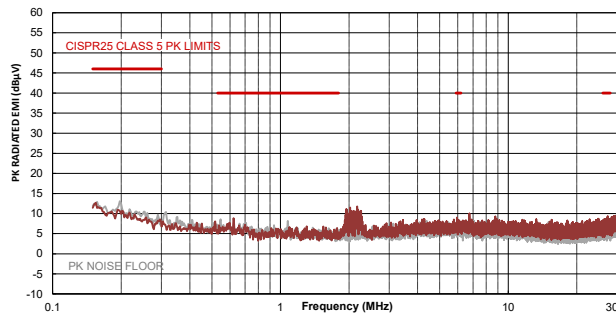
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



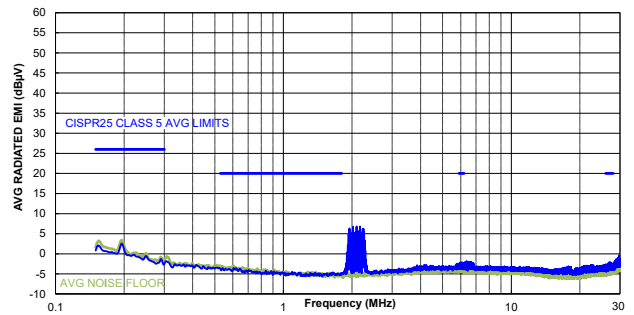
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



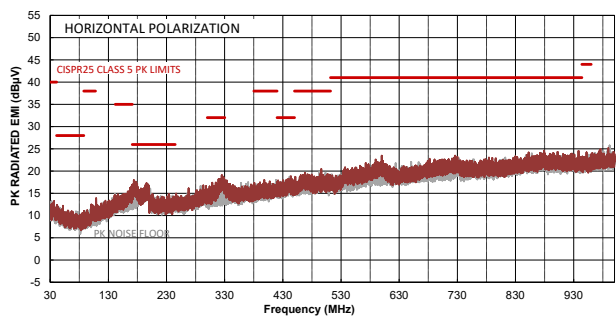
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



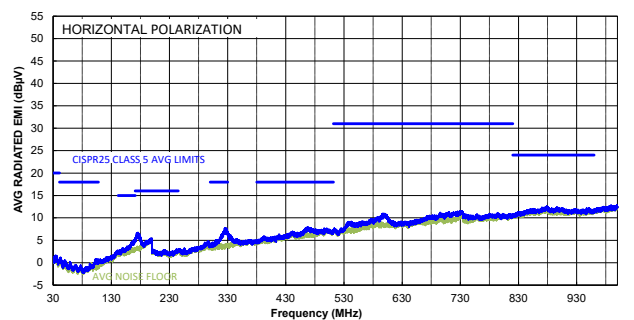
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

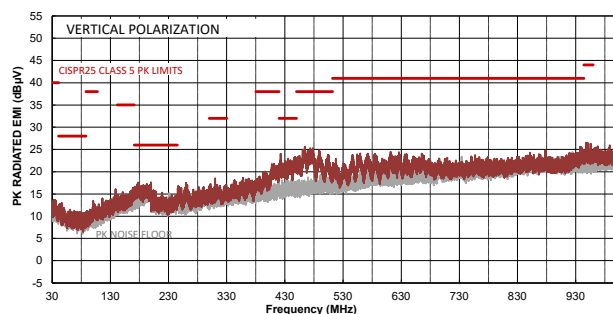


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

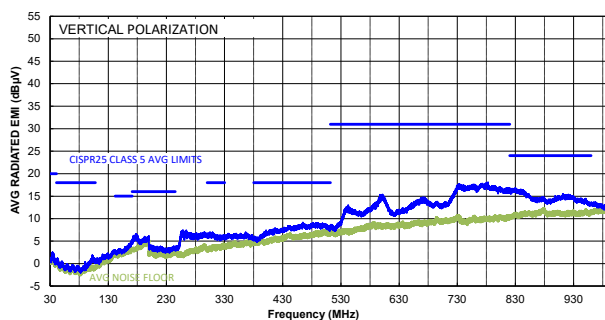
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

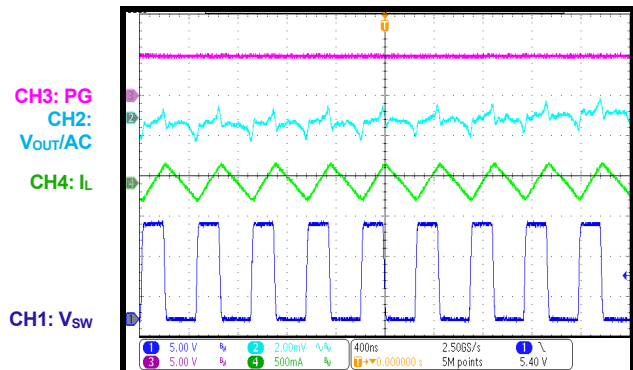
Vertical, 30MHz to 1GHz



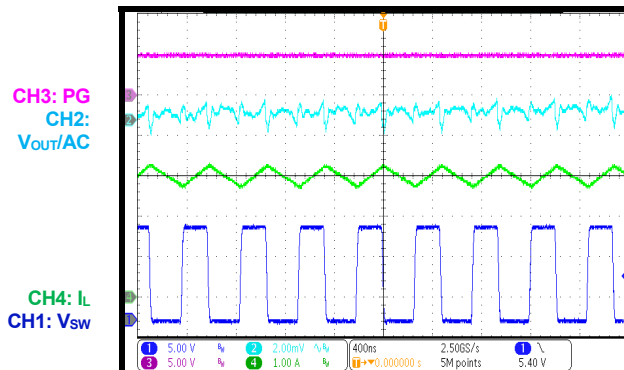
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

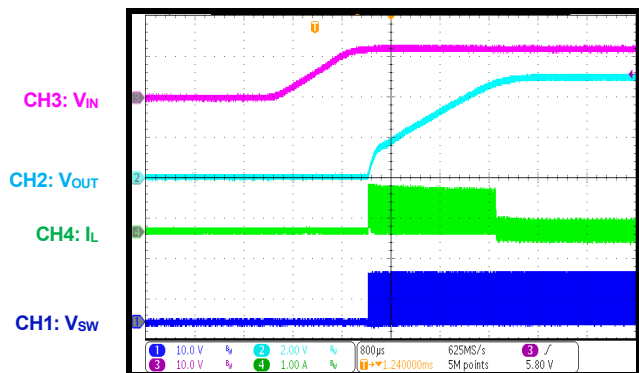
Steady State

 $I_{OUT} = 0A$


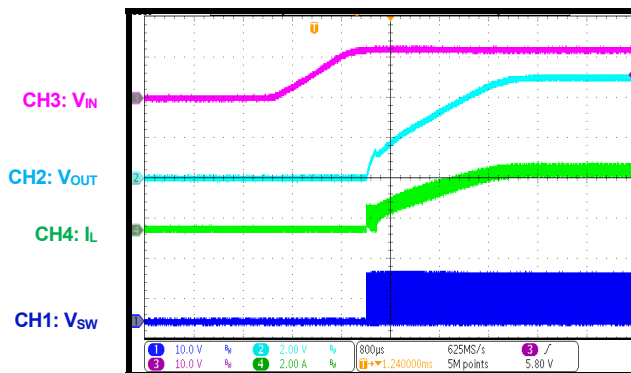
Steady State

 $I_{OUT} = 3A$


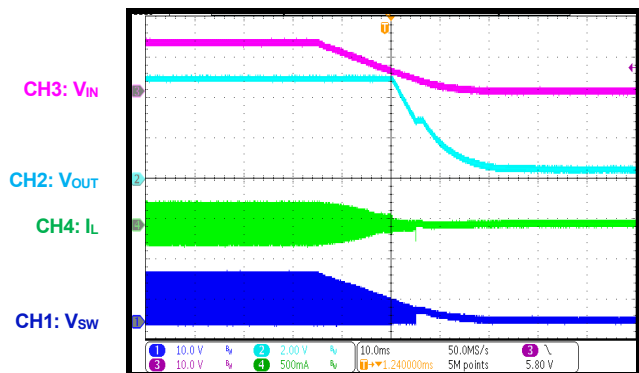
Start-Up through VIN

 $I_{OUT} = 0A$


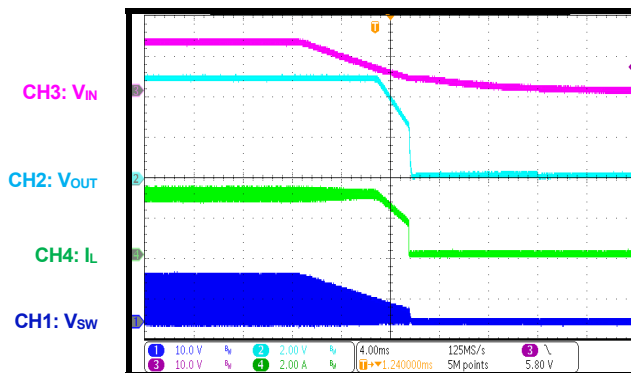
Start-Up through VIN

 $I_{OUT} = 3A$


Shutdown through VIN

 $I_{OUT} = 0A$


Shutdown through VIN

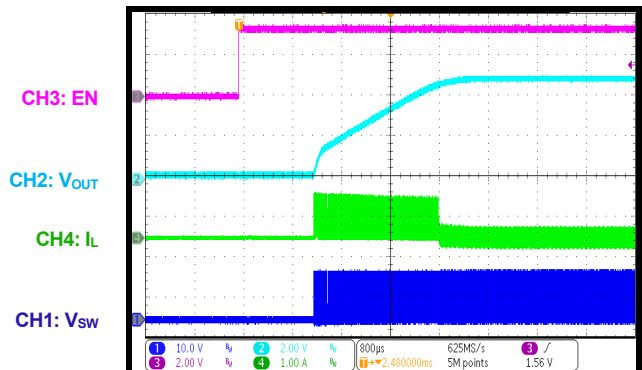
 $I_{OUT} = 3A$


EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

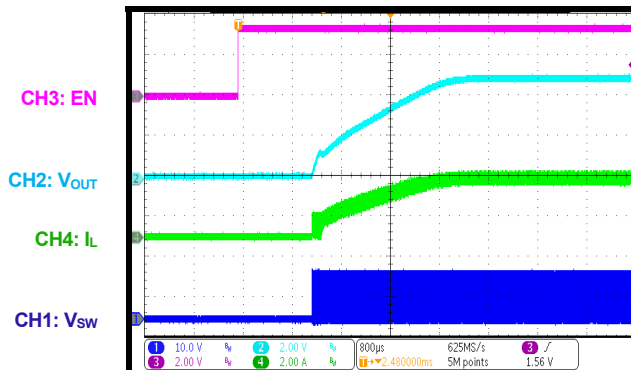
Start-Up through EN

$I_{OUT} = 0A$



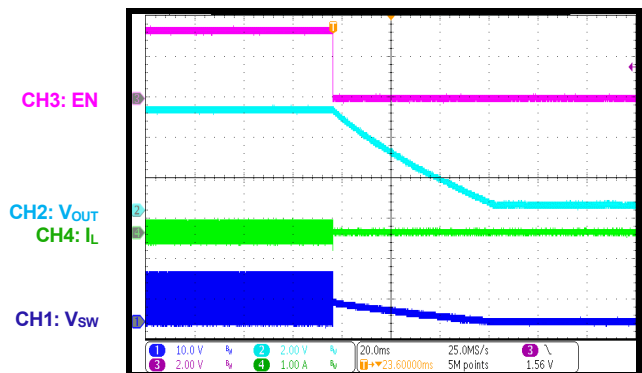
Start-Up through EN

$I_{OUT} = 3A$



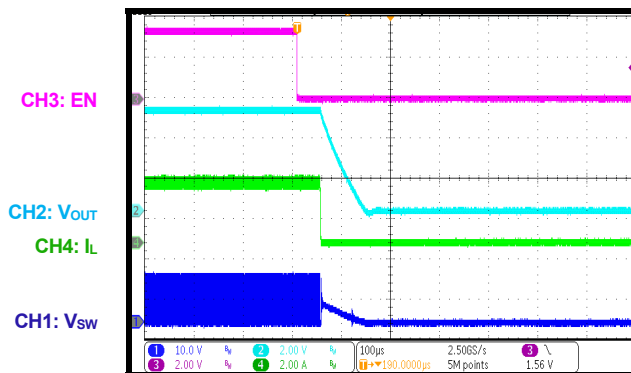
Shutdown through EN

$I_{OUT} = 0A$



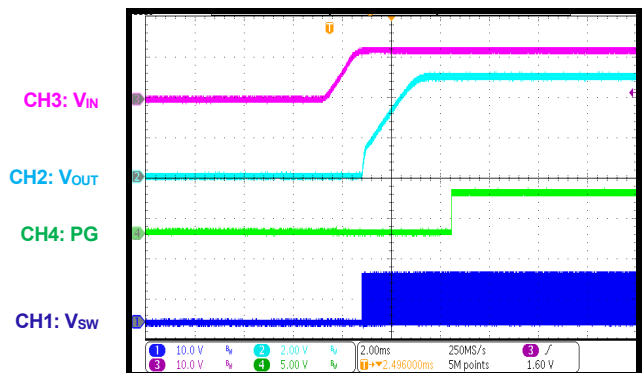
Shutdown through EN

$I_{OUT} = 3A$



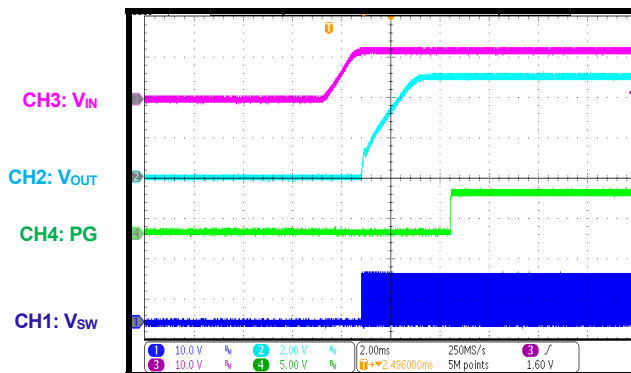
PG during Start-Up through VIN

$I_{OUT} = 0A$



PG during Start-Up through VIN

$I_{OUT} = 3A$

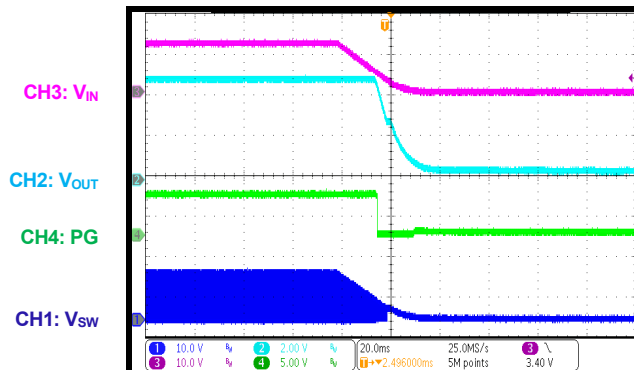


EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

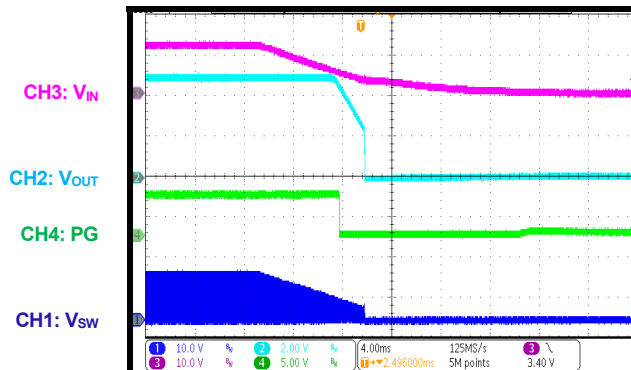
PG during Shutdown through VIN

$I_{OUT} = 0A$



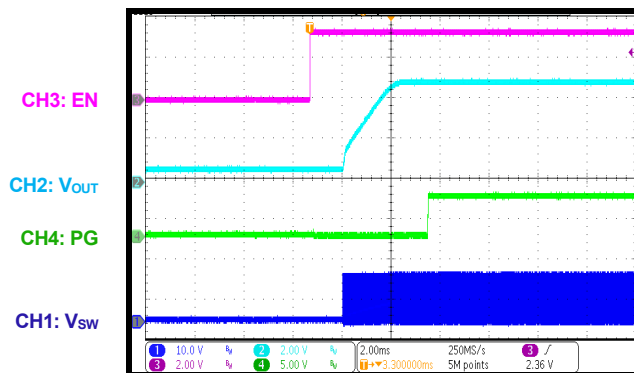
PG during Shutdown through VIN

$I_{OUT} = 3A$



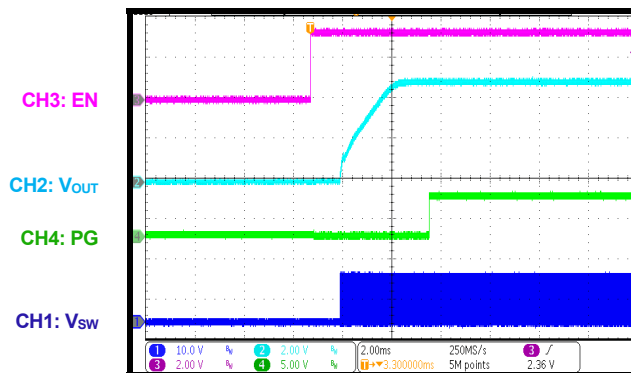
PG during Start-Up through EN

$I_{OUT} = 0A$



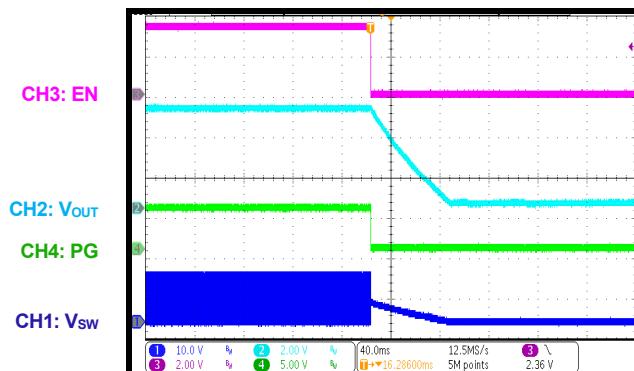
PG during Start-Up through EN

$I_{OUT} = 3A$



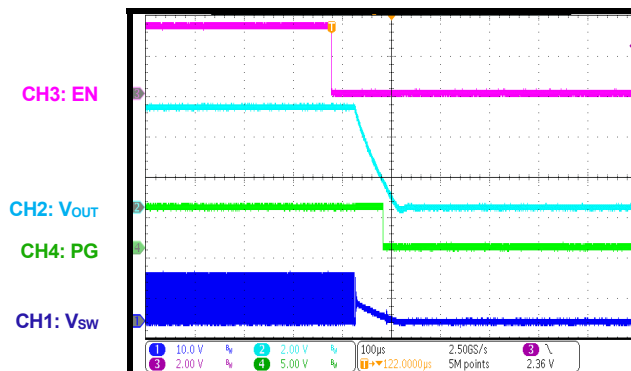
PG during Shutdown through EN

$I_{OUT} = 0A$



PG during Shutdown through EN

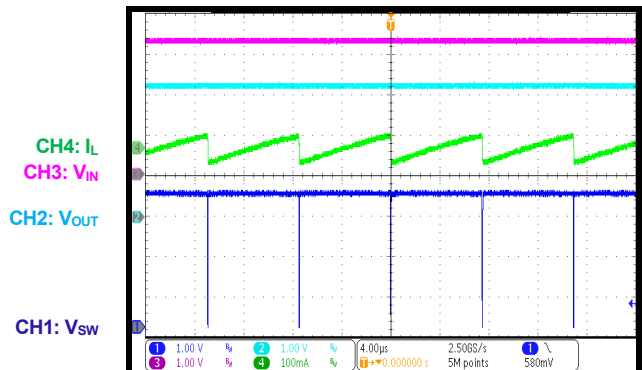
$I_{OUT} = 3A$



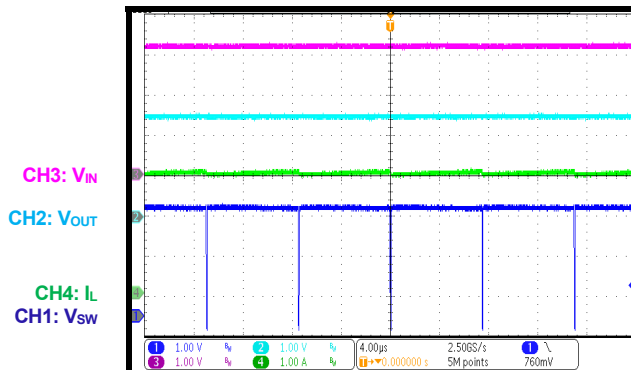
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

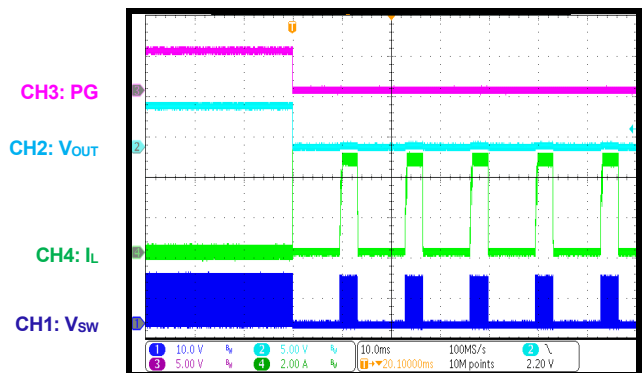
Low-Dropout Mode

 $I_{OUT} = 0A$, $V_{IN} = 3.3V$


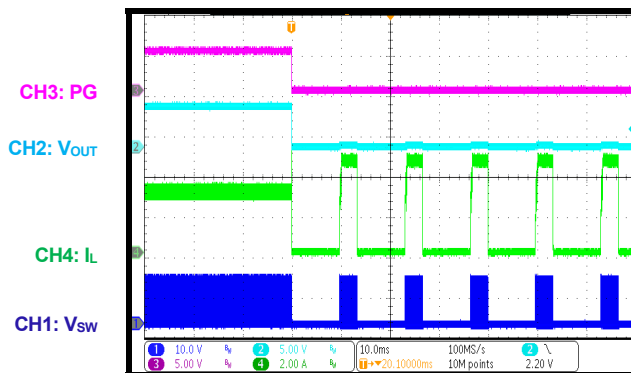
Low-Dropout Mode

 $I_{OUT} = 3A$, $V_{IN} = 3.3V$


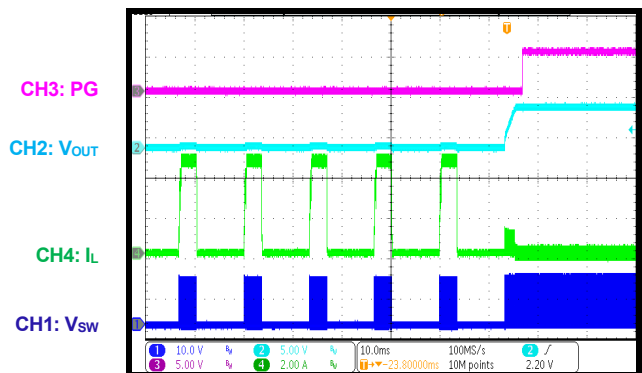
SCP Entry

 $I_{OUT} = 0A$


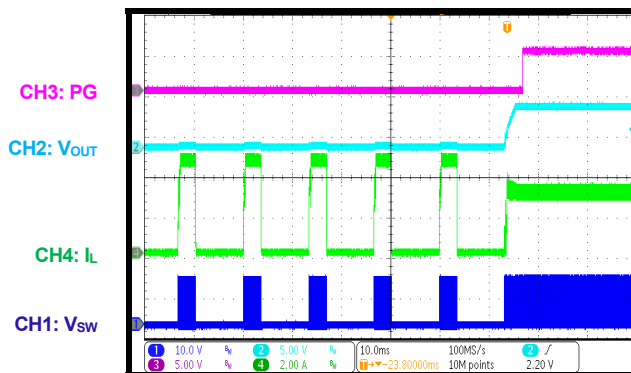
SCP Entry

 $I_{OUT} = 3A$


SCP Recovery

 $I_{OUT} = 0A$


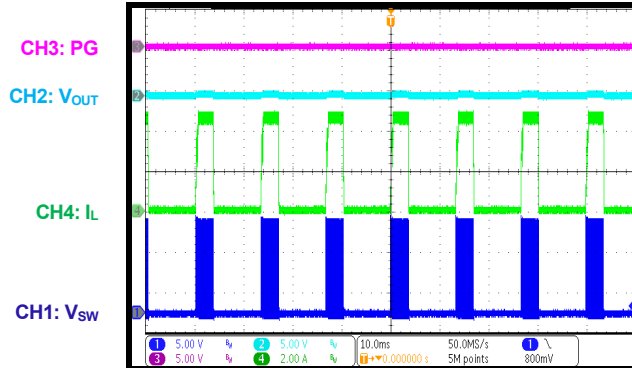
SCP Recovery

 $I_{OUT} = 3A$


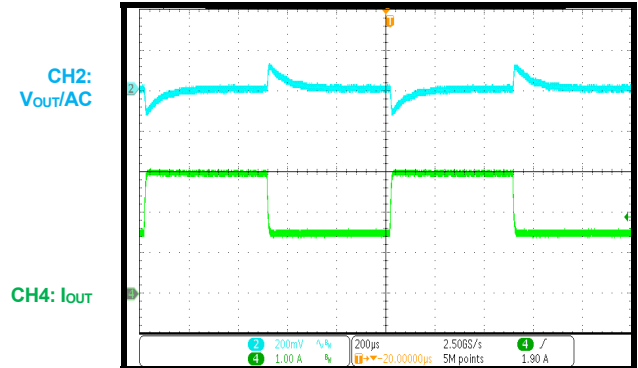
EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

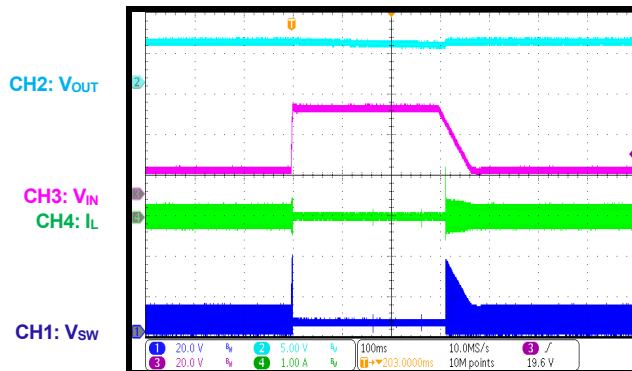
SCP Steady State

 $I_{OUT} = 0A$


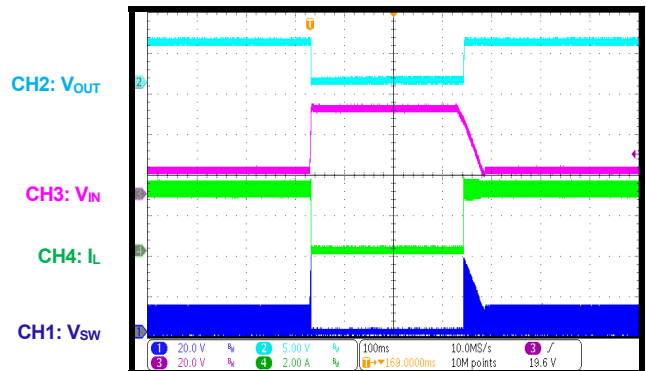
Load Transient

 $I_{OUT} = 1.5A$ to $3A$, $1.6A/\mu s$


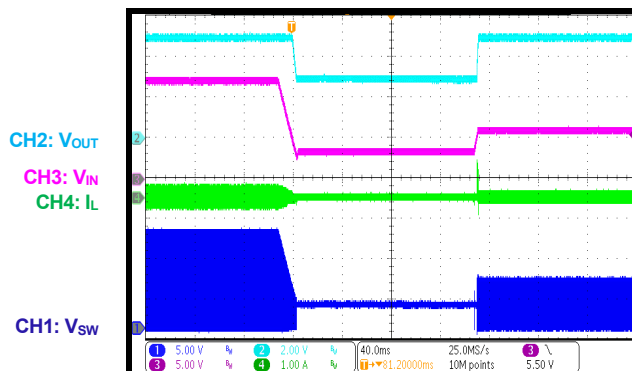
Load Dump

 $V_{IN} = 12V$ to $42V$, $I_{OUT} = 0A$


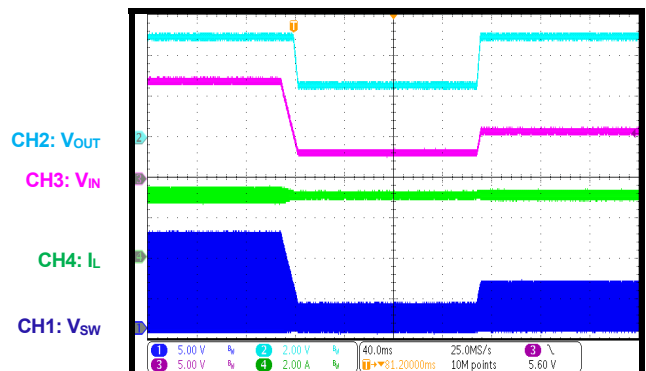
Load Dump

 $V_{IN} = 12V$ to $42V$, $I_{OUT} = 3A$


Cold Crank

 $V_{IN} = 12V$ to $3.3V$ to $6V$, $I_{OUT} = 0A$


Cold Crank

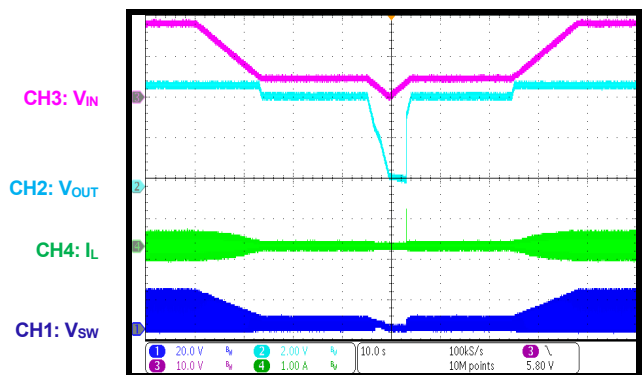
 $V_{IN} = 12V$ to $3.3V$ to $6V$, $I_{OUT} = 3A$


EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $T_A = 25^\circ C$, unless otherwise noted.

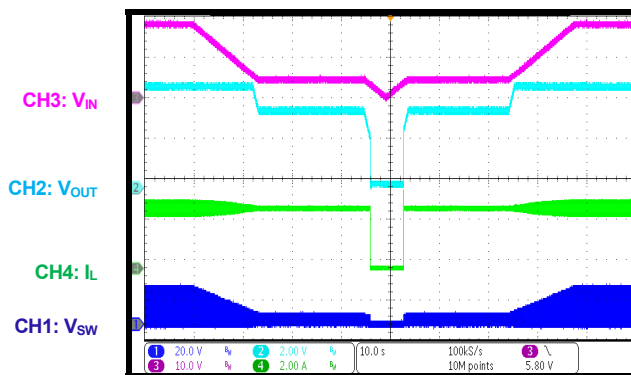
V_{IN} Ramping Down and Up

$V_{IN} = 18V$ to $4.5V$ to $0V$ to $4.5V$ to $18V$,
 $I_{OUT} = 0A$



V_{IN} Ramping Down and Up

$V_{IN} = 18V$ to $4.5V$ to $0V$ to $4.5V$ to $18V$,
 $I_{OUT} = 3A$



PCB LAYOUT

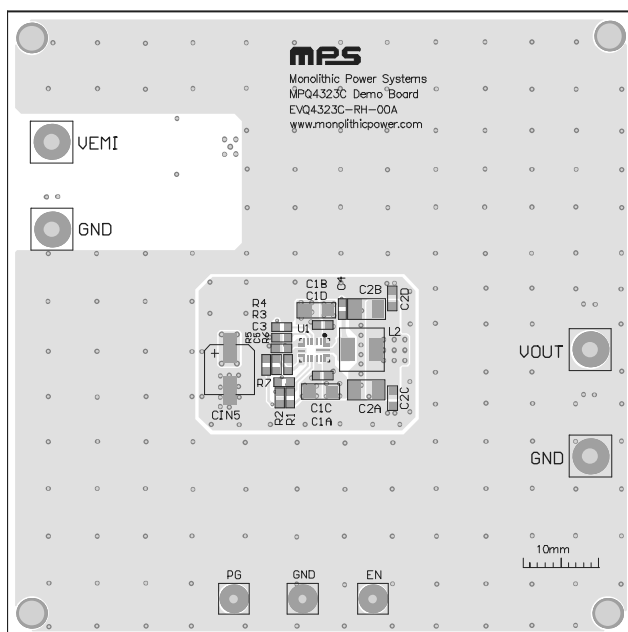


Figure 4: Top Silk and Top Layer

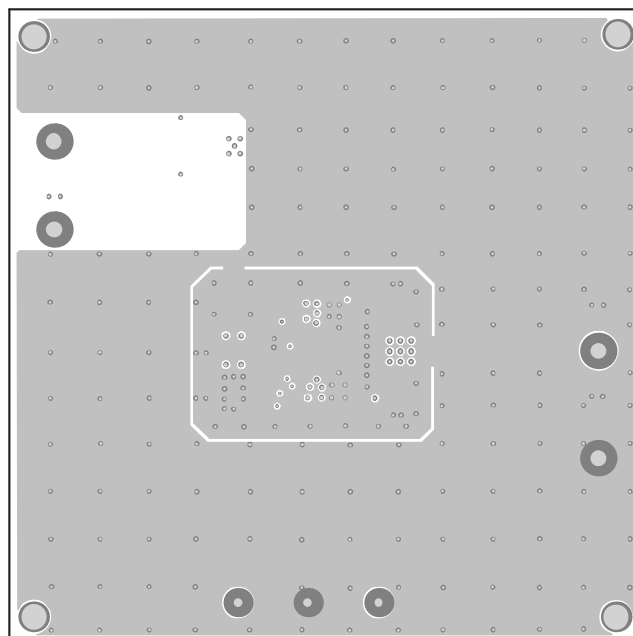


Figure 5: Mid-Layer 1

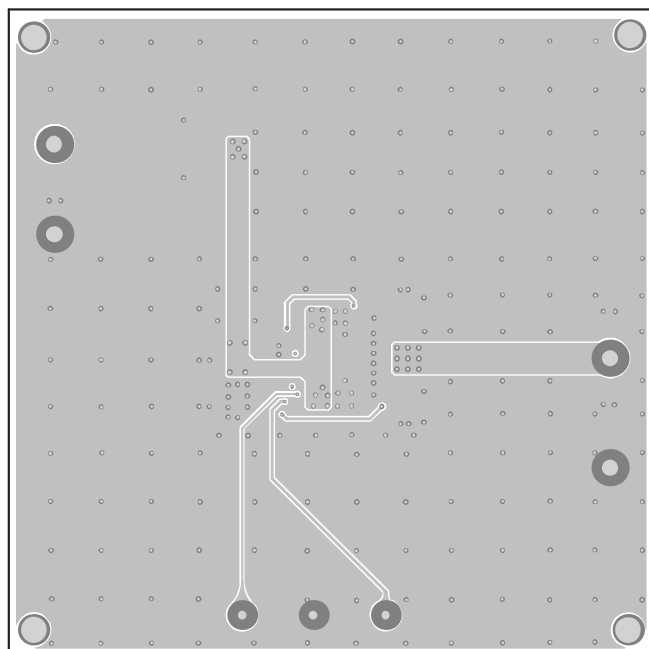


Figure 6: Mid-Layer 2

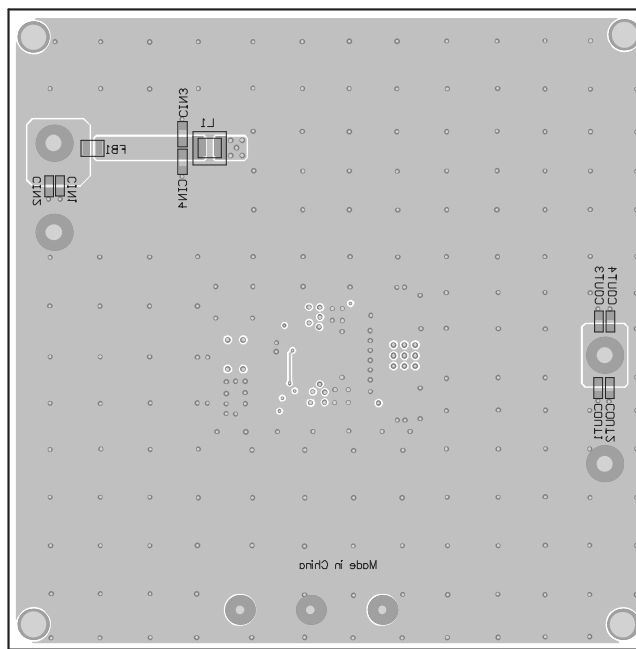


Figure 7: Bottom Layer and Bottom Silk



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/27/2022	Initial Release	-

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