



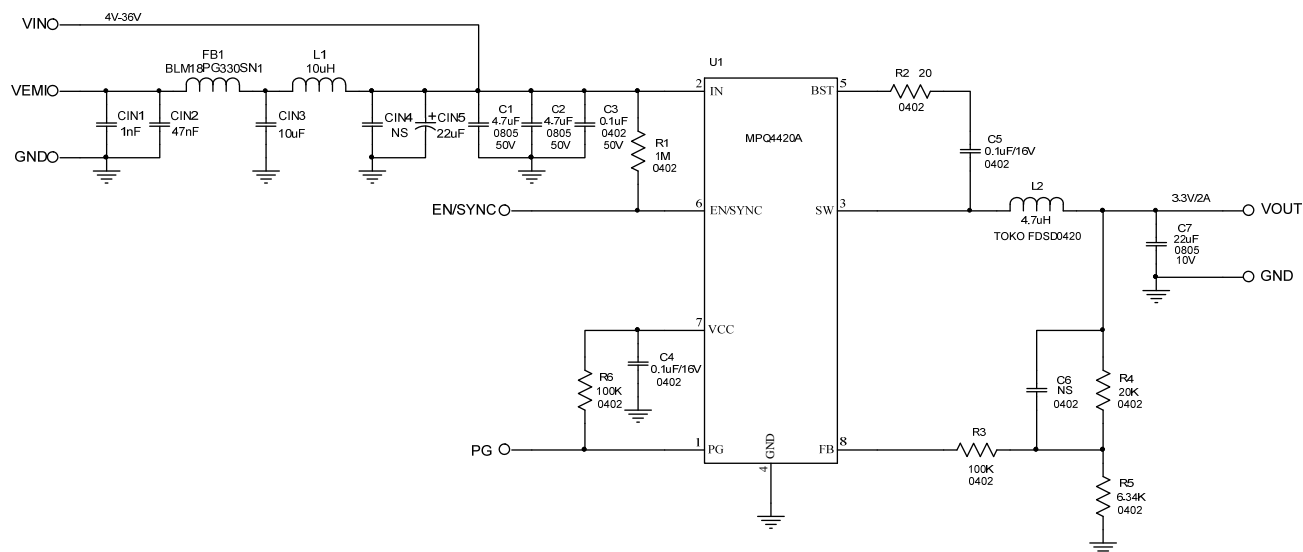
## QUICK START GUIDE

1. Connect the positive and negative terminals of the load to the VOUT and GND pins respectively.
2. Preset the power supply output to between 4V to 36V, and then turn it off.
3. Connect the positive and negative terminals of the power supply output to the VIN and GND pins respectively.
4. Turn the power supply on. The MP4420A/MPQ4420A will automatically startup.
5. To use the Enable function, apply a digital input to the EN pin. Drive EN higher than 1.65V to turn on the regulator, drive EN less than 1.05V to turn it off. An internal 500kΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.
6. Connect the EN input pin through a pull-up resistor (R1) to any voltage connected to the VIN pin. Make sure R1 big enough to limit the EN input current to less than 150μA. For example, with 12V connected to VIN, make sure  $R1 \geq (12V - 6.5V) \div 150\mu A = 36.7k\Omega$ . Connect the EN pin directly to a voltage source without any pull-up resistor requires limiting voltage amplitude to  $\leq 6V$  to prevent damage to the internal zener diode at EN pin.
7. Connect the EN input pin with an external clock with a range of 200kHz to 2.2MHz after output voltage is set to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of external clock signal should be less than 1.7μs.
8. Use R4 and R5 to set the output voltage with  $V_{FB}=0.792V$ . For R4=20kΩ, R5 can be determined by:

$$R5 = \frac{R4}{\frac{V_{OUT}}{0.792} - 1}$$

Follow the Application Information section in the device datasheet to recalculate the compensation, inductor and output capacitor values when output voltage is changed.

## EVALUATION BOARD SCHEMATIC



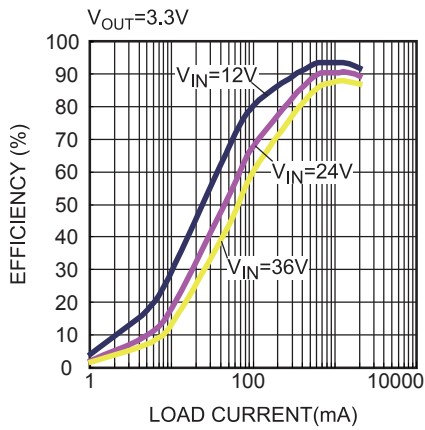
## EV4420A-J-00A BILL OF MATERIALS

Qty.	Ref	Value	Description	Package	Manufacture	Manufacture_PN
2	C1, C2	4.7μF	Ceramic Cap., 50V, X7S	0805	muRata	GRM21BC71H475KE11L
1	C3	0.1μF	Ceramic Cap., 50V, X7R	0402	TDK	C1005X7R1C104K
2	C4, C5	0.1μF	Ceramic Cap., 16V, X7R	0402	muRata	GRM155R71C104KA88D
1	C7	22μF	Ceramic Cap., 10V, X7S	0805	TDK	C2012X7S1A226M125AC
1	CIN1	1nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H102KA01D
1	CIN2	47nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H473KA61D
1	CIN3	10uF	Ceramic Cap., 50V, X7R	1210	muRata	GRM32ER71H106KA12L
1	CIN5	22μF	Electrolytic Cap.	SMD	Jianghai	VTD-63V22
2	C6, CIN4	NS				
1	FB1		Magnetic Bead, 3A	0603	muRata	BLM18PG330SN1
1	L1	10μH	Inductor, 84mΩ DCR, 3A	SMD	Coilcraft	XAL4040-103ME
1	L2	4.7μH	Inductor, 83mΩ DCR, 3.6A	SMD	TOKO	FDSD0420-H-4R7M
			Inductor, 40.1mΩ DCR, 4.5A	SMD	Coilcraft	XAL4040-472ME
1	R1	1M	Film Res., 5%	0402	Yageo	RC0402JR-071ML
1	R2	20	Film Res., 1%	0402	Yageo	RC0402FR-0720RL
1	R3	100k	Film Res., 1%	0402	Yageo	RC0402FR-07100KL
1	R4	20k	Film Res., 1%	0402	Yageo	RC0402FR-0720KL
1	R5	6.34k	Film Res., 1%	0402	Yageo	RC0402FR-076K34L
1	U1		Step-Down Regulator	TSOT23-8	MPS	MPQ4420AGJ
5	VIN, VEMI, GND, VOUT, GND		2.0 Golden Pin		HZ	
4	EN/SYNC, GND, PG, GND		1.0 Golden Pin		HZ	

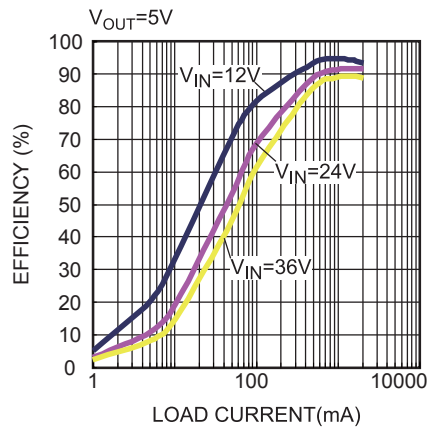
## EVB TEST RESULTS

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

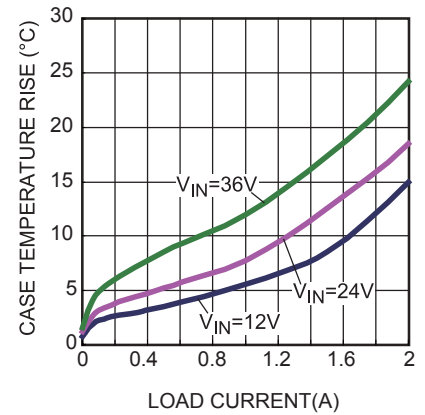
**Efficiency vs. Load Current**



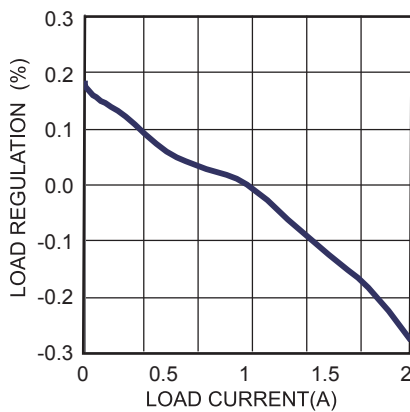
**Efficiency vs. Load Current**



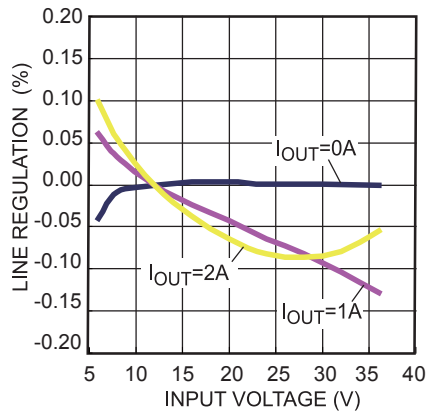
**Thermal Rise**



**Load Regulation**



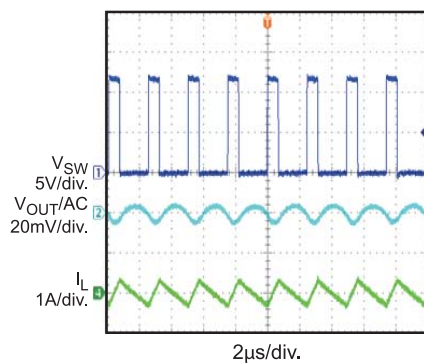
**Line Regulation**



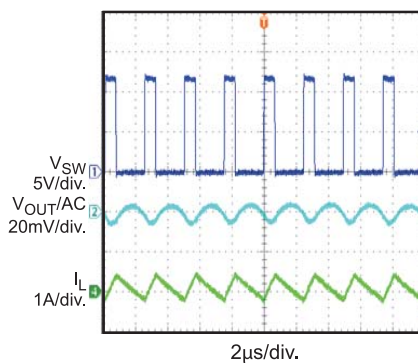
## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

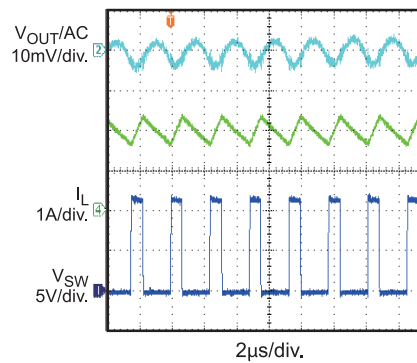
**Steady State**  
 $I_{OUT} = 0A$



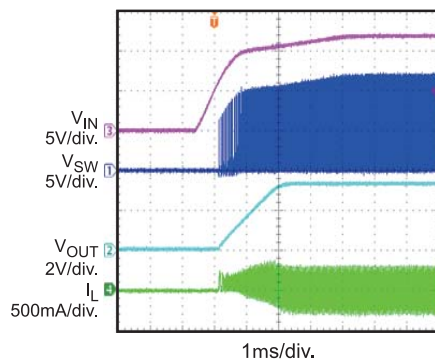
**Steady State**  
 $I_{OUT} = 0.1A$



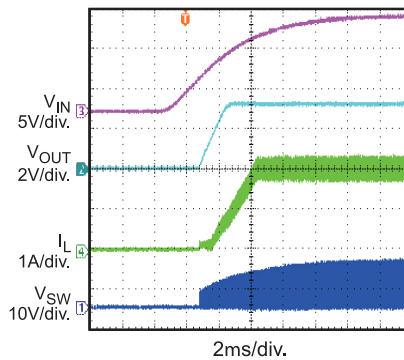
**Steady State**  
 $I_{OUT} = 2A$



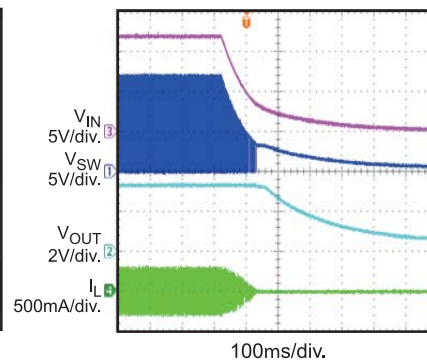
**Start-Up through  $V_{IN}$**   
 $I_{OUT} = 0A$



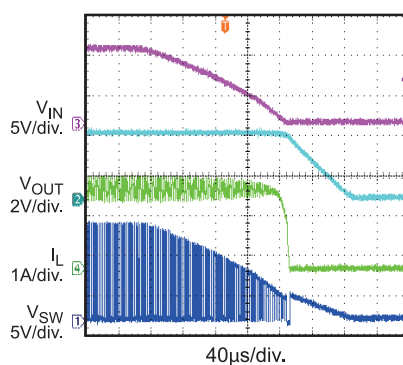
**Start-Up through  $V_{IN}$**   
 $I_{OUT} = 2A$



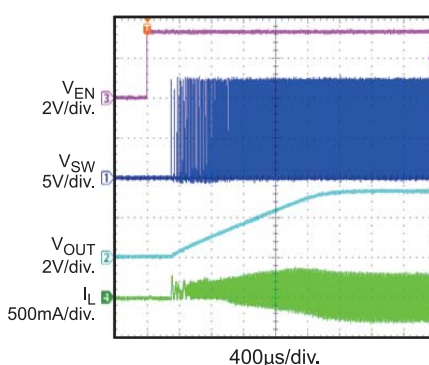
**Shutdown through  $V_{IN}$**   
 $I_{OUT} = 0A$



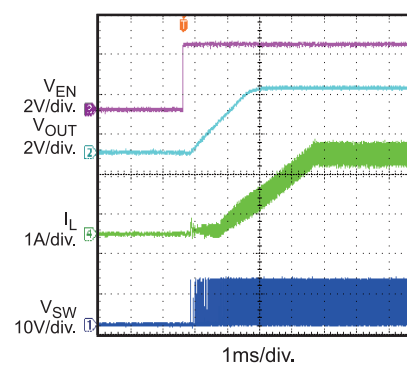
**Shutdown through  $V_{IN}$**   
 $I_{OUT} = 2A$



**Start-Up through EN**  
 $I_{OUT} = 0A$



**Start-Up Through EN**  
 $I_{OUT} = 2A$

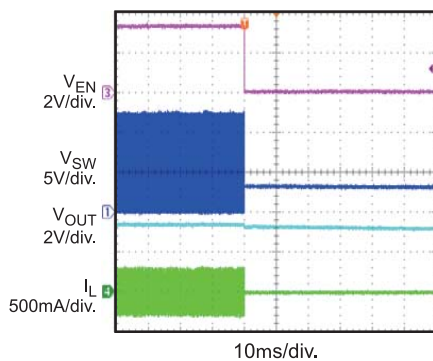


## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

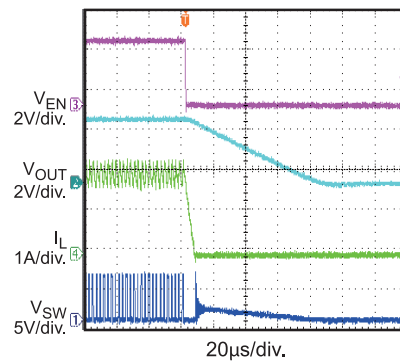
**Shutdown through EN**

$I_{OUT} = 0A$



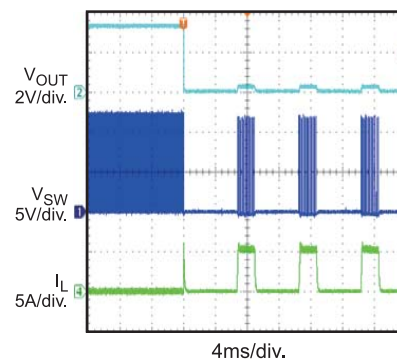
**Shutdown through EN**

$I_{OUT} = 2A$



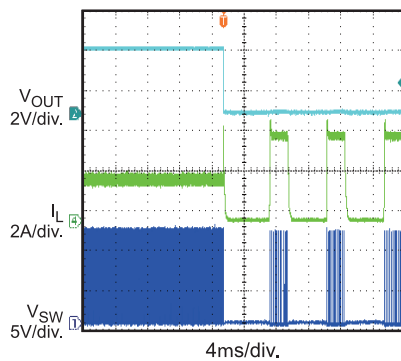
**SCP Entry**

$I_{OUT} = 0A$  to Short Circuit

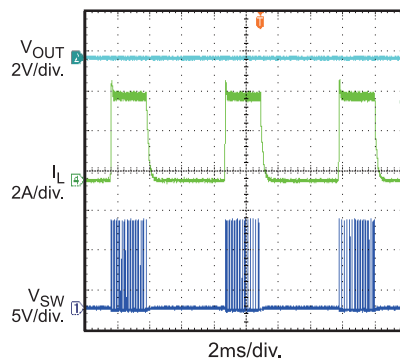


**SCP Entry**

$I_{OUT} = 2A$  to Short Circuit

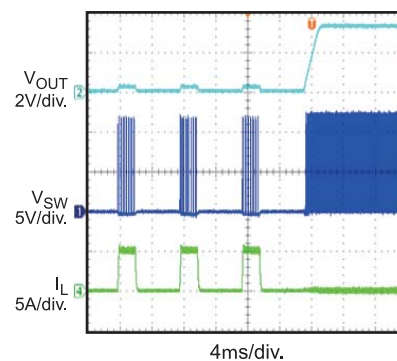


**SCP Steady State**



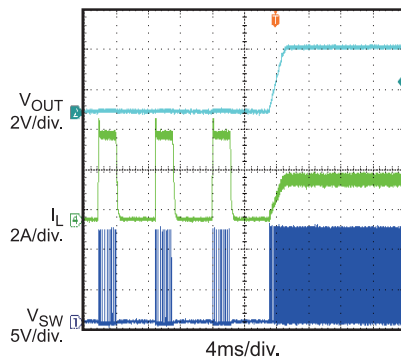
**SCP Recovery**

Short Circuit to  $I_{OUT} = 0A$



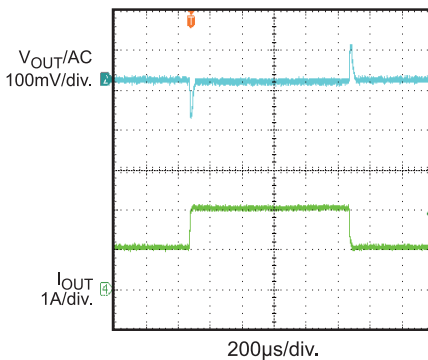
**SCP Recovery**

Short Circuit to  $I_{OUT} = 2A$



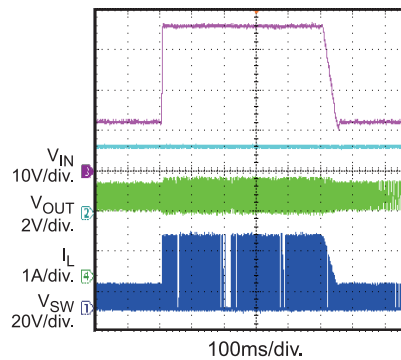
**Load Transient**

$I_{OUT} = 1A \leftrightarrow 2A$ ,  $1.6A/\mu s$



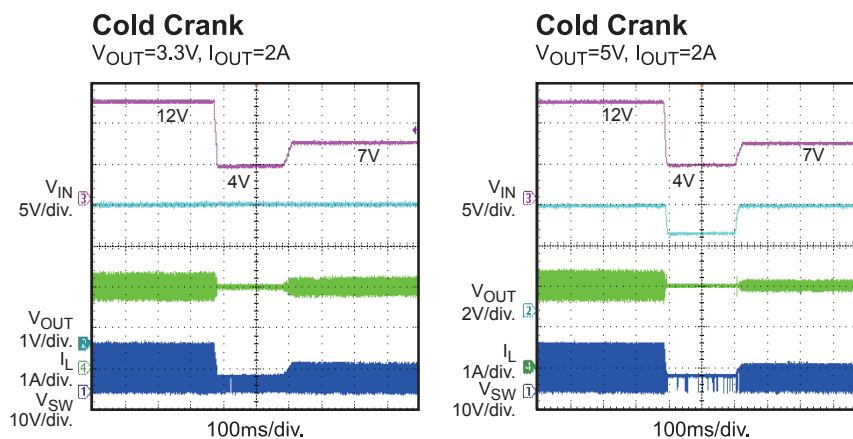
**Load Dump**

$V_{IN} = 12V \leftrightarrow 36V$ ,  $I_{OUT} = 2A$



## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.





## PRINTED CIRCUIT LAYOUT

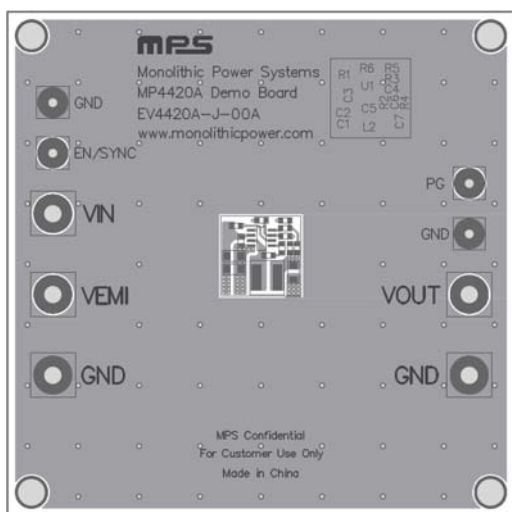


Figure 1: Top Silk Layer & Top Layer

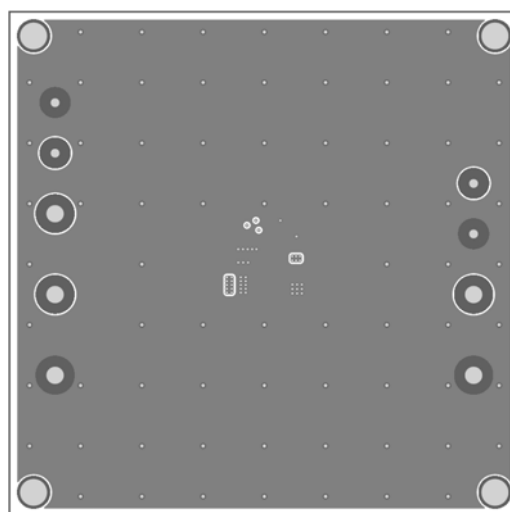


Figure 2: IN1 Layer

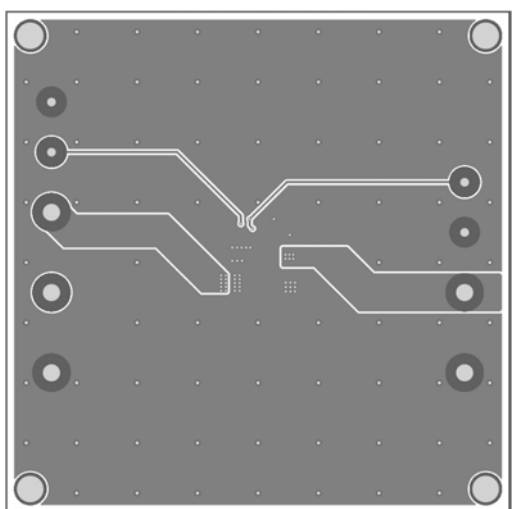


Figure 3: IN2 Layer

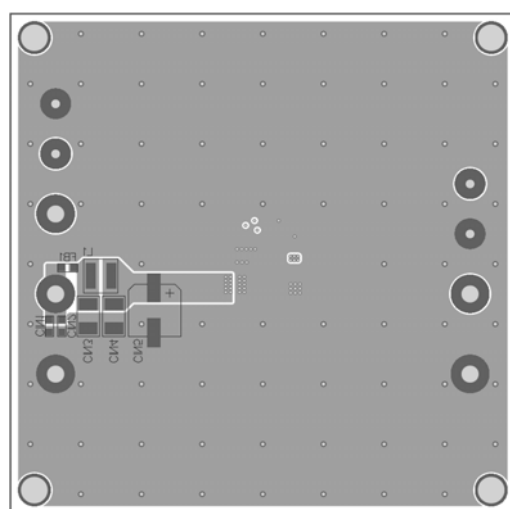


Figure 4: Bottom Silk Layer & Bottom Layer

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