# EV2770-L-00A

## 16V, 6A, I²C-Controlled, Single-Cell Switching Charger with Power Path Management and 3.65A Boost Output Evaluation Board

## DESCRIPTION

The EV2770-L-00A is an evaluation board designed to demonstrate the capabilities of the MP2770, a highly-integrated, flexible, switch-mode battery charge management and system power path management device. It is designed for single-cell, Li-ion and Li-polymer batteries used in a wide variety of portable applications.

The MP2770 has an integrated IN to SYS pass-through path to pass input voltage ($V_{IN}$) to the system, even while charging is disabled. When $V_{IN}$ is present, the device operates in charge mode. The MP2770 manages the input power and meets the majority of the system's power demand using its integrated input current limit ($I_{IN\_LIM}$) and $V_{IN}$ regulation function.

If $V_{IN}$ is not present, the MP2770 enters boost mode to power IN or SYS from the battery.

The IC can flexibly configure the charging and boost parameters via the I²C interface. These configurable parameters include the input clamp voltage, $I_{IN\_LIM}$, charge current ($I_{CHG}$), charger full voltage, boost output voltage ($V_{BST}$), and current limit ($I_{LIMIT}$).

The EV2770-L-00A supports 5V to 15V input sources, including standard USB host ports and wall adapters with fast charging capabilities.

The EV2770-L-00A supports boost output operation by supplying 4.3V to 16V with a maximum 3.65A load.

## PERFORMANCE SUMMARY (1)

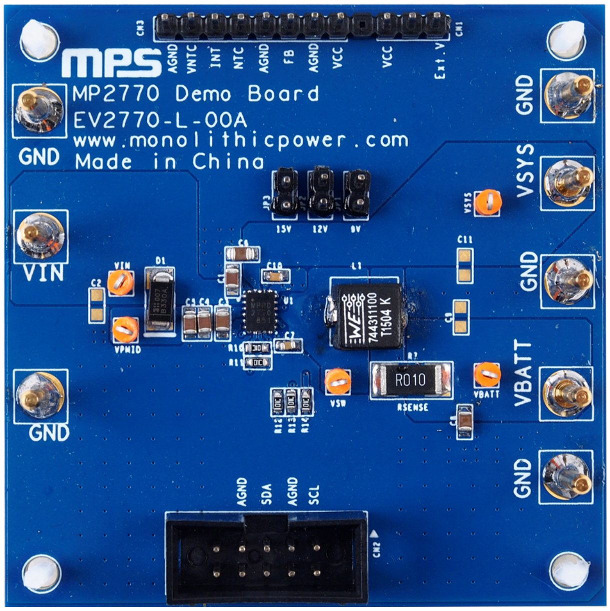
Specifications are at $T_A$ = 25°C, unless otherwise noted.

| Parameters | Conditions | Value |
|---|---|---|
| Input voltage ($V_{IN}$) range | | 4V to 16V |
| Battery voltage ($V_{BATT}$) | $V_{IN}$ = 5V to 15V, $I_{BATT}$ = 0.5A to 6A | 4.2V |
| Maximum battery current ($I_{BATT}$) | $V_{IN}$ = 5V to 15V | 6A |
| Typical charge efficiency | $V_{IN}$ = 9V, $V_{BATT}$ = 3.8V, $I_{BATT}$ = 3A | 93.7% |
| Peak charge efficiency | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{BATT}$ = 1.5A | 96.6% |
| Typical boost efficiency | $V_{IN}$ = 9V, $V_{BATT}$ = 3.8V, $I_{BST}$ = 2A | 92.8% |
| Peak boost efficiency | $V_{IN}$ = 5V, $V_{BATT}$ = 3.8V, $I_{BST}$ = 1A | 96.2% |
| Switching frequency ($f_{SW}$) | | 600kHz |

**Note:**

1) Efficiency data is tested on an EV2770-L-00A with a 1µH inductor and 10mΩ current-sense resistor.

## EVALUATION BOARD




**LxWxH (6.35cmx6.35cmx1.3cm)**

| Board Number | MPS IC Number |
|---|---|
| EV2770-L-00A | MP2770GL-0000 |

## QUICK START GUIDE

The EV2770-L-00A is designed to test the MP2770, which is used as a standalone switching charger with power path management and dual boost outputs on the battery side. The board also can work with the PD controller IC for USB Type-C detection and configuration, as well as USB A/B output detection and configuration. This GUI cannot be used to intrude the PD controller while working with the MP2770. It just describes how to evaluate the MP2770's operation using the EV2770-L-00A.

The board's layout can accommodate most commonly used capacitors. Its preset to charge mode by default, and the charger full voltage is preset to 4.2V for single-cell Li-ion batteries. The EV2770-L-00A can be used with the jumpers on the board (not connected to the I²C connector). Only CN2 should be connected to the I²C connector.

### Evaluation Board Set-Up

The following materials are required to use the evaluation board: a computer with at least one USB port, a USB cable, and a USB to I²C communication device (EVKT-USBI2C-02) (see Figure 1).


**Figure 1: USB to I²C Communication Interface**

1. Install the MP2770 GUI [2]. To check that the software is installed properly, open the GUI by clicking on the "MP2770 Evaluation Kit.exe" file.
2. Set up the measurement equipment for the MP2770 (see Figure 2).

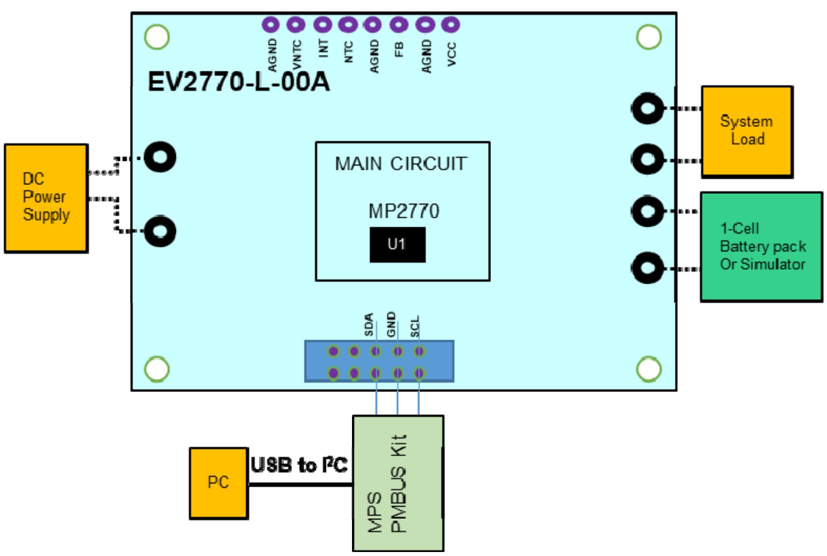



**Figure 2: Measurement Equipment Set-Up**

3. Launch the MP2770 evaluation software. Figure 3 on page 4 shows the MP2770 evaluation GUI.

**Note:**

2) The GUI can be downloaded from the MPS website.

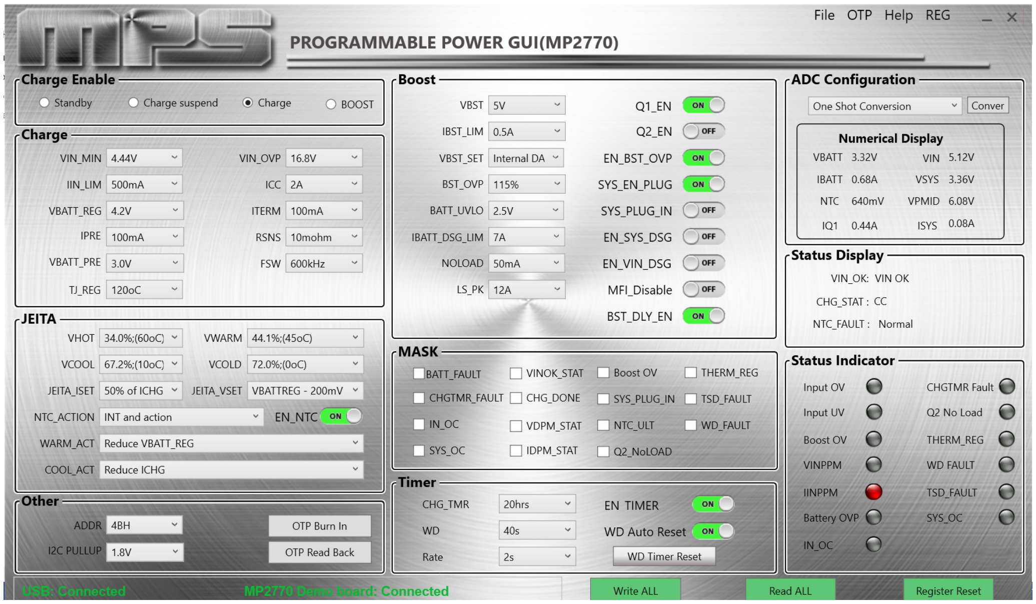



**Figure 3: MP2770 Evaluation GUI**

## PROCEDURE

Once the evaluation board is connected properly, follow the guidelines below to configure the MP2770:

1. Preset the input power supply and battery simulator to the proper values.
2. Turn on the battery simulator first, then turn on the power supply.
3. Float the SYS load connection, since Q2 is off in default mode.
4. Ensure that the USB to I²C communication interface and the EV2770-L-00A are connected correctly. The should be indicated at the bottom left with “USB: Connected” and “MP2770 Demo Board: Connected” in green (see Figure 3).
5. Select the MP2770’s operation mode (see Figure 4). After start-up, the IC operates in charge mode by default.

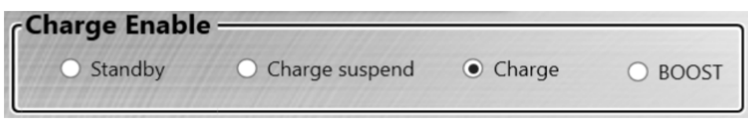



**Figure 4: MP2770 GUI Mode Selection**

6. Set the charging parameters (see Figure 5).

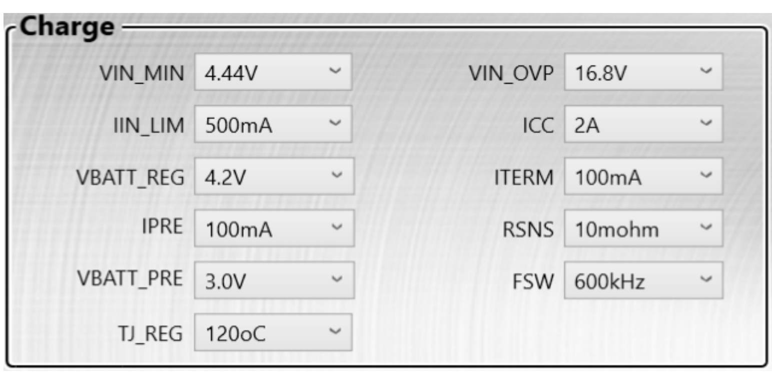



**Figure 5: MP2770 Charging Parameters Setting**

a. VIN_MIN: The minimum input voltage ($V_{IN}$) can be set between 3.12V and 18.36V, with 12mV/step. VIN_MIN is set to 4.44V by default.

b. IIN_LIM: The input current limit ($I_{IN\_LIM}$) can be set to 500mA, 900mA, 1000mA, 1200mA, 1500mA, 1800mA, 2000mA, 2100mA, 2400mA, 2800mA, 3000mA, 3200mA, or 3500mA, depending on the adapter inserted to comply with the power delivery (PD) controller specifications. IIN_LIM is set to 500mA by default.

c. VBATT_REG: VBATT_REG can be set to 3.6V, 4.1V, 4.15V, 4.2V, 4.3V, 4.35V, 4.4V, or 4.45V. VBATT_REG is set to 4.2V by default.

d. IPRE: The pre-charge current ($I_{PRE}$) can be set to 50mA, 100mA, 200mA, or 400mA. IPRE is set to 100mA by default.

e. VBATT_PRE: The battery pre-charge threshold ($V_{BATT\_PRE}$) is the $V_{BATT}$ threshold when the device exits pre-charge mode and enters constant current (CC) charge mode. VBATT_PRE can be set to 2.5V, 2.8V, or 3V. VBATT_PRE is set to 3V by default.

f. TJ_REG: If the junction temperature ($T_J$) reaches the thermal regulation threshold ($T_{J\_REG}$), then the IC enters thermal regulation, and the charge current ($I_{CHG}$) decreases to reduce power loss and keep $T_J$ from exceeding $T_{J\_REG}$. TJ_REG can be set to 60°C, 80°C, 100°C, or 120°C. TJ_REG is set to 120°C by default.

g. VIN_OVP: The MP2770 has wide 4V to 16V $V_{IN}$ range. The device can limit this threshold by lowering the $V_{IN}$ over-voltage protection (OVP) threshold ($V_{IN\_OVP}$). VIN_OVP can be set to 6.4V, 11.2V, 14V, or 16.8V. Also when The MP2770 can also be configured an as output source for the PD controller, and can provide the proper $V_{IN\_OVP}$ for the load according to the sink requirement. VIN_OVP is set to 16.8V by default.

h. ICC: The fast charge current ($I_{CC}$) can be set between 0.5A and 6A, with 0.1A/step. ICC is set to 2A by default.

i. ITERM: The charge termination current ($I_{TERM}$) can be set to 50mA, 100mA, 200mA, or 400mA. ITERM is set to 100mA by default.

j. RSNS: The internal sense resistor can be set to 5mΩ or 10mΩ. RSNS is set to 10mΩ by default. If RSNS is set to 5mΩ, the ICC value is halved in operation.

k. FSW: The switching frequency ($f_{SW}$) can be set to 500kHz, 800kHz, or 1MHz. FSW is set to 600kHz by default.

7. Set the JIETA parameters (see Figure 6).

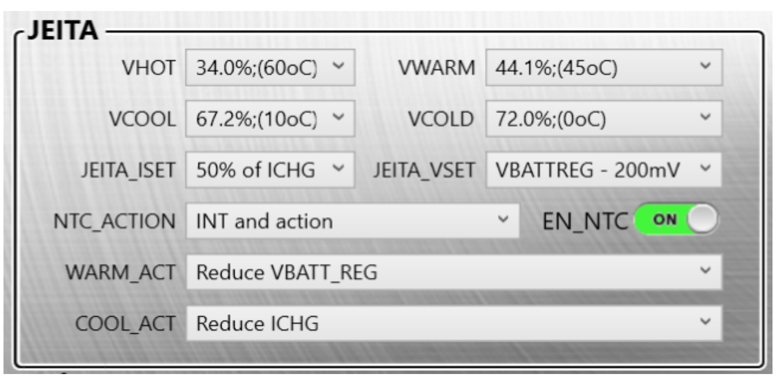



**Figure 6: MP2770 GUI JIETA Setting**

a. EN_NTC: The EN_NTC control enables and disables the MP2770's NTC function. EN_NTC is enabled by default. If EN_NTC is disabled, the VNTC voltage is not present, and the NTC function is disabled.

b. NTC_ACTION: The NTC_ACTION bit has two setting options: "INT and action" and "issue INT". NTC_ACTION is set to "INT and action" by default. When NTC_ACTION is set to "INT and action", an INT signal is generated when the NTC voltage ($V_{NTC}$) changes to a different voltage range, and the IC acts as the JIETA requirement (set via the GUI). If NTC_ACTION is set to "issue INT", an "INT" signal is generated when $V_{NTC}$ changes to a different voltage range. There is not action from the IC.

c. VHOT, VWARM, VCOOL, and VCOLD: The NTC hot, warm, cool, and cold falling thresholds threshold ($V_{HOT}$, $V_{WARM}$, $V_{COOL}$, and $V_{COLD}$, respectively) each have two bits that provide four threshold settings. Users can select a value according to an NTC thermistor and the required JIETA temperature. Contact an MPS FAE to use this information to calculate the appropriate JIETA design value.

d. JEITA_ISET: The JEITA_ISET bit can be set to 0%, 10%, 20%, or 50% of $I_{CHG}$. JEITA_ISET is set to 50% of $I_{CHG}$ by default. If $I_{CHG}$ should be lower during the NTC warm or cool period, this bit selects how much $I_{CHG}$ decreases.

e. JEITA_VSET: The JEITA_VSET bit can be set to ($V_{BATT\_REG}$ - 100mV), ($V_{BATT\_REG}$ - 150mV), ($V_{BATT\_REG}$ - 200mV), or ($V_{BATT\_REG}$ - 250mV). JEITA_VSET is set to ($V_{BATT\_REG}$ - 200mV) by default. If $V_{BATT\_REG}$ should be lower during the NTC warm or cool period, this bit selects how much $V_{BATT\_REG}$ decreases.

f. WARM_ACT and COOL_ACT: Both the WARM_ACT and COOL_ACT bits have four setting options: "no action", "reduce VBATT_REG", "reduce ICHG", and "reduce both VBATT_REG and ICHG while NTC is warm or cool". The default action during the NTC warm period is to reduce $V_{BATT\_REG}$. The default action during the NTC cool period is to reduce $I_{CHG}$.

8. Set the timer parameters (see Figure 7).


**Figure 7: MP2770 GUI Timer Setting**

The charger safety timer (CHG_TMR) can be enabled and disabled by the EN_TIMER control bit. CHG_TMR can be set to 5hrs, 10hrs, 15hrs, or 20hrs. CHG_TMR is set to 20hrs by default. The watchdog timer (WD) can be set to 40s, 80s, or 160s. The WD functions can be enabled and disabled by the WD setting.

9. Set the boost mode parameters (see Figure 8 on page 6). The parameter setting bits are in the left column, and the control bits are in the right column.

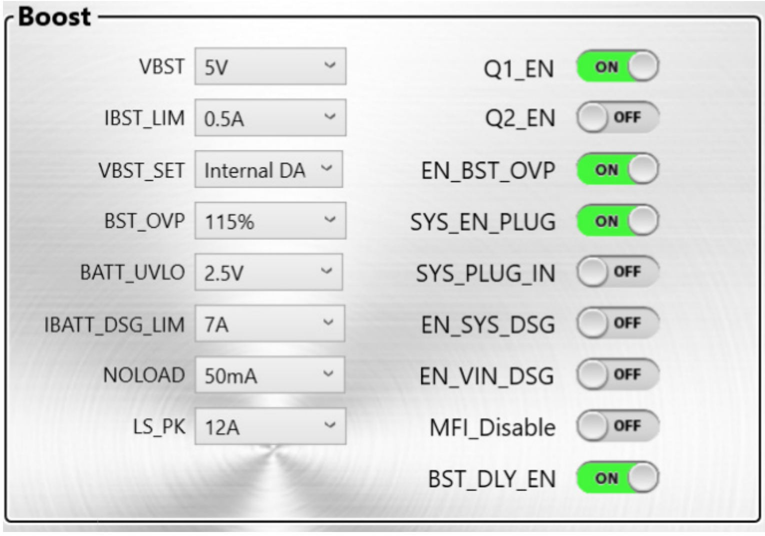



**Figure 8: MP2770 GUI Boost Parameter Setting**

***Control Bits***

a. Q1_EN: The QI_EN bit enables Q1, which controls the IN output port. It is enabled by default.

b. Q2_EN: The Q2_EN bit enables Q2, which controls the SYS output port. It is disabled by default.

c. EN_BST_OVP: The boost OVP function is enabled by default. It is recommended to disable the boost OVP function during evaluation to avoid triggering boost OVP while conducting transient tests.

d. SYS_EN_PLUG: The SYS_EN_PLUG bit is enabled by default. Disable SYS_EN_PLUG during evaluation.

e. SYS_PLUG_IN: The SYS_PLUG_IN bit is not a control bit. SYS_PLUG_IN is the system (SYS) plug-in detection function. If SYS_PLUG_IN shows “ON”, then that means a SYS plug in has been detected. Write 0 to SYS_PLUG_IN to clear this bit when the SYS plug-in detection function is disabled.

f. EN_SYS_DSG: SYS_DSG is the dummy load at the SYS pin. It is disabled by default.

g. EN_VIN_DSG: VIN_DSG is the dummy load at the IN pin. It is disabled by default.

h. MFI_DISABLE: When the MFI function is enabled, the MP2770 can maintain a normal boost output voltage ($V_{BST}$) for 2ms if the boost output current ($I_{BST}$) is between the IBST_LIM setting and (1.6 x IBST_LIM). The MFI function can be disabled by setting this bit to “ON”. It is set to “OFF” by default.

i. BST_DLY_EN: After the boost control code is sent, there is 30ms delay before boost operation begins. The BST_DLY_EN enables this delay function. This delay can be disabled by setting BST_DLY_EN to “OFF”. It is set to “ON” by default.

***Parameter Settings***

a. VBST: VBST sets $V_{BST}$. $V_{BST}$ can be set between 4.3V and 16V, with 20mV/step. VBST is set to 5V by default.

b. IBST_LIM: IBST_LIM sets the boost output current limit ($I_{BST\_LIM}$). $I_{BST\_LIM}$ can be set between 0.5A and 3.65A, with 50mA/step. IBST_LIM is set to 0.5A by default.

c. VBST_SET: $V_{BST}$ can be set by an internal digital-to-analog converter (DAC) via the VBST register or by an external feedback (FB) resistor divider. The EV2770-L-00A provides four external settings with R3, R4, R5, and R2 (5V, 9V, 12, and 15V). There are three jumpers to set $V_{BST}$ (see Table 1)

**Table 1: Setting $V_{BST}$ via the External FB Setting**

| Jumper | $V_{BST}$ | Factory Setting |
|---|---|---|
| JP1 | 9V | NC |
| JP2 | 12V | NC |
| JP3 | 15V | NC |

When all three jumpers are not connected, $V_{BST}$ is set to 5V by default.

d. BST_OVP: BST_OVP sets the boost OVP threshold ($V_{BST\_OVP}$). $V_{BST\_OVP}$ can be set to 110%, 115%, or 120% of $V_{BST}$. BST_OVP is set to 115% by default.

e. BATT_UVLO: In discharge mode, the IC shuts down if the $V_{BATT}$ drops below the $V_{BATT}$ UVLO falling threshold. This threshold can be set to 2.5V or 2.7V. BATT_UVLO is set to 2.5V by default.

f. IBATT_DSG_LIM: The battery current ($I_{BATT}$) is sensed and compared. If $I_{BATT}$ reaches the battery discharge current limit ($I_{BATT\_DSG\_LIM}$), then it is limited to this value as the load continues to increase and $V_{BST}$ decreases. $I_{BATT\_DSG\_LIM}$ can be set between 5A and 8A, with 0.5A/step. $I_{BATT\_DSG\_LIM}$ can also be disabled via the IBATT_DSG_LIM setting.

g. NOLOAD: No load detection only applies to the Q2-controlled output (when SYS is connected to the load), so no load detection is only valid when Q2 is enabled. When the SYS port load drops to the no load detection threshold, the Q2_NO_LOAD status bit is set and is indicated in the GUI. This threshold can be set to one of four options (25mA, 50mA, 75mA, or 100mA), with 25mA/step. NOLOAD is set to 50mA by default.

h. LS_PK: LS_PK sets the low-side MOSFET (LS-FET) peak current limit ($I_{LS\_PK}$). If $I_{BATT\_DSG\_LIM}$ is disabled, then $I_{LS\_PK}$ limits the peak inductor current ($I_L$) to protect the IC from operating at currents outside of the safe range. $I_{LS\_PK}$ can be set to 12A or 10.5A. LS_PK is det to 12A by default.

10. Configure the analog-to-digital converter (ADC) (see Figure 9).

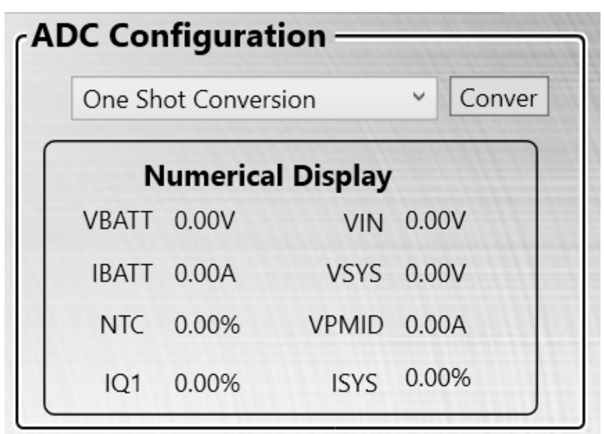



**Figure 9: MP2770 GUI ADC Configuration**

The ADC always works in charge mode or boost mode. In standby mode or when only the battery is present, the ADC function can be set to one-shot conversion or continuous conversion. When the ADC is set to one-shot conversion, this bit does a one-time ADC conversion. When it is set to continuous conversion, the ADC is always in conversion after start-up.

11. After parameters are set, connect the power supply terminals to:
    a. Positive (+): VIN
    b. Negative (-): GND
12. Connect the battery terminals to:
    a. Positive (+): VBATT
    b. Negative (-): GND
13. After making the connections, turn on the power supply.
14. Record the waveform from the test points on the board.

Figure 10 shows the status GUI window, which displays the IC operation status.

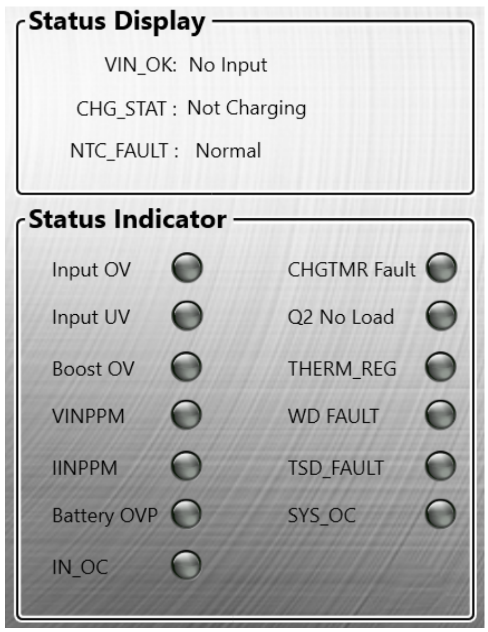



**Figure 10: MP2770 GUI Status Display and Indicator**

# EVALUATION BOARD SCHEMATIC

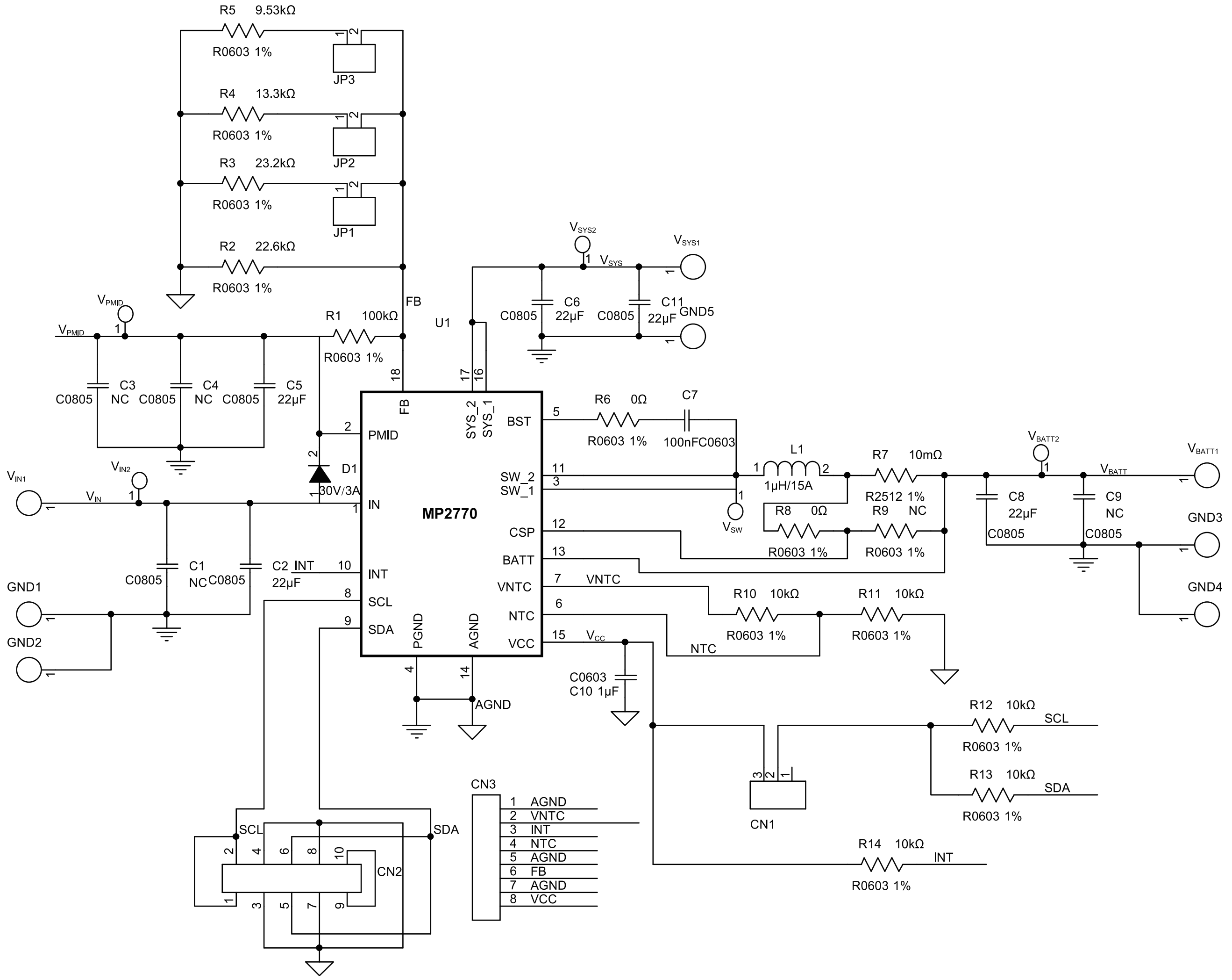



**Figure 2: Evaluation Board Schematic**

# EV2770-L-00A BILL OF MATERIALS

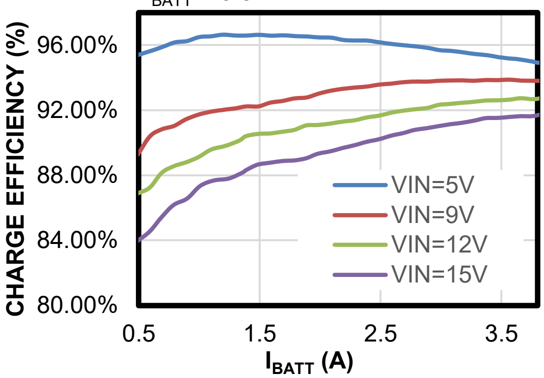
| Qty | Ref | Value | Description | Package | Manufacturer | Manufacturer PN |
|---|---|---|---|---|---|---|
| 6 | C1, C3, C4, C5, C6, C8 | 22µF | Ceramic capacitor, 25V, X5R | 0805 | Murata | GRM21BR61E226ME44L |
| 3 | C2, C9, C11 | NC | | | | |
| 1 | C7 | 100nF | Ceramic capacitor, 25V, X7R | 0603 | Murata | GCJ188R71E104KA12D |
| 1 | C10 | 1µF | Ceramic capacitor, 25V, X7R | 0603 | Murata | GCM188R71E105KA64D |
| 1 | R1 | 100kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-07100KL |
| 1 | R2 | 22.6kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-0722K6L |
| 1 | R3 | 23.2kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-0723K2L |
| 1 | R4 | 13.3kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-0713K3L |
| 1 | R5 | 9.53kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-079K53L |
| 2 | R6, R8 | 0Ω | Film resistor, 1% | 0603 | Yageo | RC0603FR-070RL |
| 1 | R7 | 10mΩ | Film resistor, 1%, 2W | 2512 | Yageo | RL2512FR-070R01L |
| 1 | R9 | NC | | | | |
| 2 | R10, R11 | 10kΩ | Film resistor, 1% | 0603 | Yageo | RC0603FR-0710KL |
| 3 | R12, R13, R14 | 10kΩ | Film resistor, 5% | 0603 | Yageo | RC0603JR-0710K |
| 1 | L1 | 1µH | Inductor, 1µH, 4.6mΩ, 15A | SMD | Wurth | 744311100 |
| 1 | D1 | 30V | Schottky diode, 3A | SMA | Diodes | B330A |
| 1 | CN1 | 3-pin | 2.54mm connector | DIP | Any | |
| 1 | CN2 | 5-pin | Header, I$^2$C connector, dual-row | DIP | Any | |
| 1 | CN3 | 8-pin | 2.54mm connector | DIP | Any | |
| 3 | JP1, JP2, JP3 | 2-pin | 2.54mm connector | DIP | Any | |
| 5 | VIN, VPMID, VSYS, VBATT, VSW | 1-pin | Test point | DIP | Any | |
| 8 | GND, VIN, GND, GND, VSYS, GND, VBATT, GND | 1-pin | 2.0mm male needle | DIP | Any | |
| 1 | U1 | MP2770 | Single-cell switching charger | QFN | MPS | MP2770R2 |

## EVB TEST RESULTS

**Performance curves and waveforms are tested on the evaluation board. $V_{IN}$ = 5V to 15V, $V_{BATT}$ = 3.8V, $T_A$ = 25°C, unless otherwise noted.**

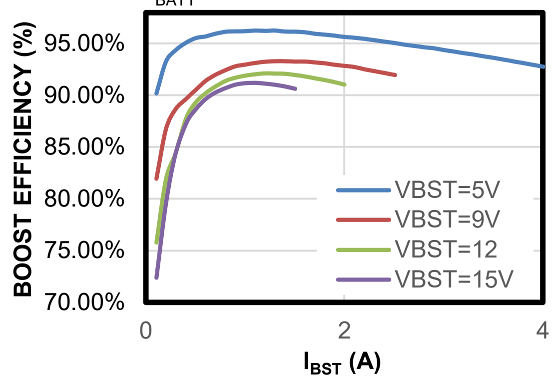
**Charge Efficiency vs. $I_{BATT}$**

$V_{BATT}$ = 3.8V



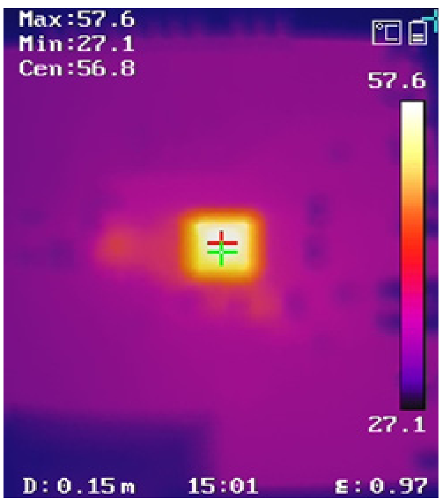

**Boost Efficiency vs. $I_{BST}$**

$V_{BATT}$ = 3.8V



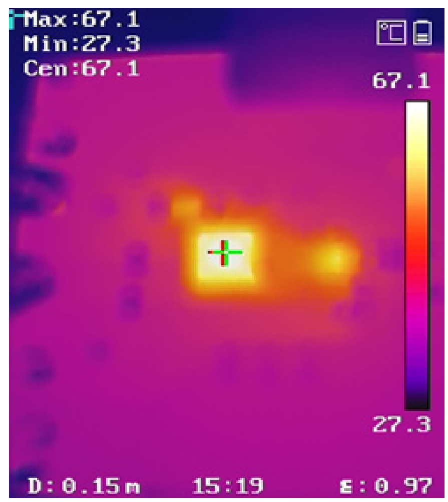

**Thermal Performance**

Charge mode, $V_{IN}$ = 15V, $V_{BATT}$ = 3.8V, $I_{BATT}$ = 3A, no forced airflow, $T_{CASE}$ = 57.6°C




**Thermal Performance**

Boost mode, $V_{BST}$ = 15V, $V_{BATT}$ = 3.8V, $I_{BST}$ = 1.5A, no forced airflow, $T_{CASE}$ = 67.1°C

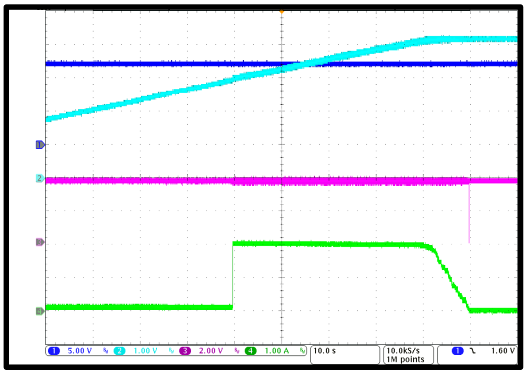


## EVB TEST RESULTS

**Performance curves and waveforms are tested on the evaluation board. $V_{IN}$ = 5V to 15V, $V_{BATT}$ = 0V to 4.2V, $T_A$ = 25°C, unless otherwise noted.**

### Battery Charge Curve

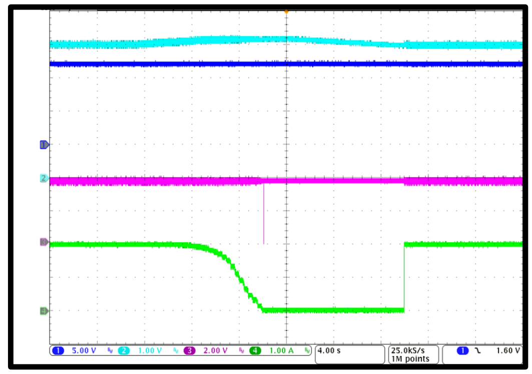
$V_{IN}$ = 12V, $V_{BATT\_REG}$ = 4.2V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA



CH1: $V_{PMID}$
CH2: $V_{BATT}$
CH3: $V_{INT}$
CH4: $I_{BATT}$

### Auto-Recharge

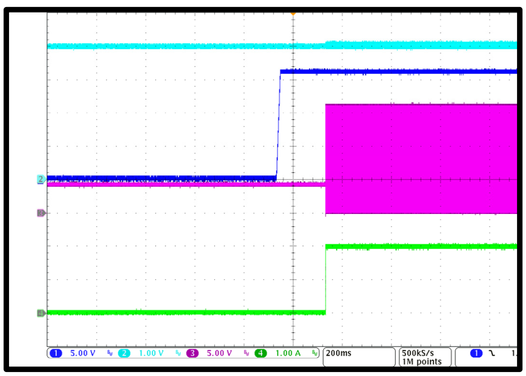
$V_{IN}$ = 12V, $V_{BATT\_REG}$ = 4.2V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA



CH1: $V_{PMID}$
CH2: $V_{BATT}$
CH3: $V_{INT}$
CH4: $I_{BATT}$

### Start-Up through VIN

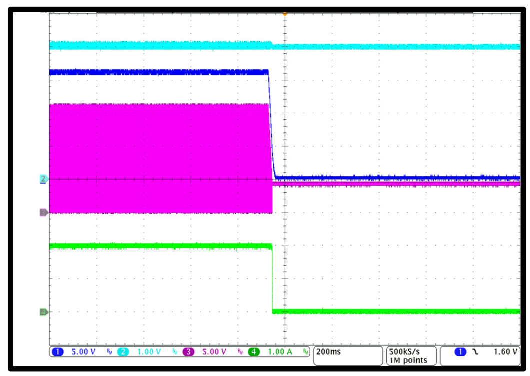
$V_{IN}$ = 16V, $V_{BATT}$ = 4V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA



CH1: $V_{IN}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$

### Shutdown through VIN

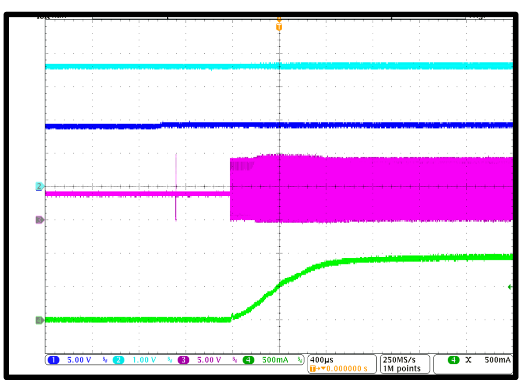
$V_{IN}$ = 16V, $V_{BATT}$ = 4V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA



CH1: $V_{IN}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$

### Start-Up through Q1

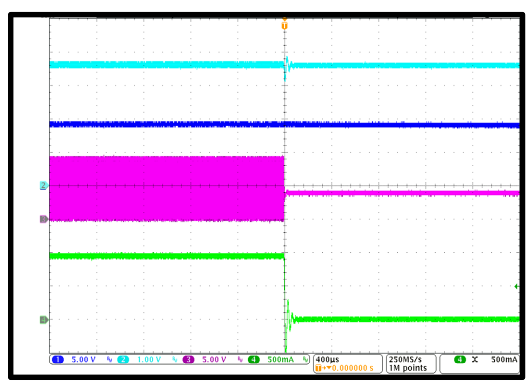
Charge mode, $V_{IN}$ = 9V, $V_{BATT}$ = 3.6V, $I_{CC}$ = 2A



CH1: $V_{PMID}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$

### Shutdown through Q1

Charge mode, $V_{IN}$ = 9V, $V_{BATT}$ = 3.6V, $I_{CC}$ = 2A



CH1: $V_{PMID}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$

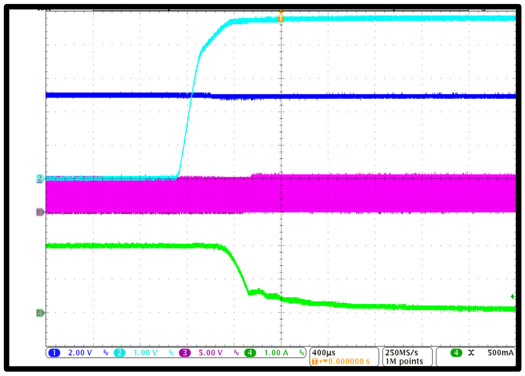
## EVB TEST RESULTS *(continued)*

**Performance curves and waveforms are tested on the evaluation board. $V_{IN}$ = 5V to 15V, $V_{BATT}$ = 0 to 4.2V, $T_A$ = 25°C, unless otherwise noted.**

### Start-Up through Q2

Charge mode, $V_{IN}$ = 5V, $V_{BATT}$ = 3.6V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA, $I_{SYS}$ = 3A

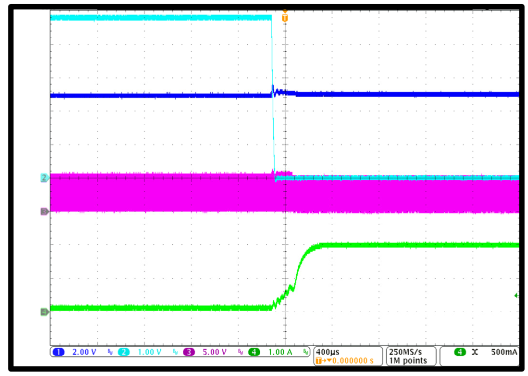
CH1: $V_{PMID}$
CH2: $V_{SYS}$
CH3: $V_{SW}$
CH4: $I_{BATT}$



### Shutdown through Q2

Charge mode, $V_{IN}$ = 5V, $V_{BATT}$ = 3.6V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA, $I_{SYS}$ = 3A

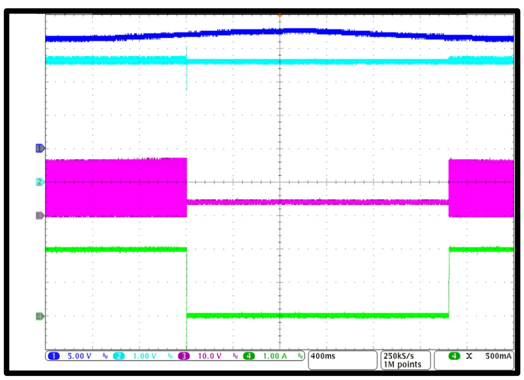
CH1: $V_{PMID}$
CH2: $V_{SYS}$
CH3: $V_{SW}$
CH4: $I_{BATT}$



### $V_{IN}$ OVP

Charge mode, $V_{IN}$ = 16V, $V_{BATT}$ = 3.6V, $I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA, $V_{IN\_OVP}$ = 16.8V

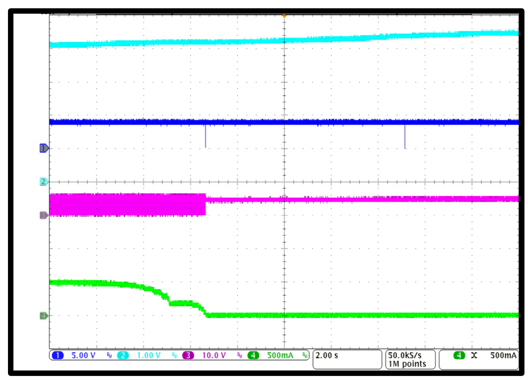
CH1: $V_{IN}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$



### $V_{BATT}$ OVP

Charge mode, $V_{IN}$ = 5V, $V_{BATT}$ = up to 4.4V, $I_{CC}$ = 2A

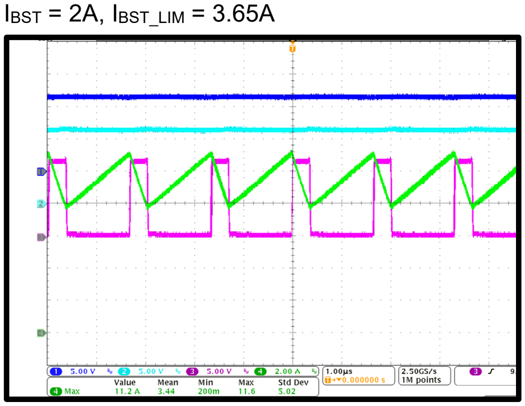
CH1: $V_{INT}$
CH2: $V_{BATT}$
CH3: $V_{SW}$
CH4: $I_{BATT}$



### Boost Mode Steady State

Boost mode, $V_{BST}$ = 12V, $V_{BATT}$ = 3V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A

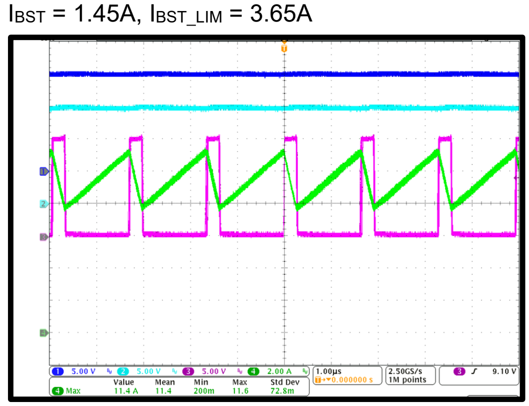
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_L$



### Boost Mode Steady State

Boost mode, $V_{BST}$ = 15V, $V_{BATT}$ = 3V, $I_{BST}$ = 1.45A, $I_{BST\_LIM}$ = 3.65A

CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_L$



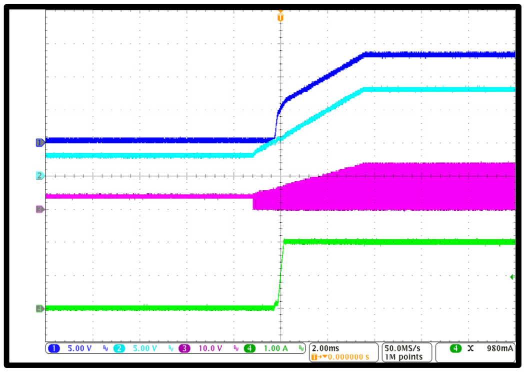
## EVB TEST RESULTS *(continued)*

**Performance curves and waveforms are tested on the evaluation board. $V_{IN}$ = 5V to 15V, $V_{BATT}$ = 0 to 4.2V, $T_A$ = 25°C, unless otherwise noted.**

### Boost On (Single-Output)

Boost mode, $V_{BST}$ = 15V, $V_{BATT}$ = 3.5V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A

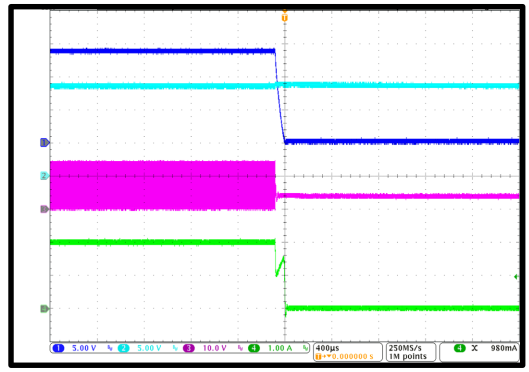
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_{BST}$



### Boost Off (Single-Output)

Boost mode, $V_{BST}$ = 15V, $V_{BATT}$ = 3.5V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A

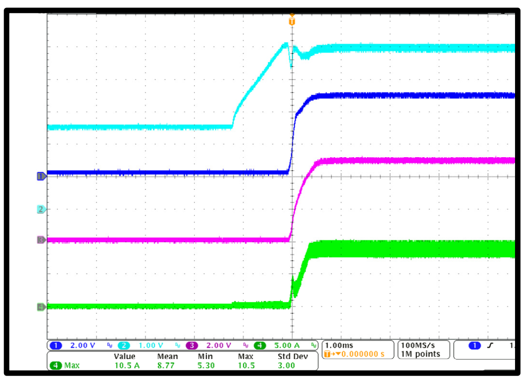
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_{BST}$



### Boost On (Dual-Output)

Boost mode, $V_{BST}$ = 5V, $V_{BATT}$ = 3V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A, Q2 is on, $I_{SYS}$ = 2A

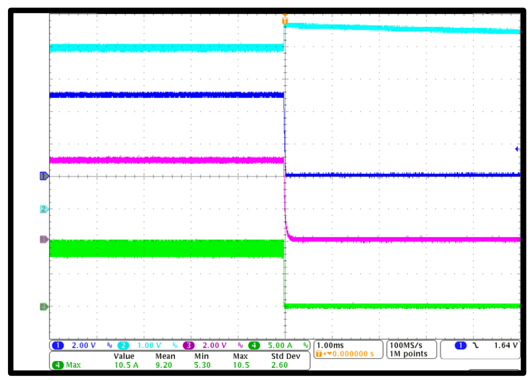
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SYS}$
CH4: $I_L$



### Boost Off (Dual-Output)

Boost modem $V_{BST}$ = 5V, $V_{BATT}$ = 3V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A, Q2 is on, $I_{SYS}$ = 2A

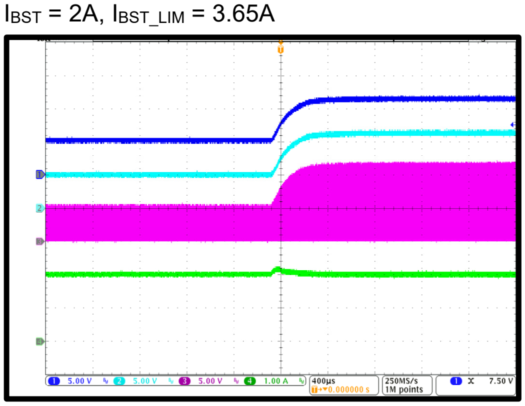
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SYS}$
CH4: $I_L$



### Boost Voltage Transient

Boost mode, $V_{BST}$ = 5V to 12V, $V_{BATT}$ = 3V, $I_{BST}$ = 2A, $I_{BST\_LIM}$ = 3.65A

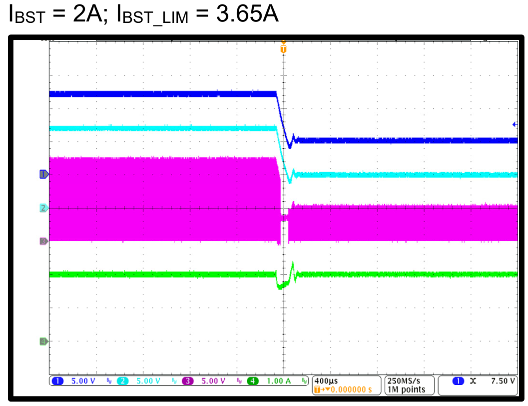
CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_{BST}$



### Boost Voltage Transient

Boost mode, $V_{BST}$ = 12V to 5V, $V_{BATT}$ = 3V, $I_{BST}$ = 2A; $I_{BST\_LIM}$ = 3.65A

CH1: $V_{IN}$
CH2: $V_{PMID}$
CH3: $V_{SW}$
CH4: $I_{BST}$

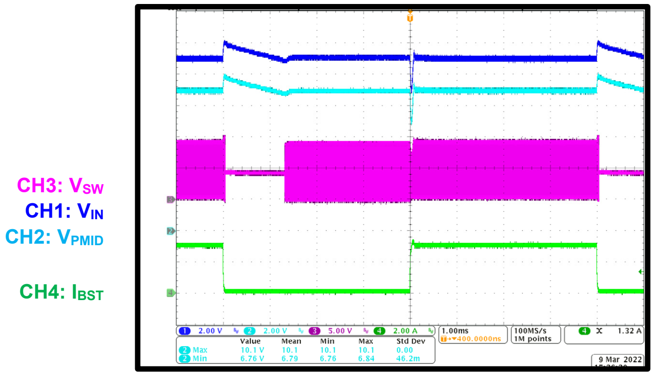


## EVB TEST RESULTS *(continued)*

**Performance curves and waveforms are tested on the evaluation board. $V_{IN}$ = 5V to 15V, $V_{BATT}$ = 0 to 4.2V, $T_A$ = 25°C, unless otherwise noted.**

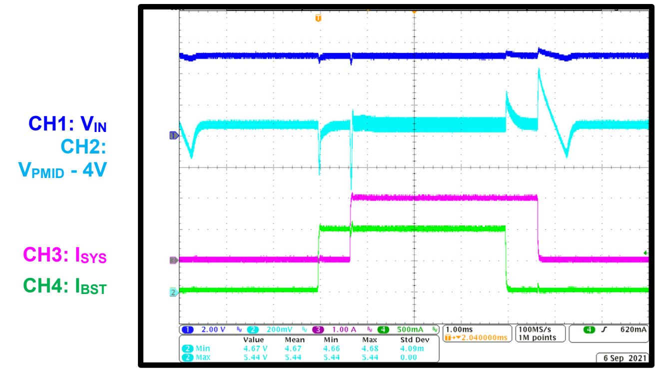
**Boost Load Transient (Single Output)**

Boost mode, $V_{BST}$ = 9V, $V_{BATT}$ = 4V,
$I_{BST}$ = 0A to 3A, $I_{BST\_LIM}$ = 3.65A



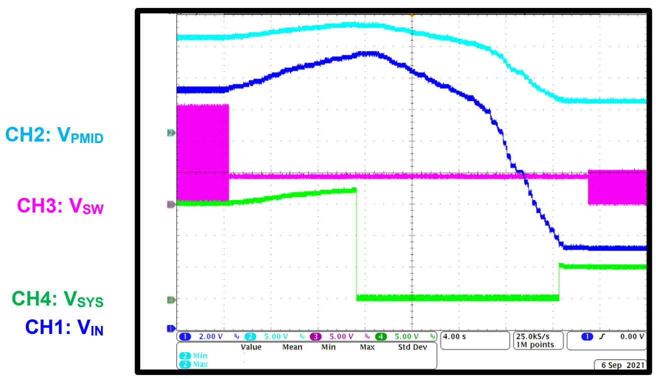

**Boost Load Transient (Dual Output)**

Boost mode, $V_{BST}$ = 5V, $V_{BATT}$ = 3V,
$I_{BST}$ = 0A to 1A, $I_{BST\_LIM}$ = 3.65A, Q2 is enabled,
$I_{SYS}$ = 0A to 2A



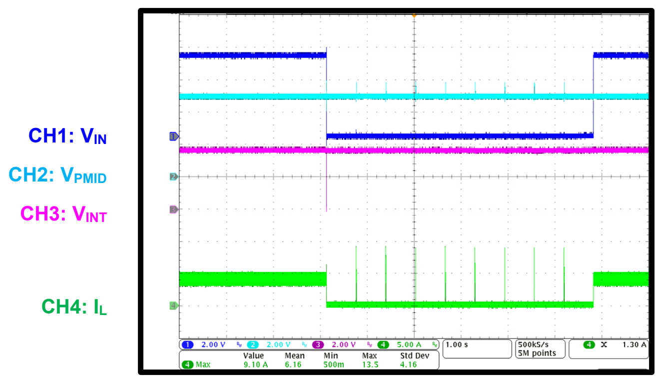

**Boost OVP**

Boost mode, $V_{BST}$ = 15V, $V_{BATT}$ = 4V,
$I_{BST}$ = 100mA, $I_{BST\_LIM}$ = 3.65A, Q2 is enabled,
$I_{SYS}$ = 100mA



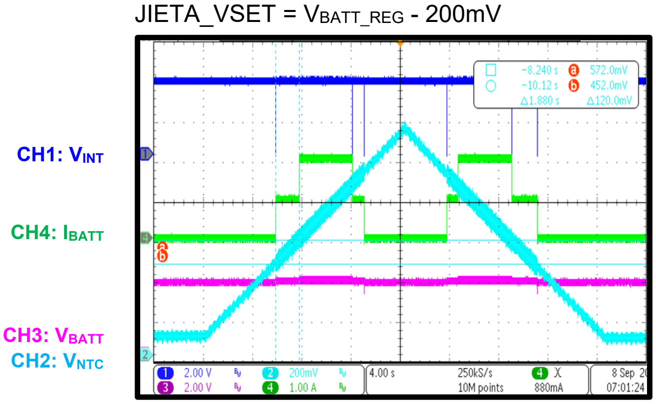

**Boost Load SCP**

Boost mode, $V_{BST}$ = 5V, $V_{BATT}$ = 4V, $I_{BST}$ = 3A,
$I_{BST\_LIM}$ = 3.65A



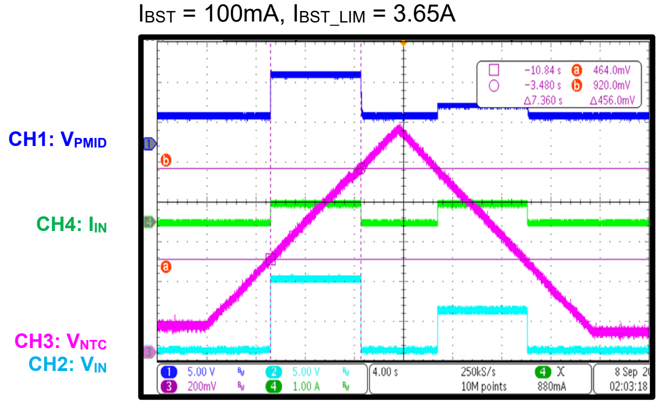

**NTC Function in Charge Mode**

Charge mode, $V_{IN}$ = 5V, $V_{BATT}$ = 3.5V,
$I_{CC}$ = 2A, $I_{IN\_LIM}$ = 3500mA, JIETA_ISET = 50%,
JIETA_VSET = $V_{BATT\_REG}$ - 200mV




**NTC Function in Boost Mode**

Boost mode, $V_{BST}$ = 9V, $V_{BATT}$ = 4V,
$I_{BST}$ = 100mA, $I_{BST\_LIM}$ = 3.65A



## PCB LAYOUT

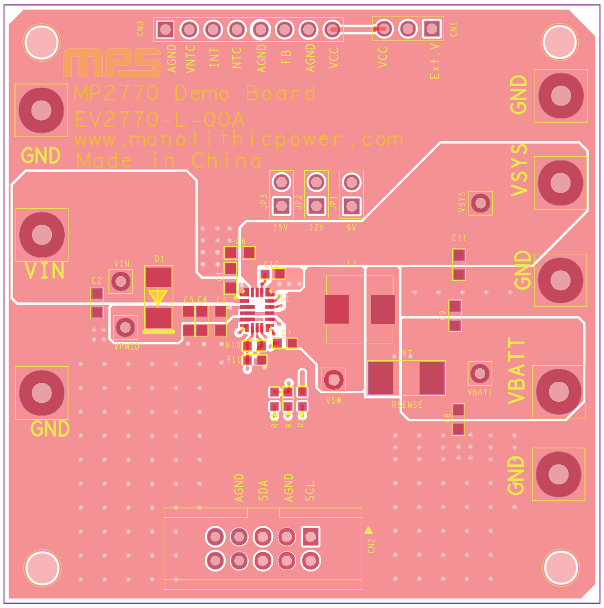



Figure 3: Top Silk and Top Layer

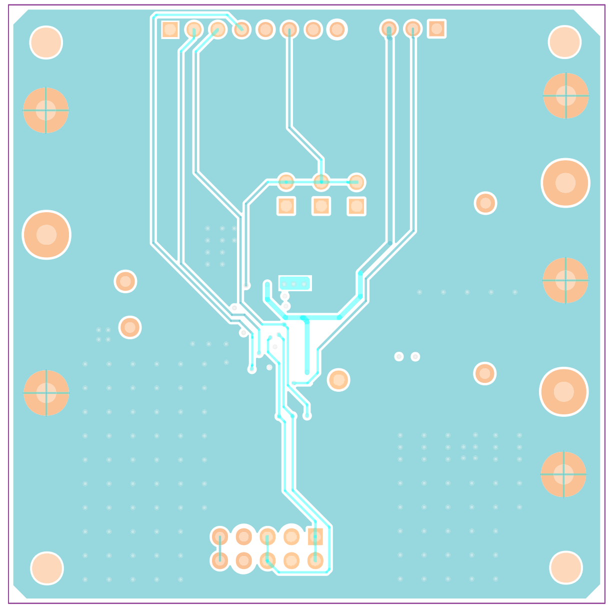


Figure 4: Mid-Layer 1

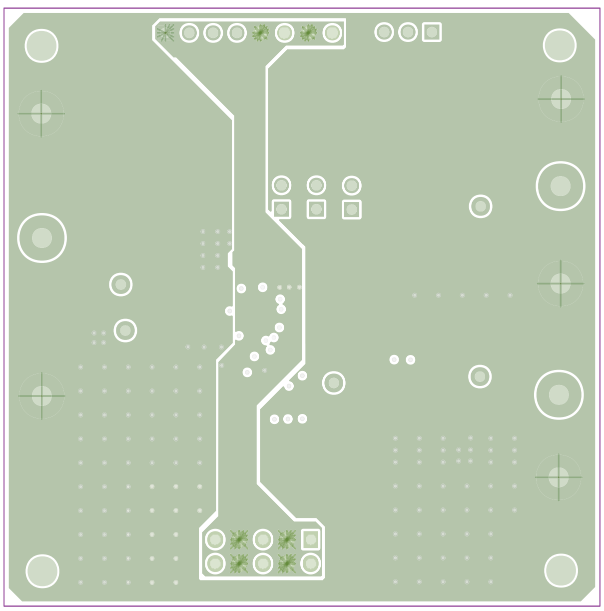


Figure 5: Mid-Layer 2

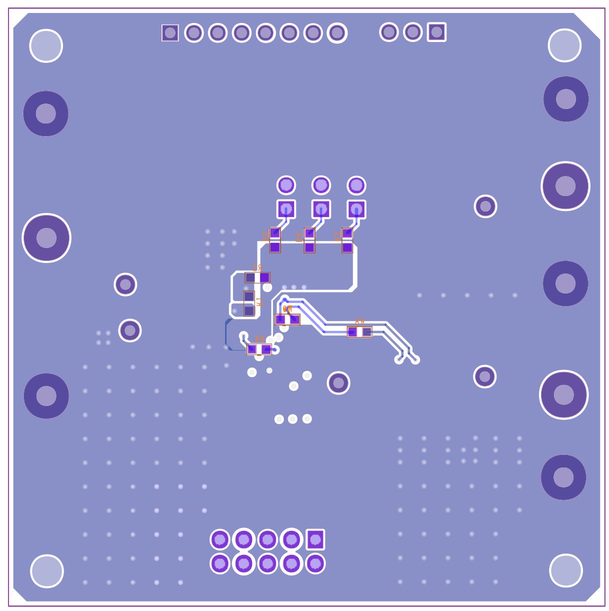


Figure 6: Bottom Layer