XU-AWG

PCI Express XMC Module with two 12 GSPS DACs

V2.2

FEATURES

Two 16-bit DAC channels:

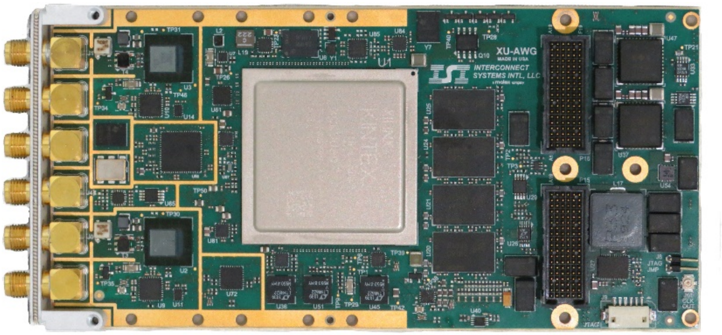
- AD9162 DAC supports enhanced 2nd and 3rd Nyquist and "Frequency Doubling" 2x Modes
- Single-Ended AC-Coupled Outputs with Programmable DC Bias
- Digital Inverse Sinc Filter
- 48-Bit NCO
- Fixed Deterministic Latency
- Interpolation Filters: 1x (bypass mode), 2x, 3x, 4x, 6x, 8x,12x,16x, 24x
- Internal or External Reference Clock
- Internal TI LMK04828 or LMK04821 Master Reference PLL with Zero Delay Mode
- Individually Delay Controlled Reference Clock to Each DAC Slave PLL and FPGA
- Advanced Triggering Input Registered to JESD204B Reference Clock
- External Clock and Trigger Inputs
- Reference Clock Output
- XCKU060 Xilinx Kintex Ultrascale FPGA
- 4GB DDR4 DRAM in 2 Banks Each with 64-Bit Interface

APPLICATIONS

- High Speed Arbitrary Waveform Generation
- RADAR and Jammers
- Electronic Warfare
- IP Development
- Instrumentation and Automated Test Equipment

SOFTWARE

- VHDL FrameWork Logic
- Windows/Linux Drivers
- C++ DevKit



DESCRIPTION

The XU-AWG is an XMC module with two 8-lane high-speed serial links: one on XMC connector P15 and one on P16. These links can support several protocols (up to 8-lane PCIe, Aurora or user defined). The XU-AWG features two AC-coupled single-ended DAC outputs with programmable DC bias. The Analog Devices AD9162 high performance RF DACs employ synchronization support, interpolation, fixed latency and unique output circuits providing improved frequency synthesis in the 2nd and 3rd Nyquist zones.

A Xilinx Kintex Ultrascale XCKU060 FPGA with 4GB DDR4 RAM memory provides a high-performance DSP core for demanding applications such as RADAR and wireless IF generation. The close integration of the analog front-end, memory, and host interface with the FPGA enables real-time signal processing.

The XU-AWG XMC module couples a powerful multi-channel PCIe DMA architecture with a high performance 8-lane PCI Express link connected to the carrier. PCIe link speeds up to Gen3 are supported; however, the actual PCIe link performance depends on the XMC carrier and the host system.

The XU-AWG FPGA design can be fully customized using VHDL and the FrameWork Logic Devkit. Xilinx JESD204B IP license, purchased separately from Xilinx, is required for logic development.

A software development kit for host development includes C++ libraries and 64-bit drivers for Windows and Linux. An application demonstrating the module's features, including streaming DAC samples from disk, is provided.

This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	**Part Number**	**Description**
XU-AWG	80335-0-L0 80335-1-L0	XU-AWG XMC Module 2x16b DACs 4.8 GSPS 1x (module only; XMC-PCIe x8 Adapter is not included) XU-AWG XMC Module 2x16b DACs 5.0 GSPS 1x (module only; XMC-PCIe x8 Adapter is not included)
XU-AWG XMC PCIE ASSY 4.8 GSPS INT PWR	90657-0-L0	XU-AWG XMC Module 80335-0-L0 and XMC-PCIe x8 Adapter 80363-4-L0 assembly (recommended for standard PC/Server deployment)
XU-AWG XMC PCIE ASSY 4.8 GSPS EXT PWR	90658-0-L0	XU-AWG XMC Module 80335-0-L0 and XMC-PCIe x8 Adapter 80363-5-L assembly (allows to use module with VPWR other than +12V)
XU-AWG XMC PCIE ASSY 5 GSPS INT PWR	90655-0-L0	XU-AWG XMC Module 80335-1-L0 and XMC-PCIe x8 Adapter 80363-4-L0 assembly (recommended for standard PC/Server deployment)
XU-AWG XMC PCIE ASSY 5 GSPS EXT PWR	90656-0-L0	XU-AWG XMC Module 80335-1-L0 and XMC-PCIe x8 Adapter 80363-5-L0 assembly (allows to use module with VPWR other than +12V)
Logic		
XU-AWG FrameWork Logic	55046	XU-AWG FrameWork Logic board support package for RTL
Cables		
SMA to BNC cable	67048G	SMA plug to BNC plug cable Assembly, 50 Ohms, RG-316, 36” length
JTAG Panel Board with Connector	80355-1-L0	JTAG Adapter Cable Assy to use with Xilinx Platform USB Cable (included with standard product)
Adapters		
XMC-PCIe x8 Adapter	80363-4-L0	XMC-PCIe X8 Adapter Card - XU High Heat (recommended option for standard PC/Server deployment; included with P/N 90655-0-L0 and P/N 90657-0-L0
XMC-PCIe x8 Adapter	80363-5-L0	XMC-PCIe X8 Adapter Card - XU High Heat External Power (allows to use module with VPWR other than +12V; included with P/N 90656-0-L0 and P/N 90658-0-L0)
Embedded PC Hosts		
ePC-Duo	90602-0-L0	EPC-DUO SE LMK04828 NO TIMING MODULE
	90602-1-L0	EPC-DUO SE LMK04828 GPS-500 CMOS
	90602-2-L0	EPC-DUO SE LMK04828 GPS LC_XO
	90602-3-L0	EPC-DUO SE LMK04828 GPS-500 LVDS
	90602-4-L0	EPC-DUO SE LMK04828 IEEE-1588
	90602-5-L0	EPC-DUO DIFF LMK04828 NO TIMING MODULE
	90602-6-L0	EPC-DUO DIFF LMK04828 GPS-500 CMOS
	90602-7-L0	EPC-DUO DIFF LMK04828 GPS LC_XO
	90602-8-L0	EPC-DUO DIFF LMK04828 GPS-500 LVDS
	90602-9-L0	EPC-DUO DIFF LMK04828 IEEE-1588
	90602-10-L0	EPC-DUO SE LMK048281NO TIMING MODULE

	90602-11-L0 90602-12-L0 90602-13-L0 90602-14-L0 90602-15-L0 90602-16-L0 90602-17-L0 90602-18-L0 90602-19-L0	EPC-DUO SE LMK04821 GPS-500 CMOS EPC-DUO SE LMK04821 GPS LC_XO EPC-DUO SE LMK048281GPS-500 LVDS EPC-DUO SE LMK048281 IEEE-1588 EPC-DUO DIFF LMK04821 NO TIMING MODULE EPC-DUO DIFF LMK04821 GPS-500 CMOS EPC-DUO DIFF LMK04821 GPS LC_XO EPC-DUO DIFF LMK04821 GPS-500 LVDS EPC-DUO DIFF LMK04821 IEEE-1588
SBC-Nano	90665-0-L0	SBC-NANO x4 PCIE 1 Gbe DEV KIT XU
DIO Breakout Board		
DIO 2x13 TWINAX BREAKOUT BOARD	80365-4-L0	DIO 2x13 Breakout Board with 30" Twinax Cable, SMA connectors and Retaining Hardware

XU-AWG

BLOCK DIAGRAM

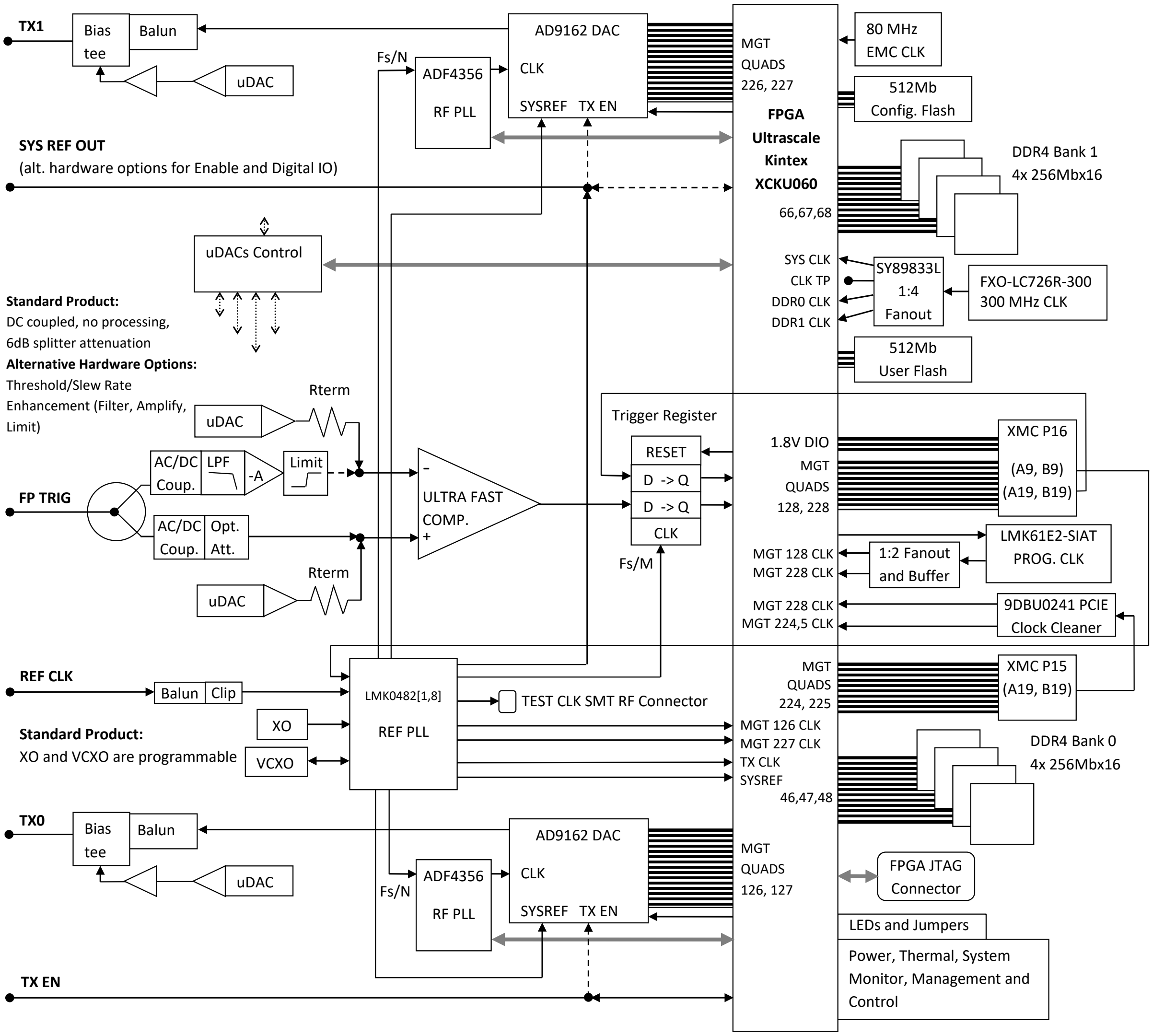


Figure 1. XU-AWG Module Block Diagram

Clocking and Triggering Notes:

The master PLL (Texas Instruments LMK04821 or LMK04828 depending on the module option) provides lower speed system clocks and the references for the slave microwave DAC PLLs. The master PLL accommodates either the on-board precision reference or a user provided external reference. External reference can be supplied from the front panel External Clock input or the XMC P16 connector.

P/N 80335-0-L0 employs LMK04821 master PLL. The DAC update rate range for this option is 1.5 GSPS to 4.8 GSPS in 1x (bypass) interpolation mode.

P/N 80335-1-L0 employs LMK04828 master PLL. The DAC update rate range for this option is 1.5 GSPS to 5.0 GSPS in 1x (bypass) interpolation mode.

Since the DAC update rates are limited by the characteristics of the master PLL, DAC itself and the overall system architecture, not all DAC update rates in the specified range can be utilized. Contact factory for additional information and available options.

The XU-AWG employs advanced triggering scheme. In addition to the software generated trigger, a hardware trigger signal can be used, either from the front panel External Trigger input or the XMC P16 connector. The front panel trigger signal processing circuit utilizes ultrafast comparator and employs software programmable threshold levels.

The SYSREF output signal can be used by system designers for various synchronization purposes.

The front panel TX Enable labeled signal is connected to the generic DIO pin in FPGA bank 45. This DIO is disabled (tri-stated) with supplied standard logic. However, it can be used with a custom logic for the hardware control of the DAC outputs or as a general use DIO with convenient front panel access. Since the FPGA bank 45 is powered by 1.8V, the logic levels for this signal must be 1.8 V LVCMOS standard compliant. To prevent possible FPGA damage, never apply voltage outside of the 0 V to 1.8 V range to TX Enable pin, even when this DIO pin is disabled in logic. It is a good practice to leave this input unconnected when not used in the logic.

Operating Environment Ratings

The XU-AWG module can be used in a variety of applications with different operating environment temperature, shock and vibration levels. It can be ordered with environmental ratings L0 through L4 and qualified for compliance. Shock, vibration and temperature testing are available. Contact the factory for Ruggedization Levels available.

Figure 2. Assembled XU-AWG module

Figure 3. XU-AWG view with a standard heat spreader installed. Custom heat spreader can be designed if needed; contact factory for further information.

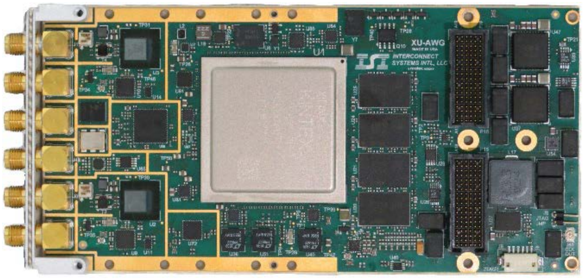


Figure 4. XU-AWG top side with the heat spreader removed

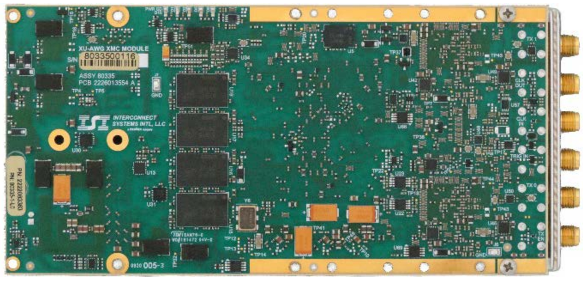


Figure 5. XU-AWG bottom side

Standard Features

General	
Front Panel Connector Type	SMA Jacks (6 total)
DAC Outputs	2
DAC Output	3.0 dBm @165 MHz and 50 Ohm load
DAC Output DC Bias	-0.3 V to +0.3 V; 0.0 V Default
DAC Output Impedance	50 Ohm @ 165 MHz Note: The output impedance decreases with increasing frequency due to the parasitic capacitance in the DAC output path (~1 pF)
DAC Device	AD9162 (two per board)
DAC Update Rate	Up to 4.8 or 5.0 GSPS in 1x bypass mode depending on module option Up to 12 GSPS in interpolation modes
DAC JESD 204B Interface Rate	Up to 12.5 Gbps; 8 lanes per DAC
Interpolation	1x (bypass), 2x, 3x, 4x, 6x, 8x, 12x, 16x, 24x options
Modulator	Complex modulator with 48-bit dual modulus NCO
Calibration	AC Gain and DC Offset errors are digitally corrected and stored in non-volatile calibration memory.

Host Interface	
Type	PCI Express Gen 3.0 Eight Lane*
Sustained Data Rate	Up to 6 GB/sec*

SYSREF Output Frequency	250 MHz (max)
SYSREF Output Signal Range	0.25 V to 1.5 V
TX EN Input	LVCMOS18 logic levels Note: TX EN input is disabled in supplied standard logic; leave open when not used

FPGA	
Device	Xilinx Kintex Ultrascale XCKU060-2FFVA1517E
Speed Grade	-2
Temperature Range	0°C to +100°C (Extended)
System Logic Cells	725,550
CLB Flip-Flops	663,360
CLB LUTs	331,680
Maximum Distributed RAM (Mb)	9.1
Block RAM/FIFO w/ECC (36Kb)	1,080
GTH Transceivers	32
Configuration	QSPI flash memory or JTAG

Memories	
DRAM Size	4 GB total in 2 Banks; 8 devices @ 256 Mb x16 each
DRAM Type	SDRAM DDR4-2666

Digital IO Connector	
DIO pins, total	36 on board

Connector	XMC P15

Note: PCIe max speed and the sustained data rate are dependent on the system where the XU-AWG module is deployed and cannot be guaranteed by ISI.

Clocks and triggering	
Clock Sources	System Reference: Onboard TCXO or External (Front Panel or P16) Master PLL: LMK04821 or LMK04828. Slave (DAC) PLL: ADF4356 x2
Front Panel Reference Clock Input	50 Ohm; AC-coupled
Reference Clock Input Range	0.5 to 3.0 Vp-p (min/max)
Reference Clock Input Frequency	250 MHz (max)
Reference Clock Input Slew Rate	0.5 V/ns (min)
Jitter	<350 fs RMS (typ.)
Triggering	Software or External (Front Panel or P16)
Front Panel Trigger Input	50 Ohm; DC-coupled
Trigger Input Threshold	Programmable; 1.0 V Default
Trigger Input Signal Range	0 to 2.5 V
Trigger Input Threshold Hysteresis	50 mV (typ.)
Trigger Input Slew Rate	50 V/µs (min); 1 V/ns or faster is recommended
Multi-module Synchronization	Achievable when the following conditions are met: Ext Ref Clk = JESD204B Sys Ref Clk Ext Trigger derived from Ext Ref Clk

Signal Standards	LVCMOS18 default; see Xilinx select IO user guide (UG571). DIOs routed as differential pairs on P16 rows C and F except C19 and F19 which can source 1.8V (up to 500mA) to user circuits
Connector	XMC P16

Power Management	
Temperature and Power Monitor	Accessible by the host software
Alarms	Software programmable warning and failure levels
FPGA Over-temperature Monitor	Failure level alarm disables power
Power Control	Power sequencing; power good indication; continuous power state monitoring with shutdown in case of a failure
Heat Sinking	Conduction cooling (VITA20 subset) and fan support

Physicals	
Form Factor	Single width IEEE 1386 Mezzanine Card
Size	75 x 150 mm
Weight	~160g (w/o heatsink)
Hazardous Materials	Lead-free and RoHS compliant

System Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked

ABSOLUTE MAXIMUM RATINGS				
Exposure to conditions exceeding these ratings may cause board damage!				
Parameter	**Min**	**Max**	**Units**	**Conditions**
Supply Voltage, 3.3V to GND	0	3.6	V	
Supply Voltage, VPWR to GND	0	14.0	V	
Operating Temperature	0	+70	℃	Non-condensing, forced air cooling required
Storage Temperature	-40	+100	℃	
ESD Rating	-	2,000	V	Human Body Model
Vibration	-	5	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS				
Parameter	**Min**	**Typ.**	**Max**	**Units**
Supply Voltage, 3.3V	3.15	3.3	3.45	V
Supply Voltage, VPWR*	4.75	12.0	14.0	V
Operating Temperature	0		60	℃
Forced Air Cooling				Approximate 200 LFM

Note: XU-AWG module is specified and tested at VPWR = 12.0 V. However, it is capable of operation at VPWR = 5.0 V. Contact sales for more information if operation at VPWR = 5.0V is required.

	ELECTRICAL CHARACTERISTICS Typical over recommended operating free-air temperature range 0°C to +60°C and VPWR = 12.0 V unless otherwise noted.			
Group	**Parameter**	**Typ.**	**Units**	**Notes**
Analog Outputs	Output signal frequency range*	10 – 3,000	MHz	50 Ohm Load
	SFDR	70	dBc	165 MHz Single Tone Output, 1x Interpolation fdac = 4.8 GSPS for 80335-0 option fdac = 5.0 GSPS for 80335-1 option
	Channel to Channel Crosstalk	-90	dB	165 MHz Single Tone Output, 1x Interpolation fdac = 4.8 GSPS for 80335-0 option fdac = 5.0 GSPS for 80335-1 option
	Gain Error	+/-2.0	% of FS	Calibrated at 165 MHz; FS = 3.0 dBm with 50 Ohm load (FS = Full Scale)
	Output DC Bias Adjustment Range	+/-0.3	V	Software Programmable; 0.0 V Default
Power**	Supply Current	3.5 1.5	A	12.0 V (VPWR) 3.3 V
	Power Dissipation	50	W	VPWR = 12.0 V

*Output signal frequency range is affected by the XU-AWG DAC output balun transformer’s performance (Mini Circuits TC1-1-13MX+), sampling rate, mode of operation, interpolation and digital filter settings. Contact ISI sales for additional information if a higher output signal frequency is desired.

**Power consumption depends on the DAC mode of operation, sampling rate, output signal frequency, FPGA utilization and other factors.

Architecture and Features

The XU-AWG module architecture integrates an analog front end with an FPGA computing core, memories, and an XMC VITA 42.3-2006 PCI Express 8-lane host interface. This architecture tightly couples the FPGA to the analog and enables the module to perform real-time signal processing with low latency and extremely high rates. The XU-AWG is ideal as a front end for demanding applications for complex signal generation used in arbitrary waveform generators, RADAR, electronic warfare and similar applications.

Analog Front End

The analog front end of the XU-AWG module has two DAC outputs, which can be simultaneously updated. The DAC device (Analog Devices AD9162) employs unique output circuit which allow improved frequency synthesis in the 2nd and 3rd Nyquist zones.

The DAC features programmable interpolation, filtering and mixing to support frequency digital up-conversion (DUC) of the baseband waveform. The DUC features the lower speed baseband signal up-conversion to high-speed IF, significantly unburdening the FPGA processing for many communications and RADAR signal applications. The DAC has a complex modulator with a 48-bit dual modulus NCO. For detailed information on the AD9162 DAC’s advanced features please refer to the part’s datasheet on the Analog Devices web site.

The DAC NCO can be configured to generate a sinusoidal signal on the DAC output without using memory or streamed data.

The DAC channels operate synchronously for simultaneous DAC updates using the PLL which can be referenced to an external timing input. Trigger modes include frames of programmable size, external and software. Multiple modules achieve DAC alignment using an external reference clock at the JESD204B system reference clock rate along with an external trigger derived from the external reference clock. The trigger component in the logic can be customized to accommodate a variety of triggering requirements.

DAC Output Modes Comparison

“**NRZ**” (Non-Return to Zero) is the traditional DAC mode. The output will have a traditional Sinc frequency response, which can be digitally flattened up to about 40% of the sampling rate with an Inverse Sinc filter built into the DAC (typically 3.8 dB loss and +/-0.05 dB flatness in the digital signal).

“**2x NRZ**” is the 2x “DDR” clocked 2x interpolated output which allows operation beyond the first Nyquist zone mode.

“RZ” (Return to Zero) mode with a duty cycle of ½ (the output is pulsed “on” for Ton which is ½ of each Ts sampling period). The “RZ” (Return to Zero) mode has trade-offs (approximately -6dB (½ amplitude) compared to “2x NRZ” mode) but is generally accepted as an analog performance enhancement to the traditional DAC “NRZ” mode when operating at higher frequencies. As the DAC clock frequency increases the DAC output settling time takes a larger percentage of the sample period, and this settling can be non-linear or asymmetrical adding impairments which depends on the specific output code transition. Also, parasitic elements, delays and “strays” have a larger impact on circuit operation and balance making the output transitions less ideal at higher frequencies. This introduces non-linear inter-code interference in an NRZ DAC mode. However, in a RZ DAC mode all transitions are from and to “zero” and have little or no memory of the prior output code which reduces non-linear inter-code interference and the associated output distortion.

“**Mix”** mode has a different frequency shaping function and can be thought of as “chopping” (modulating) the DAC output at the DAC sample rate shifting the output power to near the sample rate.

DAC Output Circuit Frequency Response

The output circuit on the XU-AWG converts the DAC output current to a single-ended output voltage with a balun transformer.

The XU-AWG DAC outputs are AC-coupled and incorporate a programmable DC Level DAC circuit which is used with a bias tee to provide DC levels in the on the outputs if needed. The DAC return loss degrades with increasing frequency due to the parasitic capacitance in the DAC output.

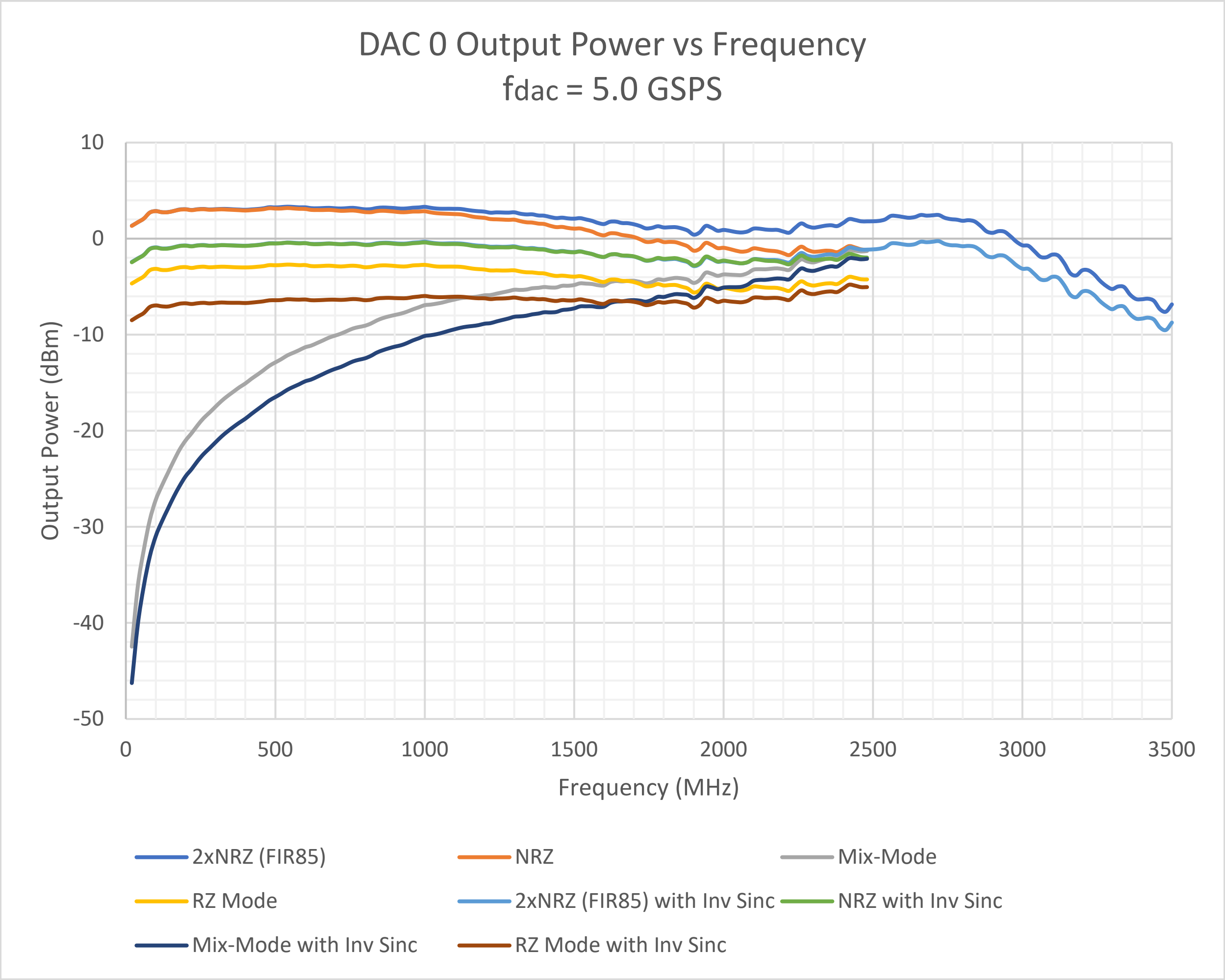


Figure 6. XU-AWG DAC 0 typical output signal amplitude vs frequency plot in different modes of operation and Rload =50 Ohm (adjusted for connecting cable losses)

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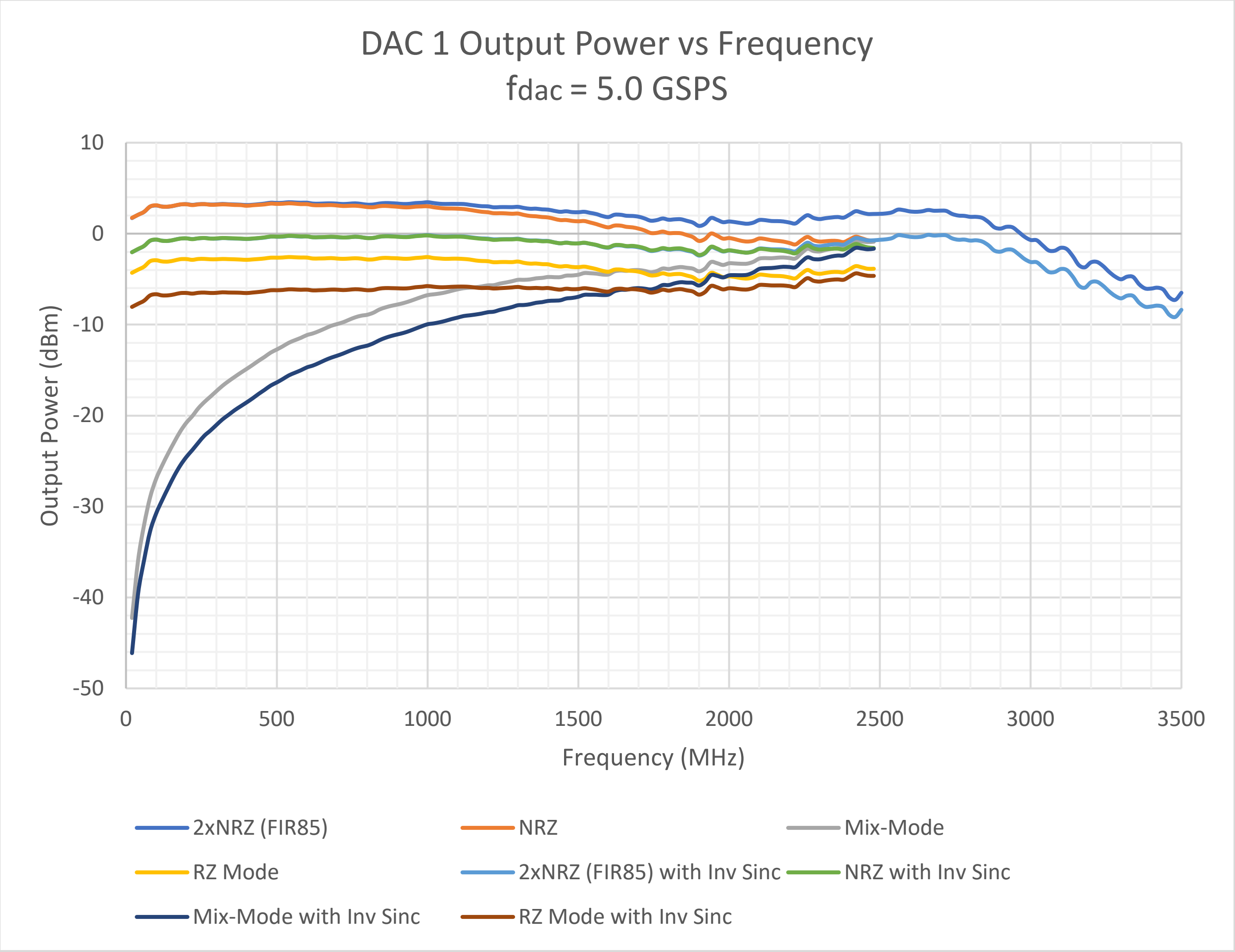
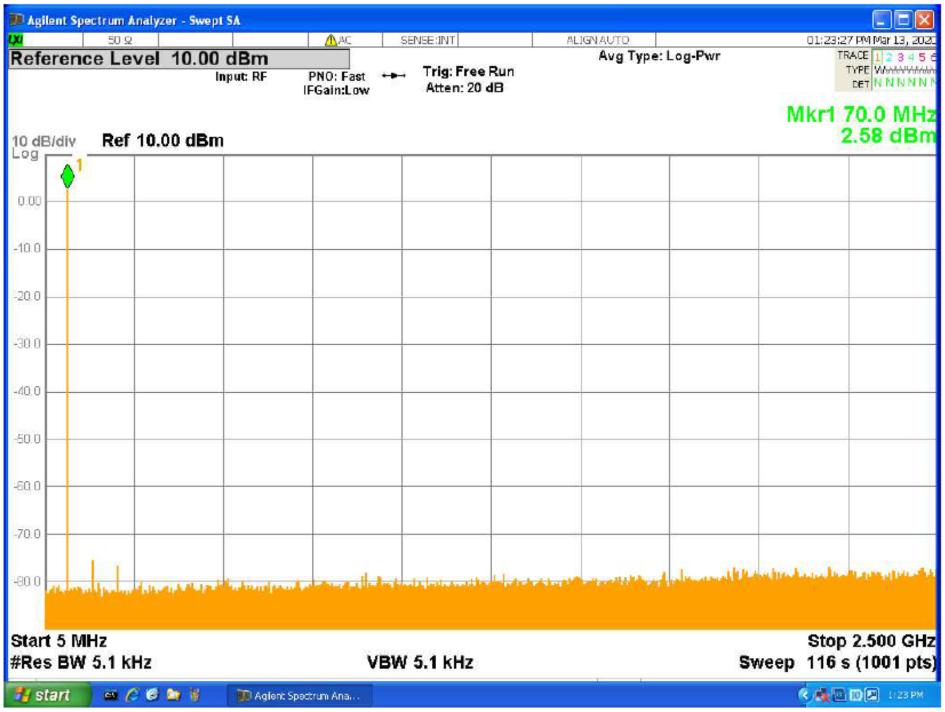


Figure 7. XU-AWG DAC 1 typical output signal amplitude vs frequency plot in different modes of operation and Rload =50 Ohm (adjusted for connecting cable losses)

The XU-AWG output standard balun transformer performs well from 10 MHz to 2.25 GHz. Above 2.5 GHz phase imbalance may impact distortion performance. To take advantage of the higher frequency capability of the used DACs higher frequency balun transformers may be used on the module outputs. Contact factory for further information.



Agilent Spectrum Analyzer - Swept SA

50 Ω AC SENSE:INT ALIGN AUTO 01:23:27 PM Mar 13, 2020

Reference Level 10.00 dBm

Input: RF PNO: Fast IFGain:Low Trig: Free Run Atten: 20 dB Avg Type: Log-Pwr

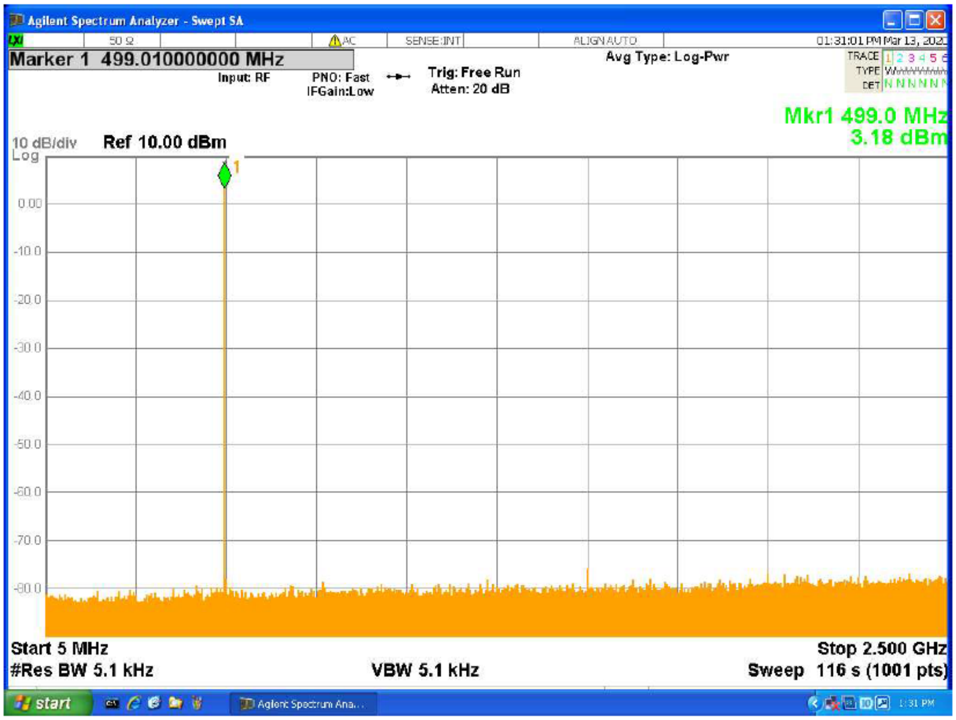
Mkr1 70.0 MHz 2.58 dBm

10 dB/div Ref 10.00 dBm

Start 5 MHz Stop 2.500 GHz

#Res BW 5.1 kHz VBW 5.1 kHz Sweep 116 s (1001 pts)

Figure 8. XU-AWG typical single tone output spectrum at fdac = 5.0 GSPS; fout = 70 MHz (2xNRZ/FIR85 mode)



Agilent Spectrum Analyzer - Swept SA

50 Ω AC SENSE:INT ALIGN AUTO 01:31:01 PM Mar 13, 2020

Marker 1 499.010000000 MHz

Input: RF PNO: Fast IFGain:Low Trig: Free Run Atten: 20 dB Avg Type: Log-Pwr

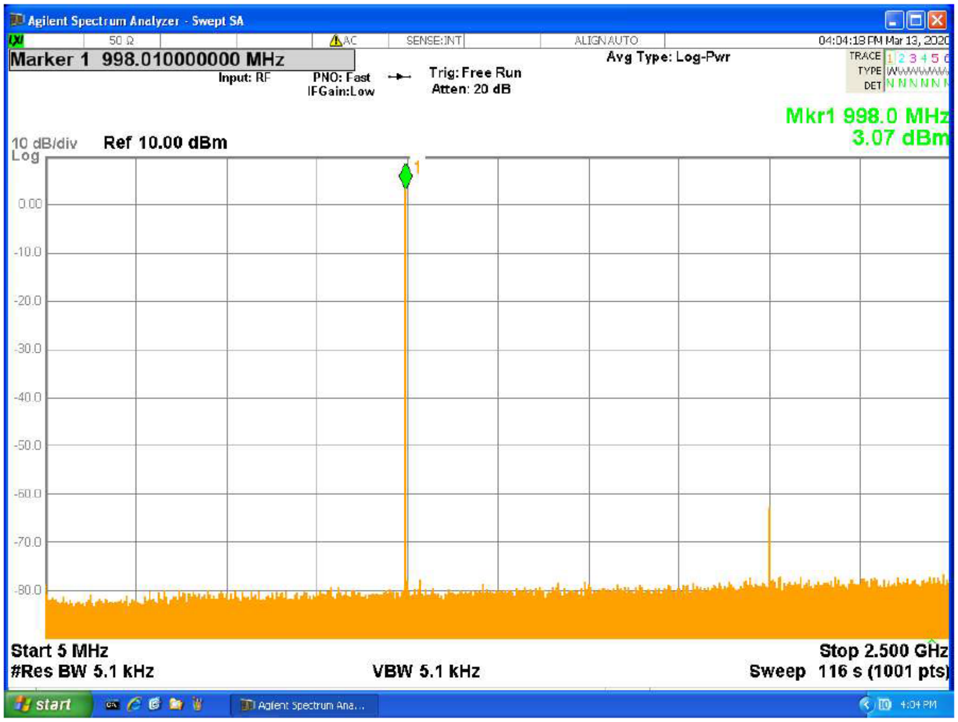
Mkr1 499.0 MHz 3.18 dBm

10 dB/div Ref 10.00 dBm

Start 5 MHz Stop 2.500 GHz

#Res BW 5.1 kHz VBW 5.1 kHz Sweep 116 s (1001 pts)

Figure 9. XU-AWG typical single tone output spectrum at fdac = 5.0 GSPS; fout = 500 MHz (2xNRZ/FIR85 mode)



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Marker 1 998.010000000 MHz

Input: RF

PNO: Fast
IFGain:Low

Trig: Free Run
Atten: 20 dB

Avg Type: Log-Pwr

Mkr1 998.0 MHz
3.07 dBm

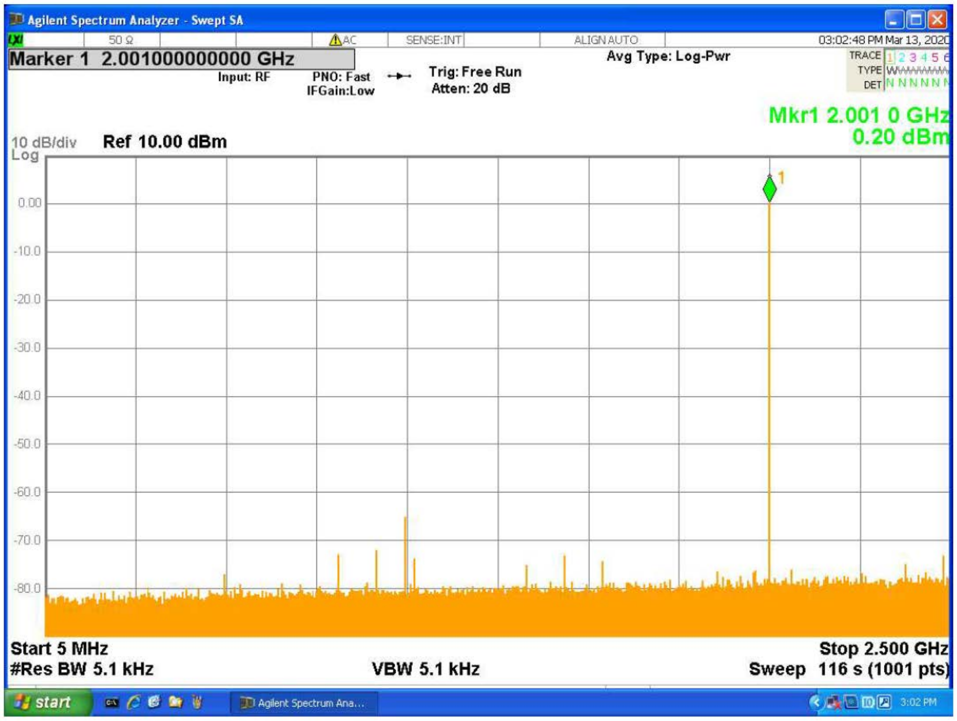
Ref 10.00 dBm

Start 5 MHz
#Res BW 5.1 kHz

VBW 5.1 kHz

Stop 2.500 GHz
Sweep 116 s (1001 pts)

Figure 10. XU-AWG typical single tone output spectrum at fdac = 5.0 GSPS; fout = 1.0 GHz (2xNRZ/FIR85 mode)



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Marker 1 2.001000000000 GHz

Input: RF

PNO: Fast
IFGain:Low

Trig: Free Run
Atten: 20 dB

Avg Type: Log-Pwr

Mkr1 2.001 0 GHz
0.20 dBm

Ref 10.00 dBm

Start 5 MHz
#Res BW 5.1 kHz

VBW 5.1 kHz

Stop 2.500 GHz
Sweep 116 s (1001 pts)

Figure 11. XU-AWG typical single tone output spectrum at fdac = 5.0 GSPS; fout = 2.0 GHz (2xNRZ/FIR85 mode)

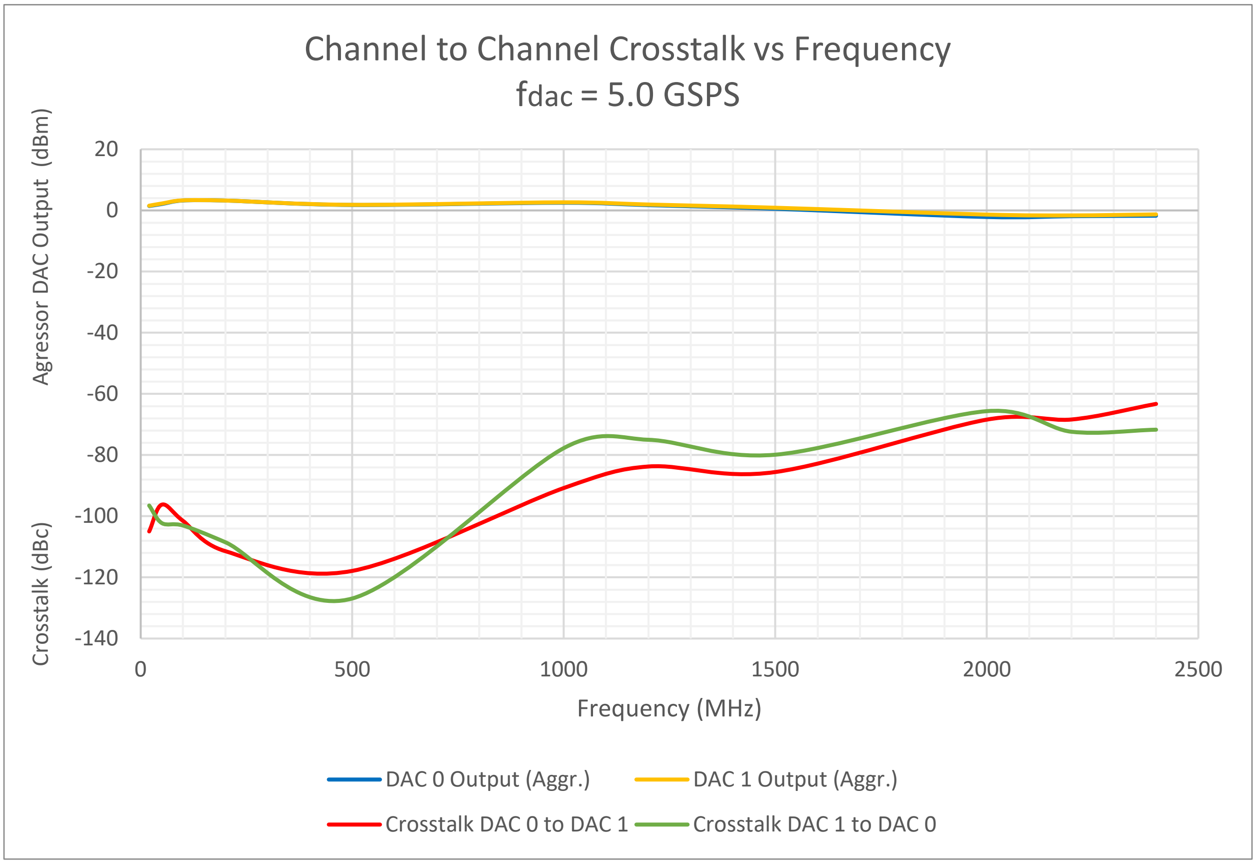


Figure 12. XU-AWG typical channel to channel crosstalk vs frequency plot

FPGA Core

The XU-AWG has a Xilinx Ultrascale XCKU060-2FFVA1517E FPGA and memory at its core for DSP and control. The FPGA fabric integrates logic, memory and connectivity features that make the FPGA capable of applying the DSP processing power to virtually any algorithm and sustaining performance in real-time. The FPGA has direct access to two DDR4 DRAM banks. These memories are used as FPGA working space for computation, required by DSP functions like FFTs, and bulk data storage needed for waveform calculations.

Firmware for the FPGA completely defines the data flow, signal processing, module controls, and host interfaces, allowing user customization of the XU-AWG functionality.

PCI Express Host Interface

The XU architecture supports an 8-lane PCI Express link from the host. A multi-channel DMA provides the data streaming mechanism utilizing the PCI Express interface. This architecture provides an efficient and flexible host interface supporting high data rates with minimal host support. Host data may be streamed continuously to the DACs. Firmware is provided in the FrameWork Logic tools allowing user applications to rapidly integrate data streams and controls.

Private Data Links

The XU-AWG supports private data links on the P15 and/or P16 connector that can be used for system integration. The XMC P15 and P16 connectors each have 8 lane links connected to FPGA GTH transceivers. The GTH lanes can be used to support high rate data transfers. Standard product uses P15 connected GTH lanes as a PCI Express 8-lane Gen 3 interface. For P16 connected GTH lanes, maximum data rates with deterministic performance may be implemented in performance-driven systems using little or no protocol. For more complex systems, other protocols such as Aurora may be used.

Module Management

Module status is monitored using the XU-AWG alert mechanism. The alerts provide information on the timing of important events such as triggering, buffer underflow, and thermal overload. Packets contain data about the specific alert and include a system timestamp. This provides a precise overview of the module operation by recording the occurrence of these real-time events.

FPGA Configuration

The XU-AWG has a non-volatile configuration memory that holds the FPGA application image.

For FPGA configuration a standard JTAG interface is used in conjunction with the Xilinx Vivado development tool. The XU-AWG module has two JTAG modes of operation controlled by the JTAG Mode Selection Header J8.

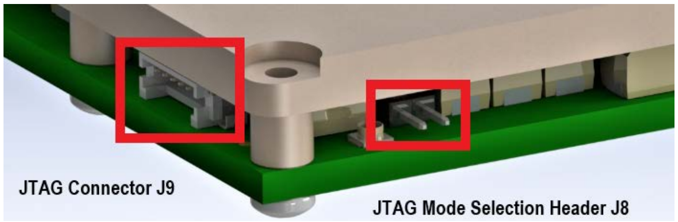


Figure 13. XU-AWG JTAG Connector J9 and JTAG Mode Selection Header J8

In first JTAG programming mode an external JTAG programmer such as Xilinx Platform USB Cable (or similar) along with the ISI JTAG Adapter Cable 80355-1-L0 must be used. P/N 80355-1-L0 is provided with the standard product; it is also available separately for purchase from ISI LLC. Connect the Xilinx Programmer's 14-pin ribbon cable connector to the 14-pin socket on the ISI JTAG Adapter Cable and then connect the JTAG Adapter cable's 6-pin white connector to the XU-AWG JTAG Connector J9. Make sure to install the 2-pin shorting jumper (supplied with standard product) on the XU-AWG JTAG Selection header J8 before attempting to program FPGA in this mode.

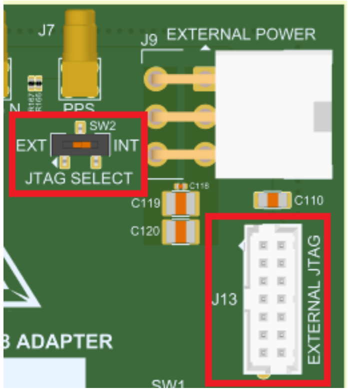


Figure 14. 80363 Adapter's JTAG Selection Switch SW2 and External JTAG Header J13

The second JTAG programming mode can be used when XU-AWG is assembled on the recommended XMC to PCIe 8 lane Adapter (80363-4 or 80363-5). The 80363 Adapter has a built-in JTAG programmer, so no external JTAG programming hardware is required. JTAG signals from adapter are routed to the XU-AWG through the XMC Connector P15. A standard USB Type A to micro USB cable is required to connect adapter with a host with the Xilinx Vivado tool installed. Connect the micro USB end of the cable to the micro USB receptacle on the 80363 Adapter's front panel and the other end to the host PC USB port. Make sure the 2-pin shorting jumper is removed from the XU-AWG JTAG Mode Selection Header J8 before attempting to program FPGA in this mode. The 80363 Adapter's JTAG mode selection switch SW2 must be in "INT" (internal) position.

The 80363 Adapter allows to use an external JTAG programmer as well if desired. Connect the Xilinx Programmer's 14-pin ribbon cable connector to the 14-pin JTAG header J13 on the 80363 Adapter. Adapter's JTAG mode selection switch

SW2 must be in “EXT” (external) position. Again, the shorting jumper on the XU-AWG J8 JTAG Mode Selection Header must be removed.

Please note that the XU-AWG module is shipped from the factory with the shorting jumper on the JTAG Mode Selection Header J8 removed, so the module is set for the second mode of JTAG programming utilizing P15 connector as described above.

In addition to JTAG programming modes, the ISI *DAQ* application software allows convenient in-system FPGA flash configuration memory programming directly from the GUI. Note that a full system shutdown and reboot is required to load the programmed FPGA configuration file from the FPGA flash memory.

Software Tools

A software development kit for the XU-AWG provides comprehensive support including device drivers, data buffering, module controls, and utilities that allow developers to be quickly productive. At the most fundamental level, the software development kit delivers data buffers to your application without the burden of low-level real-time control of the module. Software classes provide C++ developers a powerful, high level interface to the module that makes real-time, high-speed data acquisition easier to integrate into applications. Qt Creator project files are provided to compile and build C/C++ applications on 64-bit Windows or Linux operating systems. Visual Studio solution files are also provided for 64-bit Windows. For additional help please contact technical support.

The provided *DAQ* application allows use of the XU-AWG module straight out of the box. The *DAQ* application provides module configuration, dynamic waveform generation, system monitoring, and logic reconfiguration. The *Binview* utility provides data viewing, analysis, and export capability to other software packages. The *WaveGenerator* utility is available for generating waveform files.

Logic Tools

The FrameWork Logic tools support RTL development. The standard logic provides a hardware interface layer that allows designers to concentrate on the application-specific portions of the design. Designers build upon the ISI components for data handling, hardware interfaces and system functions, the Xilinx IP core library, and third party IP. RTL source for the FrameWork Logic is provided for customization.

The FrameWork Logic User Guide provides more detail.

Cables

The XU-AWG module uses coaxial cable assemblies for the analog I/O. The mating cable should have an SMA male connector with 50 Ohm characteristic impedance for best signal quality. Use high quality low loss cables to achieve the best possible performance.

DIO Breakout Board and Cables

The DIO Breakout Board 80365-4 (available separately from ISI LLC) supplied with the 30” high-speed Twinax cable assembly, provides user with convenient access to XU-AWG FPGA DIO signals via standard SMA connectors.

The following table and illustrations show the FPGA DIO signals that are available when XU-AWG is installed on the XMC-PCIe x8 80363-4 or 80363-5 Adapter and used with 80365-4 Breakout board (Fig. 15). The DIO signals are routed from FPGA to the XMC P16 connector and further to the adapter’s J1 DIO connector as high quality 100 Ohms differential / 50 Ohms single-ended tightly length-matched traces to achieve the best possible signal integrity and minimal timing skew between the DIO signals. The Adapter is connected to the 80365 Breakout Board with a high-speed flat Twinax cable. The DIO signals on the Breakout board are routed to the 50 Ohm SMA type connectors. DIO signals have 1.8V LVCMOS logic levels. To prevent FPGA damage, the voltage levels on DIO signals should be always kept within the 0 V to 1.8V range when driven from outside.

XU-AWG			80363 Adapter	80365 Breakout Board
DIO SIGNAL	**FPGA Pin**	**P16 Pin**	**Front Panel Connector J1 Pin**	**SMA Connector**
P16_DIO_0_P	AN18	C1	3	P0
P16_DIO_0_N	AN17	C2	5	N0
P16_DIO_2_P	AU17	C3	15	P2
P16_DIO_2_N	AU16	C4	17	N2
P16_DIO_4_P	AT18	C5	4	P4
P16_DIO_4_N	AT17	C6	6	N4
P16_DIO_6_P	AR18	C7	16	P6
P16_DIO_6_N	AR17	C8	18	N6
P16_DIO_1_P	AM19	F1	9	P1
P16_DIO_1_N	AN19	F2	11	N1
P16_DIO_3_P	AV19	F3	21	P3
P16_DIO_3_N	AW18	F4	23	N3
P16_DIO_5_P	AT19	F5	10	P5
P16_DIO_5_N	AU19	F6	12	N5
P16_DIO_7_P	AR20	F7	22	P7
P16_DIO_7_N	AT20	F8	24	N7
Signal Ground			1, 2, 7, 8, 13, 14, 19, 20, 25, 26	

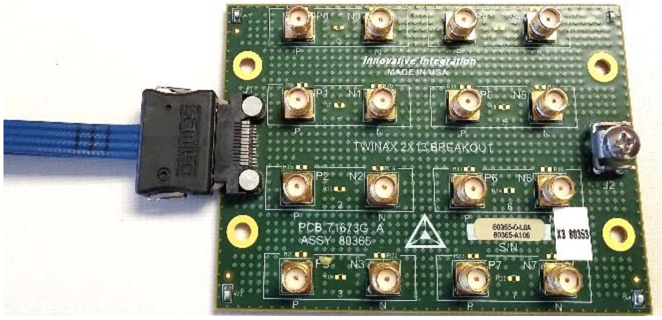


Figure 15. 80365-4 Breakout Board

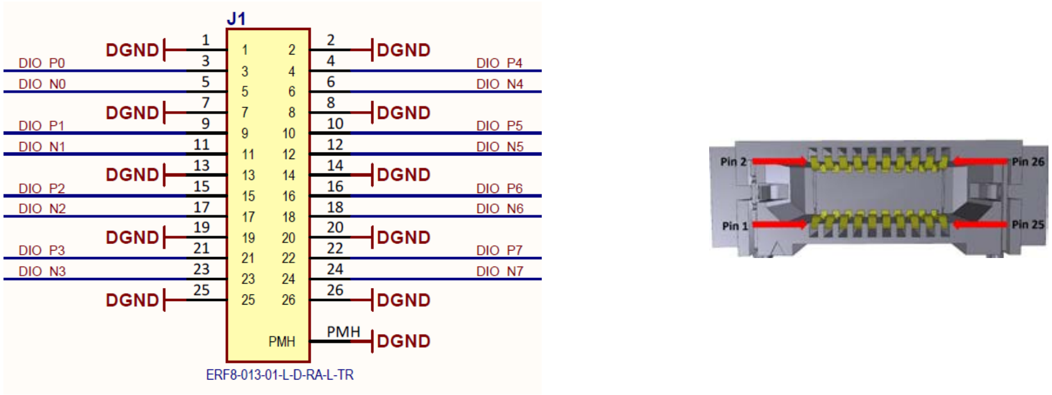


Figure 16. 80365-4 Breakout Board J1 DIO Connector Signals

XU-AWG

XMC Adapter Cards

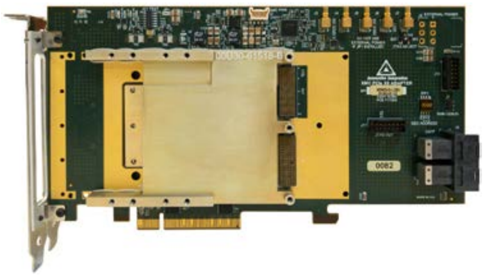
XMC modules can be used in standard desktop systems or compact PCIe/PXIe chassis using an adapter card. The adapter cards are software transparent. Few different adapter cards are available from ISI each with its own unique set of features.

XMC-PXIe Adapter (80341)
(for use in PXIe systems)

External clock and trigger inputs
2x QSFP connectors
High-speed DIO connector
Advanced power control and cooling
3U double-slot PXIe card (single-slot version w/o QSFP and DIO connectivity is also available).

XMC-PCIe x8 Adapter (80363)
(for use in standard PCs or Servers)

XMC to 8 lane PCIe
External clock, trigger and 1 PPS inputs
On-board USB to JTAG Programmer
High-speed DIO Connector
High-speed expansion port (Dual Mini-SAS or 2x QSFP with the optional Extension card)
Forced air or conduction cooling
External Power option available
XMC Module Voltage and Current Test Header
Advanced power control and cooling features
~ ¾ full-length PCIe card



VPX-XMC Adapter (80260)
(for use in VPX systems)

XMC to VPX; 8x PCIe Lanes
Conduction or air cooling
3U size VPX card

XMC Carriers

XMC modules can be also used with various standalone carriers available from ISI.

ePC Duo with Dual PCI Express XMC Module Sites (90602)

Windows/Linux embedded PC
Hosts basic size COM Express type 6 module
High Performance Intel i7 Quad Core CPU
8x USB, 1x 1 GbE; 2x 10 GbE, DisplayPort, 4x QSFP
Up to 4 SATA 3 speed high performance SSDs
High-speed x8 interconnect link between modules
Low-jitter PLL based programmable sample clocks and triggers to XMC modules and externals
XMC DIO Connector
GPS or IEEE-1488 synchronization option
On-board USB to JTAG programmer
Advanced system power control and monitoring
Wide 9 – 32 V DC operation

ePC-Nano (80342)

Windows/Linux Embedded Single Board Computer
Hosts mini size COM Express type 6 module
Extremely small form-factor (appr. 80 x 160 mm footprint)
Low power Intel Atom x7-E3950 Quad Core advanced processor with 8GB DDR3L Memory
Single XMC IO Site
x4 PCIe lanes to XMC module
Mini DisplayPort connector
1x GbE Port
2x USB 3.0 Ports
DIO connector
On-board USB to JTAG programmer
8 – 14 V DC operation

eInstruments PCI Express XMC Node (90181)

XMC module carrier with 2.5 Gbps cabled PCI Express link to Host Computer
x1 PCI Express lane
~ 180 MB/s to host PC data transfer rate
Up to 5 meter cable at full rate
12 V DC operation

Usage and Market

The XU-AWG is a digital device and apparatus exclusively for use in business, industrial and commercial environments. The XU-AWG peripheral is not marketed, sold or otherwise made available for home or residential environment use.

The XU-AWG is exclusively for use with wired input and output signals. The XU-AWG peripheral is not an intentional radio transmitter or receiver and is not marketed, sold or otherwise made available for connection to wireless media (with an antenna, etc.).

The XU-AWG is not a “PC” (“personal” or “portable computer” marketed for home or residential environment use) or “PC” peripheral and is not marketed, sold or otherwise made available as a “PC” or “PC” peripheral.

The XU-AWG may be sold as a subassembly where the integrator/purchaser takes responsibility for their assembled digital device’s or apparatus’s compliance. Consult ISI/Molex for clarification and assistance.

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