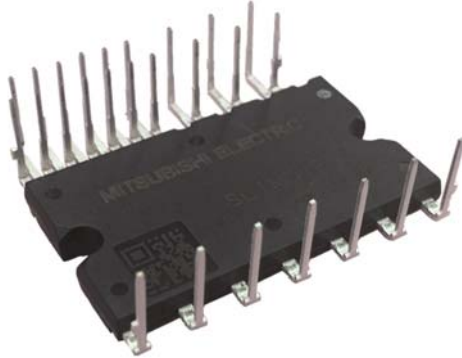


< DIIPM >

# SLIMDIP-W

TRANSFER MOLDING TYPE  
INSULATED TYPE

## OUTLINE



Normal terminal type

## MAIN FUNCTION AND RATINGS

- RC-IGBT inverter bridge for three phase DC-to-AC power conversion
- Built-in bootstrap diodes with current limiting resistor
- Open emitter type

## APPLICATION

- AC 100~240V (DC voltage:400V or below) three phase low power motor inverter drive

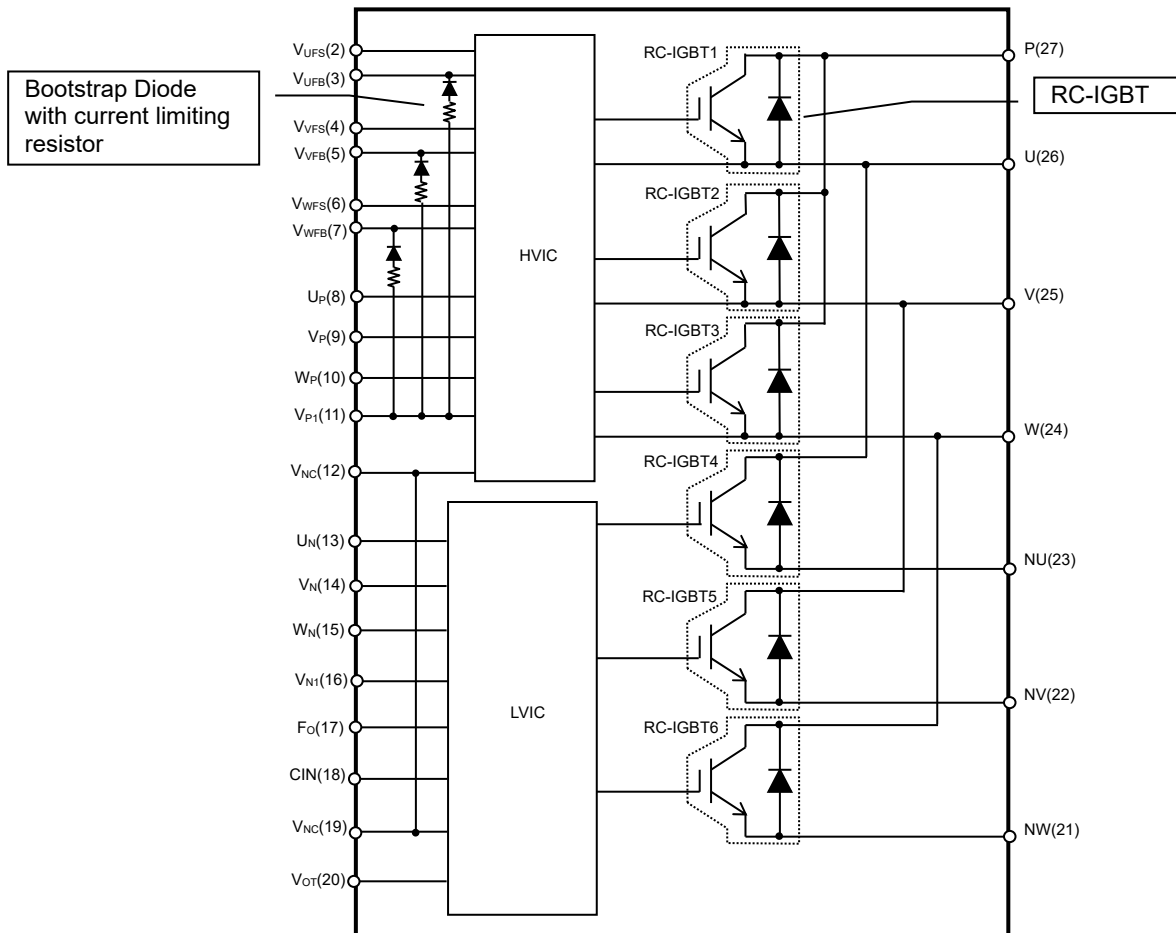
## TERMINAL LINE UP

Terminal	Part number	Suffix
Normal terminal	SLIMDIP-W	500
Short terminal	SLIMDIP-W	505

## INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage protection (UV)
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply) and OT fault
- Temperature monitoring : Outputting LVIC temperature by analog signal
- Input interface : Schmitt-triggered 3V, 5V input compatible, high active logic.
- UL Recognized : UL1557 File E323585

## INTERNAL CIRCUIT



**SLIMDIP-W****TRANSFER MOLDING TYPE  
INSULATED TYPE****MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	450	V
$V_{CC(\text{surge})}$	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
$V_{CES}$	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note 1)	15	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$ , less than 1ms	30	A
$T_j$	Junction temperature	(Note 2)	-30~+150	$^\circ\text{C}$

Note1: Pulse width and period are limited due to junction temperature.

Note2 The maximum junction temperature rating of the power chips integrated within the DIIPM is  $150^\circ\text{C}$  ( $@T_C \leq 115^\circ\text{C}$ ) however, to insure safe operation of the DIIPM, the average junction temperature should be limited to  $T_{j(\text{ave})} \leq 125^\circ\text{C}$  ( $@T_C \leq 115^\circ\text{C}$ ).**CONTROL (PROTECTION) PART**

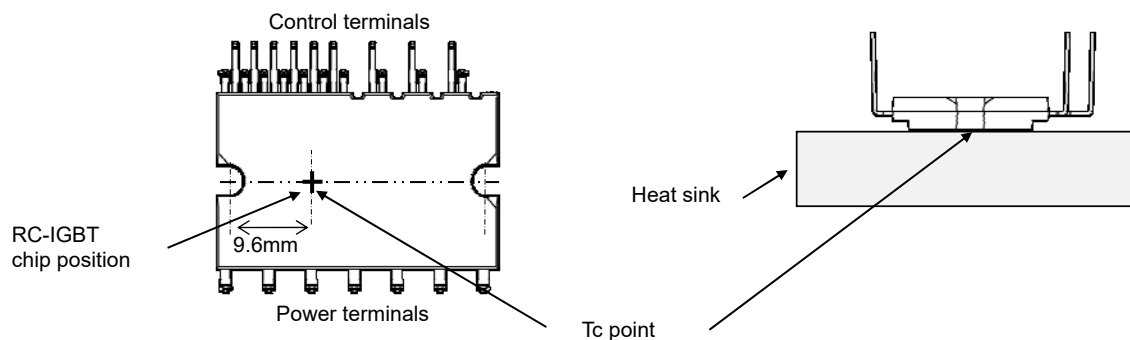
Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{NC}$ , $V_{N1}-V_{NC}$	20	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	20	V
$V_{IN}$	Input voltage	Applied between $U_P$ , $V_P$ , $W_P$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
$V_{FO}$	Fault output supply voltage	Applied between $F_O-V_{NC}$	-0.5~ $V_D+0.5$	V
$I_{FO}$	Fault output current	Sink current at $F_O$ terminal	1	mA
$V_{SC}$	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(\text{PROT})}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$ , Inverter Part $T_j = 150^\circ\text{C}$ , non-repetitive, less than $2\mu\text{s}$	400	V
$T_C$	Module case operation temperature	Measurement point of $T_C$ is described in Fig.1 (Note3)	-30~+115	$^\circ\text{C}$
$T_{\text{stg}}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{\text{iso}}$	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	$V_{\text{rms}}$

Note3  $T_C$  MEASUREMENT POINT

Fig. 1

**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 4)	Inverter RC-IGBT part (per 1/6 module)	-	-	4.0	K/W

Note 4: Grease with good thermal conductivity and long-term endurance should be applied evenly with about  $+100\mu\text{m}\sim +200\mu\text{m}$  on the contacting surface of DIIPM and heat sink. The contacting thermal resistance between DIIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about  $0.4\text{K/W}$  (per 1/6 module, grease thickness:  $20\mu\text{m}$ , thermal conductivity:  $1.0\text{W/m}\cdot\text{K}$ ).

**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}$ , $V_{IN} = 5\text{V}$	-	1.95	2.40	V
		$I_C = 15\text{A}$ , $T_j = 25^\circ\text{C}$		2.30	2.75	
$V_{EC}$	FWDi forward voltage	$V_{IN} = 0\text{V}$ , $-I_C = 15\text{A}$	-	1.60	2.20	V
$t_{on}$	Switching times	$V_{CC} = 300\text{V}$ , $V_D = V_{DB} = 15\text{V}$ $I_C = 15\text{A}$ , $T_j = 125^\circ\text{C}$ , $V_{IN} = 0 \leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)	0.60	1.00	1.40	$\mu\text{s}$
$t_{C(on)}$			-	0.35	0.60	$\mu\text{s}$
$t_{off}$			-	1.15	1.60	$\mu\text{s}$
$t_{C(off)}$			-	0.15	0.30	$\mu\text{s}$
$t_{rr}$			-	0.20	-	$\mu\text{s}$
$I_{CES}$	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	-	-	1	mA
		$T_j = 125^\circ\text{C}$			10	

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$I_D$	Circuit current	Total of $V_{P1}-V_{NC}$ , $V_{N1}-V_{NC}$	-	-	3.10	mA
		$V_D=15\text{V}$ , $V_{IN}=0\text{V}$			4.20	
$I_{DB}$		Each part of $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	-	-	0.10	
		$V_D=V_{DB}=15\text{V}$ , $V_{IN}=5\text{V}$			0.10	
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15\text{V}$ (Note 5)	0.455	0.480	0.505	V
$UV_{DBt}$	P-side Control supply under-voltage protection(UV)	Trip level	9.0	10.0	12.0	V
$UV_{DBr}$		Reset level	9.0	10.0	12.0	V
$UV_{Dt}$	N-side Control supply under-voltage protection(UV)	Trip level	10.3	-	12.5	V
$UV_{Dr}$		Reset level	10.8	-	13.0	V
$V_{OT}$	Temperature Output	Pull down R=5.1k $\Omega$ (Note 6) LVIC Temperature=95 $^\circ\text{C}$	2.76	2.89	3.03	V
$OT_t$	Over temperature protection (Note 7)	$V_D = 15\text{V}$ , Trip level	115	130	145	$^\circ\text{C}$
$OT_{th}$		Detect LVIC temperature Hysteresis of trip-reset	-	10	-	$^\circ\text{C}$
$V_{FOH}$	Fault output voltage	$V_{SC} = 0\text{V}$ , $F_o$ terminal pulled up to 5V by 10k $\Omega$	4.9	-	-	V
$V_{FOL}$		$V_{SC} = 1\text{V}$ , $I_{FO} = 1\text{mA}$	-	-	0.95	V
$t_{FO}$	Fault output pulse width	(Note 8)	20	-	-	$\mu\text{s}$
$I_{IN}$	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between $U_P$ , $V_P$ , $W_P$ , $U_N$ , $V_N$ , $W_N-V_{NC}$	-	1.70	2.35	V
$V_{th(off)}$	OFF threshold voltage		0.70	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage		0.25	0.40	-	
$V_F$	Bootstrap Di forward voltage	$I_F=10\text{mA}$ including voltage drop by limiting resistor (Note 9)	1.1	1.7	2.3	V
R	Built-in limiting resistance	Included in bootstrap Di	80	100	120	$\Omega$

Note 5 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

6 : Temperature of LVIC vs.  $V_{OT}$  output characteristics is described in Fig.3. These minimum and maximum curves are based on theoretical designed value excluding LVIC temperature=95 $^\circ\text{C}$  limits.

7 : When the LVIC temperature exceeds OT trip temperature level( $OT_t$ ), OT protection works and  $F_o$  outputs. In that case if the heatsink dropped off or fixed loosely, don't reuse that DIIPM. (There is a possibility that junction temperature of power chips exceeded maximum  $T_j(150^\circ\text{C})$ .)

8 : Fault signal  $F_o$  outputs when SC, UV or OT protection works.  $F_o$  pulse width is different for each protection modes. At SC failure,  $F_o$  pulse width is a fixed width (=minimum 20 $\mu\text{s}$ ), but at UV or OT failure,  $F_o$  outputs continuously until recovering from UV or OT state. (But minimum  $F_o$  pulse width is 20 $\mu\text{s}$ .)

9 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of Bootstrap Di  $V_F$ - $I_F$  curve (@ $T_a=25^\circ\text{C}$ ) Including Voltage Drop by Limiting Resistor (Right chart is enlarged chart.)

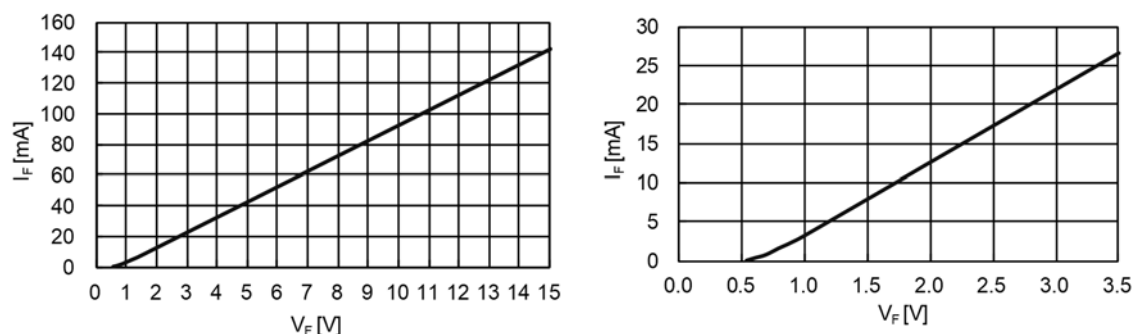
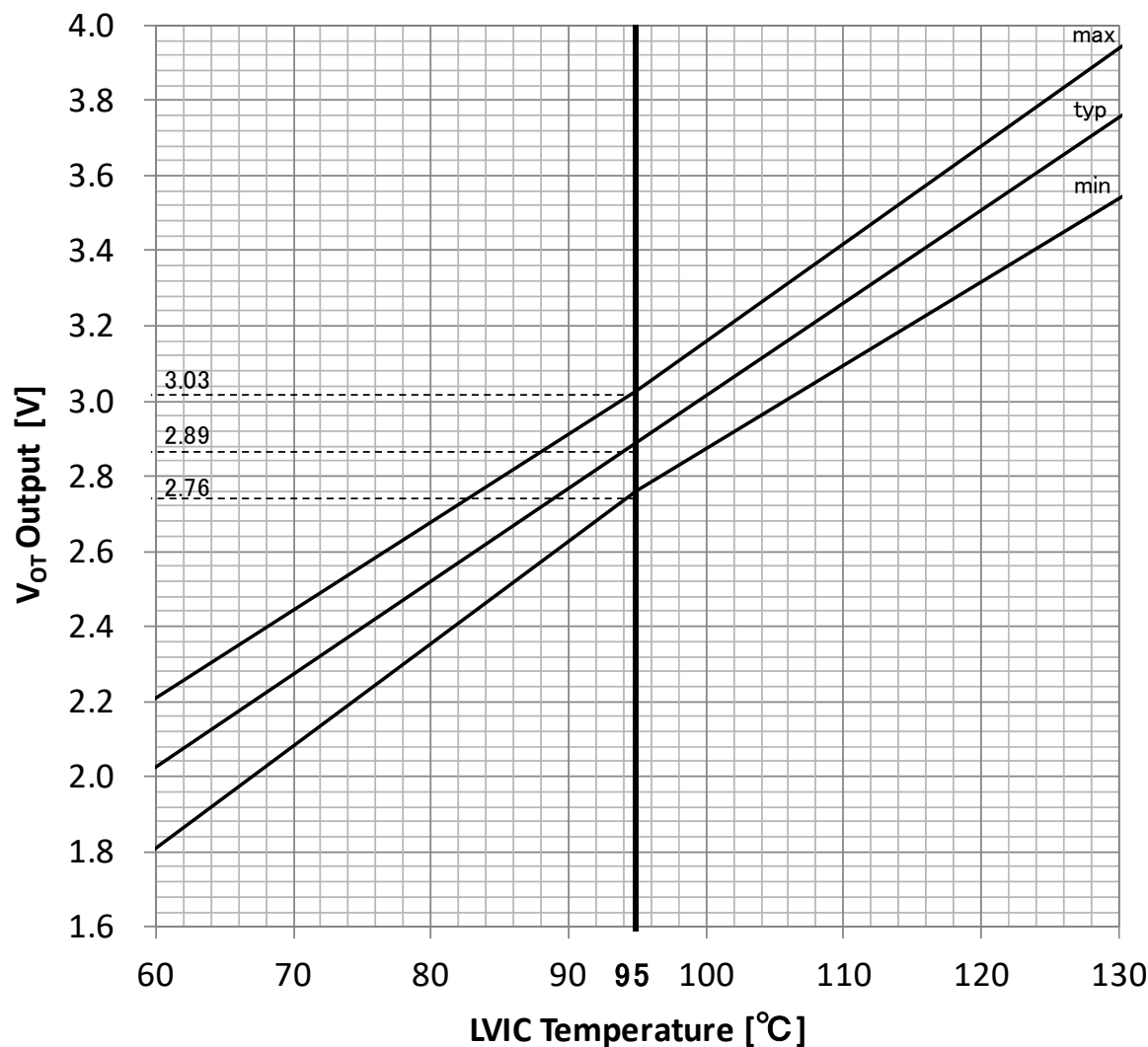
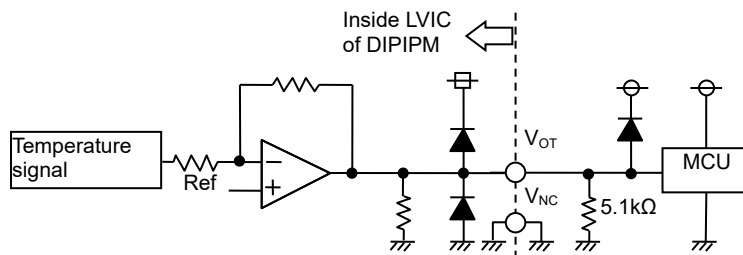


Fig. 3 Temperature of LVIC vs.  $V_{OT}$  Output CharacteristicsFig. 4 Pattern Wiring Around the Analog Voltage Output Circuit [ $V_{OT}$  terminal]

- (1)  $V_{OT}$  outputs the analog signal that is amplified signal of temperature detecting element on LVIC by inverting amplifier.
- (2) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between  $V_{OT}$  and  $V_{NC}$ (control GND), the extra circuit current, which is calculated approximately by  $V_{OT}$  output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using  $V_{OT}$  for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (3) In the case of using  $V_{OT}$  with low voltage controller like 3.3V MCU,  $V_{OT}$  output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and  $V_{OT}$  output for preventing over voltage destruction.
- (4) In the case of not using  $V_{OT}$ , leave  $V_{OT}$  output NC (No Connection).

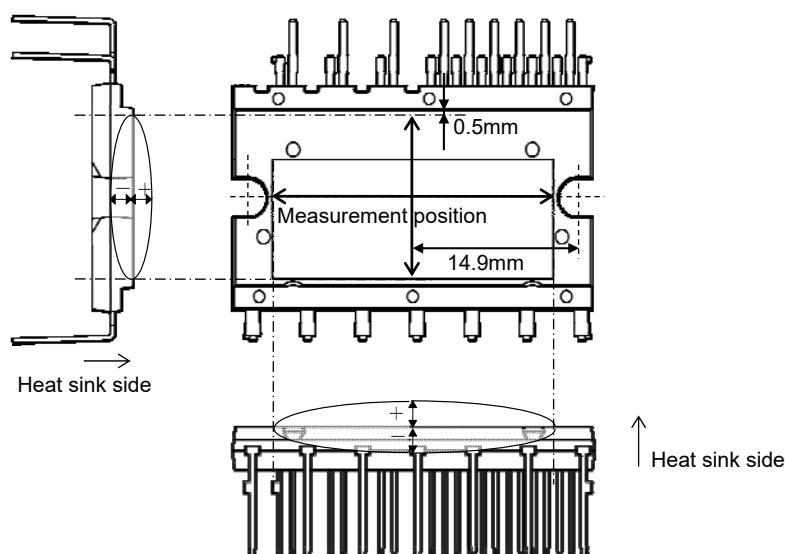
Refer the application note for SLIMDIP series about the usage of  $V_{OT}$ .

**SLIMDIP-W****TRANSFER MOLDING TYPE  
INSULATED TYPE****MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition	Reference	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 10)	JEITA-ED-4701 402 method II	0.59	0.69	0.78	N·m
Terminal strength pull	Control terminal: Load 5N Power terminal: Load 10N	JEITA-ED-4701 401 method I	10	-	-	s
Terminal strength bending	Control terminal: Load 2.5N Power terminal: Load 5N 90deg. Bend	JEITA-ED-4701 401 method III	2	-	-	times
Weight		-	-	5.5	-	g
Heat radiation part flatness	(Note 11)	-	-30	-	80	μm

Note 10: Plain washers (ISO 7089~7094) are recommended.

Note 11: Measurement positions of heat radiation part flatness are as below

**RECOMMENDED OPERATION CONDITIONS**

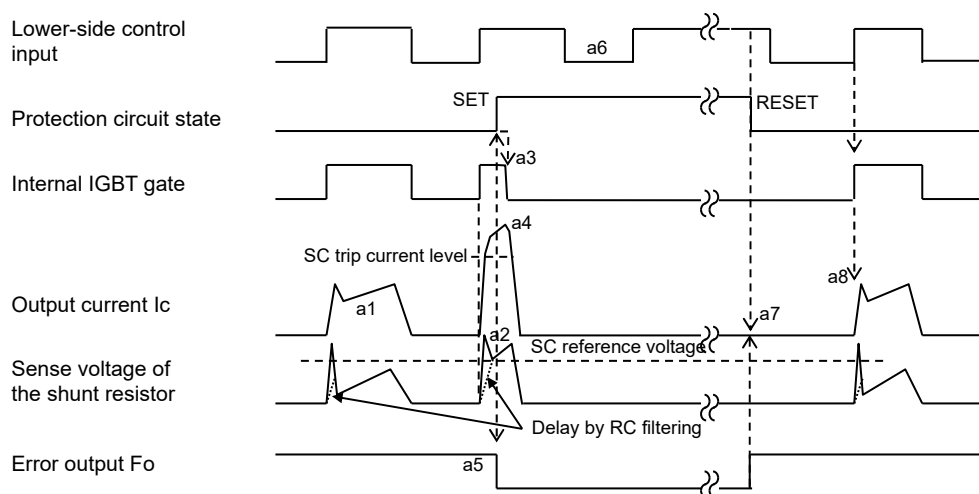
Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{NC}$ , $V_{N1}-V_{NC}$	13.5	15.0	16.5	V
$V_{DB}$	Control supply voltage	Applied between $V_{UEB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	13.0	15.0	18.5	V
$\Delta V_D$ , $\Delta V_{DB}$	Control supply variation		-1	-	+1	V/μs
$t_{dead}$	Arm shoot-through blocking time	For each input signal	1.0	-	-	μs
$f_{PWM}$	PWM input frequency	$T_C \leq 115^\circ\text{C}$ , $T_J \leq 125^\circ\text{C}$	-	-	20	kHz
PWIN(on)	Minimum input pulse width	(Note 12)	0.7	-	-	μs
PWIN(off)			0.7	-	-	
$V_{NC}$	$V_{NC}$ variation	Between $V_{NC}-NU$ , NV, NW (including surge)	-5.0	-	+5.0	V
$T_J$	Junction temperature		-20	-	125	°C

Note 12: When inputting shorter pulse than PWIN(on) / PWIN(off), DIIPM might not make response.

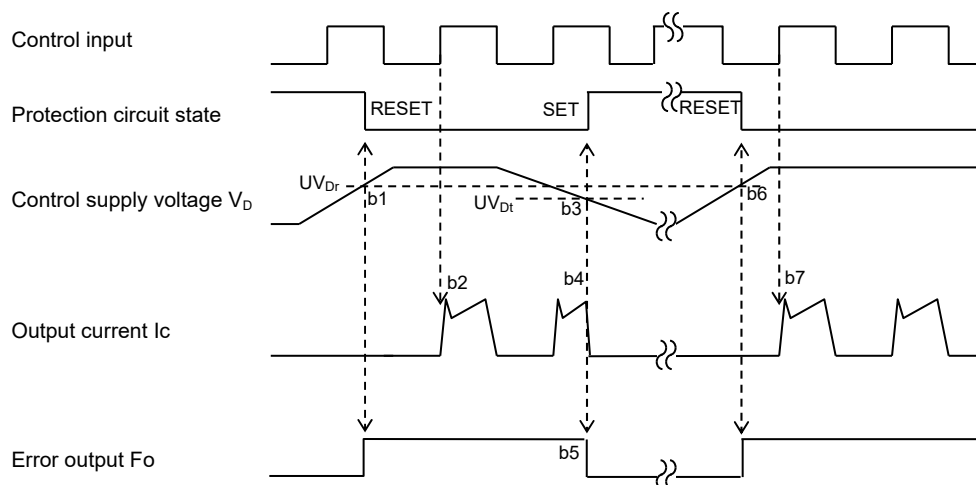
Fig. 5 Timing Charts of The DIIPM Protective Functions

**[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)**

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)  
(It is recommended to set RC time constant 1.5~2.0 $\mu$ s so that IGBT shut down within 2.0 $\mu$ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F<sub>O</sub> outputs for t<sub>Fo</sub>=minimum 20 $\mu$ s.
- a6. Input = "L": IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L $\rightarrow$ H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.

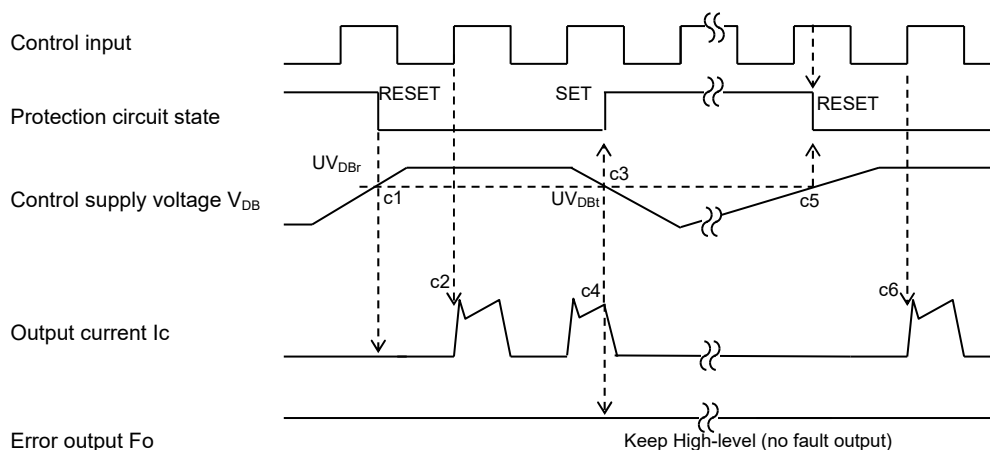
**[B] Under-Voltage Protection (N-side, UV<sub>D</sub>)**

- b1. Control supply voltage V<sub>D</sub> exceeds under voltage reset level (UV<sub>Dr</sub>), but IGBT turns ON by next ON signal (L $\rightarrow$ H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V<sub>D</sub> level drops to under voltage trip level. (UV<sub>Dt</sub>).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. F<sub>O</sub> outputs for t<sub>Fo</sub>=minimum 20 $\mu$ s, but output is extended during V<sub>D</sub> keeps below UV<sub>Dr</sub>.
- b6. V<sub>D</sub> level reaches UV<sub>Dr</sub>.
- b7. Normal operation: IGBT ON and outputs current.



**[C] Under-Voltage Protection (P-side,  $UV_{DB}$ )**

- c1. Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBr}$ , IGBT turns on by next ON signal (L→H).  
 c2. Normal operation: IGBT ON and outputs current.  
 c3.  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBt}$ ).  
 c4. IGBT of the corresponding phase only turns OFF in spite of control input signal level, but there is no  $F_o$  signal output.  
 c5.  $V_{DB}$  level reaches  $UV_{DBr}$ .  
 c6. Normal operation: IGBT ON and outputs current.

**[D] Over Temperature Protection (N-side, Detecting LVIC temperature)**

- d1. Normal operation: IGBT ON and outputs current.  
 d2. LVIC temperature exceeds over temperature trip level ( $OT_t$ ).  
 d3. All N-side IGBTs turn OFF in spite of control input condition.  
 d4.  $F_o$  outputs for  $t_{Fo}$ =minimum 20 $\mu$ s, but output is extended during LVIC temperature keeps over  $OT_t$ .  
 d5. LVIC temperature drops to over temperature reset level.  
 d6. Normal operation: IGBT turns on by next ON signal (L→H).  
 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)

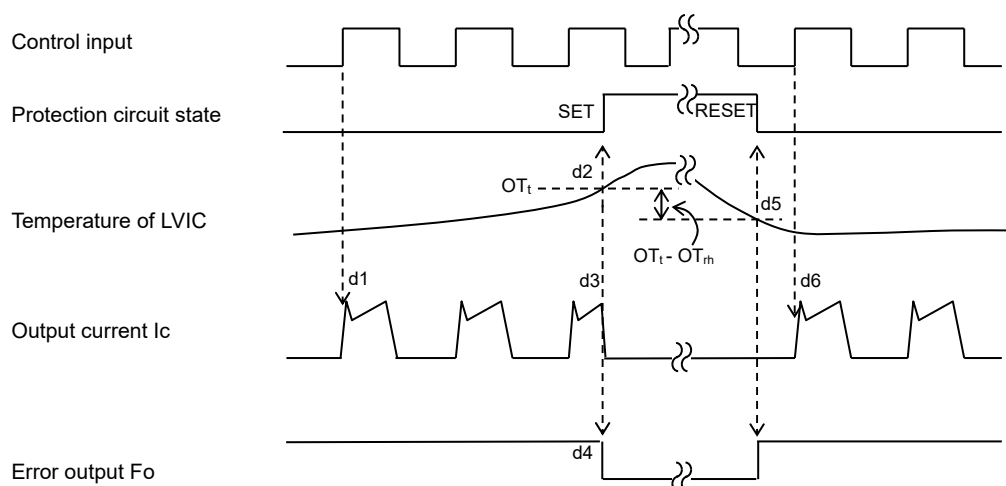
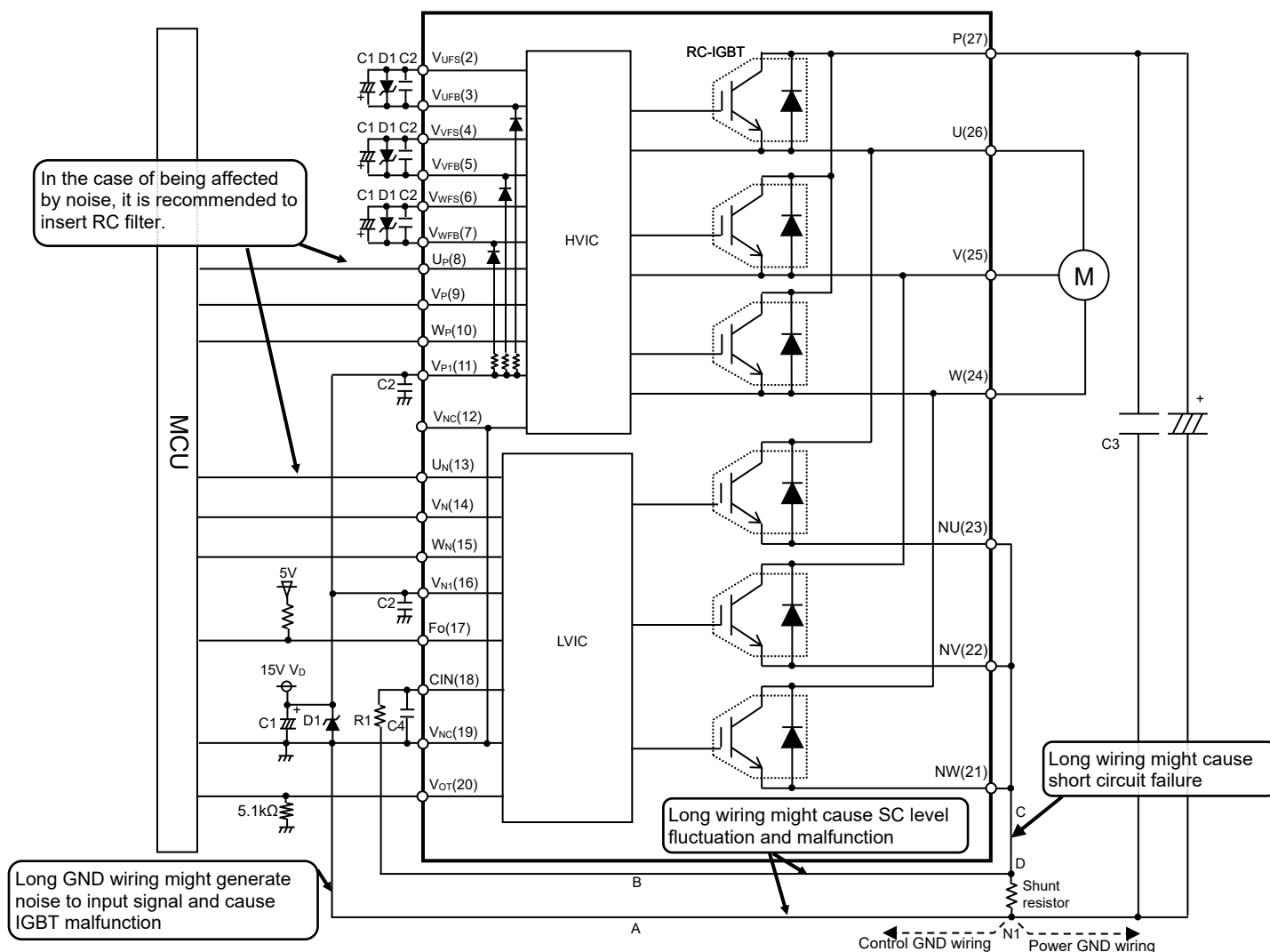


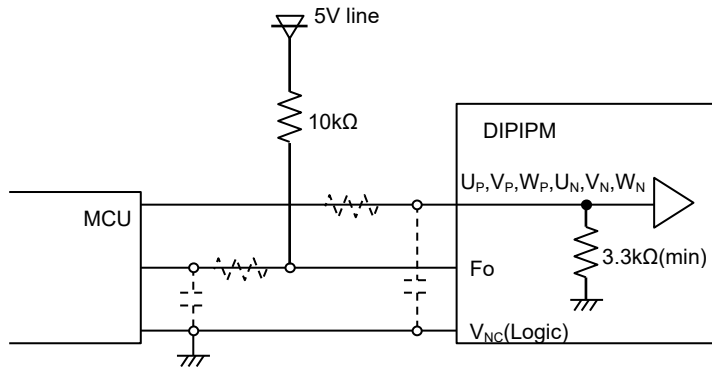
Fig. 6 Example of Application Circuit



- (1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
- (2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
- (3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
- (4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
- (5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- (6) The point D at which the wiring to C<sub>IN</sub> filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
- (7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.01μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- (8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- (9) Thanks to built-in HVIC, direct coupling to MCU without any optocoupler or transformer isolation is possible.
- (10) F<sub>O</sub> output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I<sub>F0</sub> up to 1mA. (I<sub>F0</sub> is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
- (11) Two V<sub>NC</sub> terminals are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
- (12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤ ±1V/μs, V<sub>ripple</sub> ≤ 2Vp-p.

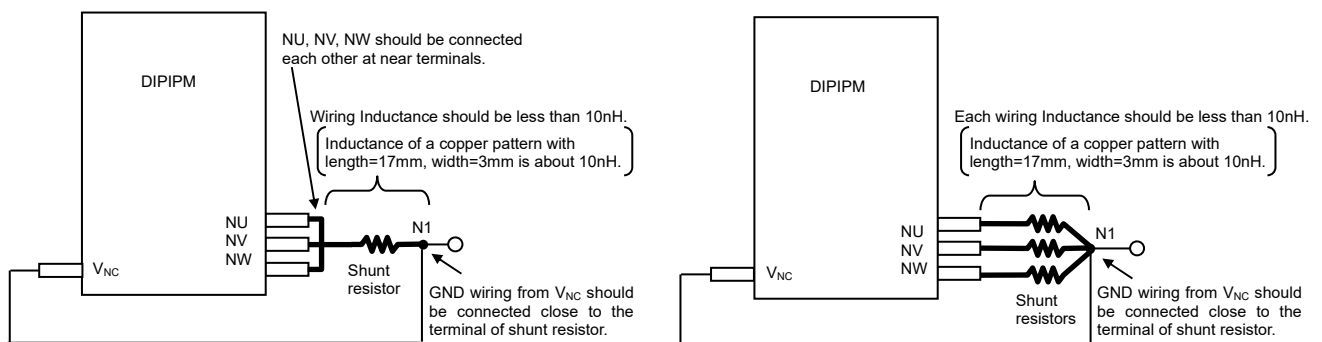


Fig. 7 MCU I/O Interface Circuit



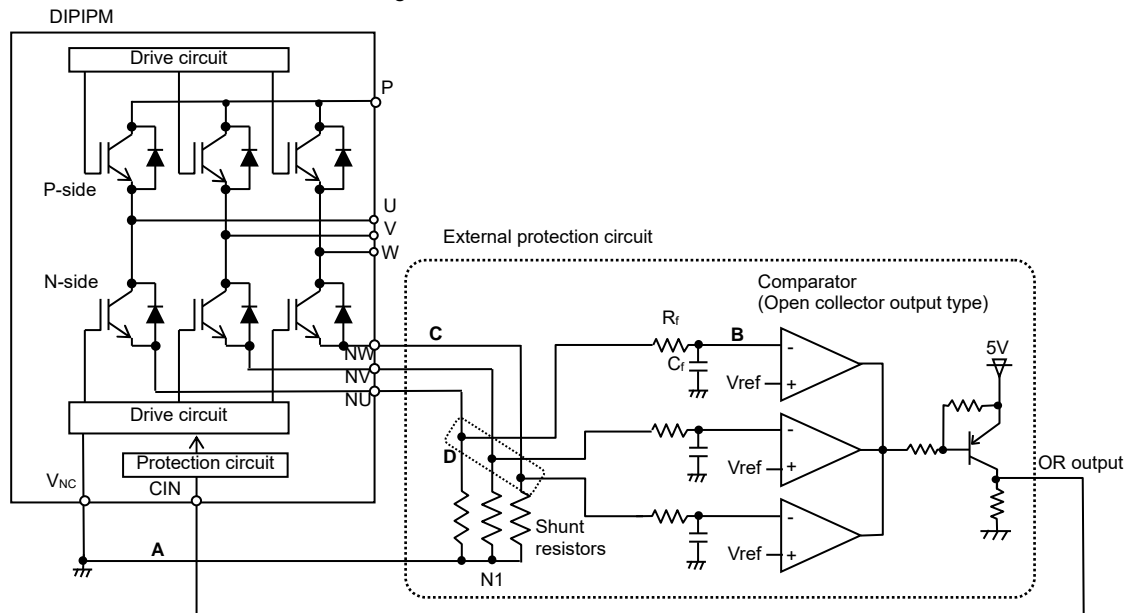
Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board. The DIIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 9 External SC Protection Circuit with Using Three Shunt Resistors

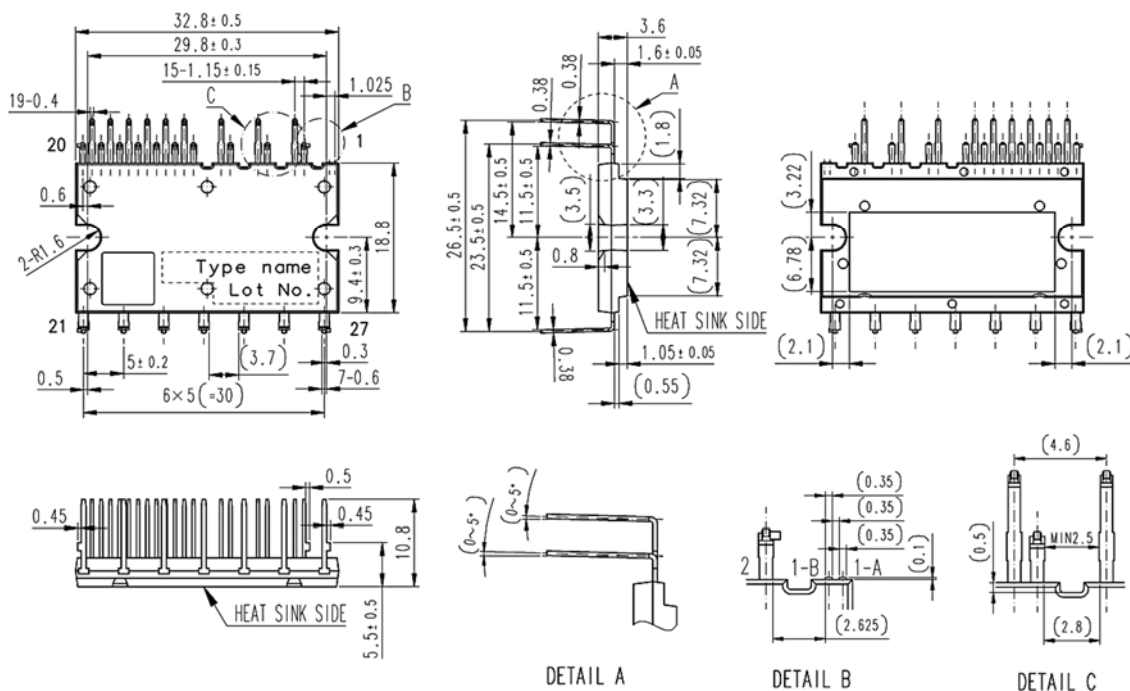
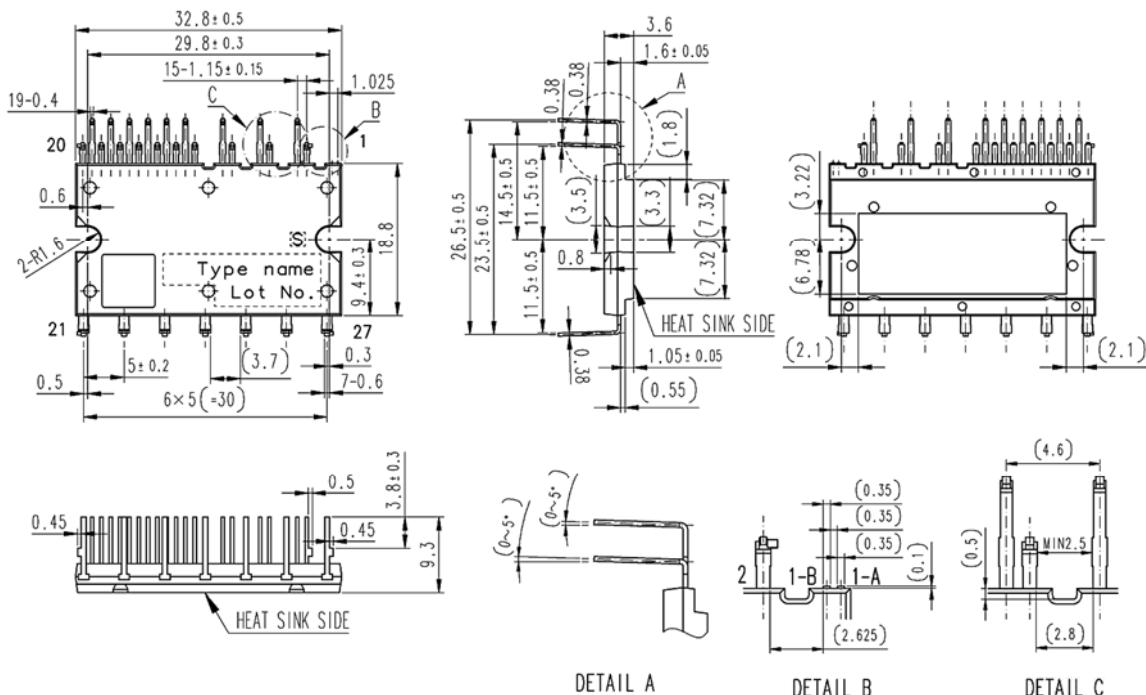


- (1) It is necessary to set the time constant  $R_r C_f$  of external comparator input so that IGBT stop within  $2\mu s$  when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) The threshold voltage  $V_{ref}$  should be set up the same rating of short circuit trip level ( $V_{sc(ref)}$  typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified maximum value.
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- (6) OR output high level should be over 0.505V (=maximum  $V_{sc(ref)}$ ).
- (7) GND of Comparator,  $V_{ref}$  circuit and  $C_f$  should be not connected to noisy power GND but to control GND wiring.

**SLIMDIP-W****TRANSFER MOLDING TYPE  
INSULATED TYPE**

Fig. 10 Package Outlines

[Dimension: mm]

**[ SLIMDIP-W Suffix:500 : Normal Terminal Type ]****[ SLIMDIP-W Suffix:505 : Short Terminal Type ]**Note: Connect only one V<sub>NC</sub> terminal (No.12 or 19) to the system GND and leave another one open.

### **Important Notice**

The information contained in this datasheet shall in no event be regarded as a guarantee of conditions or characteristics. This product has to be used within its specified maximum ratings, and is subject to customer's compliance with any applicable legal requirement, norms and standards.

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**Keep safety first in your circuit designs!**

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