Microtips TECHNOLOGY

Model No: MTD0130CMOG-1

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Record of Revision

Date	Revision No.	Summary
2020-03-31	1.0	Rev 1.0 was issued
2020-04-07	1.1	Modify some details on drawing page 4

1. Scope

This data sheet is to introduce the specification of MTD0130CMOG-1, AMOLED display module. It is composed of an AMOLED panel, driver IC and FPC. The 1.30″ display area contains 360 (RGB) x 360 pixels.

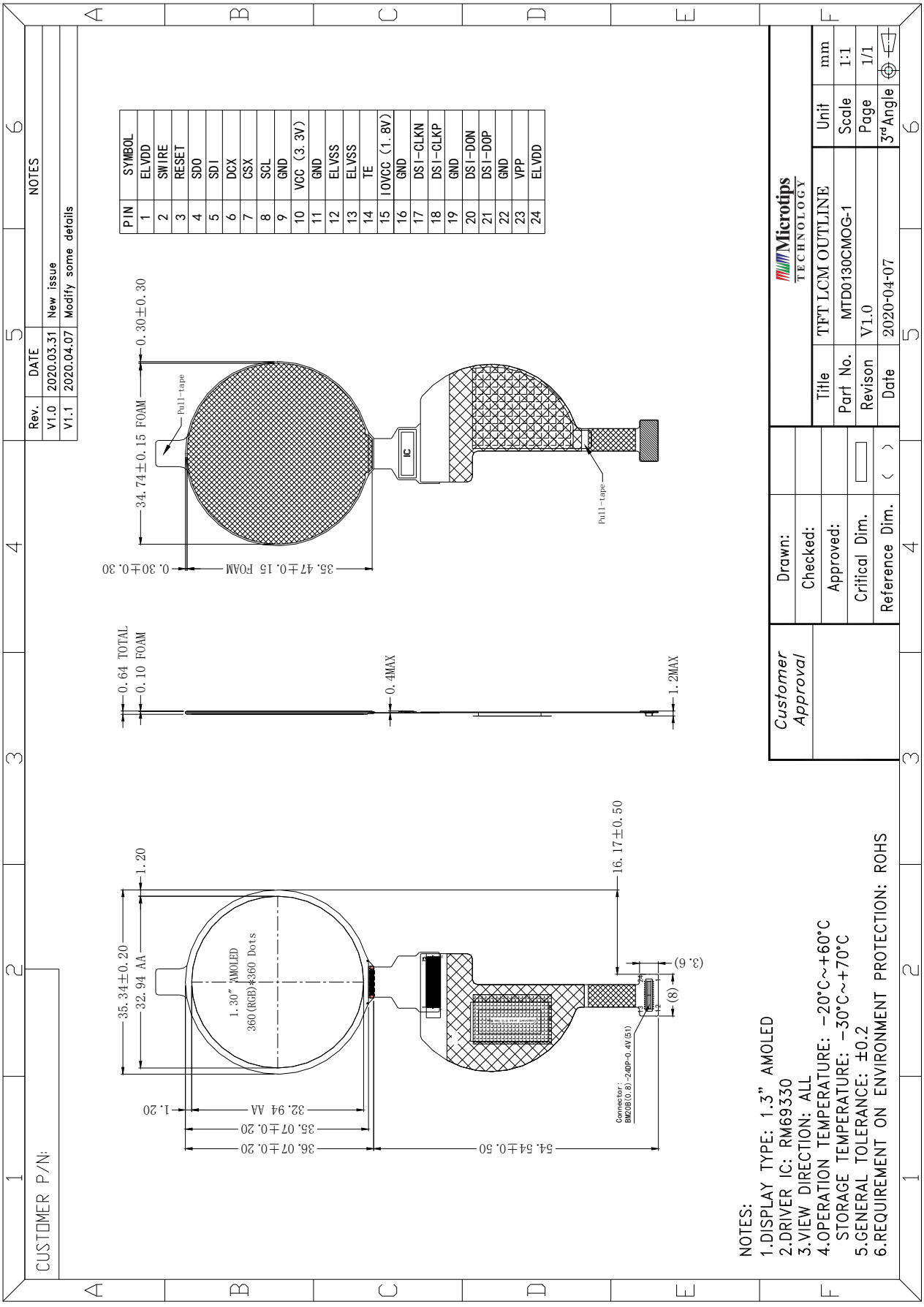
2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.

3. General Information

Item	Contents	Unit
Size	1.30	inch
Display Technology	AMOLED	/
Resolution	360(RGB) × 360	/
Display Color	16.7M	/
Interface	MIPI & SPI	/
Outline Dimension	35.34 x 36.07 x 0.64	mm
Active Area	Φ32.94	mm
Driver IC	RM69330	/
Operating Temperature	-20℃ ~ +60℃	/
Storage Temperature	-30℃ ~ +70℃	/

4. Outline Drawing



5. Interface signals

Pin No.	Pin Name	Description
1	ELVDD	Positive power supply for panel
2	SWIRE	Enable Vpos and Vneg for DCDC IC
3	RESET	Display reset
4	SDO	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal.
5	SDI	Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal.
6	DCX	Display data/command selection in 80-series MPU I/F and 4-wire SPI I/F
7	CSX	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F
8	SCL	A synchronous clock signal in SPI I/F
9	GND	Ground
10	VCC(3.3V)	Analog power for Driver IC
11	GND	Ground
12	ELVSS	Negative power supply for panel
13	ELVSS	Negative power supply for panel
14	TE	Tearing effect output pin to synchronize MCU to frame writing
15	IOVCC(1.8V)	Digital power for Driver IC
16	GND	Ground
17	DSI-CLKN	MIPI DSI Clock -
18	DSI-CLKP	MIPI DSI Clock +
19	GND	Ground
20	DSI-D0N	MIPI Data0 -
21	DSI-D0P	MIPI Data0 +
22	GND	Ground
23	VPP	External High voltage input for external OTP data program. Set GND for board.
24	ELVDD	Positive power supply for panel

6. Environment Conditions

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Power Supply voltage	PVDD	4.6	4.6	V	Fixed
	PVEE	-1.4	-4.4	V	
	VDD	2.7	3.6	V	
	VDDI	1.65	3.3	V	

6.2 Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-20	60	℃	
Storage Temperature	TSTG	-30	70	℃	

7. Electrical Specifications

7.1 Electrical characteristics

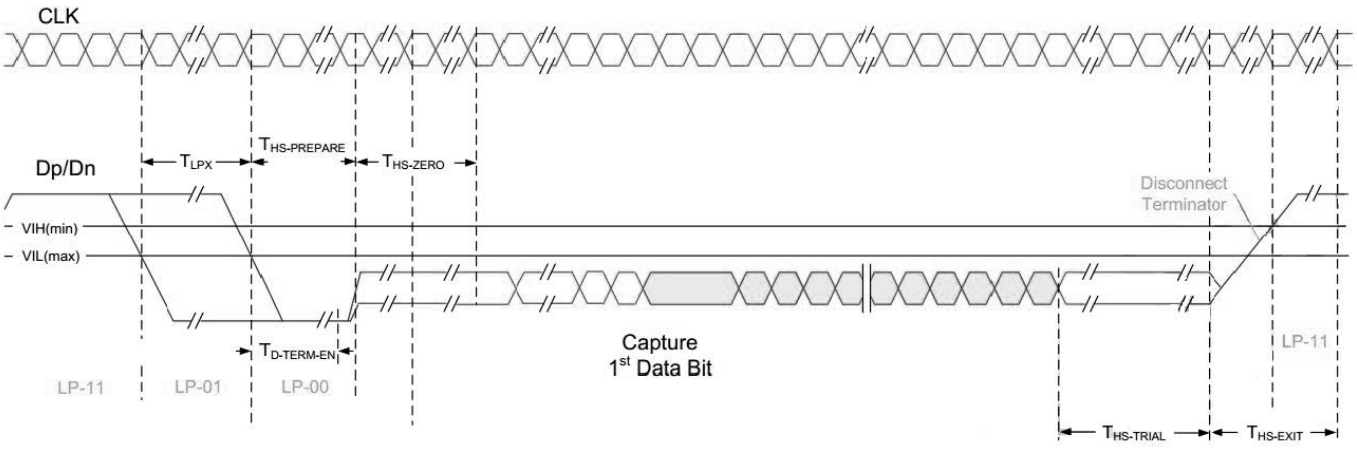
Frame rate = 60Hz, white pattern

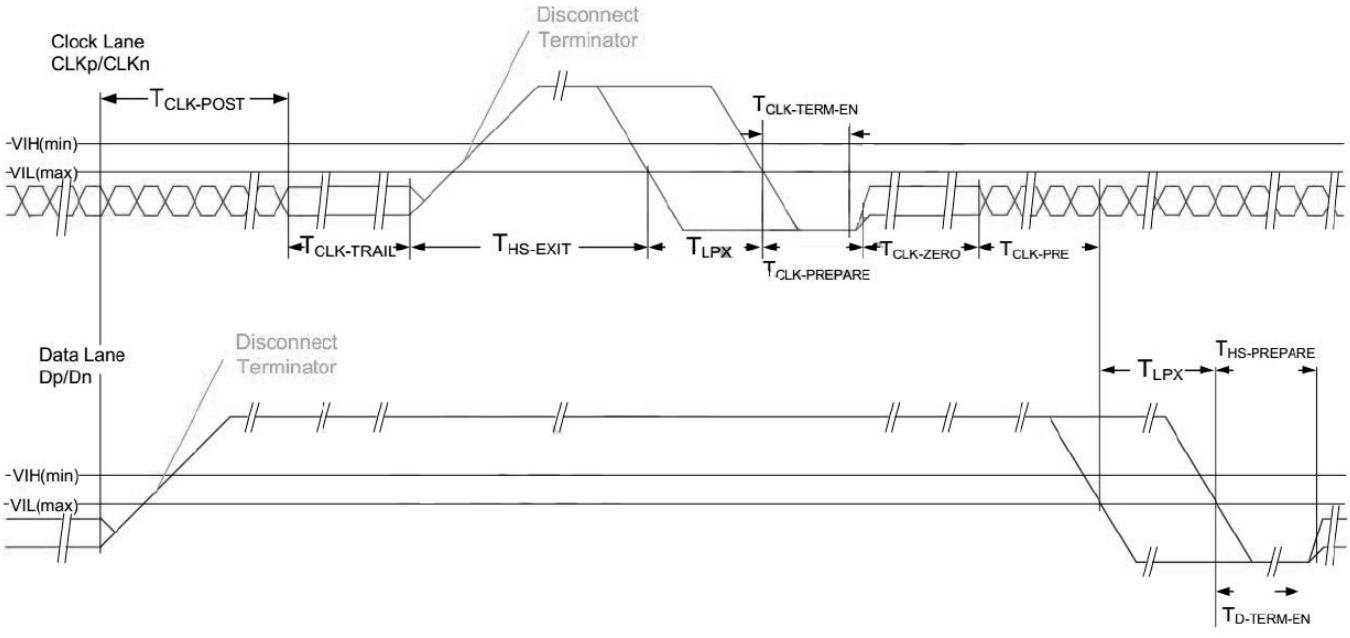
Item		Symbol	MIN	TYP	MAX	Unit	Remark
Analog Voltage		VDD (VCI)	2.7	3.3	3.6	V	Frame rate = 60Hz White pattern
Logic Voltage		VDDI	1.65	1.8	3.6	V	
OLED Positive Voltage		PVDD	-	4.6	-	V	
OLED Negative Voltage		PVEE	-1.4	-2.4	-4.4		
Logic Input Voltage	“H” level	VIH	0.8×VDDI	-	VDDI	V	VDDI=1.65~3.3V
	“L” level	VIL	0	-	0.2×VDDI	V	
Logic Output Voltage	“H” level	VOH	0.8×VDDI	-	VDDI	V	IOH= -1.0mA IOL= +1.0mA
	“L” level	VOL	0	-	0.2×VDDI	V	
Logic Input Current (except MIPI/MDDI)	“H” level	IIHD	-	-	1	μA	Vin=0~VDDI
	“L” level	IILD	-1	-	-	μA	
Logic Output Current (MIPI/ MDDI)	“H” level	IIHD	-	-	1	μA	
	“L” level	IILD	-1	-	-	μA	

Current Consumption (Display)	Normal mode	IVDD	-	1.34	-	mA	Frame rate =60Hz White pattern
		IVDDI	-	1.46	-	mA	
		IPVDD IPVEE	-	15.8	-	mA	
	Sleep in mode	IVDD	-	13	-	μA	
		IVDDI	-	4	-	μA	
		IPVDD IPVEE	-	0	-	μA	
Power Ripple	VDD, AVDD, VDDI		-45	-	+45	mV	
	PVDD, PVEE		-35	-	+35	mV	

8. Command/AC Timing

8.1 MIPI Interface Characteristics



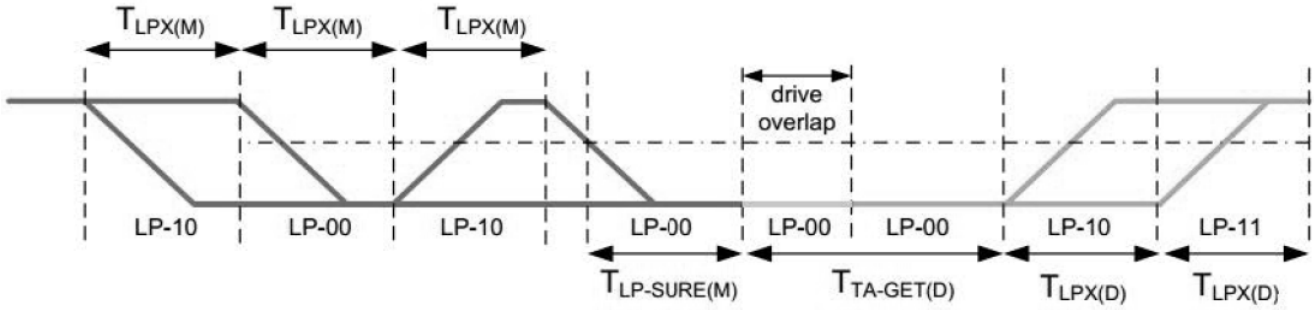


Timing Parameters:

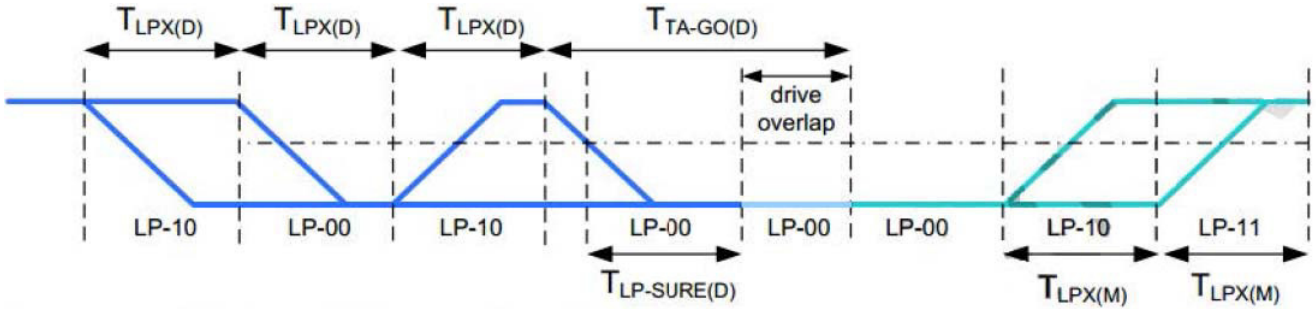
Parameter	Description	Min.	Typ.	Max.	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60ns+52*UI	-	-	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300	-	-	ns
TCLK-TERM-EN	Time for the clock lane receiver to enable the HS line state immediately before the HS-0 line state starting the HS transmission.	Time for Dn to reach VTERM-EN	-	38	ns
TCLK-PREPARE	Time that the transmitter drives the clock lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.	38	-	95	na
TCLK-RPE	Time that the HS clock shall be driven by the transmitter prior to any associated data lane beginning the transition from LP to HS mode	8	-	-	UI
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE+ time that the transmitter drives the HS-0 state prior to starting the clock.	300	-		ns
TD-TERM-EN	Time for the data lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL max.	Time for Dn to reach VTERM-EN	-	35ns+4*UI	ns
TCLK-PREPARE	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission.	40ns+4*UI	-	85ns+6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE+ time that the transmitter drives the HS-0 state prior to transmitting the sync sequence.	145ns+10UI	-	-	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	60ns+4*UI	-	-	ns

Parameter	Description	Min.	Typ.	Max.	Unit
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE+ time for lead HS-0 drive period before starting the clock.	300	-	-	ns
TCLK-RPE	Time that the HS clock is driven prior to any associated data lane beginning the transition from LP to HS mode	8	-	-	UI
TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of an HS transmission burst	60	-	-	ns

Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



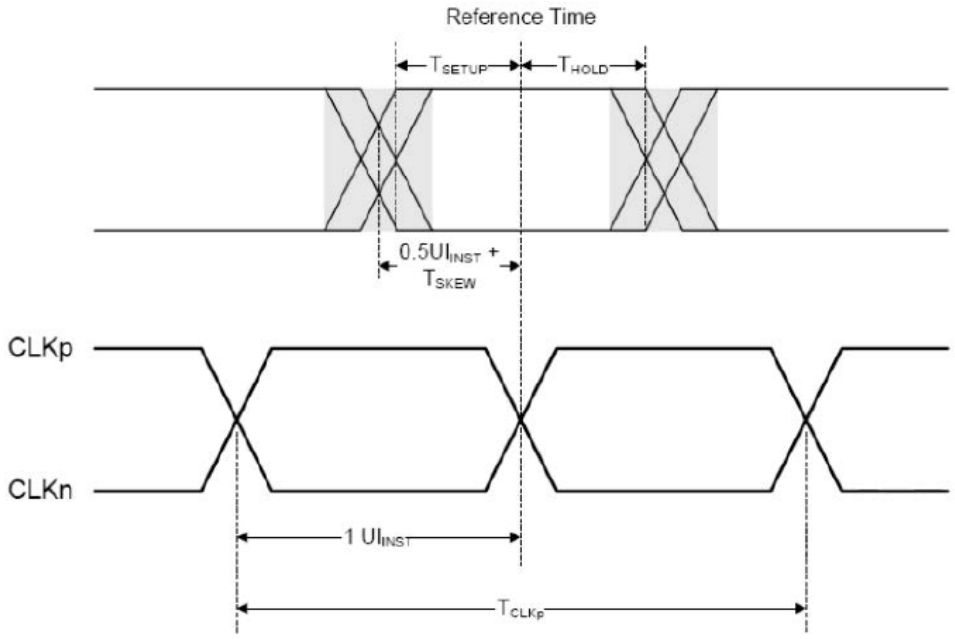
Bus turnaround (BAT) from display module to MPU timing

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{LPX(M)}$	Transmitted length of any Low-power state period of MCU to display module	50	-	150	ns Note1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a link turnaround.	$T_{LPX(M)}$	-	2* $T_{LPX(M)}$	UI Note2
$T_{LPX(D)}$	Transmitted length of any Low-power state period of display module to MCU.	50	-	150	Ns Note1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a link turnaround.		5*$T_{LPX(D)}$	-	Ns Note2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a link turnaround.		4*$T_{LPX(D)}$	-	Ns Note2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) a during a link turnaround.	$T_{LPX(D)}$		2*$T_{LPX(D)}$	Ns Note2

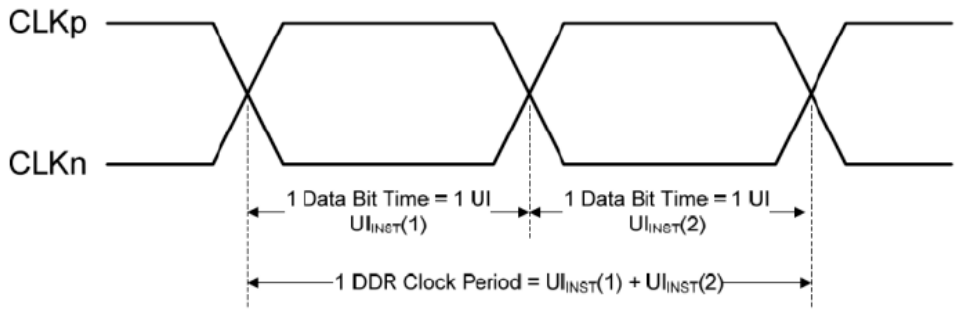
Notes:

1. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter.

8.2 MIPI Data to clock Timing Definition



DDR Clock Definition



Clock Parameter	Symbol	Min.	TYP.	Max.	Units	Notes
UI instantaneous	UIINST	2	-	12.5	ns	Note1,2

Notes:

1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

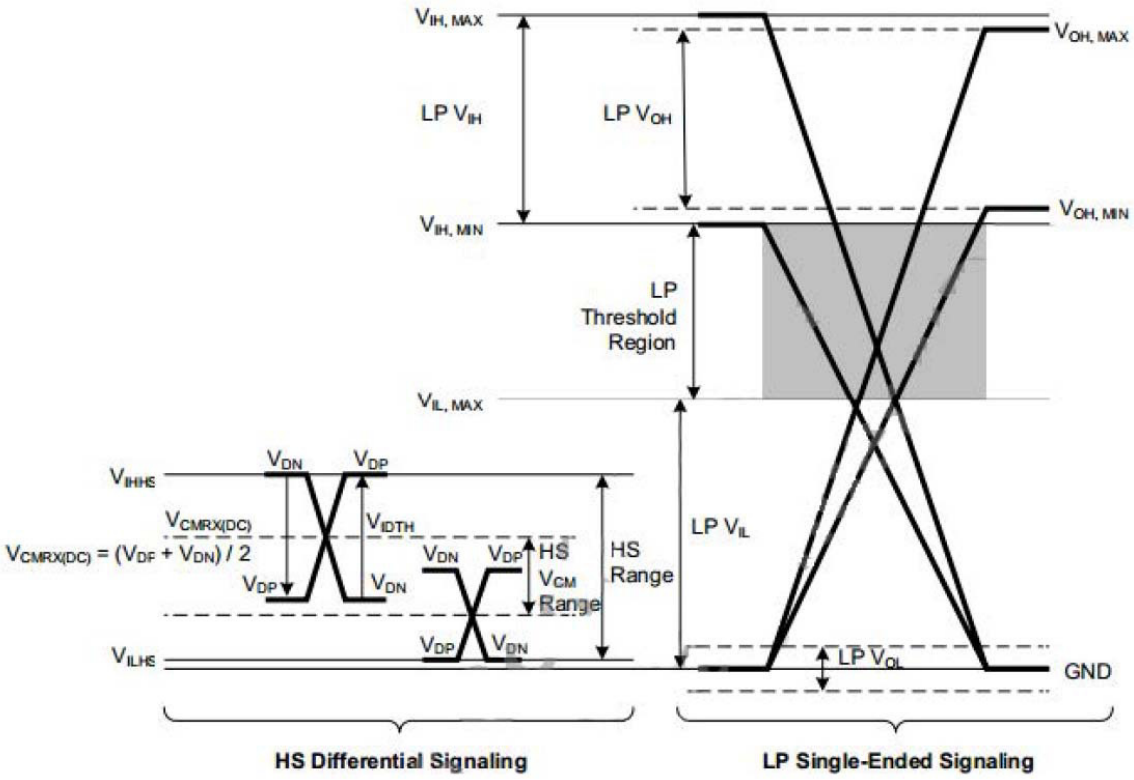
Data-Clock Timing Specifications

Parameter	Symbol	Min.	TYP.	Max.	Units	Notes
Data to clock skew [measured at transmitter]	TSKEW[TX]	-0.15	-	0.15	UIINST	Note1
Data to clock setup time [receiver]	TSETUP[RX]	0.15	-	-	UIINST	Note2
Clock to Data hold time [receiver]	THOLD[RX]	0.15	-	-	UIINST	Note2

Notes:

1. Total silicon and package delay budget of 0.3* UI_{INST}.
2. Total setup and hold window for receiver of 0.3* UI_{INST}.

8.3 MIPI D-PHY Characteristics



Item		Symbol	Min.	TYP.	Max.	Units	Test Condition
HS-RX	Differential input high threshold	VIDTH	-	-	70	mV	IOVCC=DPHYVCC=1.65~3.60V
	Differential input Low threshold	VIDTL	-70	-	-	mV	IOVCC=DPHYVCC=1.65~3.60V
	Single-ended Input low voltage	VILHS	-40	-	-	mV	IOVCC=DPHYVCC=1.65~3.60V
	Single-ended Input high voltage	VIHHS	-	-	460	mV	IOVCC=DPHYVCC=1.65~3.60V
	Common-mode Voltage HS receive Mode[1]	VCMRX(DC)	70	-	330	mV	IOVCC=DPHYVCC=1.65~3.60V
	Differential input Impedance[2]	ZID	-	100	-	Ω	IOVCC=DPHYVCC=1.65~3.60V
LP-RX	Logic 0 input voltage not in ULP state	VIL	-50	-	550	mV	IOVCC=DPHYVCC=1.65~3.60V
	Logic 1 input voltage	VIH	880	-	1350	mV	IOVCC=DPHYVCC=1.65~3.60V
	I/O leakage current	ILEAK	-10	-	10	μA	Vin=-50 mV-1350 mV
LP-TX	Thevenin output Low level	VOL	-50	-	50	mV	IOVCC=DPHYVCC=1.65~3.60V

	Thevenin output High level	VOH	1.1	1.2	1.3	V	IOVCC=DPHYVCC=1.65~3.60V
	Output impedance of LP transmitter[2]	ZOLP	110	-	-	Ω	IOVCC=DPHYVCC=1.65~3.60V
CD-RX	Logic 0 contention threshold	VILCD	-	-	200	mV	IOVCC=DPHYVCC=1.65~3.60V
	Logic 1 contention threshold	VIHCD	450	-	-	mV	IOVCC=DPHYVCC=1.65~3.60V

Notes:

1. VCMRX(DC)=(VDP+VDN)/2
2. Excluding COF/COG resistance (contact resistance and ITO wiring resistance)

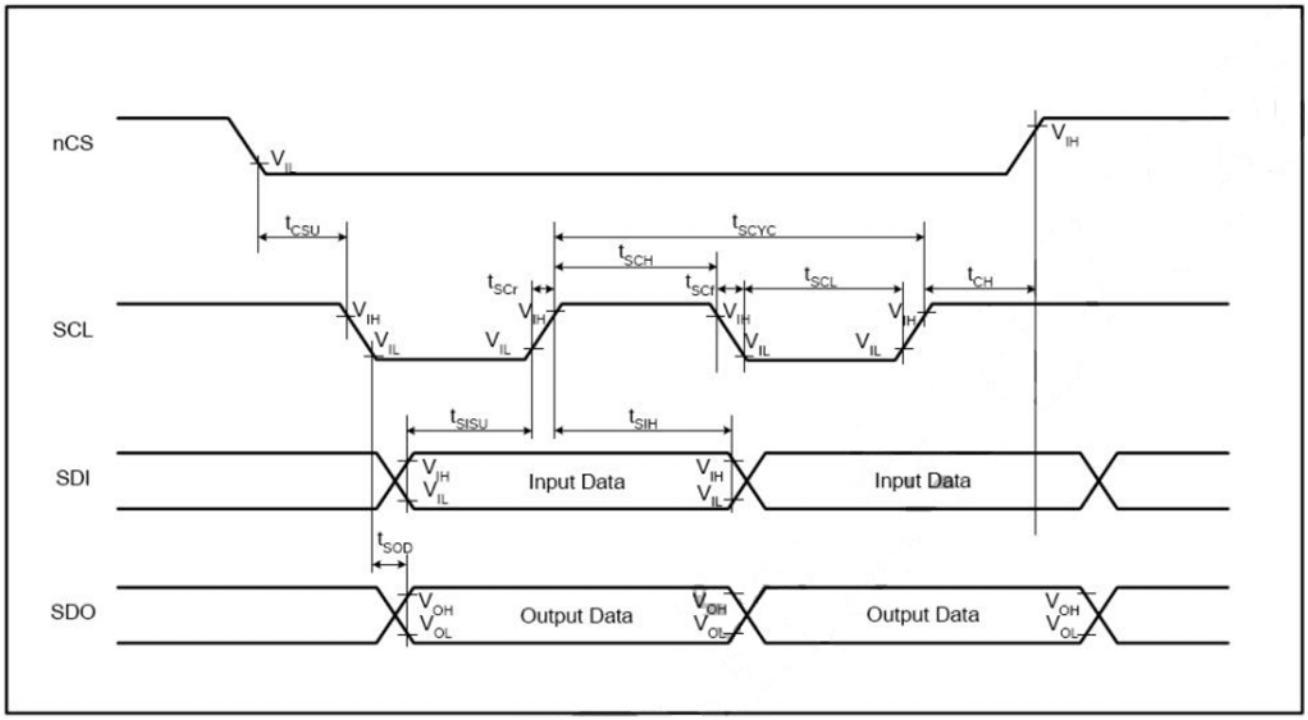
8.4 SPI Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
SCL	TSCYC	Clock cycle (Write)	20	-	ns
	TSCYC	Clock cycle (Read)	300	-	ns
	TSCH	Clock “H” pulse width (Write)	9	-	ns
	TSCH	Clock “H” pulse width (Read)	140	-	ns
	TSCL	Clock “L” pulse width (Write)	9	-	ns
	TSCL	Clock “L” pulse width (Read)	140		ns
	TSCr	Clock rise time	-	2	ns
	TSCf	Clock fall time	-	2	ns
nCS	TCSU	Chip select setup time	10	-	ns
	TCH	Chip select hold time	10	-	ns
SDI(SDA)	TSISU	Data input setup time	5	-	ns
	TSIH	Data input hold time	5	-	ns
SDO(SDA)	TSOD	Data output setup time	-	120	ns
	TSOH	Data output hold time	5	-	ns

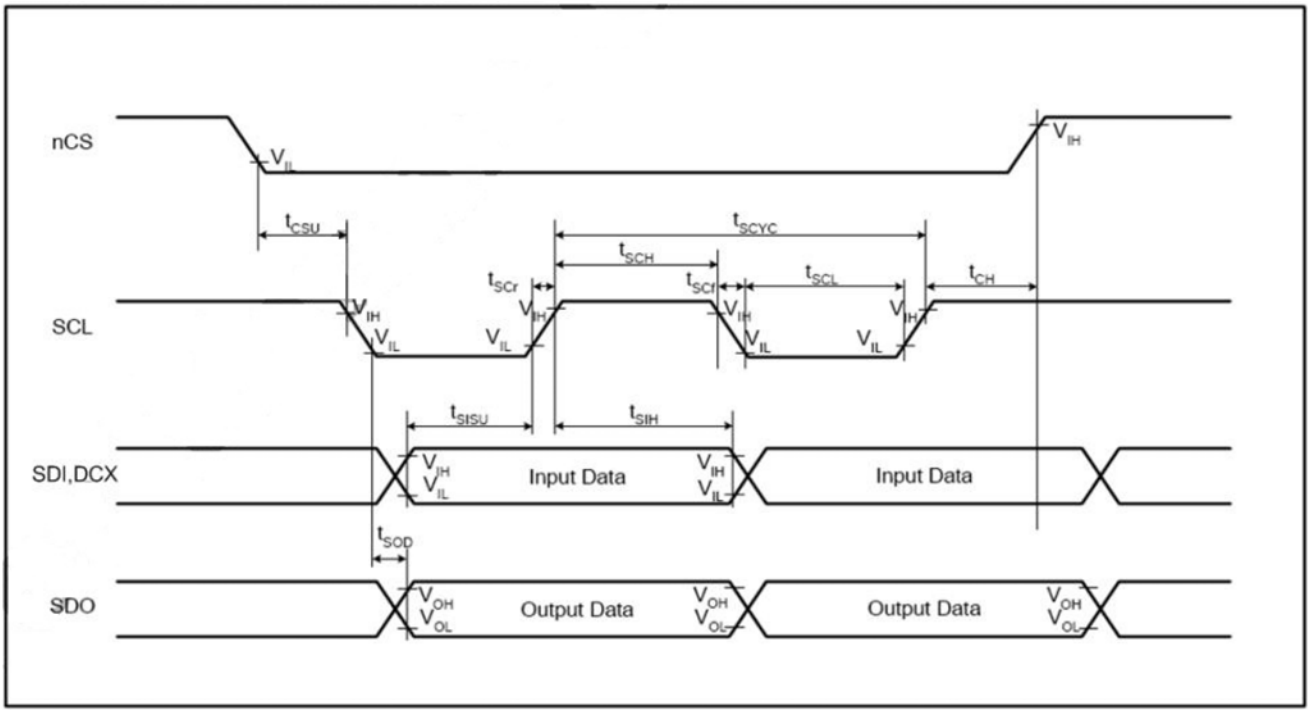
Notes:

1. Logic high and low levels are specified as 20% and 80% of VDDI for input signals.
2. Ta= -30 to 70℃, VDDI=1.65V to 3.3V, VDD=2.7V to 3.6V, GND=0V.

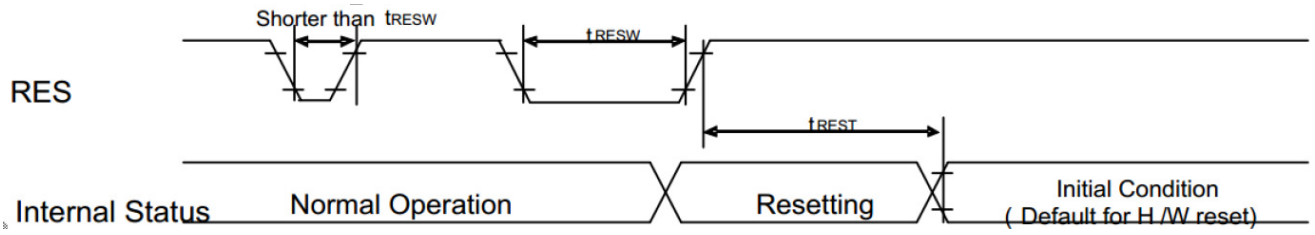
3-Wire SPI Serial Interface Characteristics



4-Wire SPI Serial Interface Characteristics



8.5 Reset Timing



VDDI=1.65 to 3.3V, VDD=2.7 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃.

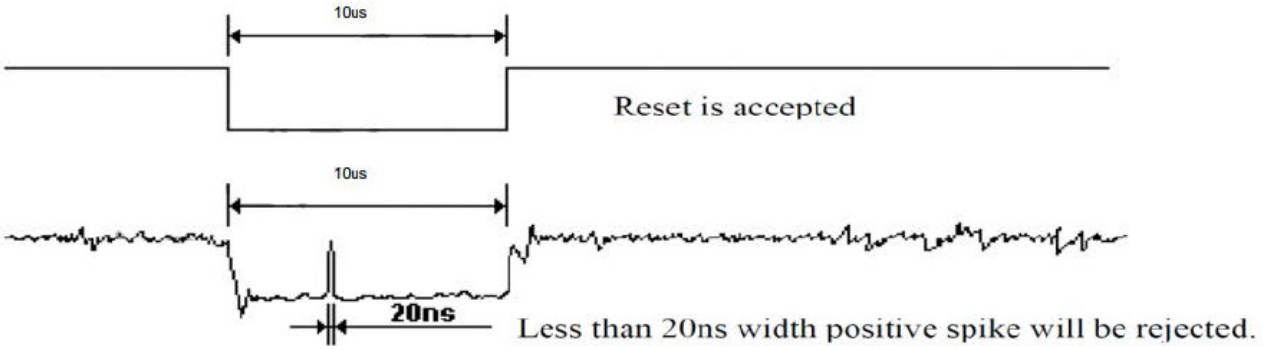
Item	Symbol	Related Pins	MIN	TYP	MAX	Unit	Remark
Reset low pulse width	tRESW	RESX	10			us	
Reset complete time	tREST				5	ms	When reset applied during Sleep in mod
					120	ms	When reset applied during Sleep out mode

Notes:

1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset starts (It depends on voltage and temperature condition.)

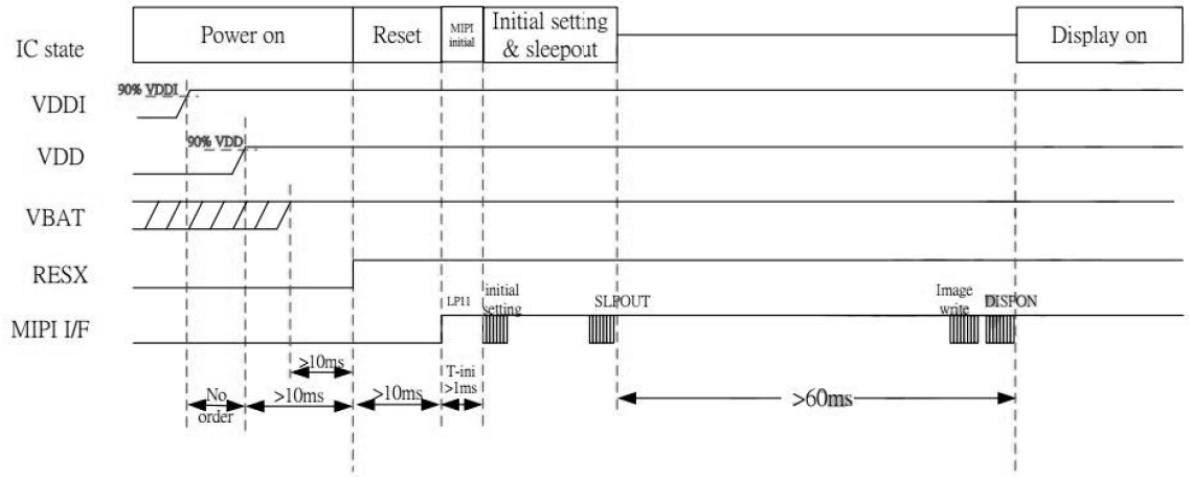
2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum times is 120 ms, when Reset starts in Sleep Out-mode. The display remains the blank state in Sleep in-mode) and then return to default condition for H/W reset.
3. During Reset complete time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST). Within 5ms after a rising edge of RESX.
4. Spike Rejection also applies during a valid reset pulse as shown below:



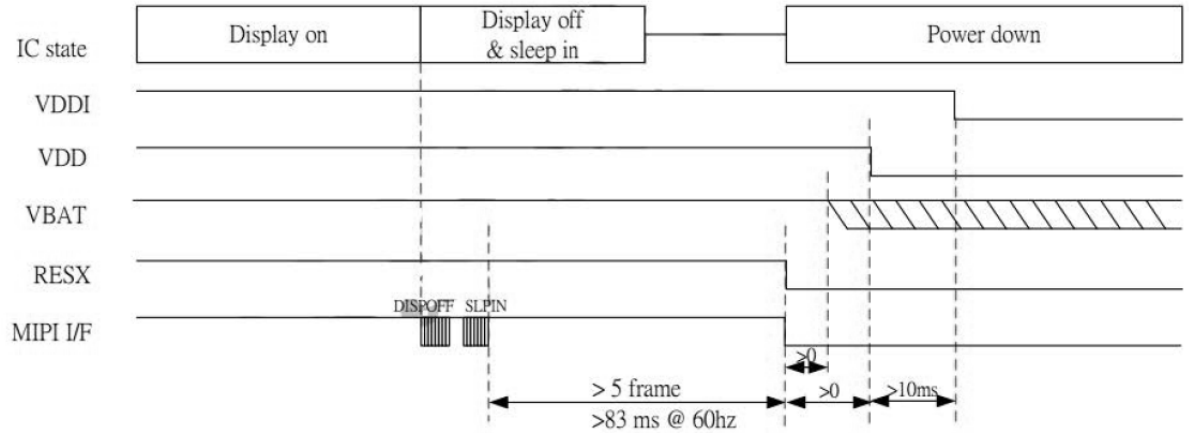
5. It is necessary to wait 5msec after releasing RESX before sending commands. Also sleep out command cannot be sent for 120msec.

8.6 Power On/Off Sequence

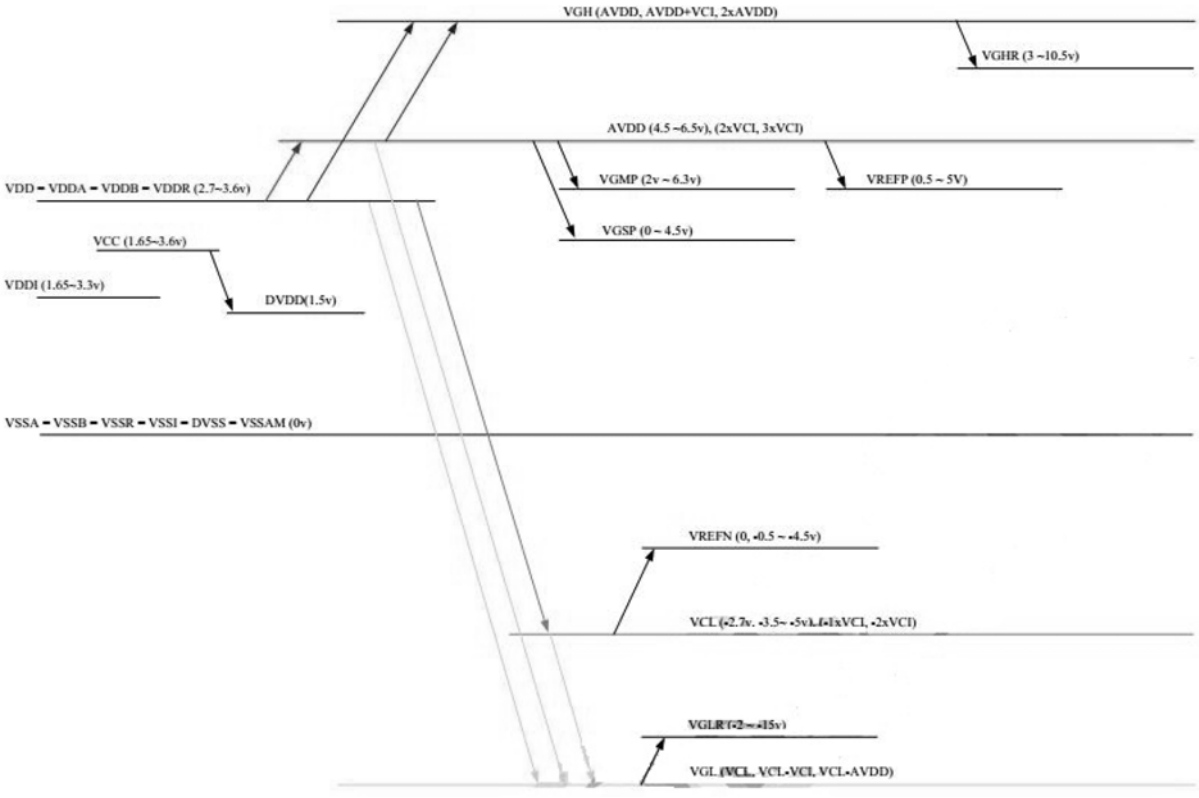
Power on sequence



Power off sequence



Supply Power (VDDI/VDD)



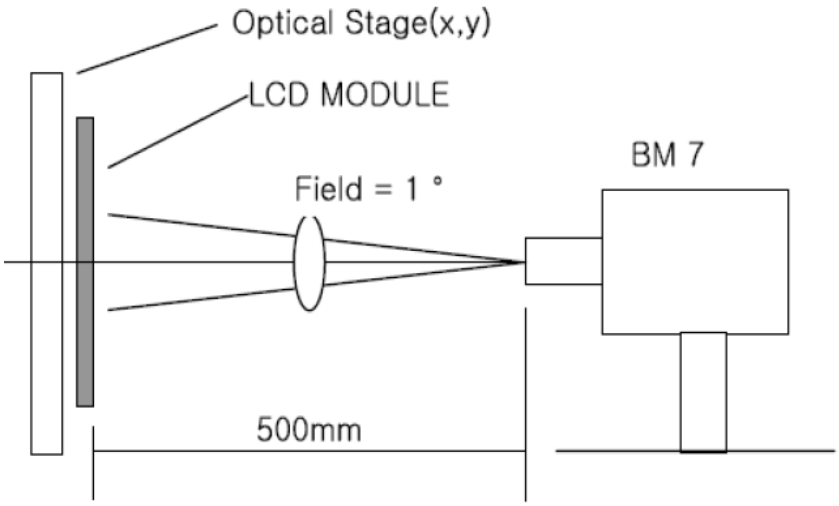
9. Optical Specification

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	10000	-	-		Note1 Note2
View Angles		ΘT	CR≧10	-	80	-	Degree	Note 4
		ΘB		-	80	-		
		ΘL		-	80	-		
		ΘR		-	80	-		
Optical Switching Time		Ton/Toff	25℃	-	2	4	ms	Note1 Note3
Chromaticity	White	x	Brightness is on	Typ-0.05	0.300	Typ+0.05		Note5, Note1
		y			0.310			
	Red	x			0.683			
		y			0.317			
	Green	x			0.230			
		y			0.719			
	Blue	x			0.137			
		y			0.05			
Luminance		L		-	400	-	cd/m2	Note1 Note6
Brightness Uniformity				85	-	-	%	Note7
NTSC				90	107	-	%	
Gamma				2.0	2.2	2.4		

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

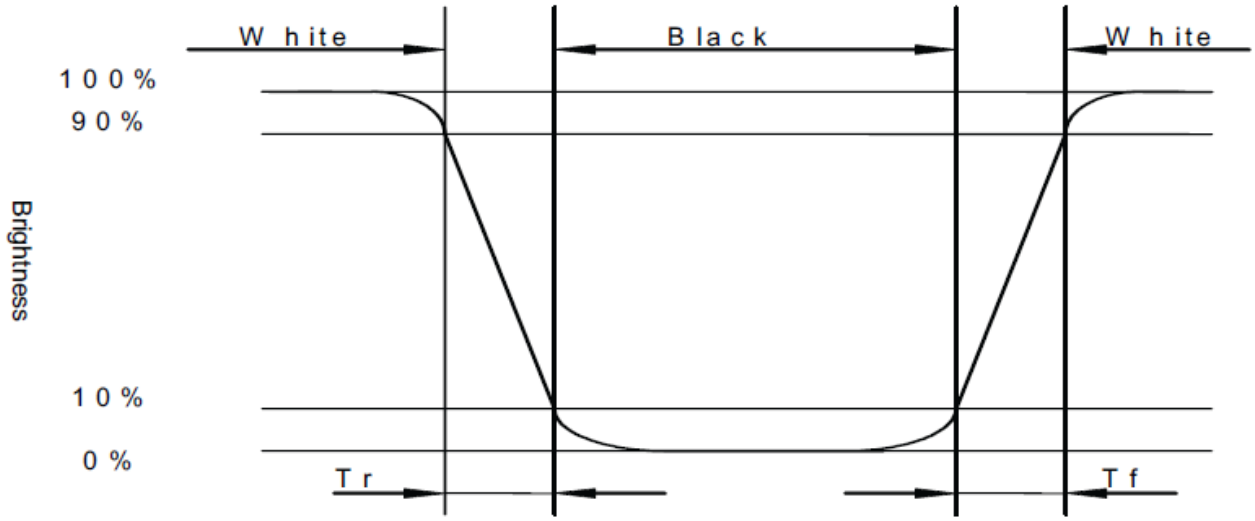


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

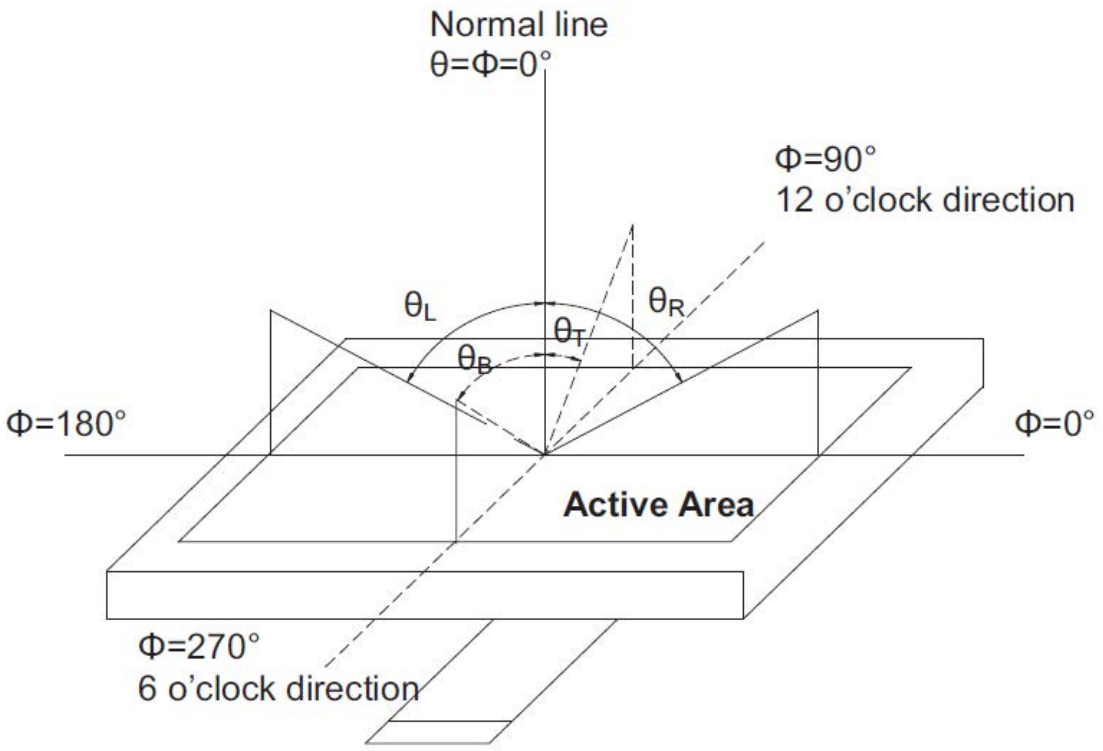
Note 3: Response time is defined as follow:

Response time is the time required for the display to transition from black to white (Rise Time, Tr) and from white to black(Decay Time, Tf).



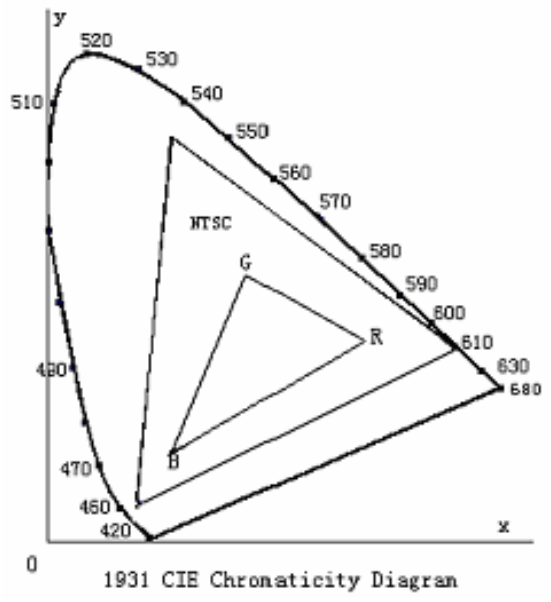
Note 4: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 5: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 6: Luminance is defined as follow:

Measure the luminance of white state at center point.

There should be no visible cross-talk in normal direction of the display when the two “cross-talk Test patterns” below are loaded.

ΔBp(Max.) = Maximum value in ΔBp1~ΔBp4

ΔBp(Min.) = Minimum value in ΔBp1~ΔBp4

ΔCT=ΔBp(Max.)/ ΔBp(Min.)

ΔCT must be less than 1.10

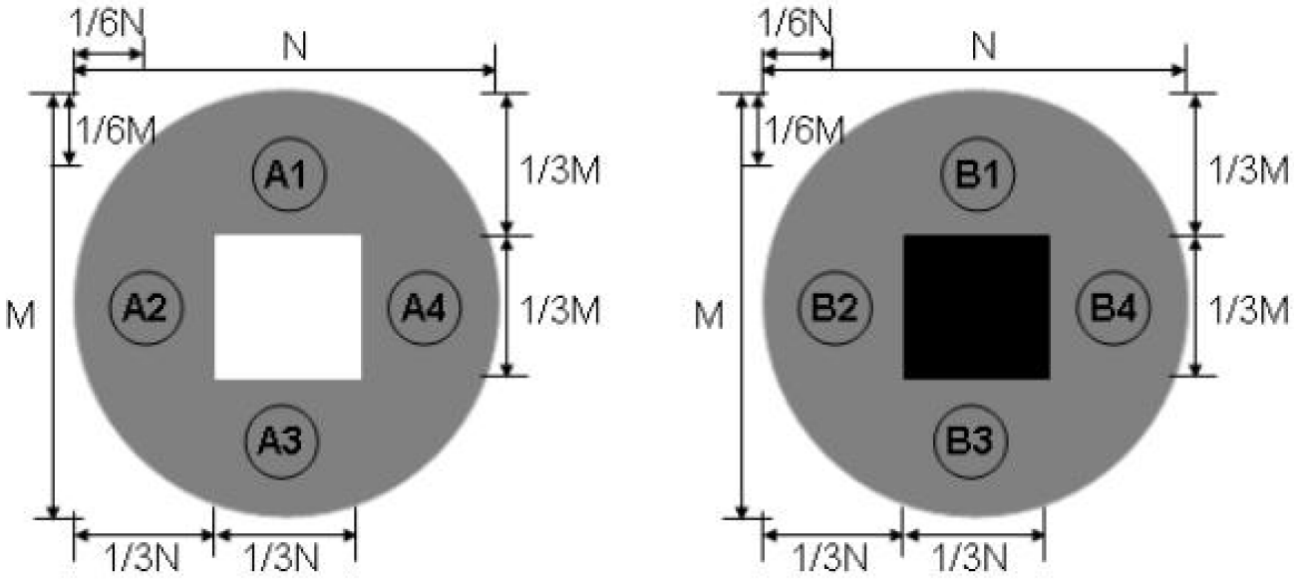


Figure: Cross-talk Test Pattern

Note 7: Uniformity. Refer to figure as below

Active area is divided into 9 measuring areas (Refer Figure as follow). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-------Active area length

W----- Active area width

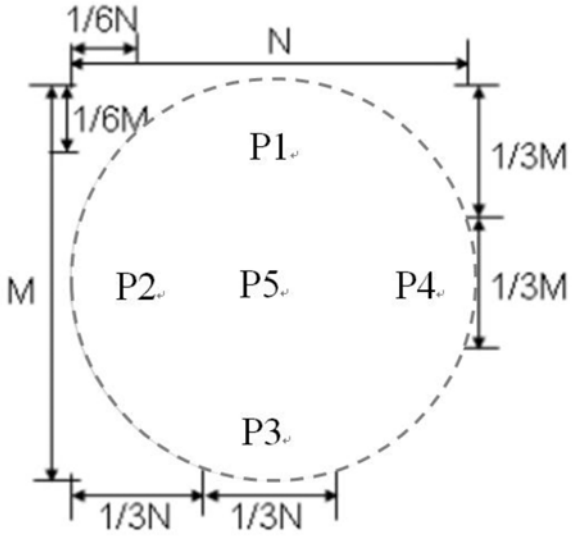


Figure: Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ta= +60℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-20℃, 120hrs	Per table in below
3	High Temp Storage	Ta= +70℃, 120hrs	Per table in below
4	Low Temp Storage	Ta= -30℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta= +50℃, 90% RH, 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-30°C ~80°C，Dwell for 30 min. 100 cycles	Per table in below
7	ESD (Operation)	Voltage:±8KV, R: 330Ω, C: 150pF Air discharge, 10time	Per table in below
8	Vibration	1.50°C 80%RH storage 5hr 2. Frequency（HZ）：5； Amplitude（mm）：20； Direction：A,Z;X&Z 45min per surface	Per table in below
9	Package Drop Test	Height -6 surfaces / 3edges / 1corner/ for Carton test & Gift Box Test 0~9kg /92cm 9.2kg~18.2kg /76cm 18.3kg~27.2kg /61cm 27.3kg~45.4kg /46cm Sample size：a box	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications Current consumption: within · 50% of initial value.
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

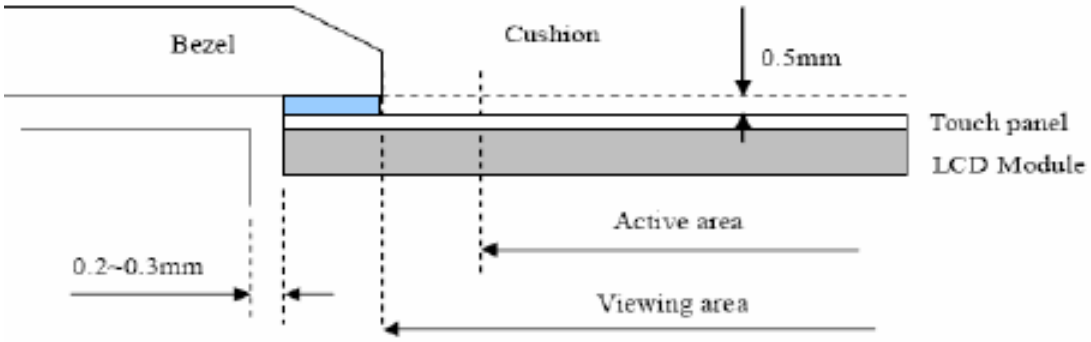
A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

A. Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.
B. In order to make the display assembly stable and firm, MT recommends to design some supporting at the display backside, especially for the display with tape-attached touch panel, such supporting is important and essential, or else, the display may drop-off from front after some period of time.
C. Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.



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