VITESSE

VSC9295 Datasheet

340 Gbps STS-1 Time Slot Interchange Switch

Features

- 136 × 136 time slot interchange (TSI) switch with non-blocking, 6528 × 6528, Synchronous Transport Signal level 1 (STS-1) switch matrix yields 340 Gigabits per second (Gbps) of aggregate bandwidth
- Bitsliced switching mode provides 13056 × 13056 connectivity at half bandwidth (68 × 68 ports), making it possible to construct a single-stage 680 Gbps fabric using just four switches
- High-speed serial TSI-to-Framer interface (TFI-5) operates at 2.488 Gbps with both equalization and pre-emphasis and legacy STS-12 622.08 Mbps support
- Provides hitless automatic reconfiguration of TSI mapping
- Supports split frame domain (two domains per device)
- Supports two overhead ports for dropping and adding overhead bytes for automatic protection switching and in-band messaging
- Monitors cross-connect program memory integrity
- Detects loss of signal (LOS) and checks input parity; inserts output parity, scrambling, and descrambling
- Transparent mode enables switching between ports at 2.488 Gbps independent of protocol
- Static bitslice and merge device capability supports other VSC9295 devices in a bitsliced fabric

Applications

- Monolithic switching
- Central switch or bitslicing engine in 340 Gbps STS-1 grooming fabrics
- Ingress or egress device for large, multi-terabit STS-1 grooming switch fabrics
- Synchronous transparent crosspoint switching for generic circuit or packet communications

General Description

The VSC9295 is a 136-port, non-blocking time slot interchange (TSI) switch. It is typically used as either an interconnection matrix or as an input or output backplane interface.

The device incorporates a fully non-blocking STS-1 switching matrix surrounded by serial backplane interfaces that provide fully integrated clock recovery and synthesis, input equalization, and output pre-emphasis. It supports the high-speed TSI-to-Framer Interface Level 5 standard (TFI-5, which is an STS-48-like frame) on each of its differential serial inputs and outputs with optional STS-12 (622 Mbps) support on a per channel basis. It can also be user-configured to operate in configurations with 68 × 68 ports with 4x bitslicing, 136 × 34 ports with 4x bitslicing, or as a static slice and merge device in support of other Vitesse TSI devices in a bitsliced fabric application.

Additional ports on the device provide convenient access to TFI5/SONET/SDH-compliant scrambling, framing, deskew, and alarm capabilities, as well as overhead byte dropping or insertion. Device configuration and status monitoring are provided using a multimode, 53 MHz CPU interface.

Block Diagram

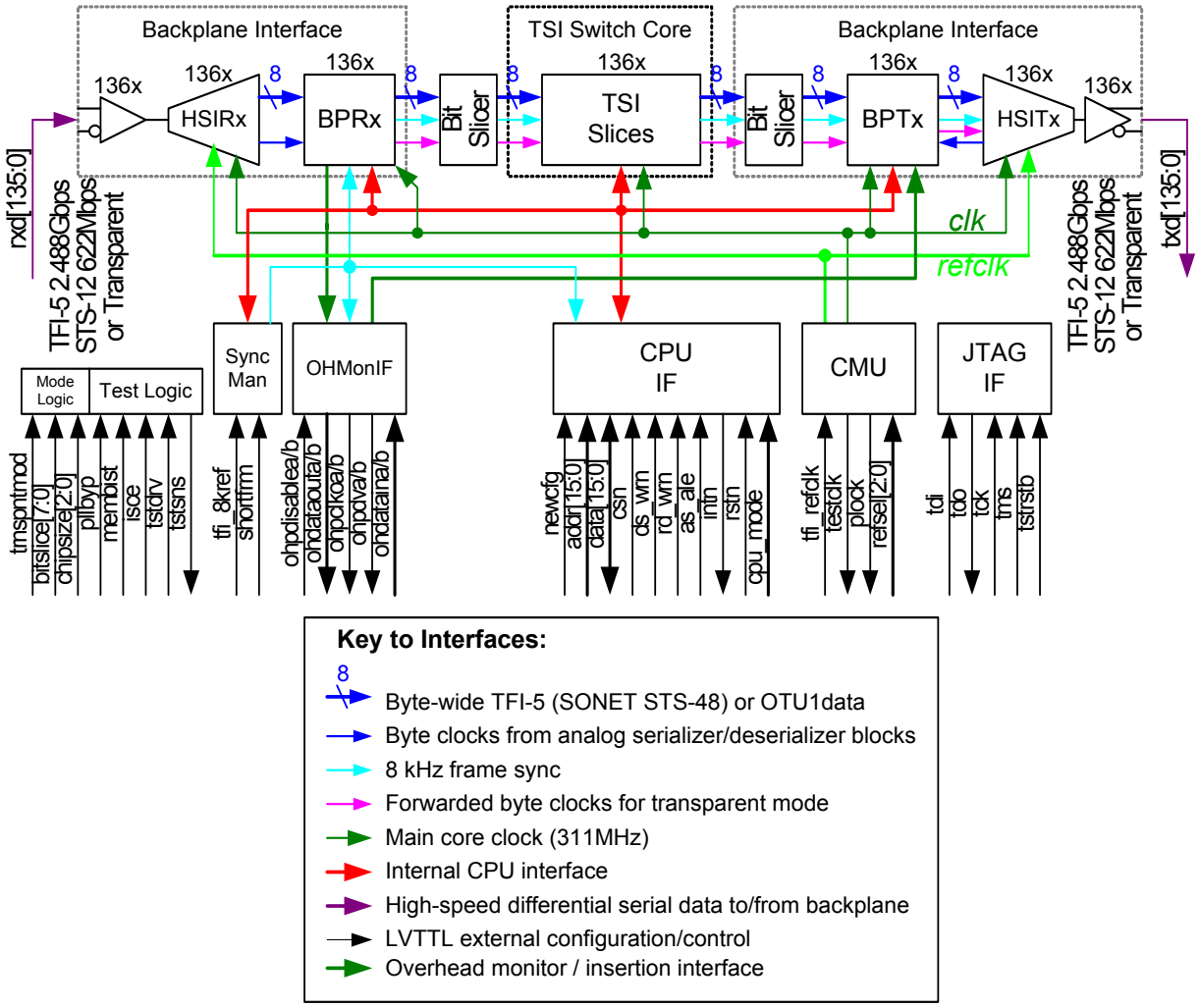


Figure 1. VSC9295 Block Diagram

CONTENTS

FIGURES

TABLES

Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.4

Revision 4.4 of this datasheet was published in April 2009. In revision 4.4 of the document, it was clarified that a single occurrence of MEMPARERRy = 1 does not indicate a permanent defect in the VSC9295 device, but represents a soft error. For information about programming firmware to respond to this occurrence, see "Memory Integrity Check," page 55.

Revision 4.3

Revision 4.3 of this datasheet was published in October 2008. The following is a summary of the changes implemented in the datasheet:

- The maximum value for the output differential voltage, high drive, was changed from 650 mV to 800 mV.
- The minimum operating temperature was changed from –20 °C ambient to –10 °C ambient.
- The package thickness was increased from 3.25 mm maximum to 3.4 mm maximum. The ball diameter was also changed. The minimum diameter changed from 0.65 mm to 0.60 mm. The maximum diameter changed from 0.85 mm to 0.90 mm. The nominal diameter remains the same at 0.75 mm.

Revision 4.2

Revision 4.2 of this datasheet was published in November 2007. The following is a summary of the changes implemented in the datasheet:

- The Motorola mode read and write timing specifications for the CPU interface were updated to include a timing relationship (Ts_as) between ds_wrn falling and as_ale rising.
- The code values for inserting unequipped (UNEQ) signals for SONET/SDH were reversed and are now corrected. FD and F5 correspond to SONET UNEQ, and FE and F6 correspond to SDH UNEQ.

Revision 4.1

Revision 4.1 of this datasheet was published in February 2007. The following is a summary of the changes implemented in the datasheet:

- For the CPU interface in the Motorola mode, timing specifying the setup time between as_ale rising and ds_wrn rising was clarified.
- The timing diagrams depicting the Motorola Simple mode were removed, because this mode is not supported in the device.
- In the CPU interface timing definitions, the symbol for the delay timing parameter was corrected from Td-ad to Td-rd.

Revision 4.0

Revision 4.0 of this datasheet was published in May 2006. The following is a summary of the changes implemented in the datasheet:

- Support for the data rate of 2.125 Gbps was removed.
- A lead(Pb)-free (second-level interconnect only) package VSC9295XSM was added.
- The tolerance settings were added for assert lock detection, and the tolerance settings were modified for de-assert lock detection.
- The electrostatic discharge voltage for the human body model and for the charged device model was added.
- High-speed (TFI-5 data) signal DC and LVCMOS DC parameter characteristics were modified to reflect final characterization.
- The power supply voltage parameters and current parameters were modified for core power supply, CMOS I/O power supply, and high-speed interface power supply.
- The timing variable definitions were modified for the CPU interface and the overhead interface.
- The high-speed interface receiver side AC parameters and receiver jitter tolerance mask definitions were modified to reflect final characterization.
- The minimum value for the data rate was modified from 2.125 Gbps to 0.622 Gbps in the high-speed interface receiver side and transmitter side AC characteristics.
- The high-speed interface transmitter side AC parameters and transmitter jitter tolerance mask definitions were modified to reflect final characterization.
- The recommended operating conditions parameter descriptions were clarified.
- The package drawing was modified to reflect the correct thickness and tolerances.
- The moisture sensitivity level rating was changed.
- The thermal resistance specifications were added for the lead(Pb)-free (second-level interconnect only) package.

Revision 2.0

Revision 2.0 of this datasheet was published in March 2005. This was the first publication of the document.

1 Product Overview

This section of the datasheet gives an overview of the VSC9295 device by providing details about its features when used in its various applications.

The VSC9295 is a multi-port TSI switch. It is most often used as the non-blocking TSI switch in an interconnection matrix, or as an input or output backplane interface. It supports the high-speed TSI-to-Framer Interface level 5 standard (TFI-5, which is an STS-48-like frame) and STS-12 frames on each of its differential serial inputs and outputs, and can be user-configured with several different port setups:

- As a 136 × 136 port TSI switch, providing an aggregate bandwidth of 340 Gbps
- As a 68 × 68 port device with 4x bitslicing (13056 × 13056 connectivity) for use as a switch element in a 680 Gbps switch fabric
- As a 136 × 34 port device with 4x bitslicing (26112 × 6528 connectivity) for use in a 1.36 terabits per second (Tbps) switch fabric
- As a 68 × 68 port device with 2x bitslicing (6528 × 6528 connectivity) for splitting 340 Gbps across two devices in power-sensitive applications
- As a static slice-and-merge device in support of other VSC9295s in bitsliced fabric applications

It is compliant with SONET/SDH requirements as stated in ANSI t1.105, Telcordia GR-253-CORE, and ITU-TG707.

Figure 2 shows the device in a 340 Gigabit (Gb) application. Figure 3 shows it in a 680 Gb bitslicing application.

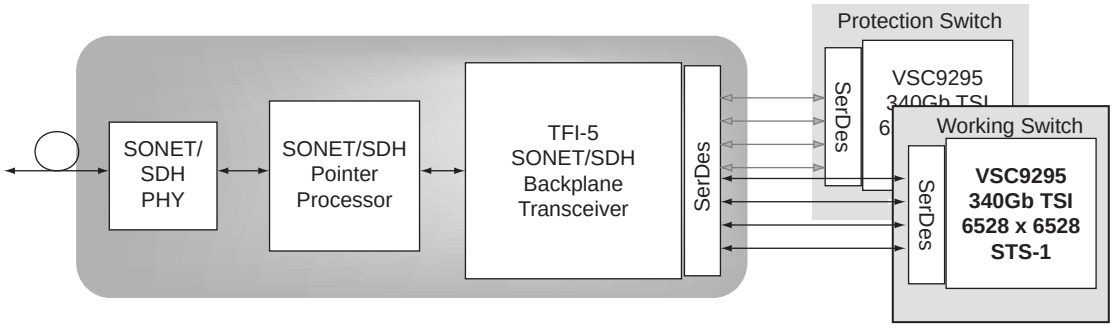


Figure 2. VSC9295 Used as a Working Switch in a Monolithic Application (340 Gb)

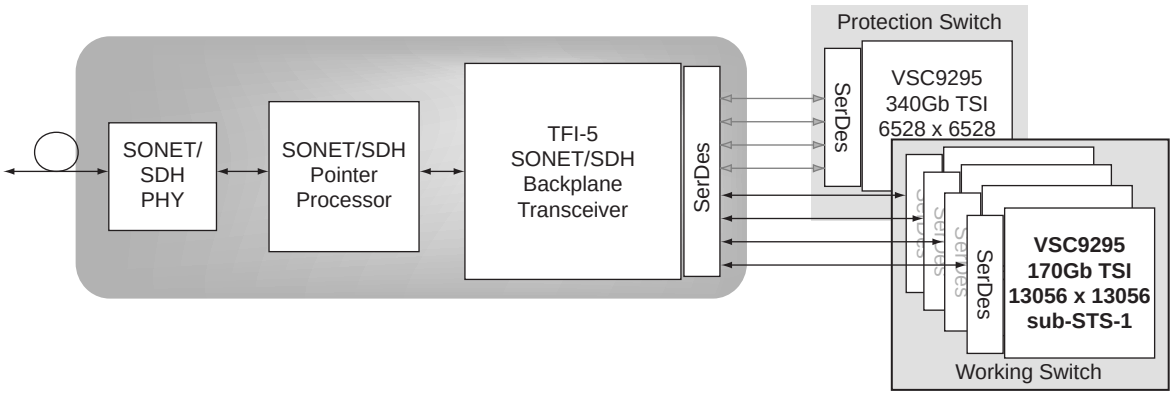


Figure 3. VSC9295 Used as a Working Switch in a Bitslicing Application (680 Gb)

1.1 Interconnection Matrix

Features of the VSC9295 interconnection matrix include:

- Time-switches and space-switches any STS-(n) signal of an incoming STS-48 into any byte position of any STS-48 output (where n is [1], [3c], or [12c]); also supports similar SDH switching to AU-3 level
- Supports switching four bit pairs ([7][6], [5][4], [3][2], [1][0]) in each STS-1 to any bit pair of any output STS-1, thereby providing a 2x linear expansion using four devices operating at half bandwidth with companion devices on line cards
- Supports switching two nibbles ([7] [6] [5] [4], [3] [2] [1] [0]) in each STS-1 to any nibble of any output STS-1, thereby allowing the 340 Gbps bandwidth to be split across two devices operating at half bandwidth (if needed for power conservation)
- Stripes STS-192 signals across four incoming ports
- Supports single-stage, unrestricted, multicast, or broadcast non-blocking structure
- Supports active and standby memory for programming and hitless switch-over
- Transfers new connection maps on the succeeding frame boundary after each user request

1.1.1 STS-1 Switching

STS-1 switching functionality is handled by the TSI core and is described in the TSI core requirements.

The device can produce TFI-5 outputs that are composed of arbitrary rearrangements of any 48 arriving STS-1 signals selected from all the arriving STS-1s on all input channels (48 STS-1s per input channel times 136 input channels) with no restrictions on multicast or broadcast. For more information about sub-STS-1 switching, see "Bitslicing and Sizing," page 22. There is no restriction on mixing the STS-1s that originate or terminate at STS-12 ports with STS-1s that originate or terminate at STS-48 ports.

1.2 Input Backplane Interface

Features of the VSC9295 input backplane interface include:

- Serial 2.488 Gbps differential TFI-5/SFI-5 STS-48/STM-16 inputs with optional 2.488 Gbps Transparent mode and optional STS-12 (622.08 Mbps) support
- Optional equalization for deterministic link jitter reduction
- Signal strength detection on inputs
- Accommodates 136 serial links; inputs are presumed frequency-synchronous and frame-aligned to within ±140 ns A1/A2 skew for TFI-5 frames, but can have unrestricted phase for Transparent mode
- On-chip data recovery de-skewing functionality to bit-align, byte-align, and frame-align all incoming STS-48s to the local clock (within the above cited tolerance)
- Flags Out-of-Frame (OOF), Loss-of-Signal (LOS), Out-of-Alignment (OOA), and parity errors for TFI-5 signals
- Checks byte-interleaved parity of incoming data versus B1 byte of following frame
- Accumulates received B1 errors over a provisionable sample period with user-programmable threshold event
- Optionally inserts Alarm Indication Signal (AIS) when channel is OOF, in a LOS condition, or OOA
- Inserts Unequipped (UNEQ) under software control, and can be user-configured to inhibit all alarms
- Optionally descrambles SONET-scrambled incoming data
- Monitors up to 99 selectable Transport Overhead (TOH) bytes per channel across all input channels and drops to Overhead Monitor port
- Optional bitslicing and bit merging (2x, 4x, and 8x) for use with other VSC9295 devices in a bitsliced fabric

1.3 Output Backplane Interface

Features of the VSC9295 output backplane interface include:

- Provides differential TFI-5/SFI-5, or transparent 2.488 Gbps serial outputs with optional STS-12 (622.08 Mbps) support
- Optionally pre-emphasizes electrical signals for deterministic link jitter reduction
- Optionally inserts byte-interleaved parity into B1 byte of the succeeding frame, including B1 error insertion capabilities
- Originates in-band messages in up to 99 overhead locations per channel by means of random access or overhead port streaming
- Optionally inserts AIS or UNEQ on a per-channel, per-time slot basis
- Optionally SONET-scrambles outgoing data
- Provides optional bitslicing and bit merging (2x, 4x, and 8x) for use with other VSC9295 devices in a bitsliced fabric

1.4 Other Ports

1.4.1 Overhead Monitor Port

The VSC9295 provides two ports for monitoring overhead from the backplane receivers and inserting data at the backplane transmitter. Each port is eight bits wide (separate input and output), and runs at 78 megabytes per second (MBps). Each port is partitioned into lower (0-67) and upper (68-135) channels.

The output overhead monitoring port provides a stream of bytes from BPRx blocks to enable protection switching decisions in an external FPGA. A total of 99 bytes per STS-48 are dropped to this port. The locations of these bytes are user-programmable as follows:

- A single group of 48 contiguous bytes from one overhead row and column location
- Three individual bytes from any three overhead row and column time slot locations
- Three groups of 16 bytes (first, second, or third set of 16 from a group of 48) from any three overhead row and column locations

The ports accept a stream of bytes to be inserted into the BPTx blocks for in-band messaging to downstream devices. A total of 99 bytes per STS-48 can be added using this port at user-programmable row and column locations as described in the bullet list above. These bytes can also be set using the CPU interface, described later in this document.

1.4.2 CPU Interface

The VSC9295 includes a generic microprocessor interface (CPUIF) that can be used to change the configuration of the device and to check status. The interface itself features:

- 16-bit data bus and 16-bit address bus
- Capability to signal changes in status of internal alarms using interrupt output pin
- Flexible interrupt masking
- Interrupt group registers for rapid fault and delta identification
- 53 MHz effective clock rate for write operations

1.4.3 Test Interface

The VSC9295 also provides an IEEE P1149.1 standard access port to control external boundary scanning.

1.4.4 Clock Synthesis for Phase-Locked Loop

The phase-locked loop (PLL) of the VSC9295 has the following attributes:

- Provides monolithic PLL clock multiplier with 8x, 16x, and 32x multiplication ratios
- Uses a 311 MHz, 155 MHz, or 78 MHz reference clock
- Provides alarms for both loss-of-reference (LOR) clock and loss-of-lock (LOL)

1.5 Data Formats

The VSC9295 can receive and transmit data in four formats:

- Short Frame—Test mode using abbreviated frame, affects all channels when active
- TFI-5—Based on a SONET STS-48 or SDH STM-16 frame
- STS-12—Based on a SONET STS-12 or SDH STM-3 frame
- Transparent—Set globally or can be associated with specific link pairs. When configured to operate in Transparent mode, data can be carried through the device at the same time as data in either of the other two modes. For example, it is possible to transparently pass data at 2.488 Gbps while simultaneously performing STS-1 level switching on other data. Note, however, that the entire device must operate at the same clock rate.

In this document, each of the above formats is referred to as an operating mode.

The TFI-5 mode, STS-12 mode, and the Short Frame mode are mutually exclusive with respect to their functionality on the device.

Another typical application of Transparent mode is one where the entire device operates at one of the supported Transparent mode rates and no STS-12 or TFI-5 data is present.

1.5.1 TFI-5 Mode (TFI-5, SONET, and SDH Frames)

The basic TFI-5 frame is based on a SONET STS-48, or a SDH STM-16 frame, so these three data formats are treated as a single operational mode. In TFI-5 mode, the frame consists of 9 rows of 90 columns, each composed of 48 bytes. Each column belongs to a separate STS-1 tributary, and the frame holds $9 \times 90 \times 48$ bytes (311040 bits), which are transmitted starting at row 1, column 1. The transmission proceeds first by columns and then by rows until row 9, column 90 is transmitted. Each byte is transmitted MSB (bit 7) first.

The data in the frame can be switched at the STS-1 level.

The frame is transmitted in 125 µs, resulting in a serial data rate of 2.488 Gbps. All received data must be aligned to within ±48 byte times of a common frame synchronization pulse, which occurs once per frame. The position of the received data relative to the frame boundary is programmable. The features of the frame are shown in Figure 4.

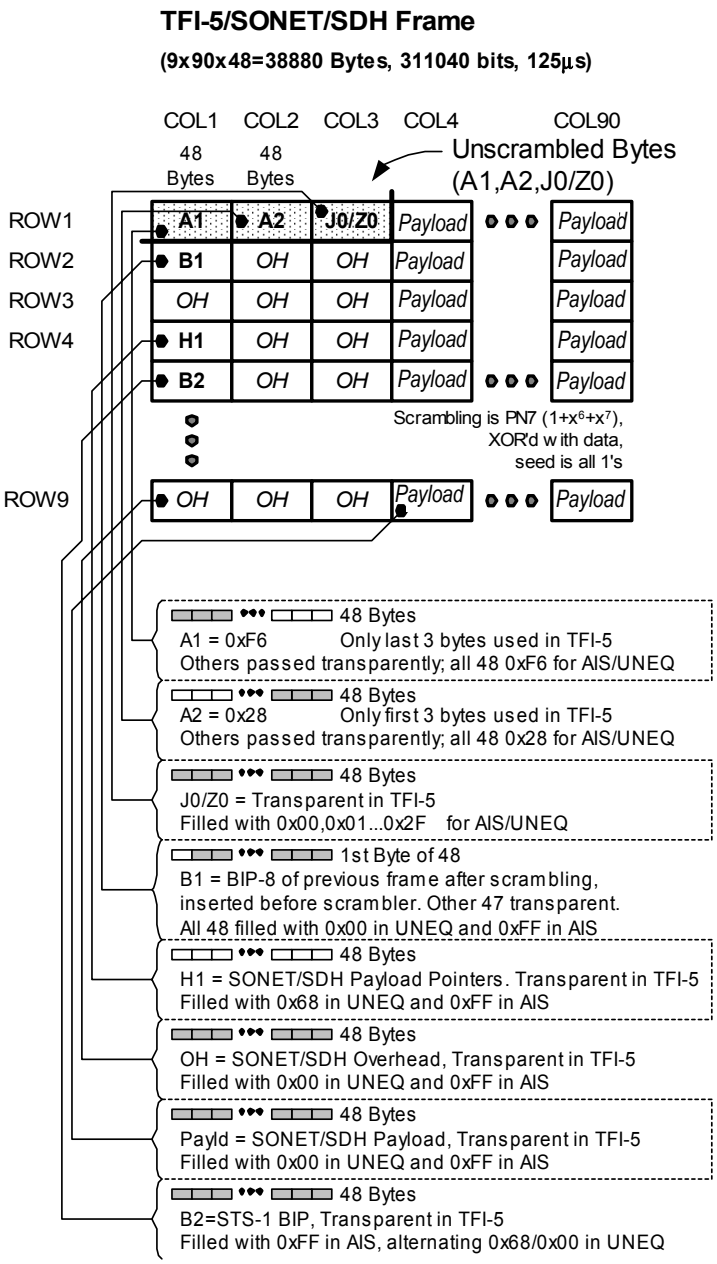


Figure 4. TFI-5/SONET/SDH Frame Format

1.5.2 Short Frame Mode

The VSC9295 Short Frame mode is used for Vitesse test purposes only. The short frame in this mode consists of two rows with three columns of overhead and three columns of payload; it contains 2 × 6 × 48 bytes (576 bytes). The frame format is shown in Figure 5.

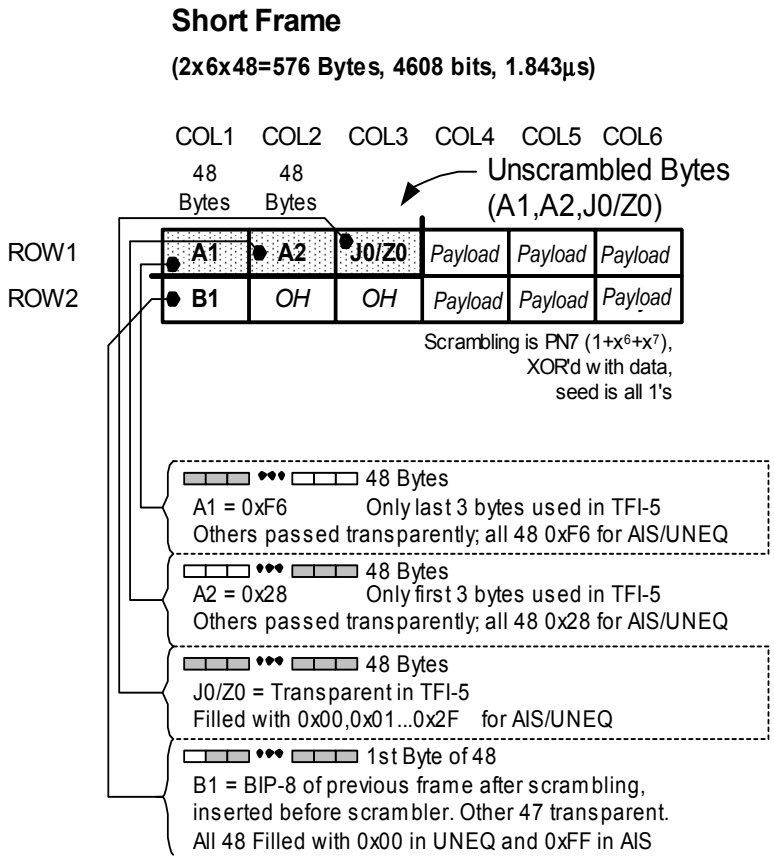


Figure 5. The VSC9295 Short Frame Format

1.5.3 STS-12 / STM-4 SONET / SDH Frames

The basic STS-12 frame is based on a SONET STS-12 or SDH STM-4 frame. The frame consists of nine rows of 90 columns. Each frame is composed of 12 bytes, each belonging to a separate STS-1 tributary. Thus, the frame holds 9x90x12 bytes (77760 bits), which are transmitted starting at row 1, column 1 and proceeding by columns and then by rows until row 9, column 90 is transmitted. Each byte transmits the MSB (bit 7) first.

The data in the frame can be switched at the STS-1 level. On entry to the switch core of the device, four redundant copies of each byte are made to feed the core at the same data rate as TFI-5 inputs.

The frame is transmitted in 125 µs, resulting in a serial data rate of 622.08 Mbps. All received data must be aligned to within ±12 byte times of a common frame synchronization pulse. A frame pulse occurs once per frame, and its position relative to the frame boundary is programmable. The features of the frame are shown in the figures below.

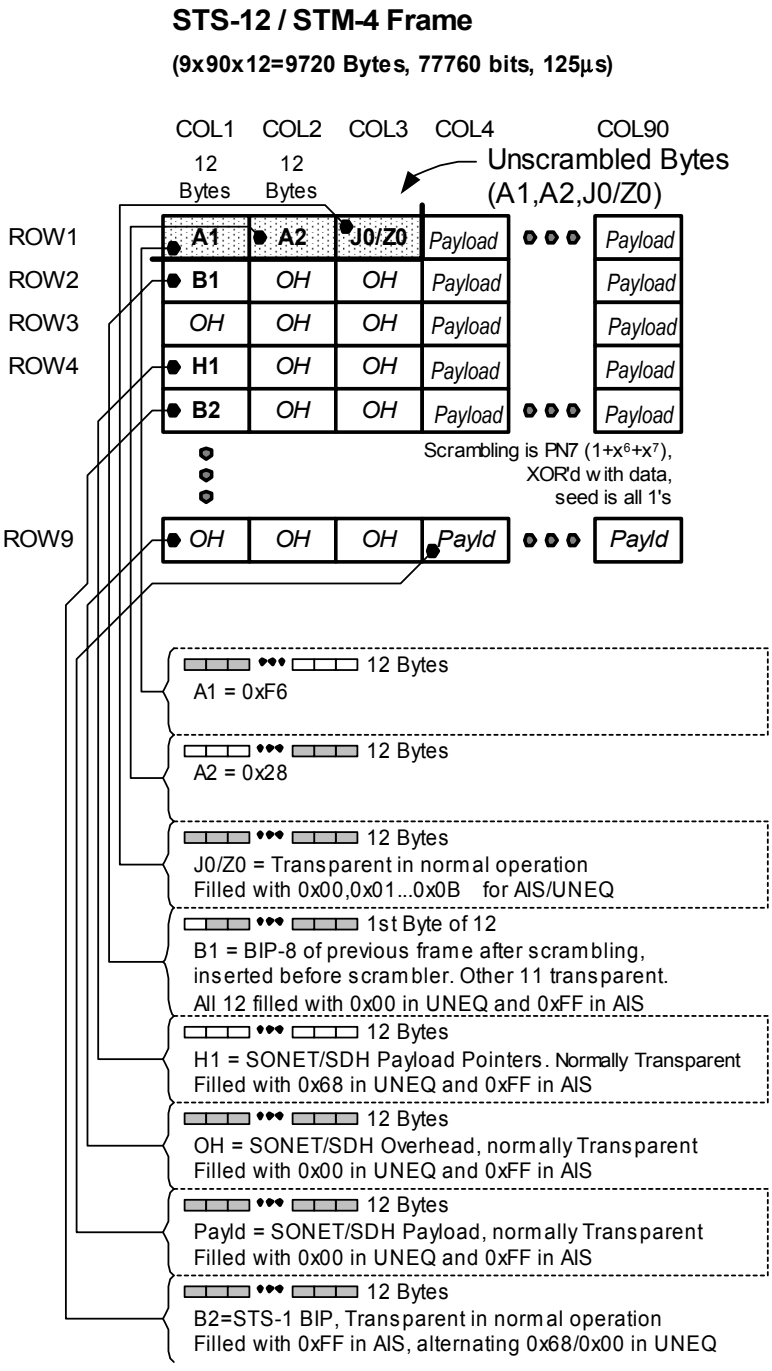


Figure 6. STS-12/STM-4 Frame Format

1.5.4 Transparent Mode

Transparent mode enables data to pass through the VSC9295 and be switched among the physical channels irrespective of its format. Each port on the device can be placed in Transparent mode independent of the settings of the other ports, but the entire device must operate at the same clock frequency. This means that mixing transparent data and TFI-5 data requires that the transparent data be at 2.488 Gbps.

Transparent mode signals can have a data rate of 2.488 Gbps. Signal data rates must be an exact multiple (8x,16x, or 32x) of the reference frequency provided on tfi_refclk. For a description of minimum transition density requirements on all input signals, see "High-Speed Interface Receiver," page 62.

Transparent mode signals can be switched in their entirety (no STS-1 grooming) between any input port set in Transparent mode and any output port set in Transparent mode with no restrictions on multicast or broadcast.

In the Transparent mode of the VSC9295, the data format is irrelevant; data is passed through the device unaltered. The data stream is, however, re-timed internally using the clock recovered from the data itself. No frame pulse is required.

The data must meet the following requirements:

- Data frequency (symbol rate) must be an exact multiple of the reference clock
- Data average transition density must be greater than 12.5%, with 50% density of 1 signals required if AC-coupled
- Data rate must be 2.488 Gbps

Note that since write copying is not enabled until after the change from TSI to Transparent modes, the channel must be re-provisioned to work properly. In other words, it is not possible to provision the switch with a space, time, bitslice value, and then change to the Transparent mode and get a transparent version of the signal specified by the space value.

1.6 Miscellaneous Functions

This section contains the miscellaneous functions for the VSC9295 device.

1.6.1 Frame Synchronization

The VSC9295 accepts an 8 kHz external reference frame sync. This signal can be internally offset by an arbitrary number of byte positions to form a reference frame pulse that indicates the reference point for deskewing the incoming TFI-5 data. All incoming TFI-5 data must be frame-synchronous to within a tolerance specified by the BPRx block (±140 ns). The device continues to function if the external frame sync is absent, however, and it is also able to tolerate a programmable amount of jitter on the external frame sync when it is present. For detailed information on external frame synchronization, see "Frame Synchronization Manager," page 34.

1.6.2 Internal Frame Distribution

The internal frame sync is distributed by the SyncMan block to all the BPRx blocks. From BPRx blocks 34 and 102, latency-corrected frame pulses are sent to the Rx bitslicer blocks that forward them to the TSI core blocks. The TSI core slices produce latency corrected frame sync pulses. These frame sync pulses go to the Tx bitslicer blocks that forward them to the BPTx blocks.

1.6.3 Dual Frame Domains

In addition, the VSC9295 supports two frame domains; two portions of the device can be operated with different frame offsets versus the external reference frame sync for use in pre-grooming or post-grooming of a smaller volume of traffic. This is accomplished by having two, separate internal frame pulse distribution networks with separately controlled offsets originating from the SyncMan block. Each BPRx and each pair of slices within the TSI core has a means of selecting its membership in one of the two frame domains. Each pair of BPTx blocks receives a sync forwarded from the associated even-numbered TSI core slice.

There are two master channels for the sync distribution: BPRx 34 and BPRx 102. When operating with split domains, these two channels each select different frame syncs from the SyncMan by means of their FSYNC_SEL bits. These channels become the sources for fsync0 and fsync1 respectively.

After the domains for BPRx 34 and 102 are selected, all other BPRx blocks can be programmed to be on either domain. In the TSI core, each channel can select its own domain by setting its DOMAIN bit (0=sync from channel 34, 1=sync from channel 102). The choice results in the appropriate sync being forwarded to the associated BPTx, allowing each pair of consecutive outputs to have its frame domain selectable. The DOMAIN0 bit (belonging to the even-numbered slice in each pair of TSI slices) determines the frame domain of the corresponding BPTx and the BPTx one position higher (for example, DOMAIN0 in the address space for TSI slices 0/1 controls which domain BPTx0 and BPTx1 are on, but both DOMAIN0 and DOMAIN1 for TSI slices 0/1 must be programmed identically).

The user is responsible for programming the device so that data is not switched across the two domains.

1.6.4 Bitslicing and Sizing

The VSC9295 can be configured to operate at half bandwidth (68 channels in and out) with 2x the connectivity in the TSI core, enabling the individual switching of each bit pair [7:6],[5:4],[3:2], and [1:0] within each STS-1, with no restrictions on multicast or broadcast.

In addition, the VSC9295 can be user-configured to operate at half bandwidth (68 channels in and out) with 6528 × 6528 connectivity in the TSI core. This enables the individual switching of each nibble [7:4] and [3:0] within each STS-1 with no restrictions on multicast or broadcast.

The switch core bitslicing mode must be set globally for the device with the bitslice[1:0] pins. For more information, see Table 1, page 23.

To enable the device to be used to bitslice and bit-merge data streams in a fabric of switches, the VSC9295 incorporates a static bitslicing capability. This is independent of the switch functionality, and supports 2-way, 4-way, and 8-way bitslicing. Its operating modes are selected with the setting of the bitslice[7:2] pins.

There are bitslicer blocks between the TSI core and the BPTx (controlled by bitslice[4:2], mapping to bitslice[2:0] on the bitslicer) and between the BPRx and the TSI core (controlled by bitslice[7:5], mapping to bitslice[2:0] on the bitslicer).Although each input and output channel may be powered off individually from software, it is convenient to have all the required channels powered off in certain modes. This is done using the chipsize[2:0] pins, which can set the device for 136 × 136 operation, 136 × 68 operation, 68 × 136 operation, 68 × 68 operation, or 136 × 34 operation.

The sizing modes are shown in the following table.

Table 1. I/O Sizing Modes

Mode	Chipsize[2:0]	Description	Available Switch Core Bitslicing Modes	Available Static Bitslicing Modes
HH	000	68 inputs by 68 outputs	none, 2x, 4x	none, 2x, 4x
HF	001	68 inputs by 136 outputs	none, 2x	none, 2x, 4x, 8x
FH	010	136 inputs by 68 outputs	none, 2x	none, 2x, 4x
FF	011	136 inputs by 136 outputs	none	none, 2x, 4x, 8x
FQ	110	136 inputs by 34 outputs	4x	none

The following diagrams illustrate how bitslicing works in the VSC9295. In the slicing device (either a separate VSC9295 or another device with this capability), four streams of data are combined, and each byte (such as bytes **a** and **b** in the diagram) is split into four bit pairs. Each bit pair is then striped across four output ports connected to four separate VSC9295 devices.

In the frames transmitted to the VSC9295, the A1, A2, and B1 bytes are overwritten and scrambling is performed after slicing. This makes the frame format look identical to data that is not bitsliced.

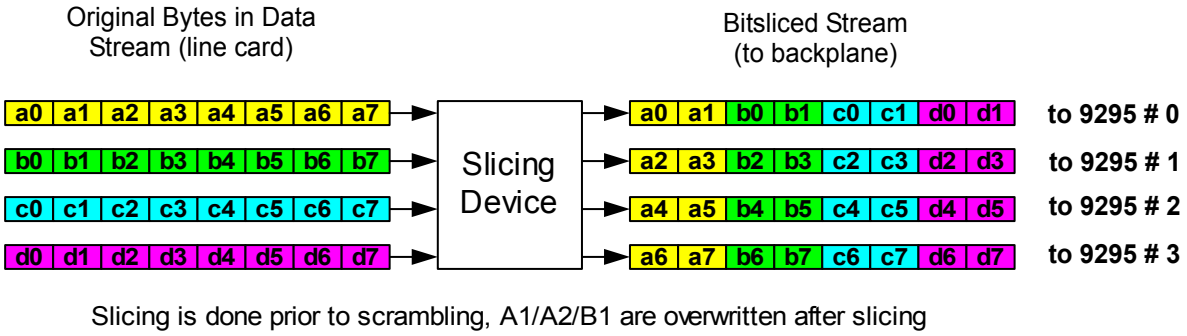


Figure 7. Four-Way Bitslicing (Slicing into 2-Bit Units)

In the switching stage, four devices in parallel are programmed identically, and each carries and switches one quarter of all the traffic passing through the fabric. The switches are capable of switching each bit pair within a byte (an STS-1 time slot) to a different location. As with the slicing stage, the switch overwrites A1, A2, and B1 and scrambles the data after switching.

Overhead monitoring and insertion is more complex when designing a fabric this way. In each device, overhead monitoring takes place before de-slicing or switching, and insertion takes place after switching and bitslicing. The external device monitoring and sourcing the overhead bytes must aggregate data from the four switches and redistribute it to four switches while also accounting for slicing.

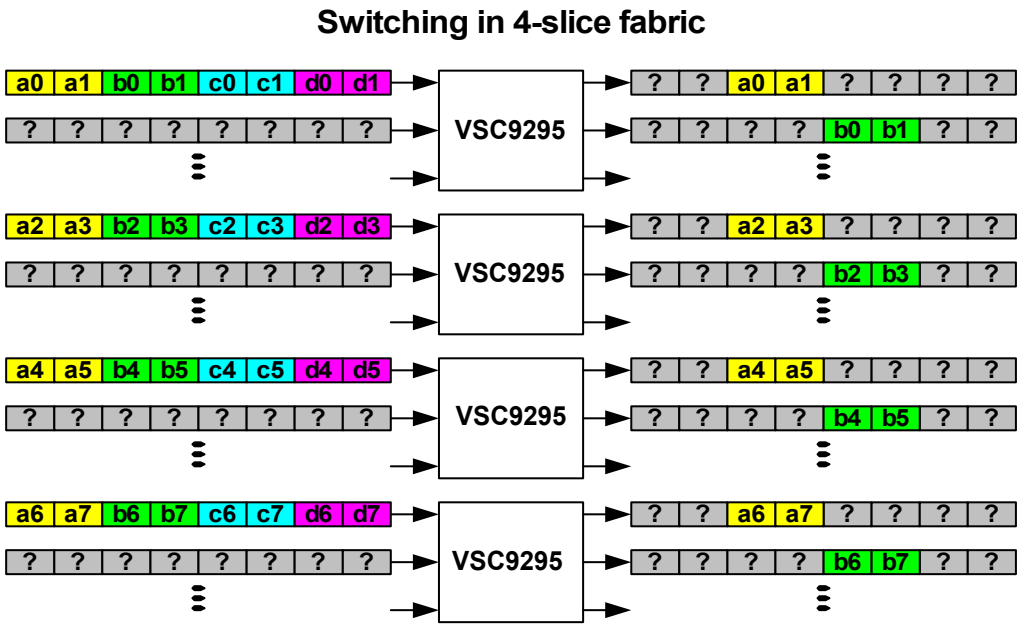


Figure 8. Four VSC9295s in Parallel Performing Bit Pair-Level Switching

After switching, an operation referred to as deslicing (or recombination or as bit-merging) occurs. In deslicing, data from the four switches arrives at a deslicing device and are recombined so that the bit pairs form back into the correct bytes.

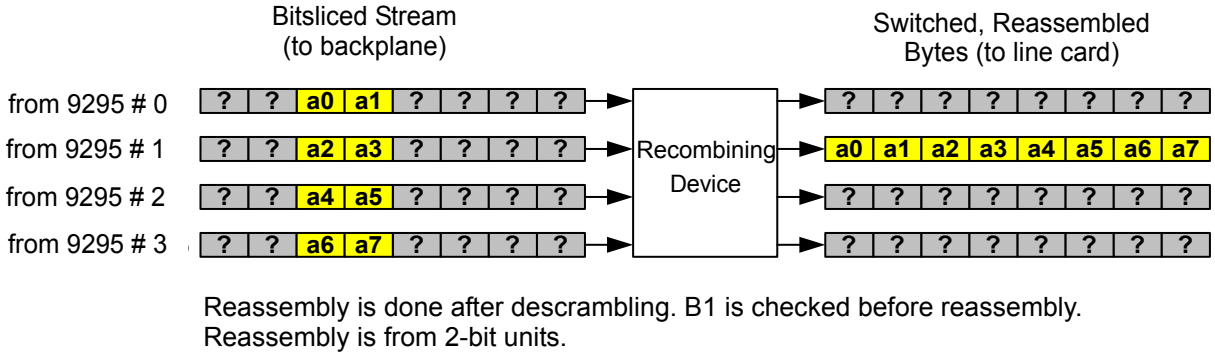


Figure 9. Deslicing a 4-Way Bitsliced Data Stream

The static bitslicing can be configured for 8x bitslicing to support future switch devices with 8x bitslicing in the switch core. An illustration of 8x bitslicing is shown in the following figure.

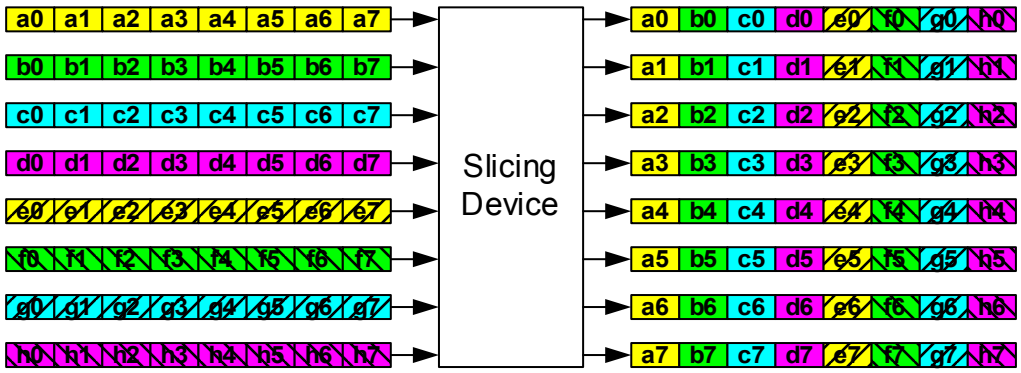


Figure 10. 8-Way Bitslicing Operation (Slicing into 1-Bit Units)

1.7 Application Information

This section contains information about the applications for the VSC9295 device.

1.7.1 Expandability

The following figure shows the VSC9295 in a 680 Gbps, one stage fabric configuration. This is enabled by bitslicing on the line cards and bit pair-level switching inside each of the VSC9295s. The devices on the line cards split the bandwidth of each STS-1 from the line card into four bit pairs. These bit pairs are then routed to the four VSC9295 devices when combined with bit pairs from other STS-1s from the same line card. All four VSC9295s are programmed identically. The bit pairs from each of the two switches are recombined on the line cards.

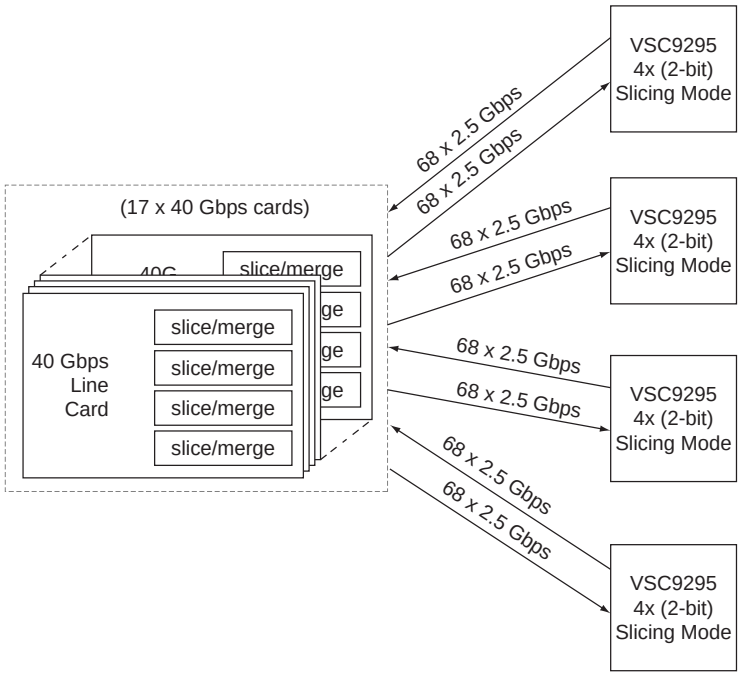


Figure 11. 680 Gbps Switch Fabric Application

Because any overhead content from the original STS-1 is split across four devices, any external hardware and software using the Overhead Monitor Interface aggregates the overhead being dropped, and also splits or recombines the overhead being added to account for the bitslicing.

Using the devices in this mode effectively shuts off half of the inputs and half of the outputs and their associated high-speed and low-speed interfaces. This achieves a power savings of 10 W in maximum power configurations.

Additional expandability is possible by first fashioning a 340 Gbps 4x bitsliced unit using various modes of the VSC9295, then incorporating four such units into the fabric application. The device can be used as a static slice and merge component, a fan out device, or as a 136 × 34, 4x bitsliced switch.

Combining these elements results in a 1.36 Tbps fabric, as shown in the following figure.

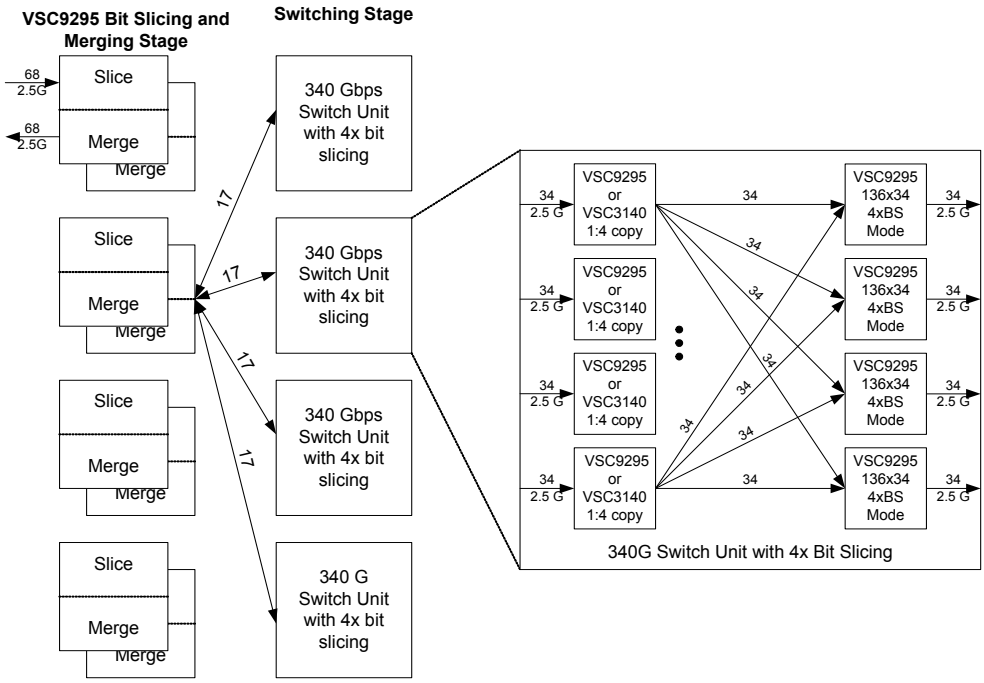


Figure 12. Example 1.36 Tbps Fabric Configuration

1.7.2 Protection Plane Schemes

By using some switching in the slice and merge devices, a 4 + 1 protection scheme can be devised as shown in the following figure. If any one of the four bit planes fails, the data is still routed through a fifth (protection) plane.

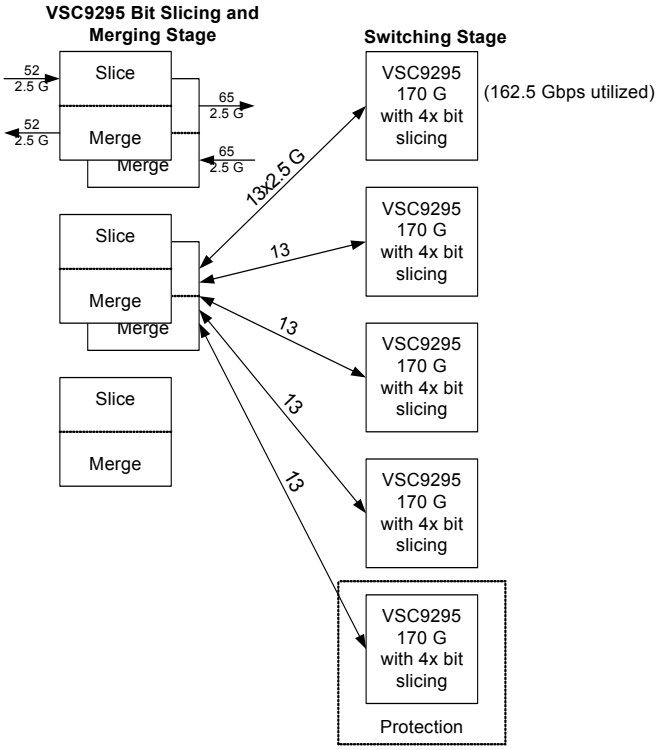


Figure 13. 680 Gbps Switch Fabric with Protection Plane

1.7.3 Cascading Multiple Devices

When necessary, multiple VSC9295 devices can be cascaded to form larger fabrics. The serial data outputs of one device connect directly to the serial data inputs of the next device. The frame offset on subsequent devices must be adjusted for the latency of the first device and so on. The following figure shows the connections.

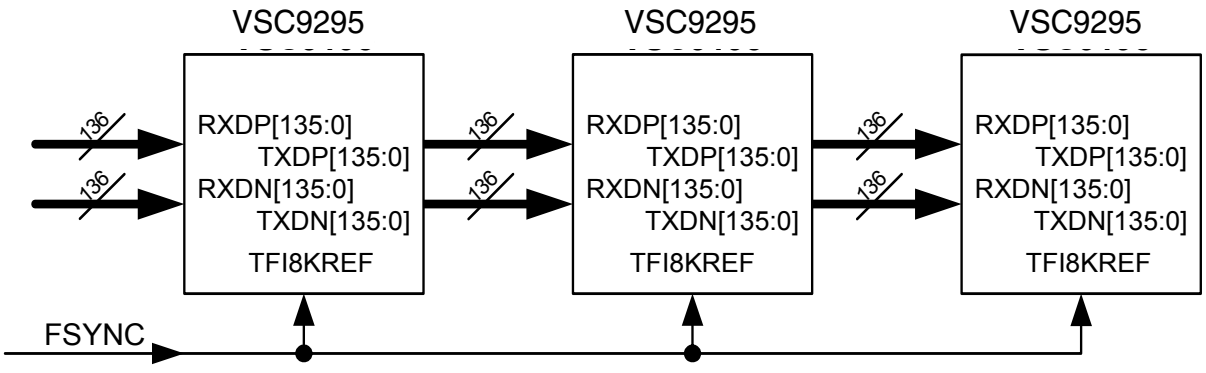


Figure 14. Cascading Multiple VSC9295 Devices

If hitless switching across a multi-stage fabric is desired, care must be taken to issue the new configuration request such that it arrives at all devices in all stages of the fabric before the next frame boundary occurs inside any of the devices. This is typically done by using hardware that accepts a request to issue a newcfg pulse, and waits for some period of time after the system frame sync before issuing the pulse.

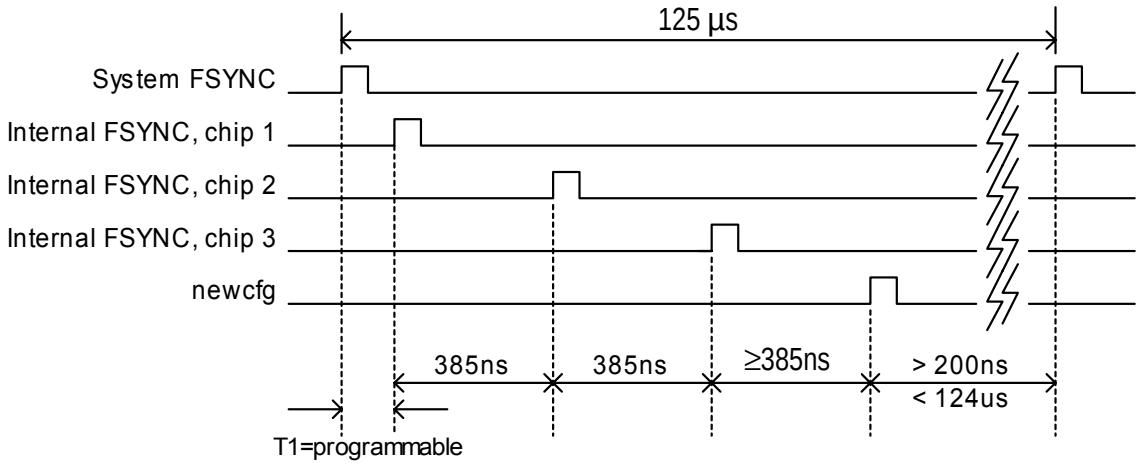


Figure 15. Timing of newcfg and FSYNC in Cascaded Applications

2 Functional Descriptions

This section of the datasheet documents VSC9295 functionality by describing its features and applications.

2.1 CPU Interface

A CPU interface (CPUIF) in the VSC9295 configures the device and monitors its status from an external controller. External pins connect to the CPUIF block, which translates signals to and from the internal bus format. The CPU interface is asynchronous to any other clocks on the device and does not consume significant power when not in use.

A block diagram of the CPUIF, including General Configuration registers, is shown in the following figure. External pins connect to the CPUIF block, which translates the external CPU interface signals to and from the internal bus format asynchronously. The VSC9295 General Configuration registers contain register map bits that pertain to the device as a whole rather than to any one block.

For more information about the layout of the address space for the CPUIF, see "Memory Map," page 73.

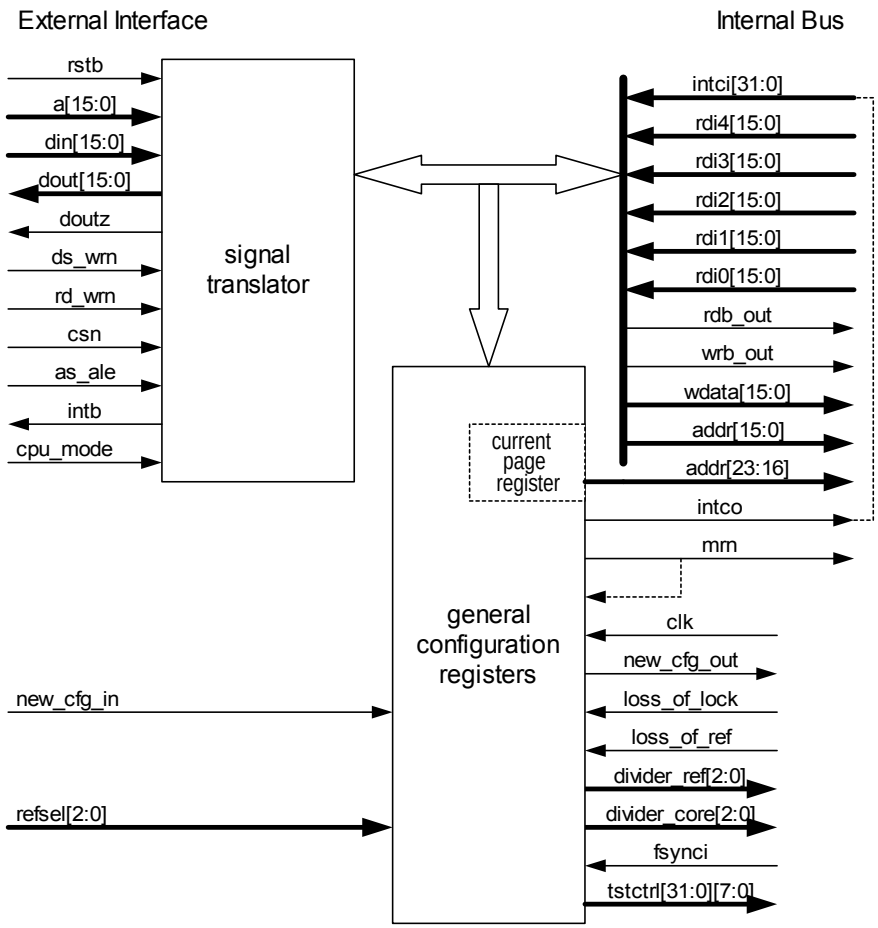


Figure 16. VSC9295 CPU Interface Block Diagram

2.1.1 Asynchronous Interfaces

The CPUIF functions in the absence of, and during the failure of, any clocks to the device. The interface functions asynchronously to any clocks on the device. However, the state of some status bits may not be updated if the CMU is not locked.

2.1.2 Memory Paging

To enable a generic 16-bit interface when the address space of the device is much larger than 2^{16}, a paging method is employed wherein a Current Page is set by writing to 0xFFFF (on any page) to set the upper 8 bits of the full 24-bit address used to access internal register locations. This register is known as CURR_PAGE[7:0].

2.1.3 Writing Individual Register Bits

Address locations specified in the registers section of this document are written to and read from in their entirety. If a modification of individual bits is required while other writable bits are to be left undisturbed, software must read the contents of the register at that address, modify the desired bits, and write the entire register contents back to that address.

2.1.4 Interrupt Generation

Functional blocks on the device may generate interrupts. These interrupts are grouped by block type and subgroup. The General Configuration registers contain the registers INTSRC0[15:0] and INTSRC1[15:0] with a bit allocated for the state of each interrupt subgroup (up to 32 subgroups total, of which 10 are currently used in the device and the others are allocated to the unused subgroups). When any one or more interrupt subgroups produces a logic HIGH output, the CPUIF drives the external intb pin LOW.

Interrupt source bits are allocated as shown in the following table. An interrupt is generated when any status delta bit is activated by a state change in a corresponding status bit, provided that the interrupt is not masked by the corresponding mask bit.

Table 2. Interrupt Source Bit Allocation

Bit	Blocks Covered	Type of Interrupt
INTSRC0[0]	General configuration registers	NEWCFGD, PLLLOLD, PLLLORD, NEWCFGD, NEWCFGBUSYD
INTSRC0[1]	BPRx68-135	OOFD, OOAD, LOSD, B1ERRD, RXLOLD, RXLOSD, ESUFLOWD, ESOFLOWD
INTSRC0[2]	BPTx0-67	TXLOLD
INTSRC0[3]	BPTx68-135	TXLOLD
INTSRC0[4]	BPRx0-67	OOFD, OOAD, LOSD, B1ERRD, RXLOLD, RXLOSD, ESUFLOWD, ESOFLOWD
INTSRC0[5]	SyncMan	BYSYNCD
INTSRC0[6]	TSI Ch 0/1,4/5,8/9 and so forth	MEMPARERRD
INTSRC0[7]	TSI Ch 2/3,6/7,10/11 and so forth	MEMPARERRD
INTSRC0[8]	TSI Ch 68/69,72/73,76/77 and so forth	MEMPARERRD
INTSRC0[9]	TSI Ch 70/71,74/75, 78/79 and so forth	MEMPARERRD
INTSRC0[15:10]	Not used	
INTSRC1[15:0]	Not used	

2.1.5 Device Reset Control

The CPUIF has control over the device reset function. The external rstb is used to signal a complete device reset.

Alternatively, a software reset can be initiated by first writing a logic 1 to the SFTRST bit in the General Configuration registers and then writing 0 to it. The SFTRST bit resets all counters and state machines (and any other flip-flops with required initial states) in the device.

2.1.6 General Configuration Registers

Registers associated with overall device operations that are themselves not localized to any particular block are contained in the CPUIF block. This includes the paging register and interrupt registers.

2.1.7 PLL Monitoring

The GCRs accept status signals from the master clock multiplier PLL, which multiplies the reference clock up to the core clock rate. The lock status of the PLL and the loss of a valid reference input are tracked by PLLLOL and PLLLOR. Changes in these signals are signalled by delta bits PLLLOLD and PLLLORD, which have corresponding mask bits PLLLOLM and PLLLORM.

2.1.8 PLL Control

The divide ratio of the PLL (the ratio of the internal VCO frequency to the input reference frequency) is controlled using the PLLDIVREF[2:0] bits.

The loop bandwidth of the Rx and Tx PLLs can be controlled with the PLL_LBW[9:0] bits. Most users will use the power-up default settings. For more information, see Table 32, page 117.

2.1.9 Switch Configuration Request

The command to copy all the programmed new connections from standby memory into active memory in the TSI core can be initiated using either hardware or software. The signal from the external new configuration pin and the output of the NEWCFG one-shot bit inside the GCRs are OR'ed and provided as an output to the TSI core. The pulse provided to the TSI core is four core clock cycles long in either case.

When either the software bit or the hardware pin is accessed, the NEWCFGD delta bit is set. If the NEWCFGM mask bit is HIGH, then setting NEWCFGD contributes to an interrupt.

To prevent unwanted configuration changes, a lockout bit NEWCFGLOCK is provided. When set HIGH, no pulses are issued to the core, but delta bit and mask bit functions continue to operate. This allows the configuration update interface to be tested without causing a configuration change.

When switching SONET or TFI-5 data, the pulse provided to the TSI core is a request to perform the standby-to-active transfer at the next frame boundary. To prevent the pulse provided to the TSI core from arriving simultaneously with the frame boundary, a brief blackout period is implemented. A request on the newconfig pin or the NEWCFG register bit that occurs before the blackout period results in a pulse being issued immediately, and a standby-to-active transfer occurring from 0 to 1 frame period later. A request arriving during the blackout results in a pulse occurring just after the blackout period, and in this case, the standby-to-active transfer in the TSI core occurs one full frame later.

Because new configuration requests are already asynchronous and can be expected to take up to one full frame to take effect, this function is invisible to the user. There are no timing restrictions on the newconfig pin or the NEWCFG register bit being asserted.

For convenience, the NEWCFGBUSY busy bit is provided. This indicates that a request has been sent to the TSI core, but that the frame boundary has not yet occurred. On the falling edge of the NEWCFGBUSY bit, the NEWCFGBUSYD bit is set, and an interrupt is generated unless NEWCFGBUSYM is set.

To support full Transparent mode applications, where the frame boundary is irrelevant, the NEWCFGHOLD bit can be set to allow all writes to standby memory to be transferred directly to active memory without writing to the NEWCFG bit.

When a switch core slice is in transparent mode, NEWCFG takes affect immediately rather than waiting for the frame boundary.

2.1.10 Test Control

Registers labeled TESTCTRL are reserved for Vitesse use in manufacturing tests.

2.1.11 Multiple Interface Modes

The CPU interface supports three operational modes:

- Intel® non-multiplexed—Separate address and data buses
- Intel multiplexed—The data bus is used to transmit address followed by data in sequence, delineated by the ale pin
- Motorola®—Separate address and data buses

The mode and the resulting meaning of the external control signals is set by the cpu_mode pin.

For timing diagrams and timing characteristics, see "AC Characteristics," page 126.

2.1.12 Intel Non-Multiplexed Mode

In this mode, data is written on the rising edge of ds_wrn when:

- csn=0
- rd_wrn=1
- as_ale=1
- Valid address is present on a[15:0]
- Valid data is present on d[15:0]

Both a[15:0] and d[15:0] must be stable before and after ds_wrn rises.

Data is driven out after the falling edge of rd_wrn when csn=0,ds_wrn=1, as_ale=1, and valid address is present on a[15:0]. During clear-on-read operations, a[15:0] must be stable before and after rd_wrn falls.

2.1.13 Multiplexed Mode, Read and Write

When configured in its Intel Multiplexed mode, the VSC9295 address and data use the d[15:0] bus sequentially. The address is latched from this bus on a falling edge of as_ale when valid address is present on d[15:0] and csn = 0. d[15:0] must be stable before and after as_ale falls.

Data is written on the rising edge of ds_wrn when csn=0, rd_wrn=1,as_ale=0 and valid data is present on d[15:0]. d[15:0] must be stable before and after ds_wrn rises.

Data is driven out after the falling edge of rd_wrn when csn=0,ds_wrn=1, as_ale=0.

2.1.14 Motorola Mode

In this mode, address is latched from the a[15:0] bus on a rising edge of as_ale when valid address is present on a[15:0] and csn=0. a[15:0] must be stable before and after as_ale falls.

Data is written on the rising edge of ds_wrn when csn=0, rd_wrn=0,as_ale=1,valid address is present on a[15:0] and valid data is present on d[15:0]. Both a[15:0] and d[15:0] must be stable before and after ds_wrn rises.

Data is driven out after the rising edge of ds_wrn when csn=0,rd_wrn=1, as_ale=1 and valid address is present on a[15:0]. During clear-on-read operations, a[15:0] must be stable before and after rd_wrn falls.

2.2 Frame Synchronization Manager

A block diagram of the Frame Synchronization Manager (SyncMan) is shown in the following figure.

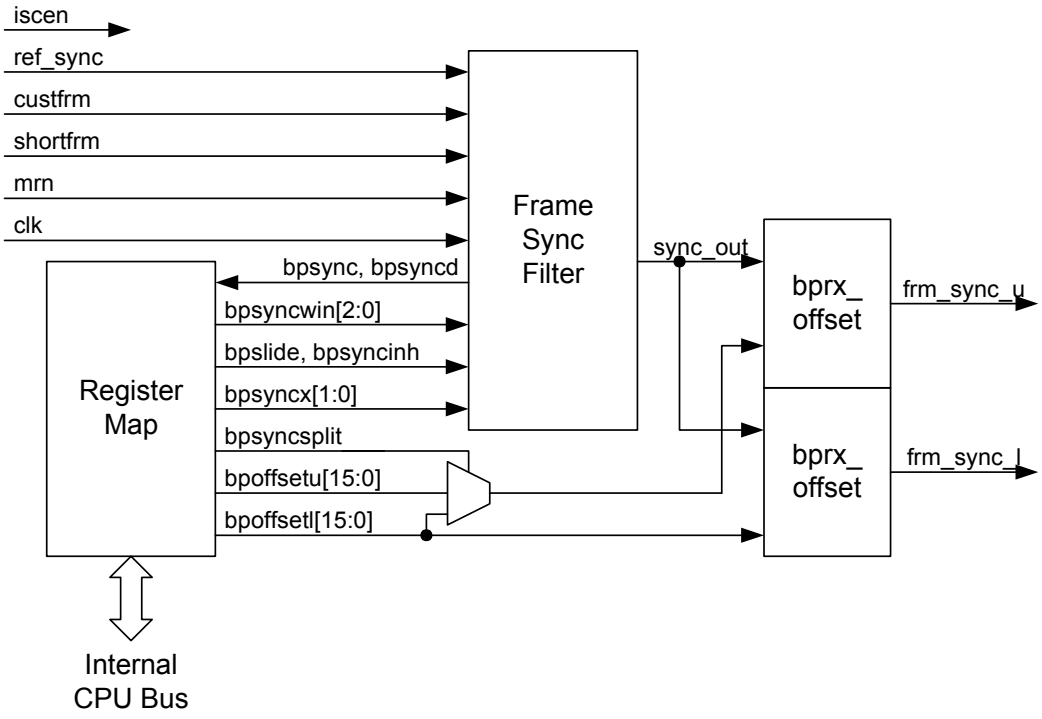


Figure 17. SyncMan Block Diagram

The SyncMan accepts the externally-provided TFI_8KREF signal from a CMOS input cell (per TFI-5 standard). It filters it and produces two shifted and filtered copies of the signal for use in on-chip frame synchronization with two frame domains.

The two domains may be locked together if desired. The SyncMan produces an alarm when FSYNC deviates from its expected position.

2.2.1 Variable Frame Length

The SyncMan allows two frame sizes:

- STS-48 Frame mode (basic TFI-5 frame); 9 rows by 90 columns by 48 STS-1 bytes, with a duration of 125 microseconds at the serial bit rate of 2.488 Gbps. This frame duration applies even if some or all of the inputs are set in STS-12 mode.
- Short Frame mode for the rapid verification and testing of the device; 2 rows by 6 columns by 48 STS-1 bytes or 576 bytes.

The selection of the frame length is controlled by external pin shortfrm.

2.2.2 Split Frame Domains

The SyncMan outputs two on-chip frame sync signals, frm_sync_u and frm_sync_l, which are passed to all the BpRx blocks. The BpRx blocks are then able to select one of these sync signals to use. This enables the device to be used to pass traffic from two different domains in a system. The bit BPSYNCSPLIT indicates whether the two on-chip frame syncs are identical or have different offsets.

2.2.3 Framesync Filtering—Filter Window

The input external frame sync is not necessarily phase-aligned with the clock used to read data out from the elastic stores in BpRx blocks. The asynchronous framesync filter operates as a flywheel and aligns the frame-sync across the time domains. The frame sync is permitted to slide ±n byte clock periods by setting the value of n in the bits BPSYNCWIN[3:0]. In this case, a change of the frame sync position by less than or equal to n byte clock cycles will not be considered as a new frame sync position.

The value of n is programmable from 1 to 15. When the frame sync loses its current position, a status signal (BPSYNC) indicates whether the frame sync is in sync or out of sync. Its corresponding delta and mask bits are BPSYNCD and BPSYNCM respectively.

2.2.4 Sync Offset Control

During frame alignment, the data is read out of the elastic stores in the BPRx blocks in the central clock domain where switching is performed. The external frame sync can be offset by a 16-bit value for each of the two frame domains that is programmable through the control registers BPOFFSETL[15:0] and BPOFFSETU[15:0].

The value of BPOFFSETL or BPOFFSETU can be adjusted so that data is centered in the elastic store (48 bytes deep) of a BpRx for a selected port. This would be the nominal frame position for that port. The frame position of all other ports should not have a skew greater than ±140 ns (±48 byte times). The situation is shown in the following figure for STS48 transactions where the nominal frame sync is the position of the selected frame sync SFS, which is either the synchronized external reference sync input or the frame sync position of the a selected framer.

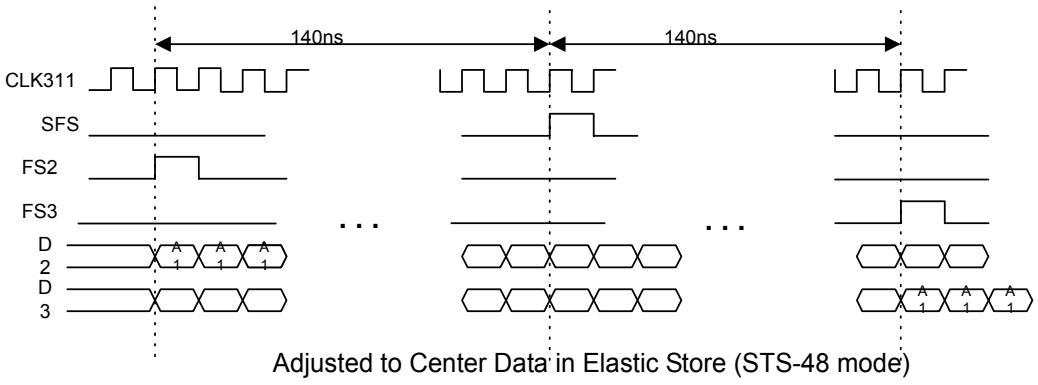


Figure 18. Frame Sync Position with BPOFFSET

In the situation where the worst-case skew of any one port with respect to the selected frame sync is greater than specified maximum skew, the position of the frame sync can be shifted by changing the value of the control registers BPOFFSETL or BPOFFSETU. The situation is as shown in the following figure for an STS-48 transaction, where the nominal frame sync is the position indicated by the dashed line NFS and SFS is the selected frame sync.

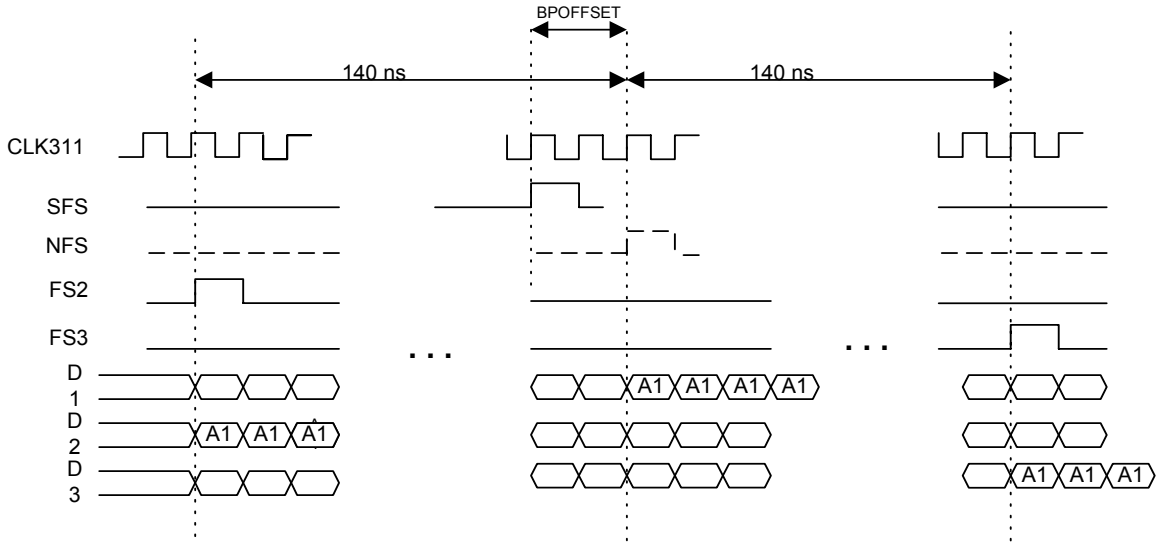


Figure 19. Frame Sync Position with BPOFFSET Adjusted for Worst-Case Skew (STS-48 Mode)

2.3 Overhead Monitor and Insertion

For monitoring and control purposes, bytes in SONET/TFI-5 overhead can be dropped from the incoming data streams and inserted into the outgoing data streams using the two overhead ports provided with the VSC9295.

When STS-12 signals are being received, four redundant consecutive copies of each byte are made, that is, the first byte received from an STS-12 stream is mapped to bytes 0-3 in the internal data stream. Therefore, the data stream appears to contain 48 bytes for overhead monitoring purposes. In Transparent mode, no overhead monitoring can be performed.

A diagram illustrating the various groups of bytes that can be monitored and inserted is shown in the following figure.

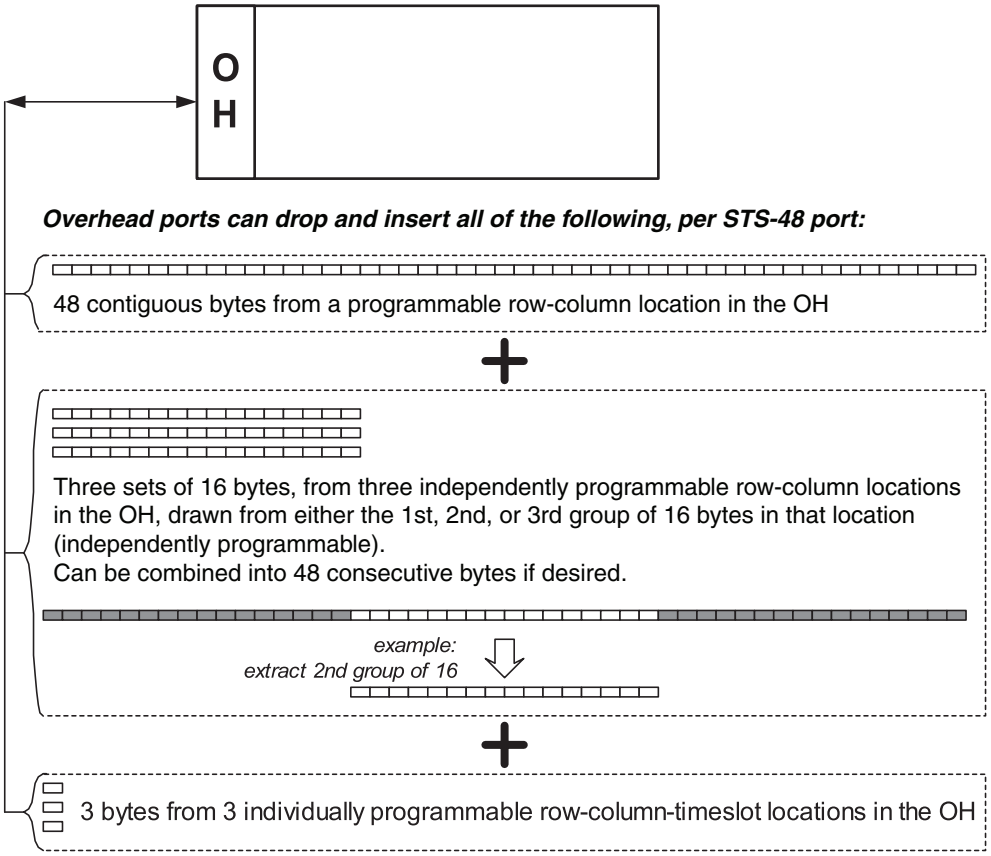


Figure 20. Summary of Overhead Monitor/Insertion Bytes

2.3.1 Transmit Side Custom Overhead Insertion

The VSC9295 device enables you to insert 48 selectable bytes into the unused overhead location at a specific row and column location in two ways. When BPI_MODE is set, the software reads and writes into provisionable byte locations. Alternately, data is read from the overhead monitor interface, fills the local overhead byte registers, and sends those bytes during the following frame.

The rows and columns into which the 48 bytes are inserted are defined by programming BPIROW[3:0] and BPICOL[1:0]. The bytes that can be programmed by the CPU are BPIBx-[7:0] where x = 0 to 47.

The register bits BPIROW and BPICOL have a default startup value of 0. This inhibits insertion of the custom overhead bytes from the programmable locations.

In short frame format, selecting a row higher than 2 on BPIROW results in no byte insertion. In Transparent mode, all insertion capability is disabled.

When using CPU access, the BPIBx, XBIx, and XXBIx data values are unknown until programmed; they are not initialized on reset. In STS-12 mode, only the values for x = 0, 4, 8 through 44 of BPIBx are placed into the outgoing data stream.

Illustration of Custom Overhead Insertion

The values of BPIxROW, BPIxCOL and BPIxTS for different values of the overhead locations of the OC-48 frame are as shown in the following figure. For example, the locations marked by the ellipse correspond to BPIxROW = 6, BPIxCOL = 2.

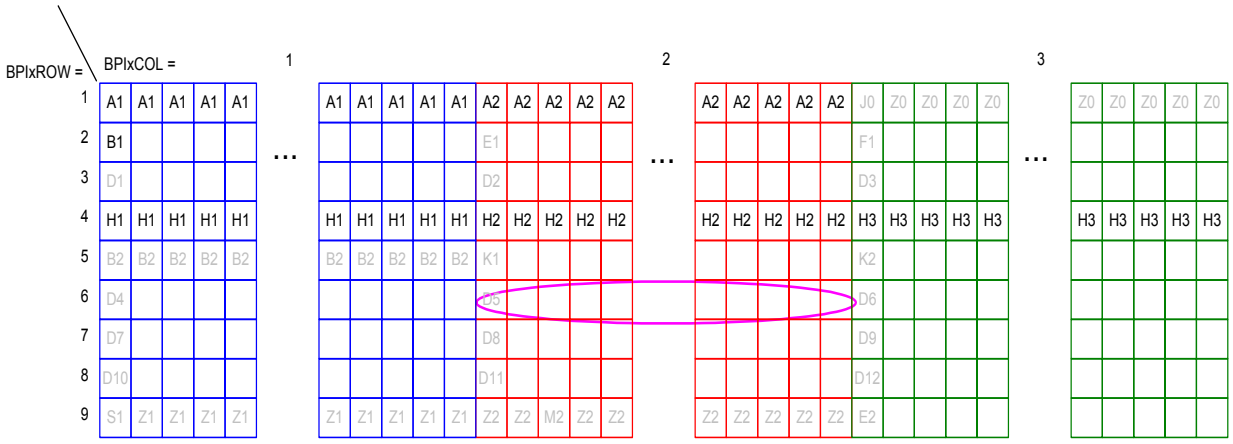


Figure 21. Format of BPIxROW, BPIxCOL

2.3.2 Extended Custom Overhead Insertion

Is is also possible to insert three custom bytes into any part of the unused overhead location at a specific row, column, and time slot in the same manner as described in the preceding section.

This is accomplished by programming XBI_ROW[3:0], XBI_COL[1:0], and XBI_TS[5:0] with the row, column, and time slot in which to insert the byte. XBIx-[7:0],where x = 0 to 2, are the bytes that can be programmed by the CPU.

The register bits XBI_ROW, XBI_COL, and XBI_TS have a default startup value of 0. This inhibits insertion of the custom overhead bytes from the programmable locations.

For short frame format, selecting a row higher than 2 on XBI_ROW results in no byte insertion. In Transparent mode, all insertion is disabled. In STS-12 mode, only the values for x = 0, 4, 8 through 44 are placed into the outgoing data stream, and the legal values of XBI_TS[5:0] are 0, 4, 8 through 44.

2.3.3 Extra Extended Custom Overhead Insertion

It is also possible to insert three sets of 16 custom bytes into any part of the unused overhead location at specific row and column locations. These 16 bytes are inserted in either the first third (bytes 0 through 15), second third (bytes 16 through 31), or the last third (bytes 24 through 47) of the 48 bytes in that row and column location. These bytes can be combined to form one set of 48 contiguous bytes by using the same row and column for all, and using a different time slot (group) value for each. This is accomplished by programming XXBI_ROW[3:0], XXBI_COL[1:0], and XXBI_TS[1:0] with the row, column, and time slot offset in which to insert the bytes. XXBI-y-[7:0], where y = 0 to 2, are the bytes that can be programmed by the CPU.

The register bits XXBI_ROW, XXBI_COL, and XXBI_TS have a default startup value of 0. This inhibits insertion of the custom overhead bytes from the programmable locations.

In short frame format, selecting a row higher than 2 on XXBI_ROW results in no byte insertion. In Transparent mode, all insertion is disabled. In STS-12 mode, only the values for time slots 0, 4, 8, and 12 of each XXBI-y are placed into the outgoing data stream.

2.3.4 Backplane Receiver Side Overhead Monitoring

The receive side byte capture of the VSC9295 mirrors the insertion capability of its transmit side, but can only stream the captured bytes to the overhead monitor port (there is no CPU access to read the captured bytes because they cannot be read in real time).

The overhead monitor captures 48 consecutive bytes from a row and column location specified by BPIROW[3:0] (1-9) and BPICOL[1:0] (1-3) and stores them locally. Three additional bytes at programmable row, column, and time slot locations specified by XBIx_ROW[3:0] (1-9), XBIx_COL[1:0] (1-3), and XBIx_TS[5:0] (0-47) are captured and stored (x = 0, 1, 2). In addition, three groups of 16 bytes, each from programmable row and column locations specified by XXBIx_ROW[3:0] (1-9) and XXBIx_COL[1:0] (1-3), are captured and stored from one of three groups (first, second, or third group of 16 in a set of 48) specified by XXBIx_TS[1:0] (x = 0, 1, 2). When any of these programmable locations overlap with each other or with the contiguous bytes, it is not expected that duplicate copies will be stored. It is the user's responsibility to avoid this overlap.

During the succeeding frame, the values captured during the previous frame are sent out on the internal overhead monitor interface while new values are being captured in a second set of memory locations. The overhead monitor interface sends the bytes from all BPRx block off-chip in sequence for processing by an external device. The byte values may be used as health factors to compare the relative quality of two signals in a protection pair, for instance.

2.3.5 Overhead Monitor Interface

The overhead monitor interface registers the data stream and sends it from the overhead monitors inside the BPRx blocks. It also receives, registers, and re-sends the optional data stream containing bytes to be inserted into the outgoing overhead in the BPTx block.

A typical use for the interface is to stream captured bytes to an FPGA that can make automatic protection switching decisions based on health factors embedded in the overhead bytes by line card devices, and to provide an in-band messaging channel to downstream devices. For capacity reasons, and to facilitate operation with split frame domains, there are two instances of the OHMonIF in a VSC9295.

Byte-Wide Interface

The VSC9295 external interfaces for the OHMonIF are eight bits wide with a clock that runs at 78 MBps. All the data captured during one frame can be transmitted through the port during the succeeding frame.

Data Valid Signal

To signal the start and end of each of each frame's data, a data valid signal ohpdv is raised coincident with the first data byte from a new frame. It falls at the end of the last data byte from that frame. At 78 MBps, with 68 channels each capturing 99 bytes, the data stream lasts for 86.574 µs out of each 125 µs frame.

The ohpdv signal also notifies the external device to begin data transfer into ohdatain[7:0].

Receive and Register Data Streams

The overhead monitor interface receives a byte-wide data stream from off-chip. The interface registers the stream and drives it onto ohmondatco[7:0] inside the device, which is connected to all BPTx blocks.

Data Stream Order

The ingoing and outgoing data streams consist of 68 consecutive groupings of 99 bytes each. Each group belongs to one of the TFI-5 ports being monitored or driven, starting with the lowest and ending with the highest. Within each group, the byte order is as follows: The three XBI bytes, followed by the three groups of XXBI bytes, followed by the 48 BPI bytes.

Interface Timing

Timing for the overhead dropping function is shown in the following figure.

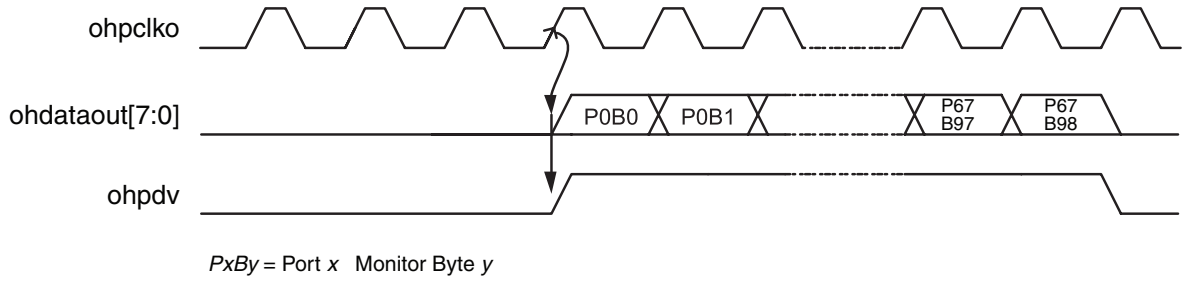


Figure 22. Overhead Monitoring Interface Timing for Dropping Bytes to ohdataout

Timing for the overhead insertion function is shown in the following figure.

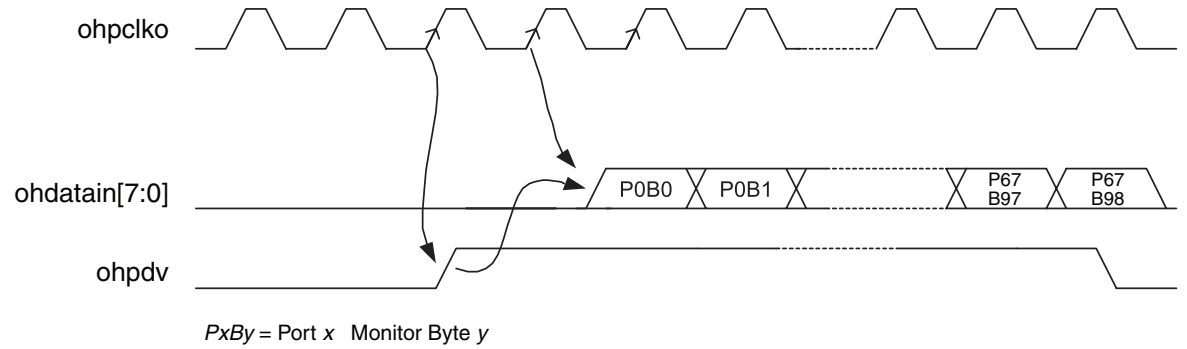


Figure 23. Overhead Monitoring Interface Timing for Accepting Bytes at ohdatain[7:0]

Disable Function

The VSC9295 OHMonIF has a disable control that forces ohdataout[7:0] to 0x00, which stops ohpclko from toggling.

2.4 Static Bitslicing Block

A block diagram of the static bitslicing block (bitslicer) is shown in the following figure.

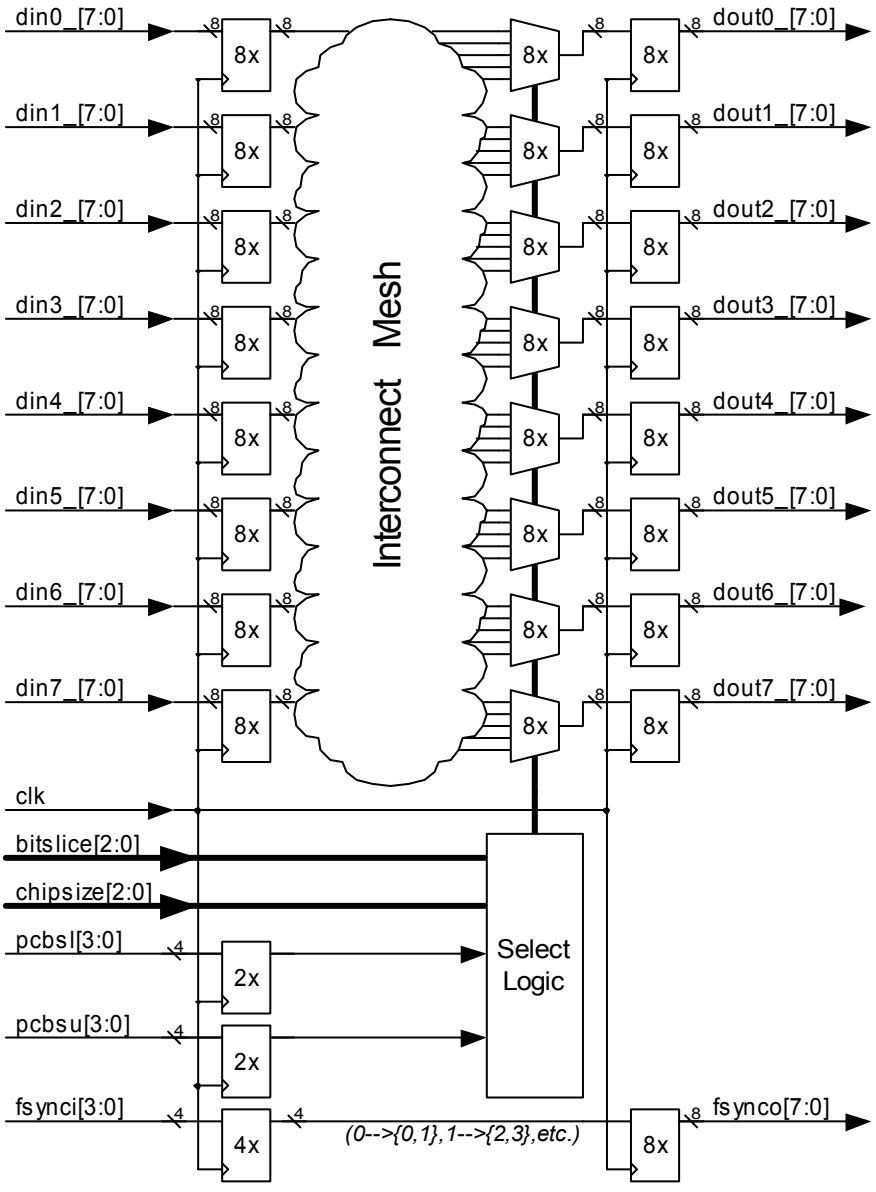


Figure 24. Bitslicer Block Diagram

The bitslicer stores and processes eight bytes of data from eight data streams, and rearranges their bits to map onto eight output ports according to the slicing mode indicated with the bitslice and chipsize control pins. The bitslice pins are taken from a separate set of bits from the bitslice bits delivered to the TSI core.

There are bitslicers between the BPRx blocks and the TSI core, and also between the TSI core and the BPTx blocks. This means that static bitslicing can be performed at both the ingress and egress of the device, before or after switching.

This function is referred to as static bitslicing to distinguish it from the bitslicing that can be done with the TSI core, which performs actual routing of bit pairs. The function of the bitslicer block is to rearrange bits in a predetermined way to allow the VSC9295 to be used solely for slicing and merging data in a switch fabric that utilizes bitslicing.

The block also participates in TSI switching in the FQBS4 bitslicing mode of the switch core. In the FQBS4 mode, bit pairs from two streams of 2x bit-sliced data from two TSI core slice pairs are combined by selecting bit pairs from each based on the values of pcbsl and pcbsu, which can change every clock cycle.

2.4.1 Bitslicing Modes and Bit Pair Select Mode

There are seven modes in which the bitslicer can operate. These modes are described in the following table. The bitslice pins are taken from a separate set of bits from the bitslice bits delivered to the TSI core. The mode defaults to PassThru for any combination not listed in the table.

Table 3. Bitslicer Modes

Mode	Bitslice [2:0]	Chip Size [2:0]	Description
PassThru	000	0xx	Pass all bits on all input ports directly to the same bits on corresponding output ports.
2x-uprlowr	001 or 010	011 or 001	2x slice input ports [0,1] onto output ports [0,1], [2,3] onto [2,3].
4x-uprlowr	011	011 or 001	4x slice input ports [0,1,2,3] onto output ports [0,1,2,3] and [4,5,6,7] onto [4,5,6,7].
2x-evenodd	001 or 010	010 or 000	2x slice input ports [0,2] onto output ports [0,2], [1,3] onto [1,3], [4,6]-[4,6] and [5,7]-[5,7].
4x-evenodd	011	010 or 000	4x slice input ports [0,2,4,6] onto output ports [0,2,4,6] and [1,3,5,7] onto [1,3,5,7].
8x	1xx	011 or 001	8x slice input ports [0,1,2,3,4,5,6,7] onto output ports [0,1,2,3,4,5,6,7].
PostSelect	xxx	1xx	Perform bit pair selection for ports [0,2] onto port 0 and [4,6] onto port 4. Force other ports to 0x00.

2.5 JTAG

The VSC9295 supports an IEEE 1149 standard JTAG boundary scan. All signals except those designated as test controls are accessible in the boundary scan chain. A differential pair signal is treated as one signal for boundary scan purposes.

2.5.1 JTAG Boundary Scan Input/Output

The following table lists the external I/O signals used to communicate with the JTAG TAP controller.

Table 4. JTAG External I/O Signals

Pin	Name	I/O	Type	Description
TDO	JTAG test data output	O	TTL	This signal carries test data out of the device by means of the IEEE standard P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tri-state output that is inactive except when data scan shifting is in progress.
TDI	JTAG test data input	I	TTL	The signal carries test data into the device by means of the IEEE standard P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-down resistor.
TCK	JTAG test clock	I	TTL	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	JTAG test mode select	I	TTL	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-down resistor.
TRSTB	JTAG test reset (active low)	I	TTL	This signal provides an asynchronous test access port reset using the IEEE P1149.1 test access port. TRSTB is a Schmitt-triggered input with an internal pull-*down* resistor.

2.5.2 Boundary Scan Testing

Boundary scan testing on the VSC9295 is supported with the IEEE 1149.1 standard Test Access Port (TAP) and associated circuitry. This circuitry consists of the TAP Controller, the instruction register with instruction decoder, and three types of data registers: the Device ID register, the Boundary Scan register, and the Bypass register. In general, the data registers consist of two register parts, a serial shift register, and a parallel output or shadow register. The parallel output registers maintain their values during shifting operations and are loaded with new values from the shift register during an update state.

The following figure illustrates the architecture of the boundary scan test circuitry.

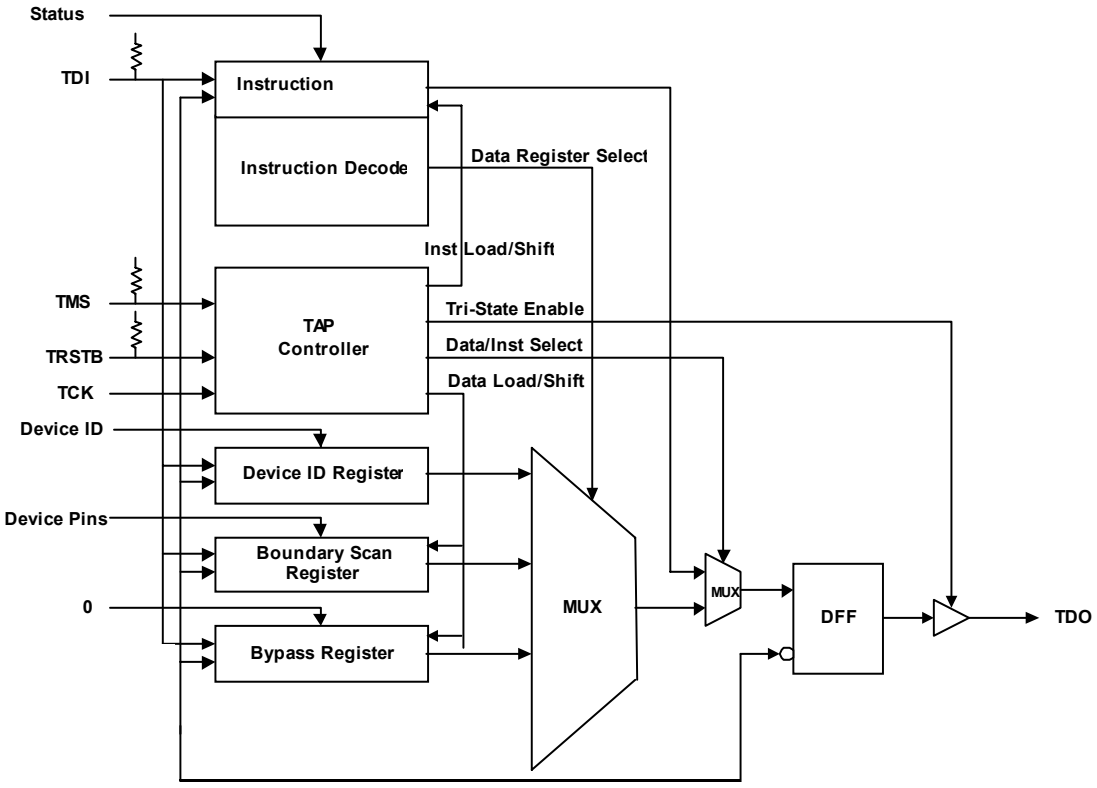


Figure 25. Boundary Scan Test Architecture

2.5.3 Instruction Register

The 4-bit instruction register and associated code determine the type of operation to be performed by the scan test logic, and which data register will be selected in the scan path and used in the operation. When in the test logic reset state, this register is initialized to the IDCODE instruction. It is loaded with status information while in the Capture-IR state in which the two least significant bits must be 01 for scan path testing purposes (currently the status information is the IDCODE instruction). Serially loaded instructions become active in the Update-IR state.

The following table lists the supported test instructions, which data register is selected for the test, and the device operating mode during the test. When the device is in the Test Operating mode, the output pins are affected by the test operation. Device inputs, outputs, and internal logic are unaffected by the test operation in normal mode.

Table 5. Boundary Scan Test Instructions

Instruction Code	Instruction	Selected Data Register	Device Operating Mode
0000	EXTEST	Boundary Scan	Test
0001	IDCODE	Device ID	Normal
0010	SAMPLE/PRELOAD	Device ID	Normal
0100	Unused	None	Test
0101	CLAMP	None	Test
1111	BYPASS	None	Normal
All Others	BYPASS	Bypass	Normal

2.5.4 Supported Test Instructions

The following table contains a description of the supported test instructions.

Table 6. Test Instruction Descriptions

Instruction	Description
EXTEST	The EXTTEST instruction provides for board-level interconnect testing and device manufacturing I/O levels testing by allowing device inputs to be observed and device outputs to be controlled. The device inputs are captured while in the Capture-DR state and subsequently shifted out on TDO with the Shift-DR state. Device outputs can be set by providing the desired values on TDI while in the Shift-DR state followed by actually driving the outputs with the loaded values at the Update-DR state.
IDCODE	The IDCODE instruction allows the Device ID register to be read by serially shifting bit values out on TDO with the Shift-DR state. This instruction is automatically loaded by entering the Test-Logic-Reset state in addition to the normal serial instruction loading mechanism.
SAMPLE/PRELOAD	The SAMPLE/PRELOAD instruction allows for observing the device inputs and internal output signals while the device is operating normally. The signal values are loaded into the Boundary Scan register during the Capture-DR state and can be observed by shifting the values out with the Shift-DR state. The pre-load aspect of this instruction occurs at the Update-DR state in which the values that are in the serial part of the Boundary Scan register are loaded into the parallel output (shadow) part. This allows the Boundary Scan register to be pre-loaded for subsequent test operations such as EXTTEST or CLAMP.
BYPASS	The BYPASS instruction allows the serial data on TDI to be transferred to TDO with only one TCK delay. This facilitates board-level testing by allowing the serial test data to quickly pass on to the next device. The Bypass register is loaded with a logic 0 during the Capture-DR state.
CLAMP	The CLAMP instruction allows the device outputs to be held in a desired state as determined by values previously loaded in the Boundary Scan register (from instructions such as SAMPLE/PRELOAD or EXTEST). Otherwise, device operation is identical to the BYPASS instruction.

2.5.5 Device ID Register

The 32-bit Device ID register is used to identify the manufacturer, part number, and version of the device through its test port. When the IDCODE instruction is loaded, the identifying information is loaded into the Device ID shift register during the Capture-DR state and can be shifted out on TDO through the use of the Shift-DR state. The device identification information is shown in the following table. Converted to binary the number would be: 0001100100101001010100011110100 1.

Table 7. Device ID Register Table

Version Number	Part Number	Manufacturer's ID	Fixed
31 28	27 12	11 1	0
0x1	0x9295	0x0F4	0x1

2.5.6 Bypass Register

The Bypass register is a 1-bit register that provides a means for system serial test data to bypass the device with only one TCK cycle delay. This register is selected to be in the scan path during the BYPASS instruction. This register is set to logic 0 during the Capture-DR state.

2.5.7 Boundary Scan Register

The 622-bit Boundary Scan register (BSR) provides the means to force values on the device outputs and to capture values on the device inputs (and internal output signals). The direction of shift is from TDI (MSB), through bits 621-0, to TDO (LSB). A BSDL file detailing the configuration of the boundary scan register is available from the factory.

2.5.8 TAP Controller

The TAP Controller is a synchronous state machine that provides control to capture and shift test data throughout the test registers. State transitions occur on the rising edge of TCK and are controlled by the TMS signal as illustrated in the following figure.

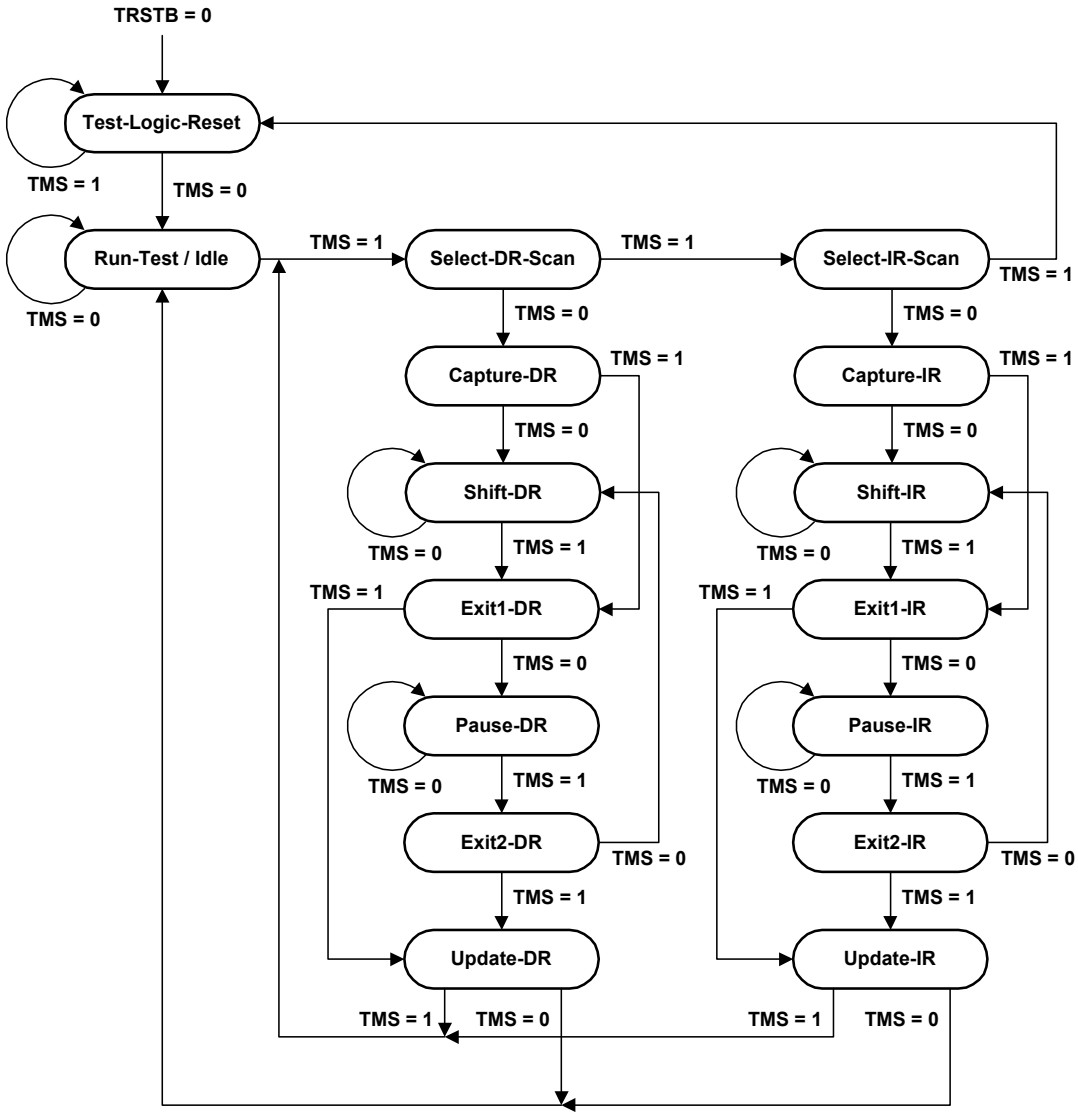


Figure 26. TAP Controller State Diagram

The following table summarizes the descriptions of the TAP controller states.

Table 8. TAP Controller State Descriptions

TAP Controller State	Description
Test-Logic-Reset	Asserting TRSTB forces the TAP Controller to asynchronously enter the Test-Logic-Reset state. This state is also entered synchronously within five TCK cycles when TMS is held high. In Test-Logic-Reset state all of the associated test logic is reset and disabled, allowing the device to operate normally. The Instruction register is loaded with the IDCODE instruction while the data registers are reset to logic 0.
Run-Test/Idle	Run-Test/Idle state is an idle state in which the test logic is disabled and the device operates normally. It is different from the Test-Logic-Reset state in that the current state of the test logic is maintained.
Select-DR-Scan, Select-IR-Scan	These states are single TCK states that allow the selection of data register scan operations or instruction register scan operations.
Capture-DR	Capture-DR state causes the selected serial data register to be loaded in parallel with a data value determined by the current instruction. The data is loaded on the rising edge of TCK as the TAP Controller transitions to the next state.
Shift-DR	Shift-DR state causes the selected data register to shift one bit in the direction going from TDI (MSB) towards TDO (LSB). Repeated single bit shifts are performed each rising TCK edge that TMS is held low.
Exit1-DR, Exit2-DR	These states are single TCK states at the end of a data register shift that allow a return to the Shift-DR state without going through the Capture-DR state, or allow the state machine to exit the data register shifting process back to the idle condition. TDO will transition to the high-impedance state on the first falling edge of TCK after the Exit1-DR state is entered.
Pause-DR	Pause-DR state allows the data register shifting process to be suspended without change or loss of the data register contents.
Update-DR	Update-DR state causes the parallel output (shadow) register part of the selected data register to be updated to match the value currently stored in the serial data register part. This update occurs on the first falling edge of TCK after the Update-DR state is entered. (Currently only the Boundary Scan register has parallel output registers.)
Capture-IR	Capture-IR state causes the Instruction register serial part to be loaded in parallel with status information. The status is loaded on the rising edge of TCK as the TAP Controller transitions to the next state. (Currently the status information is simply the IDCODE instruction.)
Shift-IR	Shift-IR state causes the Instruction register to shift one bit in the direction going from TDI (MSB) towards TDO (LSB). Repeated single bit shifts are performed each rising TCK edge that TMS is held low.
Exit1-IR, Exit2-IR	These states are single TCK states at the end of an Instruction register shift that allow a return to the Shift-IR state without going through the Capture-IR state, or allow the state machine to exit the Instruction register shifting process back to the idle condition. TDO will transition to the high-impedance state on the first falling edge of TCK after the Exit1-IR state is entered.
Pause-IR	Pause-IR state allows the Instruction register shifting process to be suspended without change or loss of the Instruction register contents.
Update-IR	Update-IR state causes the instruction currently loaded into the serial shift register part of the Instruction register to be loaded into the parallel output (shadow) register part of the Instruction register. This causes the Instruction to become active. This activation of the instruction occurs on the first falling edge of TCK after the Update-IR state is entered.

2.6 Clock Multiplier

In the VSC9295, an on-board PLL is used to multiply the reference clock up to the core clock frequency. The ratio controls are sent from the General Configuration registers in the CPU interface block. In the default power-up state of the General Configuration registers, the divide ratio of the CMU VCO versus the reference frequency is taken from the external pins refsel[2:0] rather than from the internal register. The CMU status pins loss_of_lock and loss_of_reference are made available in the General Configuration registers. The loss_of_lock signal is also sent off-chip as plock, where it is inverted. A test clock output testclkp/n is sent off-chip as a confirmation that the CMU is operating properly, independent of plock.

For more information about reference select values, see "Master Control Register Map," page 116.

2.7 TSI Switch Core (TSI)

A block diagram of one TSI core slice is shown in the following figure. There are 68 slices in the VSC9295.

The TSI core accepts 136 streams of byte-wide STS-48-like frames, and allows non-blocking connection from any of the 6528 incoming STS-1 signals to any of the 96 outgoing STS-1 signals. It accomplishes this by programming the connection map (configuration memory). Hitless switch-over is implemented by transferring the contents of the standby map to the active map at the boundary between A1 and A2.

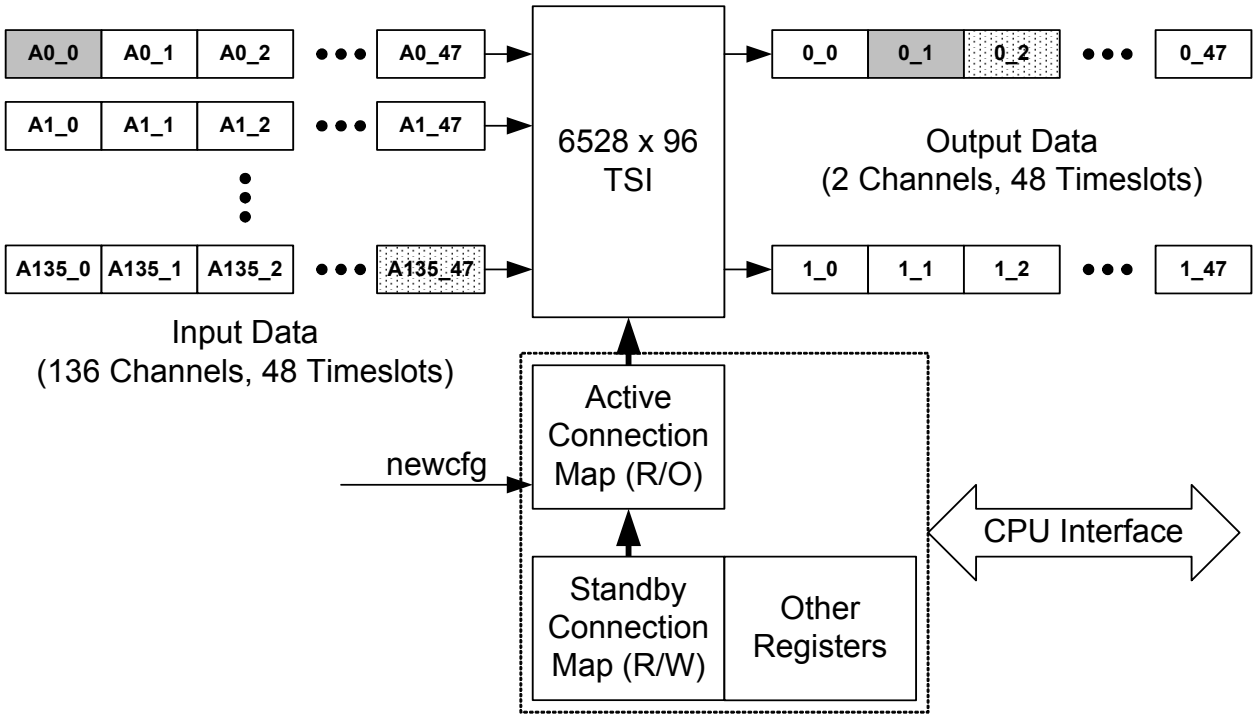


Figure 27. Block Diagram of a Single TSI Slice (One of 68)

Program memory integrity is implemented in the active map to signal a memory error should a bit in the active map be flipped by an alpha particle or other unexpected event.

The TSI core supports 4x bitslicing to allow four VSC9295s operating at half bandwidth each to be used in parallel to create a higher bandwidth switch. This feature provides an internal non-blocking connectivity of 13056 × 13056 signals. All the program memories and multiplexers of two adjacent TSI outputs are required to provide enough resources to enable this feature, so the device operates with only half its input and output ports active. Only one of the two TSI outputs are valid in this configuration.

Input data to the TSI core is duplicated on adjacent channels and manipulated when in this mode. All the connection map and switching resources of the 6528 × 96 slice are used in this mode and only one of the outputs of each slice can be used. The device operates in this mode with only half of its input and output ports active (68 inputs × 68 outputs).

As an additional mode, outputs of multiple output slices can be combined to create a 136 input × 34 output part with 4x bitslicing. Using this mode, four VSC9295s can be connected to create a 26112 × 26112, non-blocking STS-1 switch.

The TSI core also supports 2x bitslicing with half the input channels or half the output channels (or both) used. Additionally, 1x bitslicing (no bitslicing) is also supported for all modes.

2.7.1 Hitless Switching

The TSI has the capability to provide hitless switching at the STS-1 level. Hitless switching is defined as no loss of data during switching of configuration. To provide hitless switching the control logic causes the TSI to change configurations only during a frame boundary such as the A1, A2 boundary in SONET frames. A switch is initiated by the newcfg input, which is available as an external pin of the device and as a register in the master register map. Due to performing the switch on the A1, A2 boundary, any A1 bytes given to the mapping layer as allowed in TFI-5 will contain data from the previously programmed connection.

2.7.2 Broadcast and Multicast

The TSI has the capability to broadcast any one input byte onto any combination of bytes or all output bytes in time and space.

2.7.3 STS-1 Switching

The TSI has the capability to switch at the SONET STS-1 level when bitslicing is not activated. In this mode, only the lower set of active and standby configuration bytes are used to control switch configuration.

2.7.4 Bitslicing

The TSI has the capability to switch each of four bit pairs ([7,6],[5,4],[3,2],[1,0]); or each of two nibbles ([7,6,5,4] and [3,2,1,0]) within an STS-1 byte individually with no blocking restrictions. Bitslicing mode is enabled by the external pins size[1:0] and bitslice[1:0]. When enabled, multiple banks of active and standby configuration bytes are used for switch configuration.

The core also supports 2x bitslicing with either half the input channels or half the output channels used. The following table summarizes the descriptions of the various configurations of the core based on the size and bitslice inputs. The table also serves as a key for the naming convention used in the rest of this document for the number of inputs and outputs, and the bitslicing mode value. The convention consists of an abbreviation H for Half and F for Full to relate to the number of inputs and outputs (the first letter is the number of inputs, the second is the number of outputs), followed by BS, then the bitslicing mode value.

Table 9. Bitslice and Size Controls

		Size[1:0]			
		00	01	10	11
Bitslice [1:0]	00	68 x 68 with No Bitslicing (HHBS1)	68 x 136 with No Bitslicing (HFBS1)	136 x 68 with No Bitslicing (FHBS1)	136 x 136 with No Bitslicing (FFBS1)
	01	68 x 68 with 2X Bitslicing (HHBS2)	68 x 136 with 2X Bitslicing (HFBS2)	136 x 68 with 2X Bitslicing (FHBS2)	
	10				
	11	68 x 68 with 4X Bitslicing (HHBS4)			

There is one additional mode (FQBS4) that is selected by setting Chipsize[2:0] to 100. This mode uses 136 inputs and 34 outputs with 4x bitslicing.

2.7.5 Transparent Mode

In this mode, no time switching is performed. The entire data stream arriving at an input port of the TSI is sent to the output by setting the TSITRNSPNT0 or TSITRNSPNT1 bit. Note that TSITRNSPNT1 is only used with a full complement of outputs (modes HFBS1, HFBS2, FFBS1); otherwise, TSTRNSPNT0 controls Transparent mode.

Switching into and out of Transparent mode is NOT hitless because the data has not been framed. At the device level, such a switch will be phase hitless (no instantaneous change of phase).

In addition to the two register controls, there is also a device pin, txpmode, that overrides the settings of the registers. When this pin is HIGH, it is equivalent of setting both TSITRNSPNT0 and TSITRNSPNT1.

2.7.6 Connection Provisioning

For provisioning, Switch Configuration register maps are used. These represent the configuration of the output ports. Addresses in the maps refer to the output ports and time slots. The content of the register maps specifies for each output time slot (or time slot bit pair) which input channel, time slot (and bit pair or nibble) is used to get its data. Each TSI slice contains connection maps for two adjacent outputs, such as 0/1, 2/3, and so forth. The maps are used in different ways depending on the sizing and bit slicing mode setting used for the device.

There is an active map, which controls the actual switch configuration, and a standby map which holds the configuration that will be in place after the next switch-over event. The standby map is readable and writable using the CPU interface, but the active map is read only. When a new configuration operation is performed (using the newcfg pin or NEWCFG register bit) the contents of the standby maps are simultaneously transferred to the active maps at the next frame boundary.

There are three types of entries in the active maps: TSIAxxyC, TSIAxxyS, and TSIAxxyN and three types in the standby maps: TSISxxyC, TSISxxyS, and TSISxxyN. The xx denotes output time slot, and the y represents the bank number (0-3).

Table 10, page 51 and Table 11, page 52 summarize how each of these register maps is used in each of the bitslicing modes. Shaded cells mean that the register is a copy of another register and does not need to be explicitly written. For example, in FFBS1 mode (full size, no bitslicing), write to map 0 for the even output and write to map 2 for the odd output. You do not need to write to maps 1 and 3. In HHBS4 mode (half size, 4x bitslicing, as used in a 680G fabric), the four maps control a single output because only half of the

outputs are used, and the maps represent the connection for each of the four nibbles in the byte (LSN to MSN for maps 0-3).

Table 10. Register Bank Mapping for Non-Bitsliced (BS1) and 4x Bit-Sliced (BS4) Modes

Subpart	Mode					
	HHBS1	HHBS4	HFBS1	FHBS1	FQBS4[1]	FFBS1
TSIxx0C	Output 0 7=Unused [6:0] =Space	Output 0 Bitslice 0 7=Unused [6:0] =Space	Output 0 7=Unused [6:0] =Space	Output 0 Space	Output 0 Bitslice 0 Space	Output 0 Space
TSIxx0S	Output 0 Timeslot	Output 0 Bitslice 0 Timeslot	Output 0 Timeslot	Output 0 Timeslot	Output 0 Bitslice 0 Timeslot	Output 0 Timeslot
TSIxx0N	Unused	Output 0 Bitslice 0 Bitslice	Unused	Unused	Output 0 Bitslice 0 Bitslice	Unused
TSIxx1C	Output 0 7=Unused [6:0] =Space	Output 0 Bitslice 1 7=Unused [6:0] =Space	Output 0 7=Unused [6:0] =Space	Output 0 Space	Output 0 Bitslice 0 Space	Output 0 Space
TSIxx1S	Output 0 Timeslot	Output 0 Bitslice 1 Timeslot	Output 0 Timeslot	Output 0 Timeslot	Output 0 Bitslice 0 Timeslot	Output 0 Timeslot
TSIxx1N	Unused	Output 0 Bitslice 1 Bitslice	Unused	Unused	Output 0 Bitslice 0 Bitslice	Unused
TSIxx2C	Unused	Output 0 Bitslice 2 7=Unused [6:0] =Space	Output 1 7=Unused [6:0] =Space	Unused	Output 0 Bitslice 1 Space	Output 1 Space
TSIxx2S		Output 0 Bitslice 2 Timeslot	Output 1 Timeslot		Output 0 Bitslice 1 Timeslot	Output 1 Timeslot
TSIxx2N		Output 0 Bitslice 2 Bitslice	Unused		Output 0 Bitslice 1 Bitslice	Unused
TSIxx3C	Unused	Output 0 Bitslice 3 7=Unused [6:0] =Space	Output 1 7=Unused [6:0] =Space	Unused	Output 0 Bitslice 1 Space	Output 1 Space
TSIxx3S		Output 0 Bitslice 3 Timeslot	Output 1 Timeslot		Output 0 Bitslice 1 Timeslot	Output 1 Timeslot
TSIxx3N		Output 0 Bitslice 3 Bitslice	Unused		Output 0 Bitslice 1 Bitslice	Unused

1. For FQBS4, entries in two consecutive TSI register maps must be used to fully specify the content of one output time slot. For example, to program the contents of output channel 0, time slot 0, one would program TSI000C,TSI000S and TSI000N of the register map for TSI slices 0/1 to specify the content of bits 0 and 1 (the LSBs), TSI002C,TSI002S and TSI002N to specify the content of bits 2 and 3, TSI000C,TSI000S and TSI000N of the register map for TSI slices 2/3 to specify the content of bits 4 and 5 and TSI002C,TSI002S and TSI002N of the register map for TSI slices 2/3 to specify the content of bits 6 and 7 (the MSBs).

Table 11. Register Bank Mapping by TSI Mode for 2x Bit-Sliced (BS2) Modes

Subpart	Mode		
	HHBS2	HFBS2	FHBS2
TSIxx0C	Output 0 Bitslice 0 7=Unused [6:0] =Space	Output 0 Bitslice 0 7=Unused [6:0] =Space	Output 0 Bitslice 0 Space
TSIxx0S	Output 0 Timeslot	Output 0 Bitslice 0 Timeslot	Output 0 Bitslice 0 Timeslot
TSIxx0N	Output 0 1=Bitslice 0=Unused	Output 0 Bitslice 0 1=Bitslice 0=Unused	Output 0 Bitslice 0 1=Bitslice 0=Unused
TSIxx1C	Output 0 Bitslice 1 7=Unused [6:0] =Space	Output 0 Bitslice 1 7=Unused [6:0] =Space	Output 0 Bitslice 0 Space
TSIxx1S	Output 0 Bitslice 1 Timeslot	Output 0 Bitslice 1 Timeslot	Output 0 Bitslice 0 Timeslot
TSIxx1N	Output 0 Bitslice 1 1=Bitslice 0=Unused	Output 0 Bitslice 1 1=Bitslice 0=Unused	Output 0 Bitslice 0 1=Bitslice 0=Unused
TSIxx2C	Unused	Output 1 Bitslice 0 7=Unused [6:0] =Space	Output 0 Bitslice 1 Space
TSIxx2S		Output 1 Bitslice 0 Timeslot	Output 0 Bitslice 1 Timeslot
TSIxx2N		Output 1 Bitslice 0 1=Bitslice 0=Unused	Output 0 Bitslice 1 1=Bitslice 0=Unused
TSIxx3C	Unused	Output 1 Bitslice 1 7=Unused [6:0] =Space	Output 0 Bitslice 1 Space
TSIxx3S		Output 1 Bitslice 1 Timeslot	Output 0 Bitslice 1 Timeslot
TSIxx3N		Output 1 Bitslice 1 1=Bitslice 0=Unused	Output 0 Bitslice 1 1=Bitslice 0=Unused

2.7.7 Transparent Mode Provisioning

In the VSC9295 Transparent mode, only the input channel from which the output data stream is routed needs to be specified. Therefore, the only configuration bits whose values are used are TSIS000C (in standby map) and TSIA000C (in active map). If the VSC9295 is in HFBS1, HFBS2, or FFBS1 mode, TSITRNPNT1 is active, and TSI002C (in standby map) and TSIA002C (in active map) is used for Transparent mode switching to output 1.

2.7.8 Path AIS and UNEQ Insertion

To pass AIS or UNEQ on STS-1s that are not in use, the device inserts AIS or UNEQ on a per time slot (bit pair) basis. The user is responsible for making sure that the correct bitslice and time slot are set when in these modes. To insert one of these special signals, the TSIAxxxyC[7:0] (channel) bits are set to one of the codes shown in Table 12, page 54. When the device is configured with two frame domains, the user must choose the signal from the appropriate frame domain.

In the AIS signal, a value of 0xFF is forced in place of the data. The J0/Z0 byte for each STS-1 so configured will contain an 8-bit value corresponding to the time slot number (0x00 for time slot 0 to 0x3F for time slot 47).

In the SDH UNEQ, a value of 0x00 is forced in place of the data. The J0/Z0 byte for each STS-1 so configured will contain an 8-bit value corresponding to the time slot number (0x00 for time slot 0 to 0x3F for time slot 47). The value of the H1 byte is set to 0x68. Downstream circuitry in another block rewrites the frame boundary (A1 and A2 bytes), however these are re-written by the TSI core when in UNEQ. The value of B2 should reflect the correct byte interleaved parity for the STS-1, excluding the section overhead. This means setting B2 to the same value as H1 in every second frame, and to 0x00 in the opposite frames. The ordering for the B2 values does not matter because either can come out first.

The SONET UNEQ signal differs slightly from the SDH UNEQ. For SONET, some equipment can tolerate a value of 0x68 in H1, while some cannot. The most correct value is 0x60. To enable this functionality for UNEQ, the value of TSIAxxyC[7:0] is set to 0xFD (channel 253, which does not exist). This also results in the B2 value alternating between 0x60 and 0x00 in successive frames. It does not matter which value of the B2 byte is the first.

In modes where only half of the inputs are used, the MSB of the TSIAxxyC value does not matter. Therefore in HHBS1 mode, AIS can be obtained with either 0x7F or 0xFF in TSIAxxyC[7:0].

When in bitslice mode, outgoing bytes are composed of bit pairs from different sources and the value of bits within the H1 and B2 cannot be pre-determined. However, the VSC9295 can be used as a deslicing device for a fabric of VSC9295 devices, so the bits within H1 is filled according to their position within the byte. Therefore, the uppermost bit pair in the outgoing byte should contain the uppermost two bits of the 0x68 or 0x60 value.

Table 12. Code Setting and Domain for Functions

Code	Function	Domain
FF	AIS	0
FE	SDH UNEQ	0
FD	SONET UNEQ	0
FC	PRBS/USERPAT	0
F7	AIS	1
F6	SDH UNEQ	1
F5	SONET UNEQ	1
F4	PRBS/USERPAT	1

2.7.9 Generated Pattern Insertion

For diagnostic purposes and test applications, the TSI is able to insert either a PRBS pattern or a user-defined pattern. A 2^{23}–1 pattern is used for the PRBS pattern. The user-defined pattern can be of a programmable length, varying from 1 to 12 bytes.

The PRBS pattern is continuously running at the system clock frequency. The user-defined pattern is stored in USERPAT and will repeat itself every PATLEN bytes. PATSEL selects between PRBS and user-defined pattern modes.

Since this function resides in the special frame generator block, the selection and pattern apply for a range of outputs. Furthermore, no provision is made to have groups of outputs related to each other; each group of outputs may have a PRBS pattern in a different state.

To route test data to an output time slot, the appropriate TSIAxxyC[7:0] should have a value 0xFC (channel 252, which does not exist) for frame domain 0, and 0xF4 (channel 244) for domain 1 (if used).

Each channel uses only a predetermined SFG block. There are eight sections to the switch core. For each section, there are two SFG blocks, one for each frame domain (in case split frame domains are used). If split frame domains are used, both SFG blocks for each core section must be programmed by the user.

The outputs are allocated to SFG blocks as shown in Table 13, page 54.

Table 13. SFG Block Outputs

SFG Block	Associated Outputs
SFG 0/1	TxD 0, 1, 4, 5, 8, 9, 12, 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33
SFG 2/3	TxD 2, 3, 6, 7, 10, 11, 14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35
SFG 4/5	TxD 68, 69, 72, 73, 76, 77, 80, 81, 84, 85, 88, 89, 92, 93, 96, 97, 100, 101
SFG 6/7	TxD 70, 71, 74, 75, 78, 79, 82, 83, 86, 87, 90, 91, 94, 95, 98, 99, 102, 103
SFG 8/9	TxD 36, 37, 40, 41, 44, 45, 48, 49, 52, 53, 56, 57, 60, 61, 64, 65
SFG 10/11	TxD 38, 39, 42, 43, 46, 47, 50, 51, 54, 55, 58, 59, 62, 63, 66, 67
SFG 12/13	TxD 104, 105, 108, 109, 112, 113, 116, 117, 120, 121, 124, 125, 128, 129, 132, 133
SFG 14/15	TxD 106, 107, 110, 111, 114, 115, 118, 119, 122, 123, 126, 127, 130, 131, 134, 135

2.7.10 TSI Configuration Change

External to the device, there are two methods of invoking a transfer from the Standby Configuration Maps to the Active Maps:

- CPU access
- A pulse on an external pin of the device

Both of these methods result in a pulse on the newcfg pin of the TSI core. This asynchronous pulse is treated as a request to transfer the standby map to the active map at the next A1/A2 boundary. Note that because the register transfer occurs at the A1/A2 boundary, the resulting first 45 A1 positions of the resulting frame in which the transfer occurs (if used for user data) is that of the old programming state.

When a slice is in Transparent mode, the request on new_cfg is processed immediately without regard to the frame boundary. Note that since one core block can contain two independent slices, and the transparency could be set differently on each.

2.7.11 Memory Integrity Check

This feature gives early indication and localization of a connection failure due to the upset of a bit in the active configuration map, which may occur due to external factors such as alpha particle impacts. On a TSI configuration change, the even parity of the bits in each configuration word is computed and stored in the associated bit TSIAxxyP.

Each bank's parity register, TSIxxyP is constantly and asynchronously compared to the parity of register bank y, and if a discrepancy arises, the MEMPARERRy bit for the slice is set. Any change of MEMPARERRy is signalled by raising MEMPARERRDy, which generates an interrupt unless masked by MEMPARRERRMy. The location of the error is encoded and placed in PARERRyLOC[5:0] with straight binary encoding. If no parity error exists, PARERRyLOC[5:0] is set to 0x1F. Memory parity checking is disabled during a configuration change and for three clock cycles afterward.

Parity errors are ignored in register banks that are not used in the device's operational mode. For example, in HHBS1 mode, register banks 2 and 3 are not used, and parity errors in these banks do not trigger the MEMPARERR2 or MEMPARERR3 signals. All parity is ignored in Transparent mode. In these modes, the PARERRyLOC bits and TSIAxxyP bits are still active and can be read.

The purpose of MEMPARERRy is to indicate an upset of a connection map bit by an external event. A single occurrence of MEMPARERRy = 1 does not indicate a permanent defect in the device, but represents a soft error, such as might be caused by an alpha particle impact or a power supply event that exceeds the recommended operating conditions. Program firmware to respond to MEMPARERRy as follows:

1. Use PARERRyLOC[5:0] to identify the connection map register that was affected.
2. If the polling of MEMPARERRy was used as the detection method, read MEMPARERRDy to clear the interrupt bit. This step is not required if MEMPARERRDy was used as the detection method.
3. Compare the active and the standby map contents for the register indicated by PARERRyLOC[5:0].
4. Record whether the map contents are different and log the event as a connection map register upset (if the contents do not match) or a parity bit upset (if the contents still match).
5. Perform a standby-to-active transfer using a NEWCFG register write or the newcfg pin to refresh the active map.
6. Resume normal operation. If traffic was interrupted by a real connection map register upset on an active STS-1, traffic should now be restored.

Repeated MEMPARERRy occurrences at the same register location or a failure to clear the MEMPARERRy or MEMPARERRDy bit after executing the procedure may indicate something other than a random soft error. The system should switch to a protection card and indicate to an operator that the card on which the error was observed needs intervention, such as further diagnostics.

2.7.12 Reset State

On power-up, or if a reset is executed, the TSI defaults to having all outputs in UNEQ_SDH mode, corresponding to having TSIAxxyC reset to 0xFE. Each register also defaults to sending time slot 5, bitslice 0, corresponding to TSIAxxyS set to 0x05 and TSIAxxyN set to 0x0.

2.8 Low-Speed Backplane Receiver

A block diagram of the BPRx is shown in the following figure.

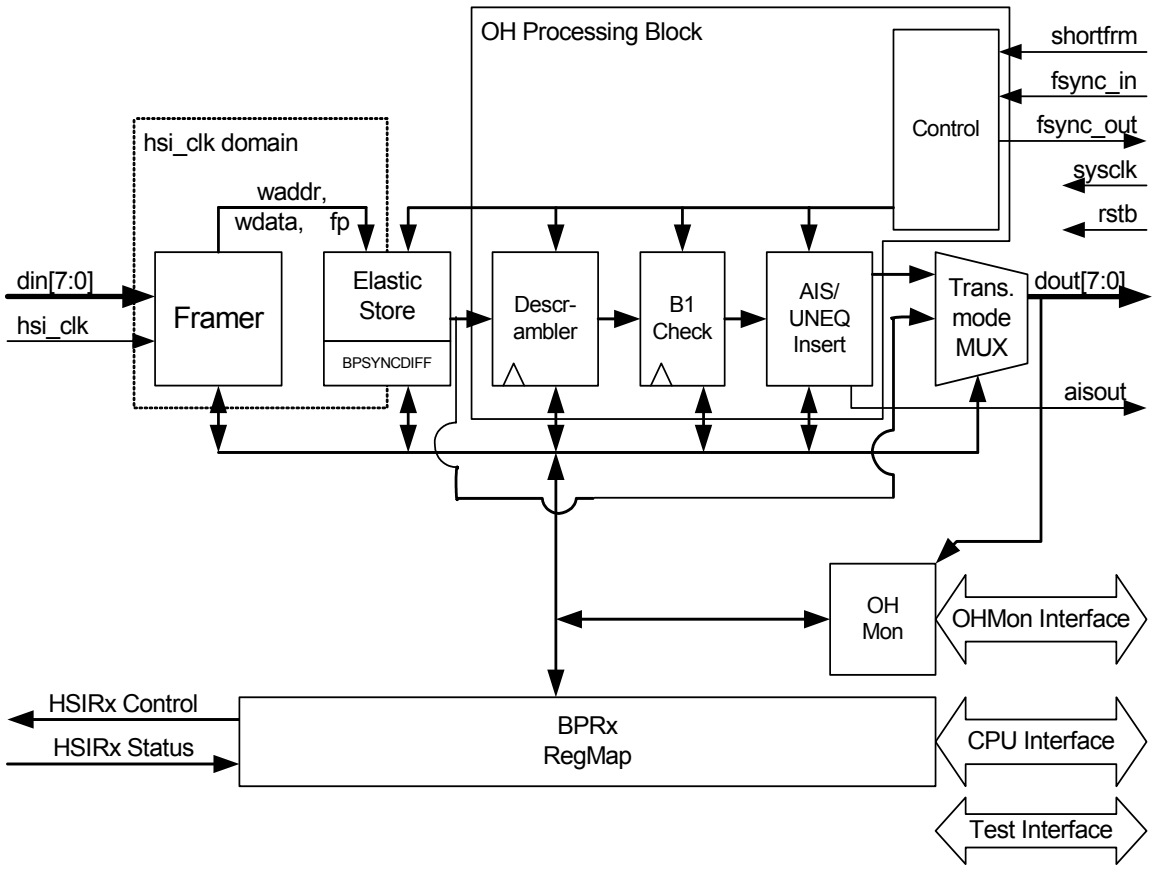


Figure 28. BPRx Block Diagram

The data input to the block consists of a 2.488–2.6 Gbps data stream demultiplexed to byte wide data at a clock rate of 311–312.5 MHz. The interface also handles data originating from an STS-12 formatted input at 622 Mbps, which is pre-formatted by the associated HSIRx block to look like an STS-48 frame where

four consecutive copies of each STS-12 appear. Transparent mode passes the received data and clock to the output without manipulation. There is no frame alignment to a central sync pulse required in this mode.

When receiving TFI-5 data (SONET STS-48-like frames) or pre-formatted STS-12 data, the input data to each port goes to an internal framer, which byte aligns and frames on an 8-bit data input. The framer then delivers the newly byte aligned and addressed data to the elastic store. Data from the elastic store is optionally de-scrambled and B1 parity is checked on the output data. Control generates the timing control signals for the other functions in the device. The control block is synchronized to the reference sync from the frame sync filter. In addition, the backplane receiver interface can be provisioned to monitor 99 bytes (3 individual bytes plus 3 groups of 16 bytes plus one set of 48 bytes) corresponding to various row and column overhead locations selectable by the user. The backplane receiver interface generates out of frame (OOF) status, a B1 error indication, loss of signal (LOS) status, and out of alignment (OOA) status which are accessible to the user through the CPU interface. Status and control for the associated HSIRx block are also accessed using the BPRx register map.

2.8.1 Frame Formats

The BPRx supports three frame formats:

- TFI-5 frames, STS-48-like frames at a line rate of 2.488 Gbps with 9 rows of 90 columns of 48 time slots
- STS12 frames which are formatted as STS48 frames with four copies of each byte activated with the STS12SEL bit
- Short frames for fast verification and functional test, 2 rows of 6 columns of 48 time slots (Vitesse use only, activated by the SHORTFRM pin

2.8.2 Out-of-Frame Detection (OOF)

Frame alignment for TFI-5 frames is found by searching for the 32-bit pattern 0xF6F62828 in the A1, A2 byte locations of the 2.488 Gbps input signal. The in-frame state is entered when two valid framing patterns have been detected with 125 us spacing. The OOF state is entered if the incoming signal has five consecutive framing patterns with errors. It is possible to configure the device to do quick-framing, that is. the detection of one correct pattern causing a transition to the in-frame state and the detection of one incorrect pattern causing a transition to the OOF state, by setting the control register bit QFR. The OOF state, delta and mask bits are available through the CPU interface register bits OOF, OOFD and OOFM respectively.

2.8.3 Frame Offset Detection

The status register BPSYNCDIFF[15:0], can be used to determine the number of clock cycles from the extracted frame sync to the internal frame sync as an aid for systems that need to adjust the frame boundary position arriving at the input. This count will start at extracted frame pulse (retimed to the core clock domain) and a snapshot will be taken at the internal frame sync and made available to the CPU interface. Sometimes when moving the position of the internal frame sync (by changing BPOFFSET or FM_SEL) or when switching between TFI-5 and STS12 modes, it is necessary to perform a FIFO reset by asserting and then de-asserting the FIFORESET bit in a BPRx to re-initialize the BPSYNCDIFF measurement.

2.8.4 Elastic Store

The elastic store is 96 bytes deep and used to frame align the input data to the core frame domain and hand it off to the core clock domain. The store holds the data until the port can be frame synchronized. The worst case skew between an input port and the selected frame sync (either the external line sync or the frame sync position from the selected internal port framer) can be ± 150.4 ns (± 47 bytes) at the TFI-5/STS-48

rate. The write pointer (driven by the framer and hsi_clk) and the read pointer (driven by the Control block and core clock) is compared to produce an indication as to when the FIFO has overflowed or underflowed during normal operation (after framing has occurred). These conditions are signalled by the ESOFLOW and ESUFLOW bits. Interrupts are generated by the associates ESOFLOWD and ESUFLOWD delta bits, which are masked by ESOFLOWM and ESUFLOWM respectively.

It should be noted that in STS12 mode the de-skew window is delayed by 9.6 ns. This makes the window delay in STS12 mode +160/–140.8 ns with reference to the window in STS48 mode. The available de-skew window for mixed STS48/STS12 operation (where both windows overlap) is thus +150.4/–140.8 ns. This is simplified to ±140 ns elsewhere in the document.

2.8.5 Out-Of-Alignment (OOA) Detection

If skew of the port from the 'nominal' frame sync position is greater than the specified maximum skew, the data corresponding to that port read out from the elastic store will not be frame-aligned. If the value of BYSYNCDIFF is such that ESOFLOW or ESUFLOW is set, then the Out-Of-Alignment alarm (OOA) is declared. The alarm is cleared when the value of BPSYNCDIFF is within the allowed window. The delta and mask bits associated with the state bit OOA are OOAD and OOAM respectively.

2.8.6 Transparent Mode

In transparent mode, the received data are passed to the output without manipulation, but the elastic store is still used to absorb wander on the input. This means that a valid framing pattern must still be present within the data. This mode is enabled by setting the BPRXTRNSPNT bit, or asserting the *trnspntmod* control pin.

In transparent-thru mode the data is passed directly from the input to the output of the BPRX with no intervention by the framer. This is done by setting both the BPRXTHRU bit and BPRXTRNSPNT bit. This mode should be used for passing non-SONET/TFI-5 data.

2.8.7 Section Error Monitoring (B1)

The B1 byte implements a BIP-8 error code using even parity which is computed over all bits of the previous frame after scrambling and is placed in bytes B1 of the current frame before scrambling. The BIP-8 error code is calculated for every incoming frame and compared with the extracted B1 error code from the following incoming frame. B1 errors are accumulated over 1 to 32 frames specified by the B1 frame count register, B1FRMCNT[4:0]. If the total exceeds the maximum count programmed into the threshold register, B1ERRTH[5:0], the B1 Error event B1ERRE is set for the corresponding port. The associated mask bit is B1ERRM. In STS12 mode, parity calculation is only done on every fourth byte.

2.8.8 De-Scrambling

The incoming data stream is de-scrambled with the generating polynomial PN7 = $1 + x^6 + x^7$ with sequence length 127. The bytes A1, A2, J0/Z0 are not de-scrambled. It is possible to disable de-scrambling on each port using the control bit BPDSCRINH. In STS12 mode de-scrambling is only done on every fourth byte.

2.8.9 LOS Detection

If a provisioned port experiences *n* bytes with no bit transitions prior to de-scrambling, a loss of signal indication (LOS) is asserted. The value of *n* is programmable by means of the LOSTXCNT bits to a value of 256, 512 or 1024 consecutive bits (rounded to the nearest higher multiple of 8). The LOS will be reset to 0 on the presence of input bit transitions. A port experiencing LOS will set the AIS code only during the

LOS condition. The LOS state, delta and mask bits are available through the CPU interface register bits LOS, LOSD and LOSM respectively.

LOS will also OR in the effect of RXLOS in case (for whatever reason) the RXLOS condition does not force an LOS to occur.

2.8.10 Unequipped Port

The provisioning register bit (UNEQ) can be set to disable an unused input port. An unequipped port zero fills all bytes except the A1, A2 and H1 bytes. The H1 bytes is replaced with the hex value 68h.

2.8.11 AIS Insertion

AIS is automatically inserted into the downstream data port when the OOF, LOS, or OOA state is active. The AIS insertion is inhibited when the control bit BPAISINH is set for that group. The control bit FBPAIS may be used to force AIS into the data exiting the BPRx block by setting it to 1. FBPAIS takes priority over BPAISINH.

When OOF, LOS or OOA is active, the aisout pin is set to logic '1'. This will drive an optional RDI_L indication on the transmit channel with the same number. This occurs regardless of the state of BPAISINH.

2.8.12 HSIRx Control and Monitoring

The BPRx register map contains control and status bits for its associated HSIRx.

The RXEQCTRL[3:0] bits set the equalization mode of the HSIRx input receiver. The RXTERMCTL bit controls the input termination mode of the HSIRx. The threshold for the signal-strength based LOS function in HSIRx is set by RXLOSTH[1:0].

The HSIRx also returns status bits for loss-of-lock (RXLOL, RXLOLHI, RXLOL), loss of signal (RXLOS) and loss of reference (RXNOREF). There are associated delta and mask bits RXLOLD/RXLOLM and RXLOSD/RXLOSM. Since a NOREF condition forces an RXLOL to occur, there are no associated delta or mask bits.

In addition, four general-purpose control bits and four general-purpose status bits connected to the HSIRx are provided for test, diagnostic, and debug purposes. These are called RXGPC[7:0] and RXGPS[7:0].

2.9 Low-Speed Backplane Transmitter

A block diagram of the BPTx is shown in the following figure.

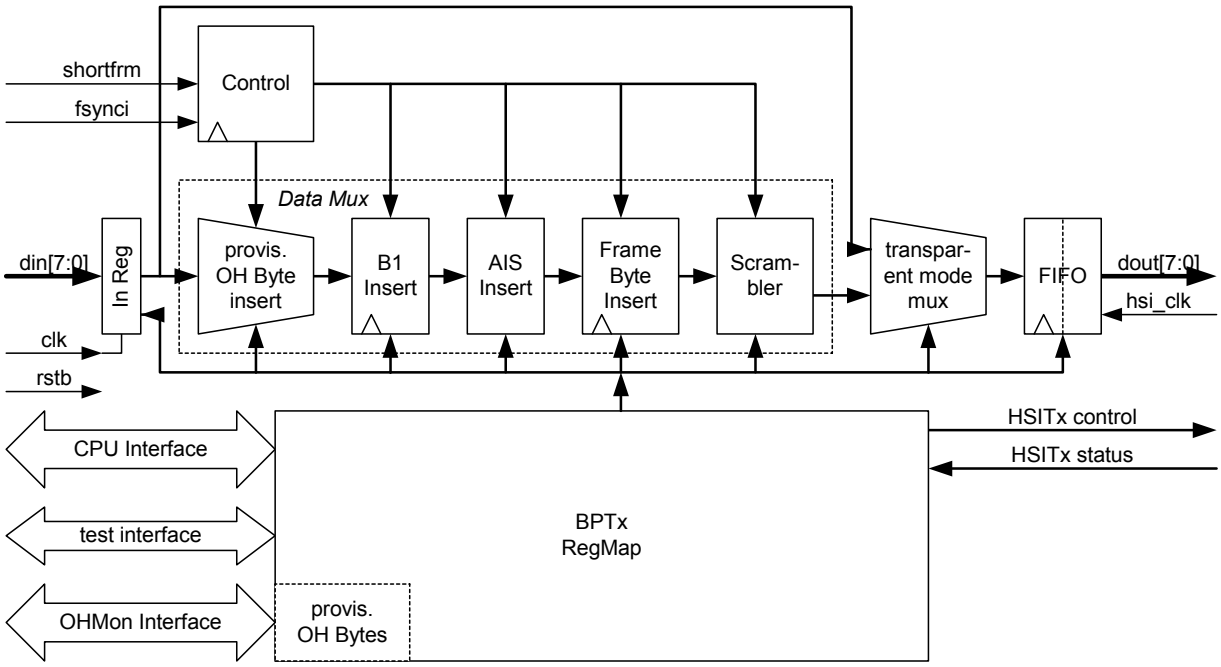


Figure 29. BPTx Block Diagram

The low-speed backplane transmitter interface prepares the outgoing data for transfer over the backplane prior to serialization by the HSITx. The BPTx adds parity bytes, framing bytes, and performs scrambling on the outgoing data stream. The outgoing data stream may be formatted in a OC48 like format (basic TFI-5 frame), with two extra columns, or the data may be passed through transparently in transparent mode to handle other formats.

When STS-12 mode is set, scrambling and parity insertion are adjusted accordingly, and the data is reformatted by mapping the first byte of each set of four consecutive bytes onto four bytes by producing for consecutive copies of each bit.

In the case of TFI-5 frames, only the last three A1 bytes, first three A2 bytes and the first B1 byte are actively used. The other SONET section and line overhead bytes may be passed through. The BPTx may also insert AIS and insert parity or framing errors for system test purposes. Functions of the HSITx requiring configuration and status bits are accessed by means of the register map contained in the BPTx. A FIFO is provided at the output to absorb clock skew and jitter in opaque mode.

2.9.1 Section BIP-8 (B1) and Error Insertion

For TFI-5 frames, the BIP-8 parity information is computed for all bits in the previous frame (after scrambling) and placed in the B1 byte of the current frame before scrambling. The B1 parity calculation can be inhibited for the channel by setting the B1CALCB bit to a 1. If B1CALCB is low, the received B1 byte is passed transparently to the output. In STS-12 Mode (STS12SEL=1), the calculation is only performed on the first byte out of every four, prior to reformatting.

One bit B1 error can be inserted in bit 7 by setting control bits B1ERRINS.

2.9.2 Framing Bytes (A1A2) and Error Insertion

When the channel is passing TFI-5 data format, the framing bytes (A1A2) of data pattern 0xF628 is inserted into the frame and overwrite the bytes delivered from the core of the device that may contain errors. To comply with the TFI-5 standard, only the last three A1 bytes and the first three A2 bytes are overwritten. The remaining A1 bytes and A2 bytes are passed transparently.

It is possible to introduce a single bit error in a fixed bit position of the A1A2 framing word (F728) by setting control bit A1A2ERRINS.

2.9.3 Line AIS insertion

When AIS insertion is enabled, the BPTx inserts all ones in the line overhead and payload sections of a frame except the A1A2 and B1 bytes. The J0 bytes and Z0 bytes are filled with a counting pattern commencing at 0x00 and ending at 0x2F to maintain transition density in this unscrambled portion of the frame. By setting the control bit AISINS, the Line AIS is accomplished per port. Note that when AIS is inserted, all A1 bytes and A2 bytes are overwritten rather than the three A1 bytes and three A2 bytes in the previous framing bytes requirement.

In transparent mode, AIS insertion does not operate.

2.9.4 Scrambling

When passing TFI-5 data, the transmit data stream is scrambled using a frame synchronous scrambler using the generating polynomial $1 + x^6 + x^7$. The bytes A1, A2, and J0/Z0 are not scrambled. Scrambling can be inhibited or allowed by changing the BPSCRAMB bit in the register map. In STS-12 mode, scrambling only operates on the first of every four bytes, prior to re-formatting.

2.9.5 Output Port Power-Down

The output HSI ports can be powered down. This is accomplished by setting the control bit BPTXDATINH. Note that the power down control for channel 36 does not shut off the associated HSI port, by design.

2.9.6 BPTx Power Down

Each BPTx can be powered off by setting its SOFTRESET bit. This is to accommodate applications using only a subset of the channels.

2.9.7 Output FIFO

A FIFO is provided at the output to maximize the timing margin when handing off data to the HSITx. The depth is four bytes.

This FIFO may need to be independently reset after an interruption of the reference clock because the clock multiplier in HSITx may need time to relock and may overflow or underflow the FIFO. A register map bit FIFORESET is provided for this purpose. This is also needed after powering off and on the associated HSITx using the BPTXDATINH bit, and also when switching between TFI-5 and STS12 modes using the STS12SEL bit.

2.9.8 HSITx Control and Monitoring

The BPTx register map contains control and status bits for its associated HSITx.

The TXEQCTRL[2:0] bits set the equalization mode of the HSITx output driver. The TXDRIVE bit controls the output amplitude setting of the HSITx. In addition, eight general-purpose control bits and

eight general-purpose status bits connected to the HSITx are provided for test, diagnostic, and debug purposes. These are called TXGPC[7:0] and TXGPS[7:0].

2.9.9 Variable Frame Length

The device allows three frame sizes:

- STS-48 frame (basic TFI-5 frame), 9 rows by 90 columns by 48 STS-1 bytes or 38880 bytes, with a duration of 125 microseconds at the serial bit rate of 2.488 Gbps
- STS-12 frame, which appears at the input of BPTx as an STS-48 frame, and at the output appears as a 4x over-sampled frame of 9 rows by 90 columns by 12 STS-1 bytes with a duration of 125 microseconds
- The short frame mode for rapid verification and testing of the device, 2 rows by 6 columns by 48 STS-1 bytes or 576 bytes

The selection of the frame length is controlled by external pin shortfrm.

2.9.10 Transparent Mode

The BPTx has an optional transparent mode where the data is not altered in any way and is passed directly to the HSI. Transparent mode is used to pass any data other than TFI-5 data.

In Transparent mode, no data is overwritten.

2.9.11 RDI_L Signaling

The BPTx is able to insert RDI_L to signal back to the sending card that the corresponding BPTx received data containing errors. If the RDIE bit is set, on receipt of a signal from the correspondingly numbered BPRx block, the bottom three LSBs of the first K2 byte (fifth row, third column of the frame) is forced to 000. This feature overwrites these bits in the K2 byte regardless of AIS insertion using the AISINS bit or any insertion of overhead bytes (BPIB, XBI or XXBI).

2.10 High-Speed Interface Receiver

The HSIRx receives serial data at 2.488 Gbps, recovers clock using a local clock recovery loop, deserializes the data to eight bits wide, and presents the data and associated byte clock to the core of the device. An optional STS-12 mode allows reception of data and clock recovery at 622.08 Mbps. This results in four consecutive identical bytes being presented to the core at the normal core clock rate.

Lock detection and signal strength detection functions are included. The HSIRx uses a reference clock to center the VCO frequency in the absence of data.

2.10.1 Data Transmission

The HSIRx receives data at transfer rates from 2.488 Gbps and 622.08 Mbps (as selected by the STS12SEL bit in the associated BPRx register map). Regardless of the selected range, the entire device must operate at the same data rate.

2.10.2 High-Speed Bit Clock Recovery

The HSIRx recovers a high-speed bit clock suitable for retiming and deserializing the incoming serial data. The sampling point (active clock edge) is optimized as shown in the following figure.

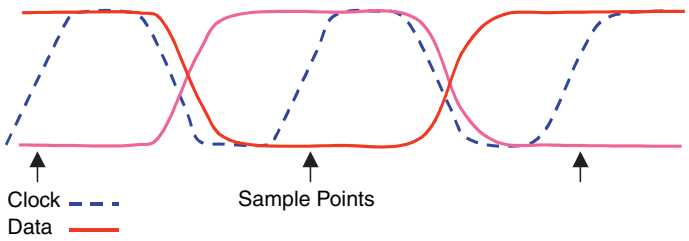


Figure 30. Data Sampling Diagram

The bit clock is derived using a low-power local clock recovery circuit in each HSIRx.

2.10.3 Consecutive Identical Digit Tolerance

The clock recovery function is tolerant to consecutive identical digits (CID) as found in SONET scrambled data. The jitter tolerance specifications is maintained in the presence of occasional 72-bit CID events.

2.10.4 Jitter Transfer Bandwidth and Peaking

The loop bandwidth (LBW) of the embedded clock recovery unit does not exceed 30 MHz under any conditions of process, temperature, supply voltage or data pattern, and does not exceed 8 MHz for 622 Mbps operation. The transfer function has a gain of –10 dB or lower at the reference clock frequency. The peak gain of the transfer function does not exceed +1 dB. The jitter transfer function must be below the mask shown in the following figure. The loop bandwidth is globally adjustable by controlling the filter, the charge pump current and the charge pump pulse width by means of the PLL_LBW register bits in the General Configuration registers.

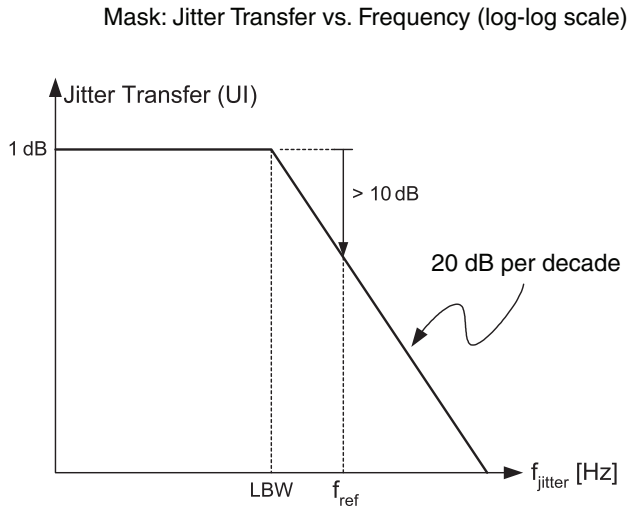


Figure 31. Jitter Transfer Mask

2.10.5 Jitter Tolerance

The clock and data recovery function meets or exceeds (be higher than) the mask shown in the following table. The upper limit (T_{JLFin}) is determined by the depth of the elastic store in BPRx rather than by any property of the clock recovery.

Table 14. Values for Jitter Tolerance Mask

Parameter	Value
T_{JLFin}	750 UI p-p
T_{JHFin} (EQ off)	0.4 UI p-p
T_{JHFin} (EQ on)	0.7 UI p-p
f_1	1.58 kHz
f_2	3 MHz

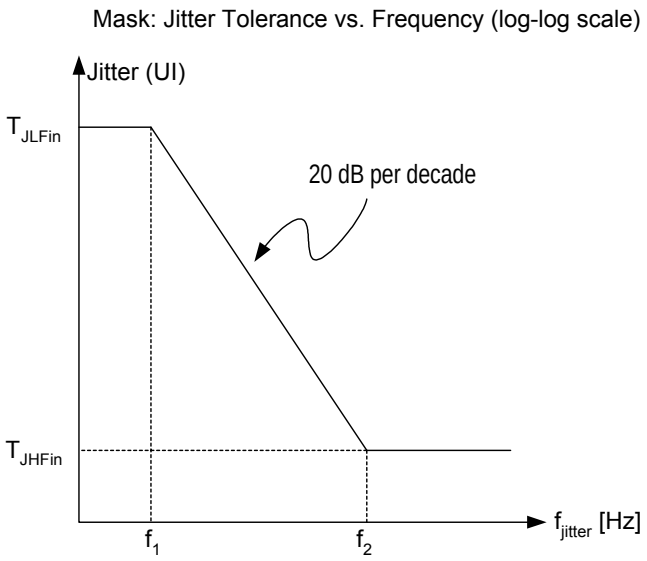


Figure 32. Jitter Tolerance Mask

2.10.6 Reference Frequency

The local clock recovery utilizes an external reference frequency to center the VCO in the absence of data to within 2000 ppm of the expected data frequency when no data is present at the input. This is provided on the refclkp/n pins. The reference clock can be at 1/8th, 1/16th or 1/32nd of the data rate. This ratio can be selected with refsel[1:0] and 1/16th represents the typical application.

2.10.7 Lock Detection and Hold-in

The HSIRx detects the frequency difference between the divided recovered clock and the reference clock and produce an indication of whether the two are within some tolerance of each other, and whether the divided recovered clock is above or below the reference clock. When it is above, it is signaled on lolhi and when it is below, it is signaled on lollo. The lol output is the logic OR of lolhi and lollo. These indications are available by means of the RXLOL, RXLOLHI, and RXLOLLO bits in the associated BPRx register map.

When the VCO frequency begins or drifts outside the lock detector threshold, the PLL locks to the reference before attempting to lock to the incoming data.

This operation may be overridden for test purposes using the fr_da (RXGPC[3]) and fc_ck (RXGPC[2]) signals for each channel. The fr_ck (RXGPC[2]) signal forces the VCO to lock to the reference frequency, and the fr_da (RXGPC[3]) signal forces the data-driven phase detector to remain engaged. The tolerance on the lock detection is selectable using the ppm[1:0] (RXGPC[1:0]) signals as shown in the following table.

Table 15. Lock Detector Tolerance Settings

RXPGC[1:0]	Assert Lock	De-Assert Lock
00	1000 ppm	8000 ppm
01	1000 ppm	16000 ppm
10	2000 ppm	16000 ppm
11	1000 ppm	8000 ppm

2.10.8 Loss of Reference Detection

When the selected reference frequency does not toggle within four cycles of the divided recovered clock, a loss of reference is declared on the noref output. This indication is available by means of the RXNOREF bit in the associated BPRx register map

2.10.9 Low-Speed Byte Clock

The 311 MHz low-speed data clock is derived from the 2.5 GHz or the recovered bit clock by dividing said clock by eight (inherent in the 1:8 demultiplexer). In 622 Mbps operation, a 311 MHz clock is still provided.

2.10.10 Serial-to-Parallel Conversion

The 8-bit bus going to the device internal core at 311 Mbps is derived by serial-to-parallel conversion of the Rx data channel at 2.5 Gbps or 622 Mbps. For detailed information, see "STS-12 Mode," page 66.

2.10.11 Serial-to-Parallel Converter Bit Order

The data bit ordering is as shown in the following figure.

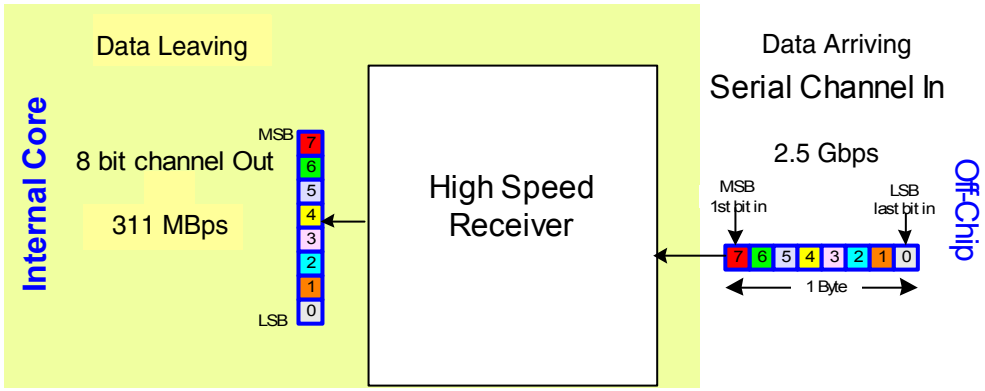


Figure 33. Backplane Receiver Multiplexer Function at 2.5 Gbps

2.10.12 STS-12 Mode

When the STS12SEL pin is asserted by a signal from the associated BPRx block, the HSIRx divides the recovered clock by four and centers the recovered clock in the 622 Mbps eye. The deserialized data is presented to the core as four consecutive identical bytes with an associated 311 MHz clock.

2.10.13 Asynchronous Reset of Deserializers

The deserializers have an asynchronous reset control for low-speed test purposes that puts the internal divider into a known state. This control is driven by the Master Reset.

2.10.14 PLL Bypass

The VSC9295 supports a mode of operation in which the PLL does not operate, and the clock on refclkp/n is used as the bit clock for low-speed test. This mode is engaged when pllbyp is high.

2.10.15 Input Receiver

Level Compatibility

The input receiver is compatible with the TFI-5/SFI-5 electrical specifications. In addition, the input cell accepts AC-coupled data, for which an internal bias network is included.

Input Receiver Equalization

The input receiver has the capability of providing optional equalization to counteract the non-ideal characteristics of electronic media or components that may occur in the signal path. It may not be necessary to use any equalization for 622 Mbps signals.The amount of equalization is controlled by the rxeqctrl[3:0] as shown in the following table. The settings are somewhat system-dependent, and the user is responsible to select the correct setting for their application. The RXEQCTRL bits are in the associated BPRx register map.

Table 16. RXEQCTRL Settings

rxeqctrl[3:0]	Minimum Trace [meters]	Maximum Trace [meters]
0000'b	0	0.125
0001'b	0.125	0.375
0010'b		
0011'b		
0101'b	0.375	0.625
0110'b		
0111'b		
1001'b	0.625	0.875
1010'b		
1011'b		
1101'b	0.875	1.0 or higher
1110'b		
1111'b		
Other codes	Unused	

Input Receiver Termination

The input receiver has two termination modes: 50 Ω to the 1.2 V supply on each pin or a floating 100 Ω between the true and complement input pins. In the floating mode, the center point of said termination is AC bypassed to ground on-chip to reduce common-mode reflections. This is controlled by means of the RXTERMCTL bit in the associated BPRx register map. Setting RXTERMCTL=1 forces termination to the 1.2 V supply.

Signal Strength Detection

The input receiver can detect when no signal is present at its input. When the input signal amplitude drops below a threshold set by losth[1:0], the LOS output is asserted. This indication is made available using the RXLOS bit in the associate BPRx register map. The threshold value is set by the RXLOSTH bits in the associate BPRx register map. The expected threshold ranges are shown in the following table.

Table 17. LOS Threshold Settings

losth[1:0]	Set Below (Typical Threshold Values)	Clear Above (Typical Threshold Values)	Comments
00	N/A	N/A	LOS disabled
01	15 mV	70 mV	Single-ended peak-to-peak
10	60 mV	100 mV	Single-ended peak-to-peak
11	95 mV	150 mV	Single-ended peak-to-peak

2.10.16 JTAG Boundary Scan Support

The HSIRx supports JTAG boundary scan such that the signal at the input pads may be observed with the on-chip JTAG test access port.

2.10.17 Power Control

Individual channels are capable of being powered off using their poweroff pins. For convenience, the chipsize pins may be used to power down predefined sets of channels.

2.11 High-Speed Interface Transmitter

Each channel of HSITx receives 8-bit parallel data and a reference clock, creates a serial bit clock at 2.488 GHz to 2.67 GHz using a clock multiplier phase-locked loop, serializes the data and transmits it off-chip by means of the output driver. A byte clock is sent to the core to drive a FIFO that returns the input parallel data. Lock detection for the PLL is included. Operation at 622.08 MBps is supported by pre-formatting the associated BPTx block.

2.11.1 Data Transmission

The HSITx transmits data at transfer rates of 2.488 Gbps and 622.08 MBps.

2.11.2 High-Speed Bit Clock Generation

The HSITx creates a high-speed bit clock suitable for driving the serializer and transmitting serial data from it.

2.11.3 Reference Frequency

The CMU locks to an external reference frequency. This is provided on the tfi_refclkp/n pins. The reference clock can be at 1/8th, 1/16th or 1/32nd of the data rate. This ratio can be selected with refsel[1:0] and 1/16th represents the typical application.

2.11.4 Lock Detection

The HSITx detects the frequency difference between the divided recovered clock dclko and the reference clock and produce an indication of whether the two are within some tolerance of each other, and whether dclko is above or below the reference clock. When it is above, it is signalled on lolhi and when it is below, it is signalled on lollo. The lol output is the logic OR of lolhi and lollo.

2.11.5 Loss of Reference Detection

When refclk does not toggle within four cycles of dclko, a loss of reference is declared on the noref output. This indication is available by means of TXGPS bit 0 in the associated BPTx register map.

2.11.6 Parallel-to-Serial Conversion

The 8-bit bus coming from internal core at 311 MBps is parallel-to-serial converted to a serial Tx data channel at 2.5 Gbps.

2.11.7 Parallel-to-Serial Converter Bit Order

The data bit ordering is shown in Figure 34.

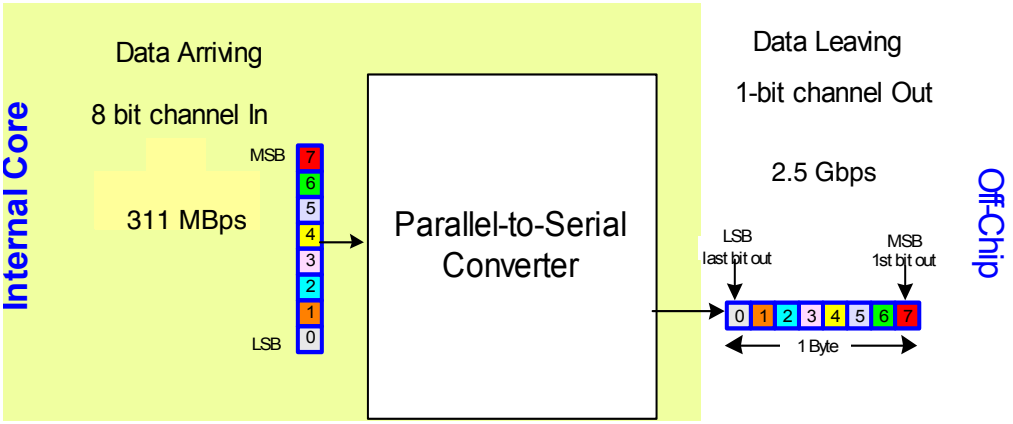


Figure 34. Backplane Transmitter Multiplexer Function at 2.5 Gbps

2.11.8 Low-Speed Byte Clock

The 311 MHz low-speed data clock is derived from the 2.5 GHz bit clock by dividing said clock by eight (inherent in the 1:8 multiplexer). The low-speed data is sampled on the rising edge of the low-speed byte clock.

2.11.9 Asynchronous Reset of Serializer

The serializer has an asynchronous reset control for low-speed test purposes that puts the internal divider into a known state. This control is driven by the master reset.

2.11.10 PLL Bypass

The VSC9295 also supports a mode in which the PLL does not operate, and the clock on bypclk is used as the bit clock for low-speed test. This mode is engaged when pllbyp is high.

2.11.11 Output Driver

The output driver is compatible with the TFI-5/SFI-5 electrical specifications. It has the capability of providing optional equalization as a means to counteract the non-ideal characteristics of electronic media or components that may occur in the signal path. It may not be necessary to use this feature for data at 622 Mbps. The amount of equalization is controlled by the drivectrl and eqctrl[2:0] bits as shown in Table 18, page 70. The amplitude and amount of equalization is controlled by the drivectl and eqctrl[2:0] bits for each channel. The settings will be somewhat system-dependent, and the user is responsible to select the correct setting for their application.

These controls are accessed using the DRIVECTL and TXEQCTRL bits in the associated BPTx register map. The control codes in the following table are the four-bit codes formed by DRIVECTRL and TXEQCTRL[2:0].

Table 18. Drive and Pre-Emphasis Settings

DRIVECTL and EQCTL[2:0]			
Control Code Decimal	**Control Code Binary**	**Output Effect**	
0	0000	Nominal drive	No pre-emphasis
1	0001	Mid drive	No pre-emphasis
2	0010	High drive	No pre-emphasis
3	0011	High drive	No pre-emphasis
4	0100	Low pre-emphasis	Short decay
5	0101	Medium pre-emphasis	Short decay
6	0110	High pre-emphasis	Short decay
7	0111	Extra high pre-emphasis	Short decay
8	1000	Low pre-emphasis	Long decay
9	1001	Medium pre-emphasis	Long decay
10	1010	High pre-emphasis	Long decay
11	1011	Extra high pre-emphasis	Long decay
12	1100	Low pre-emphasis	Medium decay
13	1101	Medium pre-emphasis	Medium decay
14	1110	High pre-emphasis	Medium decay
15	1111	Extra high pre-emphasis	Medium decay

2.11.12 Output Driver Back-Termination

The output driver has a DC output impedance of 50 Ω to the 1.2 V supply.

2.11.13 JTAG Boundary Scan Support

The HSITx supports JTAG boundary scan such that the signal at the output pads may be forced using the on-chip JTAG test access port.

2.11.14 Power Control

Individual channels are capable of being powered off using their poweroff pins. For convenience, the chipsize pins may be used to power down predefined sets of channels.

3 Registers

3.1 Memory Map

Base addresses are listed in four-digit format (from 0x0000 to 0xFFFF) instead of six-digit format.

Table 19. VSC9295 Memory Map

Base Address (Hex)	Size (Words)	Block	Base Address (Hex)	Size (Words)	Block
0x0000	512	TSI Slices 0/1	0x5A00	512	TSI Slices 90/91
0x0200	512	TSI Slices 2/3	0x5C00	512	TSI Slices 92/93
0x0400	512	TSI Slices 4/5	0x5E00	512	TSI Slices 94/95
0x0600	512	TSI Slices 6/7	0x6000	512	TSI Slices 96/97
0x0800	512	TSI Slices 8/9	0x6200	512	TSI Slices 98/99
0x0A00	512	TSI Slices 10/11	0x6400	512	TSI Slices 100/101
0x0C00	512	TSI Slices 12/13	0x6600	512	TSI Slices 102/103
0x0E00	512	TSI Slices 14/15	0x6800	512	TSI Slices 104/105
0x1000	512	TSI Slices 16/17	0x6A00	512	TSI Slices 106/107
0x1200	512	TSI Slices 18/19	0x6C00	512	TSI Slices 108/109
0x1400	512	TSI Slices 20/21	0x6E00	512	TSI Slices 110/111
0x1600	512	TSI Slices 22/23	0x7000	512	TSI Slices 112/113
0x1800	512	TSI Slices 24/25	0x7200	512	TSI Slices 114/115
0x1A00	512	TSI Slices 26/27	0x7400	512	TSI Slices 116/117
0x1C00	512	TSI Slices 28/29	0x7600	512	TSI Slices 118/119
0x1E00	512	TSI Slices 30/31	0x7800	512	TSI Slices 120/121
0x2000	512	TSI Slices 32/33	0x7A00	512	TSI Slices 122/123
0x2200	512	TSI Slices 34/35	0x7C00	512	TSI Slices 124/125
0x2400	512	TSI Slices 36/37	0x7E00	512	TSI Slices 126/127
0x2600	512	TSI Slices 38/39	0x8000	512	TSI Slices 128/129
0x2800	512	TSI Slices 40/41	0x8200	512	TSI Slices 130/131
0x2A00	512	TSI Slices 42/43	0x8400	512	TSI Slices 132/133
0x2C00	512	TSI Slices 44/45	0x8600	512	TSI Slices 134/135
0x2E00	512	TSI Slices 46/47	0x9000	64	BPRx 0
0x3000	512	TSI Slices 48/49	0x9040	64	BPRx 1
0x3200	512	TSI Slices 50/51	0x9080	64	BPRx 2
0x3400	512	TSI Slices 52/53	0x90C0	64	BPRx 3
0x3600	512	TSI Slices 54/55	0x9100	64	BPRx 4
0x3800	512	TSI Slices 56/57	0x9140	64	BPRx 5
0x3A00	512	TSI Slices 58/59	0x9180	64	BPRx 6
0x3C00	512	TSI Slices 60/61	0x91C0	64	BPRx 7
0x3E00	512	TSI Slices 62/63	0x9200	64	BPRx 8

Table 19. VSC9295 Memory Map *(continued)*

Base Address (Hex)	Size (Words)	Block	Base Address (Hex)	Size (Words)	Block
0x4000	512	TSI Slices 64/65	0x9240	64	BPRx 9
0x4200	512	TSI Slices 66/67	0x9280	64	BPRx 10
0x4400	512	TSI Slices 68/69	0x92C0	64	BPRx 11
0x4600	512	TSI Slices 70/71	0x9300	64	BPRx 12
0x4800	512	TSI Slices 72/73	0x9340	64	BPRx 13
0x4A00	512	TSI Slices 74/75	0x9380	64	BPRx 14
0x4C00	512	TSI Slices 76/77	0x93C0	64	BPRx 15
0x4E00	512	TSI Slices 78/79	0x9400	64	BPRx 16
0x5000	512	TSI Slices 80/81	0x9440	64	BPRx 17
0x5200	512	TSI Slices 82/83	0x9480	64	BPRx 18
0x5400	512	TSI Slices 84/85	0x94C0	64	BPRx 19
0x5600	512	TSI Slices 86/87	0x9500	64	BPRx 20
0x5800	512	TSI Slices 88/89	0x9540	64	BPRx 21
0x9580	64	BPRx 22	0xA280	64	BPRx 74
0x95C0	64	BPRx 23	0xA2C0	64	BPRx 75
0x9600	64	BPRx 24	0xA300	64	BPRx 76
0x9640	64	BPRx 25	0xA340	64	BPRx 77
0x9680	64	BPRx 26	0xA380	64	BPRx 78
0x96C0	64	BPRx 27	0xA3C0	64	BPRx 79
0x9700	64	BPRx 28	0xA400	64	BPRx 80
0x9740	64	BPRx 29	0xA440	64	BPRx 81
0x9780	64	BPRx 30	0xA480	64	BPRx 82
0x97C0	64	BPRx 31	0xA4C0	64	BPRx 83
0x9800	64	BPRx 32	0xA500	64	BPRx 84
0x9840	64	BPRx 33	0xA540	64	BPRx 85
0x9880	64	BPRx 34	0xA580	64	BPRx 86
0x98C0	64	BPRx 35	0xA5C0	64	BPRx 87
0x9900	64	BPRx 36	0xA600	64	BPRx 88
0x9940	64	BPRx 37	0xA640	64	BPRx 89
0x9980	64	BPRx 38	0xA680	64	BPRx 90
0x99C0	64	BPRx 39	0xA6C0	64	BPRx 91
0x9A00	64	BPRx 40	0xA700	64	BPRx 92
0x9A40	64	BPRx 41	0xA740	64	BPRx 93
0x9A80	64	BPRx 42	0xA780	64	BPRx 94
0x9AC0	64	BPRx 43	0xA7C0	64	BPRx 95
0x9B00	64	BPRx 44	0xA800	64	BPRx 96
0x9B40	64	BPRx 45	0xA840	64	BPRx 97
0x9B80	64	BPRx 46	0xA880	64	BPRx 98
0x9BC0	64	BPRx 47	0xA8C0	64	BPRx 99
0x9C00	64	BPRx 48	0xA900	64	BPRx 100
0x9C40	64	BPRx 49	0xA940	64	BPRx 101

Table 19. VSC9295 Memory Map *(continued)*

Base Address (Hex)	Size (Words)	Block	Base Address (Hex)	Size (Words)	Block
0x9C80	64	BPRx 50	0xA980	64	BPRx 102
0x9CC0	64	BPRx 51	0xA9C0	64	BPRx 103
0x9D00	64	BPRx 52	0xAA00	64	BPRx 104
0x9D40	64	BPRx 53	0xAA40	64	BPRx 105
0x9D80	64	BPRx 54	0xAA80	64	BPRx 106
0x9DC0	64	BPRx 55	0xAAC0	64	BPRx 107
0x9E00	64	BPRx 56	0xAB00	64	BPRx 108
0x9E40	64	BPRx 57	0xAB40	64	BPRx 109
0x9E80	64	BPRx 58	0xAB80	64	BPRx 110
0x9EC0	64	BPRx 59	0xABC0	64	BPRx 111
0x9F00	64	BPRx 60	0xAC00	64	BPRx 112
0x9F40	64	BPRx 61	0xAC40	64	BPRx 113
0x9F80	64	BPRx 62	0xAC80	64	BPRx 114
0x9FC0	64	BPRx 63	0xACC0	64	BPRx 115
0xA000	64	BPRx 64	0xAD00	64	BPRx 116
0xA040	64	BPRx 65	0xAD40	64	BPRx 117
0xA080	64	BPRx 66	0xAD80	64	BPRx 118
0xA0C0	64	BPRx 67	0xADC0	64	BPRx 119
0xA100	64	BPRx 68	0xAE00	64	BPRx 120
0xA140	64	BPRx 69	0xAE40	64	BPRx 121
0xA180	64	BPRx 70	0xAE80	64	BPRx 122
0xA1C0	64	BPRx 71	0xAEC0	64	BPRx 123
0xA200	64	BPRx 72	0xAF00	64	BPRx 124
0xA240	64	BPRx 73	0xAF40	64	BPRx 125
0xAF80	64	BPRx 126	0xCD00	128	BPTx 42
0xAFC0	64	BPRx 127	0xCD80	128	BPTx 43
0xB000	64	BPRx 128	0xCE00	128	BPTx 44
0xB040	64	BPRx 129	0xCE80	128	BPTx 45
0xB080	64	BPRx 130	0xCF00	128	BPTx 46
0xB0C0	64	BPRx 131	0xCF80	128	BPTx 47
0xB100	64	BPRx 132	0xD000	128	BPTx 48
0xB140	64	BPRx 133	0xD080	128	BPTx 49
0xB180	64	BPRx 134	0xD100	128	BPTx 50
0xB1C0	64	BPRx 135	0xD180	128	BPTx 51
0xB800	128	BPTx 0	0xD200	128	BPTx 52
0xB880	128	BPTx 1	0xD280	128	BPTx 53
0xB900	128	BPTx 2	0xD300	128	BPTx 54
0xB980	128	BPTx 3	0xD380	128	BPTx 55
0xBA00	128	BPTx 4	0xD400	128	BPTx 56
0xBA80	128	BPTx 5	0xD480	128	BPTx 57
0xBB00	128	BPTx 6	0xD500	128	BPTx 58

Table 19. VSC9295 Memory Map *(continued)*

Base Address (Hex)	Size (Words)	Block	Base Address (Hex)	Size (Words)	Block
0xBB80	128	BPTx 7	0xD580	128	BPTx 59
0xBC00	128	BPTx 8	0xD600	128	BPTx 60
0xBC80	128	BPTx 9	0xD680	128	BPTx 61
0xBD00	128	BPTx 10	0xD700	128	BPTx 62
0xBD80	128	BPTx 11	0xD780	128	BPTx 63
0xBE00	128	BPTx 12	0xD800	128	BPTx 64
0xBE80	128	BPTx 13	0xD880	128	BPTx 65
0xBF00	128	BPTx 14	0xD900	128	BPTx 66
0xBF80	128	BPTx 15	0xD980	128	BPTx 67
0xC000	128	BPTx 16	0xDA00	128	BPTx 68
0xC080	128	BPTx 17	0xDA80	128	BPTx 69
0xC100	128	BPTx 18	0xDB00	128	BPTx 70
0xC180	128	BPTx 19	0xDB80	128	BPTx 71
0xC200	128	BPTx 20	0xDC00	128	BPTx 72
0xC280	128	BPTx 21	0xDC80	128	BPTx 73
0xC300	128	BPTx 22	0xDD00	128	BPTx 74
0xC380	128	BPTx 23	0xDD80	128	BPTx 75
0xC400	128	BPTx 24	0xDE00	128	BPTx 76
0xC480	128	BPTx 25	0xDE80	128	BPTx 77
0xC500	128	BPTx 26	0xDF00	128	BPTx 78
0xC580	128	BPTx 27	0xDF80	128	BPTx 79
0xC600	128	BPTx 28	0xE000	128	BPTx 80
0xC680	128	BPTx 29	0xE080	128	BPTx 81
0xC700	128	BPTx 30	0xE100	128	BPTx 82
0xC780	128	BPTx 31	0xE180	128	BPTx 83
0xC800	128	BPTx 32	0xE200	128	BPTx 84
0xC880	128	BPTx 33	0xE280	128	BPTx 85
0xC900	128	BPTx 34	0xE300	128	BPTx 86
0xC980	128	BPTx 35	0xE380	128	BPTx 87
0xCA00	128	BPTx 36	0xE400	128	BPTx 88
0xCA80	128	BPTx 37	0xE480	128	BPTx 89
0xCB00	128	BPTx 38	0xE500	128	BPTx 90
0xCB80	128	BPTx 39	0xE580	128	BPTx 91
0xCC00	128	BPTx 40	0xE600	128	BPTx 92
0xCC80	128	BPTx 41	0xE680	128	BPTx 93
0xE700	128	BPTx 94	0xF600	128	BPTx 124
0xE780	128	BPTx 95	0xF680	128	BPTx 125
0xE800	128	BPTx 96	0xF700	128	BPTx 126
0xE880	128	BPTx 97	0xF780	128	BPTx 127
0xE900	128	BPTx 98	0xF800	128	BPTx 128
0xE980	128	BPTx 99	0xF880	128	BPTx 129

Table 19. VSC9295 Memory Map *(continued)*

Base Address (Hex)	Size (Words)	Block	Base Address (Hex)	Size (Words)	Block
0xEA00	128	BPTx 100	0xF900	128	BPTx 130
0xEA80	128	BPTx 101	0xF980	128	BPTx 131
0xEB00	128	BPTx 102	0xFA00	128	BPTx 132
0xEB80	128	BPTx 103	0xFA80	128	BPTx 133
0xEC00	128	BPTx 104	0xFB00	128	BPTx 134
0xEC80	128	BPTx 105	0xFB80	128	BPTx 135
0xED00	128	BPTx 106	0xFF58	8	TSI SFG Block 0
0xED80	128	BPTx 107	0xFF60	8	TSI SFG Block 1
0xEE00	128	BPTx 108	0xFF68	8	TSI SFG Block 2
0xEE80	128	BPTx 109	0xFF70	8	TSI SFG Block 3
0xEF00	128	BPTx 110	0xFF78	8	TSI SFG Block 4
0xEF80	128	BPTx 111	0xFF80	8	TSI SFG Block 5
0xF000	128	BPTx 112	0xFF88	8	TSI SFG Block 6
0xF080	128	BPTx 113	0xFF90	8	TSI SFG Block 7
0xF100	128	BPTx 114	0xFF98	8	TSI SFG Block 8
0xF180	128	BPTx 115	0xFFA0	8	TSI SFG Block 9
0xF200	128	BPTx 116	0xFFA8	8	TSI SFG Block 10
0xF280	128	BPTx 117	0xFFB0	8	TSI SFG Block 11
0xF300	128	BPTx 118	0xFFB8	8	TSI SFG Block 12
0xF380	128	BPTx 119	0xFFC0	8	TSI SFG Block 13
0xF400	128	BPTx 120	0xFFC8	8	TSI SFG Block 14
0xF480	128	BPTx 121	0xFFD0	8	TSI SFG Block 15
0xF500	128	BPTx 122	0xFFD8	8	SyncMan Registers
0xF580	128	BPTx 123	0xFFE0	32	General Configuration Registers

3.2 TSI Register Map

Each TSI slice has a 512-word address space located at the base addresses shown in the master memory map.

Table 20. TSI Register Map

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
Standby Connection Map, Bank 0 (R/W)									
0x000	:FE	TSIS000C-7	TSIS000C-6	TSIS000C-5	TSIS000C-4	TSIS000C-3	TSIS000C-2	TSIS000C-1	TSIS000C-0
continued	:00	TSIS000N-1	TSIS000N-0	TSIS000S-5	TSIS000S-4	TSIS000S-3	TSIS000S-2	TSIS000S-1	TSIS000S-0
0x001	:FE	TSIS010C-7	TSIS010C-6	TSIS010C-5	TSIS010C-4	TSIS010C-3	TSIS010C-2	TSIS010C-1	TSIS010C-0
continued	:00	TSIS010N-1	TSIS010N-0	TSIS010S-5	TSIS010S-4	TSIS010S-3	TSIS010S-2	TSIS010S-1	TSIS010S-0
0x002	:FE	TSIS020C-7	TSIS020C-6	TSIS020C-5	TSIS020C-4	TSIS020C-3	TSIS020C-2	TSIS020C-1	TSIS020C-0
continued	:00	TSIS020N-1	TSIS020N-0	TSIS020S-5	TSIS020S-4	TSIS020S-3	TSIS020S-2	TSIS020S-1	TSIS020S-0
0x003	:FE	TSIS030C-7	TSIS030C-6	TSIS030C-5	TSIS030C-4	TSIS030C-3	TSIS030C-2	TSIS030C-1	TSIS030C-0
continued	:00	TSIS030N-1	TSIS030N-0	TSIS030S-5	TSIS030S-4	TSIS030S-3	TSIS030S-2	TSIS030S-1	TSIS030S-0
0x004	:FE	TSIS040C-7	TSIS040C-6	TSIS040C-5	TSIS040C-4	TSIS040C-3	TSIS040C-2	TSIS040C-1	TSIS040C-0
continued	:00	TSIS040N-1	TSIS040N-0	TSIS040S-5	TSIS040S-4	TSIS040S-3	TSIS040S-2	TSIS040S-1	TSIS040S-0
0x005	:FE	TSIS050C-7	TSIS050C-6	TSIS050C-5	TSIS050C-4	TSIS050C-3	TSIS050C-2	TSIS050C-1	TSIS050C-0
continued	:00	TSIS050N-1	TSIS050N-0	TSIS050S-5	TSIS050S-4	TSIS050S-3	TSIS050S-2	TSIS050S-1	TSIS050S-0
0x006	:FE	TSIS060C-7	TSIS060C-6	TSIS060C-5	TSIS060C-4	TSIS060C-3	TSIS060C-2	TSIS060C-1	TSIS060C-0
continued	:00	TSIS060N-1	TSIS060N-0	TSIS060S-5	TSIS060S-4	TSIS060S-3	TSIS060S-2	TSIS060S-1	TSIS060S-0
0x007	:FE	TSIS070C-7	TSIS070C-6	TSIS070C-5	TSIS070C-4	TSIS070C-3	TSIS070C-2	TSIS070C-1	TSIS070C-0
continued	:00	TSIS070N-1	TSIS070N-0	TSIS070S-5	TSIS070S-4	TSIS070S-3	TSIS070S-2	TSIS070S-1	TSIS070S-0
0x008	:FE	TSIS080C-7	TSIS080C-6	TSIS080C-5	TSIS080C-4	TSIS080C-3	TSIS080C-2	TSIS080C-1	TSIS080C-0
continued	:00	TSIS080N-1	TSIS080N-0	TSIS080S-5	TSIS080S-4	TSIS080S-3	TSIS080S-2	TSIS080S-1	TSIS080S-0
0x009	:FE	TSIS090C-7	TSIS090C-6	TSIS090C-5	TSIS090C-4	TSIS090C-3	TSIS090C-2	TSIS090C-1	TSIS090C-0
continued	:00	TSIS090N-1	TSIS090N-0	TSIS090S-5	TSIS090S-4	TSIS090S-3	TSIS090S-2	TSIS090S-1	TSIS090S-0
0x00A	:FE	TSIS100C-7	TSIS100C-6	TSIS100C-5	TSIS100C-4	TSIS100C-3	TSIS100C-2	TSIS100C-1	TSIS100C-0
continued	:00	TSIS100N-1	TSIS100N-0	TSIS100S-5	TSIS100S-4	TSIS100S-3	TSIS100S-2	TSIS100S-1	TSIS100S-0
0x00B	:FE	TSIS110C-7	TSIS110C-6	TSIS110C-5	TSIS110C-4	TSIS110C-3	TSIS110C-2	TSIS110C-1	TSIS110C-0
continued	:00	TSIS110N-1	TSIS110N-0	TSIS110S-5	TSIS110S-4	TSIS110S-3	TSIS110S-2	TSIS110S-1	TSIS110S-0
0x00C	:FE	TSIS120C-7	TSIS120C-6	TSIS120C-5	TSIS120C-4	TSIS120C-3	TSIS120C-2	TSIS120C-1	TSIS120C-0
continued	:00	TSIS120N-1	TSIS120N-0	TSIS120S-5	TSIS120S-4	TSIS120S-3	TSIS120S-2	TSIS120S-1	TSIS120S-0
0x00D	:FE	TSIS130C-7	TSIS130C-6	TSIS130C-5	TSIS130C-4	TSIS130C-3	TSIS130C-2	TSIS130C-1	TSIS130C-0
continued	:00	TSIS130N-1	TSIS130N-0	TSIS130S-5	TSIS130S-4	TSIS130S-3	TSIS130S-2	TSIS130S-1	TSIS130S-0
0x00E	:FE	TSIS140C-7	TSIS140C-6	TSIS140C-5	TSIS140C-4	TSIS140C-3	TSIS140C-2	TSIS140C-1	TSIS140C-0
continued	:00	TSIS140N-1	TSIS140N-0	TSIS140S-5	TSIS140S-4	TSIS140S-3	TSIS140S-2	TSIS140S-1	TSIS140S-0
0x00F	:FE	TSIS150C-7	TSIS150C-6	TSIS150C-5	TSIS150C-4	TSIS150C-3	TSIS150C-2	TSIS150C-1	TSIS150C-0
continued	:00	TSIS150N-1	TSIS150N-0	TSIS150S-5	TSIS150S-4	TSIS150S-3	TSIS150S-2	TSIS150S-1	TSIS150S-0
0x010	:FE	TSIS160C-7	TSIS160C-6	TSIS160C-5	TSIS160C-4	TSIS160C-3	TSIS160C-2	TSIS160C-1	TSIS160C-0
continued	:00	TSIS160N-1	TSIS160N-0	TSIS160S-5	TSIS160S-4	TSIS160S-3	TSIS160S-2	TSIS160S-1	TSIS160S-0
0x011	:FE	TSIS170C-7	TSIS170C-6	TSIS170C-5	TSIS170C-4	TSIS170C-3	TSIS170C-2	TSIS170C-1	TSIS170C-0
continued	:00	TSIS170N-1	TSIS170N-0	TSIS170S-5	TSIS170S-4	TSIS170S-3	TSIS170S-2	TSIS170S-1	TSIS170S-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
0x012	:FE	TSIS180C-7	TSIS180C-6	TSIS180C-5	TSIS180C-4	TSIS180C-3	TSIS180C-2	TSIS180C-1	TSIS180C-0
continued	:00	TSIS180N-1	TSIS180N-0	TSIS180S-5	TSIS180S-4	TSIS180S-3	TSIS180S-2	TSIS180S-1	TSIS180S-0
0x013	:FE	TSIS190C-7	TSIS190C-6	TSIS190C-5	TSIS190C-4	TSIS190C-3	TSIS190C-2	TSIS190C-1	TSIS190C-0
continued	:00	TSIS190N-1	TSIS190N-0	TSIS190S-5	TSIS190S-4	TSIS190S-3	TSIS190S-2	TSIS190S-1	TSIS190S-0
0x014	:FE	TSIS200C-7	TSIS200C-6	TSIS200C-5	TSIS200C-4	TSIS200C-3	TSIS200C-2	TSIS200C-1	TSIS200C-0
continued	:00	TSIS200N-1	TSIS200N-0	TSIS200S-5	TSIS200S-4	TSIS200S-3	TSIS200S-2	TSIS200S-1	TSIS200S-0
0x015	:FE	TSIS210C-7	TSIS210C-6	TSIS210C-5	TSIS210C-4	TSIS210C-3	TSIS210C-2	TSIS210C-1	TSIS210C-0
continued	:00	TSIS210N-1	TSIS210N-0	TSIS210S-5	TSIS210S-4	TSIS210S-3	TSIS210S-2	TSIS210S-1	TSIS210S-0
0x016	:FE	TSIS220C-7	TSIS220C-6	TSIS220C-5	TSIS220C-4	TSIS220C-3	TSIS220C-2	TSIS220C-1	TSIS220C-0
continued	:00	TSIS220N-1	TSIS220N-0	TSIS220S-5	TSIS220S-4	TSIS220S-3	TSIS220S-2	TSIS220S-1	TSIS220S-0
0x017	:FE	TSIS230C-7	TSIS230C-6	TSIS230C-5	TSIS230C-4	TSIS230C-3	TSIS230C-2	TSIS230C-1	TSIS230C-0
continued	:00	TSIS230N-1	TSIS230N-0	TSIS230S-5	TSIS230S-4	TSIS230S-3	TSIS230S-2	TSIS230S-1	TSIS230S-0
0x018	:FE	TSIS240C-7	TSIS240C-6	TSIS240C-5	TSIS240C-4	TSIS240C-3	TSIS240C-2	TSIS240C-1	TSIS240C-0
continued	:00	TSIS240N-1	TSIS240N-0	TSIS240S-5	TSIS240S-4	TSIS240S-3	TSIS240S-2	TSIS240S-1	TSIS240S-0
0x019	:FE	TSIS250C-7	TSIS250C-6	TSIS250C-5	TSIS250C-4	TSIS250C-3	TSIS250C-2	TSIS250C-1	TSIS250C-0
continued	:00	TSIS250N-1	TSIS250N-0	TSIS250S-5	TSIS250S-4	TSIS250S-3	TSIS250S-2	TSIS250S-1	TSIS250S-0
0x01A	:FE	TSIS260C-7	TSIS260C-6	TSIS260C-5	TSIS260C-4	TSIS260C-3	TSIS260C-2	TSIS260C-1	TSIS260C-0
continued	:00	TSIS260N-1	TSIS260N-0	TSIS260S-5	TSIS260S-4	TSIS260S-3	TSIS260S-2	TSIS260S-1	TSIS260S-0
0x01B	:FE	TSIS270C-7	TSIS270C-6	TSIS270C-5	TSIS270C-4	TSIS270C-3	TSIS270C-2	TSIS270C-1	TSIS270C-0
continued	:00	TSIS270N-1	TSIS270N-0	TSIS270S-5	TSIS270S-4	TSIS270S-3	TSIS270S-2	TSIS270S-1	TSIS270S-0
0x01C	:FE	TSIS280C-7	TSIS280C-6	TSIS280C-5	TSIS280C-4	TSIS280C-3	TSIS280C-2	TSIS280C-1	TSIS280C-0
continued	:00	TSIS280N-1	TSIS280N-0	TSIS280S-5	TSIS280S-4	TSIS280S-3	TSIS280S-2	TSIS280S-1	TSIS280S-0
0x01D	:FE	TSIS290C-7	TSIS290C-6	TSIS290C-5	TSIS290C-4	TSIS290C-3	TSIS290C-2	TSIS290C-1	TSIS290C-0
continued	:00	TSIS290N-1	TSIS290N-0	TSIS290S-5	TSIS290S-4	TSIS290S-3	TSIS290S-2	TSIS290S-1	TSIS290S-0
0x01E	:FE	TSIS300C-7	TSIS300C-6	TSIS300C-5	TSIS300C-4	TSIS300C-3	TSIS300C-2	TSIS300C-1	TSIS300C-0
continued	:00	TSIS300N-1	TSIS300N-0	TSIS300S-5	TSIS300S-4	TSIS300S-3	TSIS300S-2	TSIS300S-1	TSIS300S-0
0x01F	:FE	TSIS310C-7	TSIS310C-6	TSIS310C-5	TSIS310C-4	TSIS310C-3	TSIS310C-2	TSIS310C-1	TSIS310C-0
continued	:00	TSIS310N-1	TSIS310N-0	TSIS310S-5	TSIS310S-4	TSIS310S-3	TSIS310S-2	TSIS310S-1	TSIS310S-0
0x020	:FE	TSIS320C-7	TSIS320C-6	TSIS320C-5	TSIS320C-4	TSIS320C-3	TSIS320C-2	TSIS320C-1	TSIS320C-0
continued	:00	TSIS320N-1	TSIS320N-0	TSIS320S-5	TSIS320S-4	TSIS320S-3	TSIS320S-2	TSIS320S-1	TSIS320S-0
0x021	:FE	TSIS330C-7	TSIS330C-6	TSIS330C-5	TSIS330C-4	TSIS330C-3	TSIS330C-2	TSIS330C-1	TSIS330C-0
continued	:00	TSIS330N-1	TSIS330N-0	TSIS330S-5	TSIS330S-4	TSIS330S-3	TSIS330S-2	TSIS330S-1	TSIS330S-0
0x022	:FE	TSIS340C-7	TSIS340C-6	TSIS340C-5	TSIS340C-4	TSIS340C-3	TSIS340C-2	TSIS340C-1	TSIS340C-0
continued	:00	TSIS340N-1	TSIS340N-0	TSIS340S-5	TSIS340S-4	TSIS340S-3	TSIS340S-2	TSIS340S-1	TSIS340S-0
0x023	:FE	TSIS350C-7	TSIS350C-6	TSIS350C-5	TSIS350C-4	TSIS350C-3	TSIS350C-2	TSIS350C-1	TSIS350C-0
continued	:00	TSIS350N-1	TSIS350N-0	TSIS350S-5	TSIS350S-4	TSIS350S-3	TSIS350S-2	TSIS350S-1	TSIS350S-0
0x024	:FE	TSIS360C-7	TSIS360C-6	TSIS360C-5	TSIS360C-4	TSIS360C-3	TSIS360C-2	TSIS360C-1	TSIS360C-0
continued	:00	TSIS360N-1	TSIS360N-0	TSIS360S-5	TSIS360S-4	TSIS360S-3	TSIS360S-2	TSIS360S-1	TSIS360S-0
0x025	:FE	TSIS370C-7	TSIS370C-6	TSIS370C-5	TSIS370C-4	TSIS370C-3	TSIS370C-2	TSIS370C-1	TSIS370C-0
continued	:00	TSIS370N-1	TSIS370N-0	TSIS370S-5	TSIS370S-4	TSIS370S-3	TSIS370S-2	TSIS370S-1	TSIS370S-0
0x026	:FE	TSIS380C-7	TSIS380C-6	TSIS380C-5	TSIS380C-4	TSIS380C-3	TSIS380C-2	TSIS380C-1	TSIS380C-0
continued	:00	TSIS380N-1	TSIS380N-0	TSIS380S-5	TSIS380S-4	TSIS380S-3	TSIS380S-2	TSIS380S-1	TSIS380S-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
0x027	:FE	TSIS390C-7	TSIS390C-6	TSIS390C-5	TSIS390C-4	TSIS390C-3	TSIS390C-2	TSIS390C-1	TSIS390C-0
continued	:00	TSIS390N-1	TSIS390N-0	TSIS390S-5	TSIS390S-4	TSIS390S-3	TSIS390S-2	TSIS390S-1	TSIS390S-0
0x028	:FE	TSIS400C-7	TSIS400C-6	TSIS400C-5	TSIS400C-4	TSIS400C-3	TSIS400C-2	TSIS400C-1	TSIS400C-0
continued	:00	TSIS400N-1	TSIS400N-0	TSIS400S-5	TSIS400S-4	TSIS400S-3	TSIS400S-2	TSIS400S-1	TSIS400S-0
0x029	:FE	TSIS410C-7	TSIS410C-6	TSIS410C-5	TSIS410C-4	TSIS410C-3	TSIS410C-2	TSIS410C-1	TSIS410C-0
continued	:00	TSIS410N-1	TSIS410N-0	TSIS410S-5	TSIS410S-4	TSIS410S-3	TSIS410S-2	TSIS410S-1	TSIS410S-0
0x02A	:FE	TSIS420C-7	TSIS420C-6	TSIS420C-5	TSIS420C-4	TSIS420C-3	TSIS420C-2	TSIS420C-1	TSIS420C-0
continued	:00	TSIS420N-1	TSIS420N-0	TSIS420S-5	TSIS420S-4	TSIS420S-3	TSIS420S-2	TSIS420S-1	TSIS420S-0
0x02B	:FE	TSIS430C-7	TSIS430C-6	TSIS430C-5	TSIS430C-4	TSIS430C-3	TSIS430C-2	TSIS430C-1	TSIS430C-0
continued	:00	TSIS430N-1	TSIS430N-0	TSIS430S-5	TSIS430S-4	TSIS430S-3	TSIS430S-2	TSIS430S-1	TSIS430S-0
0x02C	:FE	TSIS440C-7	TSIS440C-6	TSIS440C-5	TSIS440C-4	TSIS440C-3	TSIS440C-2	TSIS440C-1	TSIS440C-0
continued	:00	TSIS440N-1	TSIS440N-0	TSIS440S-5	TSIS440S-4	TSIS440S-3	TSIS440S-2	TSIS440S-1	TSIS440S-0
0x02D	:FE	TSIS450C-7	TSIS450C-6	TSIS450C-5	TSIS450C-4	TSIS450C-3	TSIS450C-2	TSIS450C-1	TSIS450C-0
continued	:00	TSIS450N-1	TSIS450N-0	TSIS450S-5	TSIS450S-4	TSIS450S-3	TSIS450S-2	TSIS450S-1	TSIS450S-0
0x02E	:FE	TSIS460C-7	TSIS460C-6	TSIS460C-5	TSIS460C-4	TSIS460C-3	TSIS460C-2	TSIS460C-1	TSIS460C-0
continued	:00	TSIS460N-1	TSIS460N-0	TSIS460S-5	TSIS460S-4	TSIS460S-3	TSIS460S-2	TSIS460S-1	TSIS460S-0
0x02F	:FE	TSIS470C-7	TSIS470C-6	TSIS470C-5	TSIS470C-4	TSIS470C-3	TSIS470C-2	TSIS470C-1	TSIS470C-0
continued	:00	TSIS470N-1	TSIS470N-0	TSIS470S-5	TSIS470S-4	TSIS470S-3	TSIS470S-2	TSIS470S-1	TSIS470S-0
Invalid Addresses									
0x030-0X03F	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Standby Connection Map, Bank 1 (R/W)									
0x040	:FE	TSIS001C-7	TSIS001C-6	TSIS001C-5	TSIS001C-4	TSIS001C-3	TSIS001C-2	TSIS001C-1	TSIS001C-0
continued	:00	TSIS001N-1	TSIS001N-0	TSIS001S-5	TSIS001S-4	TSIS001S-3	TSIS001S-2	TSIS001S-1	TSIS001S-0
0x041	:FE	TSIS011C-7	TSIS011C-6	TSIS011C-5	TSIS011C-4	TSIS011C-3	TSIS011C-2	TSIS011C-1	TSIS011C-0
continued	:00	TSIS011N-1	TSIS011N-0	TSIS011S-5	TSIS011S-4	TSIS011S-3	TSIS011S-2	TSIS011S-1	TSIS011S-0
0x042	:FE	TSIS021C-7	TSIS021C-6	TSIS021C-5	TSIS021C-4	TSIS021C-3	TSIS021C-2	TSIS021C-1	TSIS021C-0
continued	:00	TSIS021N-1	TSIS021N-0	TSIS021S-5	TSIS021S-4	TSIS021S-3	TSIS021S-2	TSIS021S-1	TSIS021S-0
0x043	:FE	TSIS031C-7	TSIS031C-6	TSIS031C-5	TSIS031C-4	TSIS031C-3	TSIS031C-2	TSIS031C-1	TSIS031C-0
continued	:00	TSIS031N-1	TSIS031N-0	TSIS031S-5	TSIS031S-4	TSIS031S-3	TSIS031S-2	TSIS031S-1	TSIS031S-0
0x044	:FE	TSIS041C-7	TSIS041C-6	TSIS041C-5	TSIS041C-4	TSIS041C-3	TSIS041C-2	TSIS041C-1	TSIS041C-0
continued	:00	TSIS041N-1	TSIS041N-0	TSIS041S-5	TSIS041S-4	TSIS041S-3	TSIS041S-2	TSIS041S-1	TSIS041S-0
0x045	:FE	TSIS051C-7	TSIS051C-6	TSIS051C-5	TSIS051C-4	TSIS051C-3	TSIS051C-2	TSIS051C-1	TSIS051C-0
continued	:00	TSIS051N-1	TSIS051N-0	TSIS051S-5	TSIS051S-4	TSIS051S-3	TSIS051S-2	TSIS051S-1	TSIS051S-0
0x046	:FE	TSIS061C-7	TSIS061C-6	TSIS061C-5	TSIS061C-4	TSIS061C-3	TSIS061C-2	TSIS061C-1	TSIS061C-0
continued	:00	TSIS061N-1	TSIS061N-0	TSIS061S-5	TSIS061S-4	TSIS061S-3	TSIS061S-2	TSIS061S-1	TSIS061S-0
0x047	:FE	TSIS071C-7	TSIS071C-6	TSIS071C-5	TSIS071C-4	TSIS071C-3	TSIS071C-2	TSIS071C-1	TSIS071C-0
continued	:00	TSIS071N-1	TSIS071N-0	TSIS071S-5	TSIS071S-4	TSIS071S-3	TSIS071S-2	TSIS071S-1	TSIS071S-0
0X048	:FE	TSIS081C-7	TSIS081C-6	TSIS081C-5	TSIS081C-4	TSIS081C-3	TSIS081C-2	TSIS081C-1	TSIS081C-0
continued	:00	TSIS081N-1	TSIS081N-0	TSIS081S-5	TSIS081S-4	TSIS081S-3	TSIS081S-2	TSIS081S-1	TSIS081S-0
0x049	:FE	TSIS091C-7	TSIS091C-6	TSIS091C-5	TSIS091C-4	TSIS091C-3	TSIS091C-2	TSIS091C-1	TSIS091C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS091N-1	TSIS091N-0	TSIS091S-5	TSIS091S-4	TSIS091S-3	TSIS091S-2	TSIS091S-1	TSIS091S-0
0x04A	:FE	TSIS101C-7	TSIS101C-6	TSIS101C-5	TSIS101C-4	TSIS101C-3	TSIS101C-2	TSIS101C-1	TSIS101C-0
continued	:00	TSIS101N-1	TSIS101N-0	TSIS101S-5	TSIS101S-4	TSIS101S-3	TSIS101S-2	TSIS101S-1	TSIS101S-0
0x04B	:FE	TSIS111C-7	TSIS111C-6	TSIS111C-5	TSIS111C-4	TSIS111C-3	TSIS111C-2	TSIS111C-1	TSIS111C-0
continued	:00	TSIS111N-1	TSIS111N-0	TSIS111S-5	TSIS111S-4	TSIS111S-3	TSIS111S-2	TSIS111S-1	TSIS111S-0
0x04C	:FE	TSIS121C-7	TSIS121C-6	TSIS121C-5	TSIS121C-4	TSIS121C-3	TSIS121C-2	TSIS121C-1	TSIS121C-0
continued	:00	TSIS121N-1	TSIS121N-0	TSIS121S-5	TSIS121S-4	TSIS121S-3	TSIS121S-2	TSIS121S-1	TSIS121S-0
0x04D	:FE	TSIS131C-7	TSIS131C-6	TSIS131C-5	TSIS131C-4	TSIS131C-3	TSIS131C-2	TSIS131C-1	TSIS131C-0
continued	:00	TSIS131N-1	TSIS131N-0	TSIS131S-5	TSIS131S-4	TSIS131S-3	TSIS131S-2	TSIS131S-1	TSIS131S-0
0x04E	:FE	TSIS141C-7	TSIS141C-6	TSIS141C-5	TSIS141C-4	TSIS141C-3	TSIS141C-2	TSIS141C-1	TSIS141C-0
continued	:00	TSIS141N-1	TSIS141N-0	TSIS141S-5	TSIS141S-4	TSIS141S-3	TSIS141S-2	TSIS141S-1	TSIS141S-0
0x04F	:FE	TSIS151C-7	TSIS151C-6	TSIS151C-5	TSIS151C-4	TSIS151C-3	TSIS151C-2	TSIS151C-1	TSIS151C-0
continued	:00	TSIS151N-1	TSIS151N-0	TSIS151S-5	TSIS151S-4	TSIS151S-3	TSIS151S-2	TSIS151S-1	TSIS151S-0
0x050	:FE	TSIS161C-7	TSIS161C-6	TSIS161C-5	TSIS161C-4	TSIS161C-3	TSIS161C-2	TSIS161C-1	TSIS161C-0
continued	:00	TSIS161N-1	TSIS161N-0	TSIS161S-5	TSIS161S-4	TSIS161S-3	TSIS161S-2	TSIS161S-1	TSIS161S-0
0x051	:FE	TSIS171C-7	TSIS171C-6	TSIS171C-5	TSIS171C-4	TSIS171C-3	TSIS171C-2	TSIS171C-1	TSIS171C-0
continued	:00	TSIS171N-1	TSIS171N-0	TSIS171S-5	TSIS171S-4	TSIS171S-3	TSIS171S-2	TSIS171S-1	TSIS171S-0
0x052	:FE	TSIS181C-7	TSIS181C-6	TSIS181C-5	TSIS181C-4	TSIS181C-3	TSIS181C-2	TSIS181C-1	TSIS181C-0
continued	:00	TSIS181N-1	TSIS181N-0	TSIS181S-5	TSIS181S-4	TSIS181S-3	TSIS181S-2	TSIS181S-1	TSIS181S-0
0x053	:FE	TSIS191C-7	TSIS191C-6	TSIS191C-5	TSIS191C-4	TSIS191C-3	TSIS191C-2	TSIS191C-1	TSIS191C-0
continued	:00	TSIS191N-1	TSIS191N-0	TSIS191S-5	TSIS191S-4	TSIS191S-3	TSIS191S-2	TSIS191S-1	TSIS191S-0
0x054	:FE	TSIS201C-7	TSIS201C-6	TSIS201C-5	TSIS201C-4	TSIS201C-3	TSIS201C-2	TSIS201C-1	TSIS201C-0
continued	:00	TSIS201N-1	TSIS201N-0	TSIS201S-5	TSIS201S-4	TSIS201S-3	TSIS201S-2	TSIS201S-1	TSIS201S-0
0x055	:FE	TSIS211C-7	TSIS211C-6	TSIS211C-5	TSIS211C-4	TSIS211C-3	TSIS211C-2	TSIS211C-1	TSIS211C-0
continued	:00	TSIS211N-1	TSIS211N-0	TSIS211S-5	TSIS211S-4	TSIS211S-3	TSIS211S-2	TSIS211S-1	TSIS211S-0
0x056	:FE	TSIS221C-7	TSIS221C-6	TSIS221C-5	TSIS221C-4	TSIS221C-3	TSIS221C-2	TSIS221C-1	TSIS221C-0
continued	:00	TSIS221N-1	TSIS221N-0	TSIS221S-5	TSIS221S-4	TSIS221S-3	TSIS221S-2	TSIS221S-1	TSIS221S-0
0x057	:FE	TSIS231C-7	TSIS231C-6	TSIS231C-5	TSIS231C-4	TSIS231C-3	TSIS231C-2	TSIS231C-1	TSIS231C-0
continued	:00	TSIS231N-1	TSIS231N-0	TSIS231S-5	TSIS231S-4	TSIS231S-3	TSIS231S-2	TSIS231S-1	TSIS231S-0
0x058	:FE	TSIS241C-7	TSIS241C-6	TSIS241C-5	TSIS241C-4	TSIS241C-3	TSIS241C-2	TSIS241C-1	TSIS241C-0
continued	:00	TSIS241N-1	TSIS241N-0	TSIS241S-5	TSIS241S-4	TSIS241S-3	TSIS241S-2	TSIS241S-1	TSIS241S-0
0x059	:FE	TSIS251C-7	TSIS251C-6	TSIS251C-5	TSIS251C-4	TSIS251C-3	TSIS251C-2	TSIS251C-1	TSIS251C-0
continued	:00	TSIS251N-1	TSIS251N-0	TSIS251S-5	TSIS251S-4	TSIS251S-3	TSIS251S-2	TSIS251S-1	TSIS251S-0
0x05A	:FE	TSIS261C-7	TSIS261C-6	TSIS261C-5	TSIS261C-4	TSIS261C-3	TSIS261C-2	TSIS261C-1	TSIS261C-0
continued	:00	TSIS261N-1	TSIS261N-0	TSIS261S-5	TSIS261S-4	TSIS261S-3	TSIS261S-2	TSIS261S-1	TSIS261S-0
0x05B	:FE	TSIS271C-7	TSIS271C-6	TSIS271C-5	TSIS271C-4	TSIS271C-3	TSIS271C-2	TSIS271C-1	TSIS271C-0
continued	:00	TSIS271N-1	TSIS271N-0	TSIS271S-5	TSIS271S-4	TSIS271S-3	TSIS271S-2	TSIS271S-1	TSIS271S-0
0x05C	:FE	TSIS281C-7	TSIS281C-6	TSIS281C-5	TSIS281C-4	TSIS281C-3	TSIS281C-2	TSIS281C-1	TSIS281C-0
continued	:00	TSIS281N-1	TSIS281N-0	TSIS281S-5	TSIS281S-4	TSIS281S-3	TSIS281S-2	TSIS281S-1	TSIS281S-0
0x05D	:FE	TSIS291C-7	TSIS291C-6	TSIS291C-5	TSIS291C-4	TSIS291C-3	TSIS291C-2	TSIS291C-1	TSIS291C-0
continued	:00	TSIS291N-1	TSIS291N-0	TSIS291S-5	TSIS291S-4	TSIS291S-3	TSIS291S-2	TSIS291S-1	TSIS291S-0
0x05E	:FE	TSIS301C-7	TSIS301C-6	TSIS301C-5	TSIS301C-4	TSIS301C-3	TSIS301C-2	TSIS301C-1	TSIS301C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS301N-1	TSIS301N-0	TSIS301S-5	TSIS301S-4	TSIS301S-3	TSIS301S-2	TSIS301S-1	TSIS301S-0
0x05F	:FE	TSIS311C-7	TSIS311C-6	TSIS311C-5	TSIS311C-4	TSIS311C-3	TSIS311C-2	TSIS311C-1	TSIS311C-0
continued	:00	TSIS311N-1	TSIS311N-0	TSIS311S-5	TSIS311S-4	TSIS311S-3	TSIS311S-2	TSIS311S-1	TSIS311S-0
0x060	:FE	TSIS321C-7	TSIS321C-6	TSIS321C-5	TSIS321C-4	TSIS321C-3	TSIS321C-2	TSIS321C-1	TSIS321C-0
continued	:00	TSIS321N-1	TSIS321N-0	TSIS321S-5	TSIS321S-4	TSIS321S-3	TSIS321S-2	TSIS321S-1	TSIS321S-0
0x061	:FE	TSIS331C-7	TSIS331C-6	TSIS331C-5	TSIS331C-4	TSIS331C-3	TSIS331C-2	TSIS331C-1	TSIS331C-0
continued	:00	TSIS331N-1	TSIS331N-0	TSIS331S-5	TSIS331S-4	TSIS331S-3	TSIS331S-2	TSIS331S-1	TSIS331S-0
0x062	:FE	TSIS341C-7	TSIS341C-6	TSIS341C-5	TSIS341C-4	TSIS341C-3	TSIS341C-2	TSIS341C-1	TSIS341C-0
continued	:00	TSIS341N-1	TSIS341N-0	TSIS341S-5	TSIS341S-4	TSIS341S-3	TSIS341S-2	TSIS341S-1	TSIS341S-0
0x063	:FE	TSIS351C-7	TSIS351C-6	TSIS351C-5	TSIS351C-4	TSIS351C-3	TSIS351C-2	TSIS351C-1	TSIS351C-0
continued	:00	TSIS351N-1	TSIS351N-0	TSIS351S-5	TSIS351S-4	TSIS351S-3	TSIS351S-2	TSIS351S-1	TSIS351S-0
0x064	:FE	TSIS361C-7	TSIS361C-6	TSIS361C-5	TSIS361C-4	TSIS361C-3	TSIS361C-2	TSIS361C-1	TSIS361C-0
continued	:00	TSIS361N-1	TSIS361N-0	TSIS361S-5	TSIS361S-4	TSIS361S-3	TSIS361S-2	TSIS361S-1	TSIS361S-0
0x065	:FE	TSIS371C-7	TSIS371C-6	TSIS371C-5	TSIS371C-4	TSIS371C-3	TSIS371C-2	TSIS371C-1	TSIS371C-0
continued	:00	TSIS371N-1	TSIS371N-0	TSIS371S-5	TSIS371S-4	TSIS371S-3	TSIS371S-2	TSIS371S-1	TSIS371S-0
0x066	:FE	TSIS381C-7	TSIS381C-6	TSIS381C-5	TSIS381C-4	TSIS381C-3	TSIS381C-2	TSIS381C-1	TSIS381C-0
continued	:00	TSIS381N-1	TSIS381N-0	TSIS381S-5	TSIS381S-4	TSIS381S-3	TSIS381S-2	TSIS381S-1	TSIS381S-0
0x067	:FE	TSIS391C-7	TSIS391C-6	TSIS391C-5	TSIS391C-4	TSIS391C-3	TSIS391C-2	TSIS391C-1	TSIS391C-0
continued	:00	TSIS391N-1	TSIS391N-0	TSIS391S-5	TSIS391S-4	TSIS391S-3	TSIS391S-2	TSIS391S-1	TSIS391S-0
0x068	:FE	TSIS401C-7	TSIS401C-6	TSIS401C-5	TSIS401C-4	TSIS401C-3	TSIS401C-2	TSIS401C-1	TSIS401C-0
continued	:00	TSIS401N-1	TSIS401N-0	TSIS401S-5	TSIS401S-4	TSIS401S-3	TSIS401S-2	TSIS401S-1	TSIS401S-0
0x069	:FE	TSIS411C-7	TSIS411C-6	TSIS411C-5	TSIS411C-4	TSIS411C-3	TSIS411C-2	TSIS411C-1	TSIS411C-0
continued	:00	TSIS411N-1	TSIS411N-0	TSIS411S-5	TSIS411S-4	TSIS411S-3	TSIS411S-2	TSIS411S-1	TSIS411S-0
0x06A	:FE	TSIS421C-7	TSIS421C-6	TSIS421C-5	TSIS421C-4	TSIS421C-3	TSIS421C-2	TSIS421C-1	TSIS421C-0
continued	:00	TSIS421N-1	TSIS421N-0	TSIS421S-5	TSIS421S-4	TSIS421S-3	TSIS421S-2	TSIS421S-1	TSIS421S-0
0x06B	:FE	TSIS431C-7	TSIS431C-6	TSIS431C-5	TSIS431C-4	TSIS431C-3	TSIS431C-2	TSIS431C-1	TSIS431C-0
continued	:00	TSIS431N-1	TSIS431N-0	TSIS431S-5	TSIS431S-4	TSIS431S-3	TSIS431S-2	TSIS431S-1	TSIS431S-0
0x06C	:FE	TSIS441C-7	TSIS441C-6	TSIS441C-5	TSIS441C-4	TSIS441C-3	TSIS441C-2	TSIS441C-1	TSIS441C-0
continued	:00	TSIS441N-1	TSIS441N-0	TSIS441S-5	TSIS441S-4	TSIS441S-3	TSIS441S-2	TSIS441S-1	TSIS441S-0
0x06D	:FE	TSIS451C-7	TSIS451C-6	TSIS451C-5	TSIS451C-4	TSIS451C-3	TSIS451C-2	TSIS451C-1	TSIS451C-0
continued	:00	TSIS451N-1	TSIS451N-0	TSIS451S-5	TSIS451S-4	TSIS451S-3	TSIS451S-2	TSIS451S-1	TSIS451S-0
0x06E	:FE	TSIS461C-7	TSIS461C-6	TSIS461C-5	TSIS461C-4	TSIS461C-3	TSIS461C-2	TSIS461C-1	TSIS461C-0
continued	:00	TSIS461N-1	TSIS461N-0	TSIS461S-5	TSIS461S-4	TSIS461S-3	TSIS461S-2	TSIS461S-1	TSIS461S-0
0x06F	:FE	TSIS471C-7	TSIS471C-6	TSIS471C-5	TSIS471C-4	TSIS471C-3	TSIS471C-2	TSIS471C-1	TSIS471C-0
continued	:00	TSIS471N-1	TSIS471N-0	TSIS471S-5	TSIS471S-4	TSIS471S-3	TSIS471S-2	TSIS471S-1	TSIS471S-0
Miscellaneous Control Bits									
0x070	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	TSITRNSPNT0
0x071	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	DOMAIN0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
Invalid Addresses									
0x072-0X07F	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Active Connection Map, Bank 0 (R/O)									
0x080	:FE	TSIA000C-7	TSIA000C-6	TSIA000C-5	TSIA000C-4	TSIA000C-3	TSIA000C-2	TSIA000C-1	TSIA000C-0
continued	:00	TSIA000N-1	TSIA000N-0	TSIA000S-5	TSIA000S-4	TSIA000S-3	TSIA000S-2	TSIA000S-1	TSIA000S-0
0x081	:FE	TSIA010C-7	TSIA010C-6	TSIA010C-5	TSIA010C-4	TSIA010C-3	TSIA010C-2	TSIA010C-1	TSIA010C-0
continued	:00	TSIA010N-1	TSIA010N-0	TSIA010S-5	TSIA010S-4	TSIA010S-3	TSIA010S-2	TSIA010S-1	TSIA010S-0
0x082	:FE	TSIA020C-7	TSIA020C-6	TSIA020C-5	TSIA020C-4	TSIA020C-3	TSIA020C-2	TSIA020C-1	TSIA020C-0
continued	:00	TSIA020N-1	TSIA020N-0	TSIA020S-5	TSIA020S-4	TSIA020S-3	TSIA020S-2	TSIA020S-1	TSIA020S-0
0X083	:FE	TSIA030C-7	TSIA030C-6	TSIA030C-5	TSIA030C-4	TSIA030C-3	TSIA030C-2	TSIA030C-1	TSIA030C-0
continued	:00	TSIA030N-1	TSIA030N-0	TSIA030S-5	TSIA030S-4	TSIA030S-3	TSIA030S-2	TSIA030S-1	TSIA030S-0
0X084	:FE	TSIA040C-7	TSIA040C-6	TSIA040C-5	TSIA040C-4	TSIA040C-3	TSIA040C-2	TSIA040C-1	TSIA040C-0
continued	:00	TSIA040N-1	TSIA040N-0	TSIA040S-5	TSIA040S-4	TSIA040S-3	TSIA040S-2	TSIA040S-1	TSIA040S-0
0X085	:FE	TSIA050C-7	TSIA050C-6	TSIA050C-5	TSIA050C-4	TSIA050C-3	TSIA050C-2	TSIA050C-1	TSIA050C-0
continued	:00	TSIA050N-1	TSIA050N-0	TSIA050S-5	TSIA050S-4	TSIA050S-3	TSIA050S-2	TSIA050S-1	TSIA050S-0
0X086	:FE	TSIA060C-7	TSIA060C-6	TSIA060C-5	TSIA060C-4	TSIA060C-3	TSIA060C-2	TSIA060C-1	TSIA060C-0
continued	:00	TSIA060N-1	TSIA060N-0	TSIA060S-5	TSIA060S-4	TSIA060S-3	TSIA060S-2	TSIA060S-1	TSIA060S-0
0X087	:FE	TSIA070C-7	TSIA070C-6	TSIA070C-5	TSIA070C-4	TSIA070C-3	TSIA070C-2	TSIA070C-1	TSIA070C-0
continued	:00	TSIA070N-1	TSIA070N-0	TSIA070S-5	TSIA070S-4	TSIA070S-3	TSIA070S-2	TSIA070S-1	TSIA070S-0
0X088	:FE	TSIA080C-7	TSIA080C-6	TSIA080C-5	TSIA080C-4	TSIA080C-3	TSIA080C-2	TSIA080C-1	TSIA080C-0
continued	:00	TSIA080N-1	TSIA080N-0	TSIA080S-5	TSIA080S-4	TSIA080S-3	TSIA080S-2	TSIA080S-1	TSIA080S-0
0X089	:FE	TSIA090C-7	TSIA090C-6	TSIA090C-5	TSIA090C-4	TSIA090C-3	TSIA090C-2	TSIA090C-1	TSIA090C-0
continued	:00	TSIA090N-1	TSIA090N-0	TSIA090S-5	TSIA090S-4	TSIA090S-3	TSIA090S-2	TSIA090S-1	TSIA090S-0
0X08A	:FE	TSIA100C-7	TSIA100C-6	TSIA100C-5	TSIA100C-4	TSIA100C-3	TSIA100C-2	TSIA100C-1	TSIA100C-0
continued	:00	TSIA100N-1	TSIA100N-0	TSIA100S-5	TSIA100S-4	TSIA100S-3	TSIA100S-2	TSIA100S-1	TSIA100S-0
0X08B	:FE	TSIA110C-7	TSIA110C-6	TSIA110C-5	TSIA110C-4	TSIA110C-3	TSIA110C-2	TSIA110C-1	TSIA110C-0
continued	:00	TSIA110N-1	TSIA110N-0	TSIA110S-5	TSIA110S-4	TSIA110S-3	TSIA110S-2	TSIA110S-1	TSIA110S-0
0X08C	:FE	TSIA120C-7	TSIA120C-6	TSIA120C-5	TSIA120C-4	TSIA120C-3	TSIA120C-2	TSIA120C-1	TSIA120C-0
continued	:00	TSIA120N-1	TSIA120N-0	TSIA120S-5	TSIA120S-4	TSIA120S-3	TSIA120S-2	TSIA120S-1	TSIA120S-0
0X08D	:FE	TSIA130C-7	TSIA130C-6	TSIA130C-5	TSIA130C-4	TSIA130C-3	TSIA130C-2	TSIA130C-1	TSIA130C-0
continued	:00	TSIA130N-1	TSIA130N-0	TSIA130S-5	TSIA130S-4	TSIA130S-3	TSIA130S-2	TSIA130S-1	TSIA130S-0
0X08E	:FE	TSIA140C-7	TSIA140C-6	TSIA140C-5	TSIA140C-4	TSIA140C-3	TSIA140C-2	TSIA140C-1	TSIA140C-0
continued	:00	TSIA140N-1	TSIA140N-0	TSIA140S-5	TSIA140S-4	TSIA140S-3	TSIA140S-2	TSIA140S-1	TSIA140S-0
0X08F	:FE	TSIA150C-7	TSIA150C-6	TSIA150C-5	TSIA150C-4	TSIA150C-3	TSIA150C-2	TSIA150C-1	TSIA150C-0
continued	:00	TSIA150N-1	TSIA150N-0	TSIA150S-5	TSIA150S-4	TSIA150S-3	TSIA150S-2	TSIA150S-1	TSIA150S-0
0X090	:FE	TSIA160C-7	TSIA160C-6	TSIA160C-5	TSIA160C-4	TSIA160C-3	TSIA160C-2	TSIA160C-1	TSIA160C-0
continued	:00	TSIA160N-1	TSIA160N-0	TSIA160S-5	TSIA160S-4	TSIA160S-3	TSIA160S-2	TSIA160S-1	TSIA160S-0
0X091	:FE	TSIA170C-7	TSIA170C-6	TSIA170C-5	TSIA170C-4	TSIA170C-3	TSIA170C-2	TSIA170C-1	TSIA170C-0
continued	:00	TSIA170N-1	TSIA170N-0	TSIA170S-5	TSIA170S-4	TSIA170S-3	TSIA170S-2	TSIA170S-1	TSIA170S-0
0X092	:FE	TSIA180C-7	TSIA180C-6	TSIA180C-5	TSIA180C-4	TSIA180C-3	TSIA180C-2	TSIA180C-1	TSIA180C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA180N-1	TSIA180N-0	TSIA180S-5	TSIA180S-4	TSIA180S-3	TSIA180S-2	TSIA180S-1	TSIA180S-0
0X093	:FE	TSIA190C-7	TSIA190C-6	TSIA190C-5	TSIA190C-4	TSIA190C-3	TSIA190C-2	TSIA190C-1	TSIA190C-0
continued	:00	TSIA190N-1	TSIA190N-0	TSIA190S-5	TSIA190S-4	TSIA190S-3	TSIA190S-2	TSIA190S-1	TSIA190S-0
0X094	:FE	TSIA200C-7	TSIA200C-6	TSIA200C-5	TSIA200C-4	TSIA200C-3	TSIA200C-2	TSIA200C-1	TSIA200C-0
continued	:00	TSIA200N-1	TSIA200N-0	TSIA200S-5	TSIA200S-4	TSIA200S-3	TSIA200S-2	TSIA200S-1	TSIA200S-0
0X095	:FE	TSIA210C-7	TSIA210C-6	TSIA210C-5	TSIA210C-4	TSIA210C-3	TSIA210C-2	TSIA210C-1	TSIA210C-0
continued	:00	TSIA210N-1	TSIA210N-0	TSIA210S-5	TSIA210S-4	TSIA210S-3	TSIA210S-2	TSIA210S-1	TSIA210S-0
0X096	:FE	TSIA220C-7	TSIA220C-6	TSIA220C-5	TSIA220C-4	TSIA220C-3	TSIA220C-2	TSIA220C-1	TSIA220C-0
continued	:00	TSIA220N-1	TSIA220N-0	TSIA220S-5	TSIA220S-4	TSIA220S-3	TSIA220S-2	TSIA220S-1	TSIA220S-0
0X097	:FE	TSIA230C-7	TSIA230C-6	TSIA230C-5	TSIA230C-4	TSIA230C-3	TSIA230C-2	TSIA230C-1	TSIA230C-0
continued	:00	TSIA230N-1	TSIA230N-0	TSIA230S-5	TSIA230S-4	TSIA230S-3	TSIA230S-2	TSIA230S-1	TSIA230S-0
0X098	:FE	TSIA240C-7	TSIA240C-6	TSIA240C-5	TSIA240C-4	TSIA240C-3	TSIA240C-2	TSIA240C-1	TSIA240C-0
continued	:00	TSIA240N-1	TSIA240N-0	TSIA240S-5	TSIA240S-4	TSIA240S-3	TSIA240S-2	TSIA240S-1	TSIA240S-0
0X099	:FE	TSIA250C-7	TSIA250C-6	TSIA250C-5	TSIA250C-4	TSIA250C-3	TSIA250C-2	TSIA250C-1	TSIA250C-0
continued	:00	TSIA250N-1	TSIA250N-0	TSIA250S-5	TSIA250S-4	TSIA250S-3	TSIA250S-2	TSIA250S-1	TSIA250S-0
0X09A	:FE	TSIA260C-7	TSIA260C-6	TSIA260C-5	TSIA260C-4	TSIA260C-3	TSIA260C-2	TSIA260C-1	TSIA260C-0
continued	:00	TSIA260N-1	TSIA260N-0	TSIA260S-5	TSIA260S-4	TSIA260S-3	TSIA260S-2	TSIA260S-1	TSIA260S-0
0X09B	:FE	TSIA270C-7	TSIA270C-6	TSIA270C-5	TSIA270C-4	TSIA270C-3	TSIA270C-2	TSIA270C-1	TSIA270C-0
continued	:00	TSIA270N-1	TSIA270N-0	TSIA270S-5	TSIA270S-4	TSIA270S-3	TSIA270S-2	TSIA270S-1	TSIA270S-0
0X09C	:FE	TSIA280C-7	TSIA280C-6	TSIA280C-5	TSIA280C-4	TSIA280C-3	TSIA280C-2	TSIA280C-1	TSIA280C-0
continued	:00	TSIA280N-1	TSIA280N-0	TSIA280S-5	TSIA280S-4	TSIA280S-3	TSIA280S-2	TSIA280S-1	TSIA280S-0
0X09D	:FE	TSIA290C-7	TSIA290C-6	TSIA290C-5	TSIA290C-4	TSIA290C-3	TSIA290C-2	TSIA290C-1	TSIA290C-0
continued	:00	TSIA290N-1	TSIA290N-0	TSIA290S-5	TSIA290S-4	TSIA290S-3	TSIA290S-2	TSIA290S-1	TSIA290S-0
0X09E	:FE	TSIA300C-7	TSIA300C-6	TSIA300C-5	TSIA300C-4	TSIA300C-3	TSIA300C-2	TSIA300C-1	TSIA300C-0
continued	:00	TSIA300N-1	TSIA300N-0	TSIA300S-5	TSIA300S-4	TSIA300S-3	TSIA300S-2	TSIA300S-1	TSIA300S-0
0X09F	:FE	TSIA310C-7	TSIA310C-6	TSIA310C-5	TSIA310C-4	TSIA310C-3	TSIA310C-2	TSIA310C-1	TSIA310C-0
continued	:00	TSIA310N-1	TSIA310N-0	TSIA310S-5	TSIA310S-4	TSIA310S-3	TSIA310S-2	TSIA310S-1	TSIA310S-0
0X0A0	:FE	TSIA320C-7	TSIA320C-6	TSIA320C-5	TSIA320C-4	TSIA320C-3	TSIA320C-2	TSIA320C-1	TSIA320C-0
continued	:00	TSIA320N-1	TSIA320N-0	TSIA320S-5	TSIA320S-4	TSIA320S-3	TSIA320S-2	TSIA320S-1	TSIA320S-0
0X0A1	:FE	TSIA330C-7	TSIA330C-6	TSIA330C-5	TSIA330C-4	TSIA330C-3	TSIA330C-2	TSIA330C-1	TSIA330C-0
continued	:00	TSIA330N-1	TSIA330N-0	TSIA330S-5	TSIA330S-4	TSIA330S-3	TSIA330S-2	TSIA330S-1	TSIA330S-0
0X0A2	:FE	TSIA340C-7	TSIA340C-6	TSIA340C-5	TSIA340C-4	TSIA340C-3	TSIA340C-2	TSIA340C-1	TSIA340C-0
continued	:00	TSIA340N-1	TSIA340N-0	TSIA340S-5	TSIA340S-4	TSIA340S-3	TSIA340S-2	TSIA340S-1	TSIA340S-0
0X0A3	:FE	TSIA350C-7	TSIA350C-6	TSIA350C-5	TSIA350C-4	TSIA350C-3	TSIA350C-2	TSIA350C-1	TSIA350C-0
continued	:00	TSIA350N-1	TSIA350N-0	TSIA350S-5	TSIA350S-4	TSIA350S-3	TSIA350S-2	TSIA350S-1	TSIA350S-0
0X0A4	:FE	TSIA360C-7	TSIA360C-6	TSIA360C-5	TSIA360C-4	TSIA360C-3	TSIA360C-2	TSIA360C-1	TSIA360C-0
continued	:00	TSIA360N-1	TSIA360N-0	TSIA360S-5	TSIA360S-4	TSIA360S-3	TSIA360S-2	TSIA360S-1	TSIA360S-0
0X0A5	:FE	TSIA370C-7	TSIA370C-6	TSIA370C-5	TSIA370C-4	TSIA370C-3	TSIA370C-2	TSIA370C-1	TSIA370C-0
continued	:00	TSIA370N-1	TSIA370N-0	TSIA370S-5	TSIA370S-4	TSIA370S-3	TSIA370S-2	TSIA370S-1	TSIA370S-0
0X0A6	:FE	TSIA380C-7	TSIA380C-6	TSIA380C-5	TSIA380C-4	TSIA380C-3	TSIA380C-2	TSIA380C-1	TSIA380C-0
continued	:00	TSIA380N-1	TSIA380N-0	TSIA380S-5	TSIA380S-4	TSIA380S-3	TSIA380S-2	TSIA380S-1	TSIA380S-0
0X0A7	:FE	TSIA390C-7	TSIA390C-6	TSIA390C-5	TSIA390C-4	TSIA390C-3	TSIA390C-2	TSIA390C-1	TSIA390C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA390N-1	TSIA390N-0	TSIA390S-5	TSIA390S-4	TSIA390S-3	TSIA390S-2	TSIA390S-1	TSIA390S-0
0X0A8	:FE	TSIA400C-7	TSIA400C-6	TSIA400C-5	TSIA400C-4	TSIA400C-3	TSIA400C-2	TSIA400C-1	TSIA400C-0
continued	:00	TSIA400N-1	TSIA400N-0	TSIA400S-5	TSIA400S-4	TSIA400S-3	TSIA400S-2	TSIA400S-1	TSIA400S-0
0X0A9	:FE	TSIA410C-7	TSIA410C-6	TSIA410C-5	TSIA410C-4	TSIA410C-3	TSIA410C-2	TSIA410C-1	TSIA410C-0
continued	:00	TSIA410N-1	TSIA410N-0	TSIA410S-5	TSIA410S-4	TSIA410S-3	TSIA410S-2	TSIA410S-1	TSIA410S-0
0X0AA	:FE	TSIA420C-7	TSIA420C-6	TSIA420C-5	TSIA420C-4	TSIA420C-3	TSIA420C-2	TSIA420C-1	TSIA420C-0
continued	:00	TSIA420N-1	TSIA420N-0	TSIA420S-5	TSIA420S-4	TSIA420S-3	TSIA420S-2	TSIA420S-1	TSIA420S-0
0X0AB	:FE	TSIA430C-7	TSIA430C-6	TSIA430C-5	TSIA430C-4	TSIA430C-3	TSIA430C-2	TSIA430C-1	TSIA430C-0
continued	:00	TSIA430N-1	TSIA430N-0	TSIA430S-5	TSIA430S-4	TSIA430S-3	TSIA430S-2	TSIA430S-1	TSIA430S-0
0X0AC	:FE	TSIA440C-7	TSIA440C-6	TSIA440C-5	TSIA440C-4	TSIA440C-3	TSIA440C-2	TSIA440C-1	TSIA440C-0
continued	:00	TSIA440N-1	TSIA440N-0	TSIA440S-5	TSIA440S-4	TSIA440S-3	TSIA440S-2	TSIA440S-1	TSIA440S-0
0X0AD	:FE	TSIA450C-7	TSIA450C-6	TSIA450C-5	TSIA450C-4	TSIA450C-3	TSIA450C-2	TSIA450C-1	TSIA450C-0
continued	:00	TSIA450N-1	TSIA450N-0	TSIA450S-5	TSIA450S-4	TSIA450S-3	TSIA450S-2	TSIA450S-1	TSIA450S-0
0X0AE	:FE	TSIA460C-7	TSIA460C-6	TSIA460C-5	TSIA460C-4	TSIA460C-3	TSIA460C-2	TSIA460C-1	TSIA460C-0
continued	:00	TSIA460N-1	TSIA460N-0	TSIA460S-5	TSIA460S-4	TSIA460S-3	TSIA460S-2	TSIA460S-1	TSIA460S-0
0X0AF	:FE	TSIA470C-7	TSIA470C-6	TSIA470C-5	TSIA470C-4	TSIA470C-3	TSIA470C-2	TSIA470C-1	TSIA470C-0
continued	:00	TSIA470N-1	TSIA470N-0	TSIA470S-5	TSIA470S-4	TSIA470S-3	TSIA470S-2	TSIA470S-1	TSIA470S-0
TSI Bank 0 Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0x0B0	:00	0	0	0	0	0	0	0	0
continued	:7E	0	PARERR0LOC-5	PARERR0LOC-4	PARERR0LOC-3	PARERR0LOC-2	PARERR0LOC-1	PARERR0LOC-0	MEMPARERR0
0x0B1	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRD0
0x0B2	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRM0
0x0B3	:FF	TSIA150P	TSIA140P	TSIA130P	TSIA120P	TSIA110P	TSIA100P	TSIA090P	TSIA080P
continued	:FF	TSIA070P	TSIA060P	TSIA050P	TSIA040P	TSIA030P	TSIA020P	TSIA1010P	TSIA000P
0x0B4	:FF	TSIA310P	TSIA300P	TSIA290P	TSIA280P	TSIA270P	TSIA260P	TSIA250P	TSIA240P
continued	:FF	TSIA230P	TSIA220P	TSIA210P	TSIA200P	TSIA190P	TSIA180P	TSIA170P	TSIA160P
0x0B5	:FF	TSIA470P	TSIA460P	TSIA450P	TSIA440P	TSIA430P	TSIA420P	TSIA410P	TSIA400P
continued	:FF	TSIA390P	TSIA380P	TSIA370P	TSIA360P	TSIA350P	TSIA340P	TSIA330P	TSIA320P
(invalid addresses)									
0x0B6-0X0BF	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Active Connection Map, Bank 1 (R/O)									
0X0C0	:FE	TSIA001C-7	TSIA001C-6	TSIA001C-5	TSIA001C-4	TSIA001C-3	TSIA001C-2	TSIA001C-1	TSIA001C-0
continued	:00	TSIA001N-1	TSIA001N-0	TSIA001S-5	TSIA001S-4	TSIA001S-3	TSIA001S-2	TSIA001S-1	TSIA001S-0
0X0C1	:FE	TSIA011C-7	TSIA011C-6	TSIA011C-5	TSIA011C-4	TSIA011C-3	TSIA011C-2	TSIA011C-1	TSIA011C-0
continued	:00	TSIA011N-1	TSIA011N-0	TSIA011S-5	TSIA011S-4	TSIA011S-3	TSIA011S-2	TSIA011S-1	TSIA011S-0
0X0C2	:FE	TSIA021C-7	TSIA021C-6	TSIA021C-5	TSIA021C-4	TSIA021C-3	TSIA021C-2	TSIA021C-1	TSIA021C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA021N-1	TSIA021N-0	TSIA021S-5	TSIA021S-4	TSIA021S-3	TSIA021S-2	TSIA021S-1	TSIA021S-0
0X0C3	:FE	TSIA031C-7	TSIA031C-6	TSIA031C-5	TSIA031C-4	TSIA031C-3	TSIA031C-2	TSIA031C-1	TSIA031C-0
continued	:00	TSIA031N-1	TSIA031N-0	TSIA031S-5	TSIA031S-4	TSIA031S-3	TSIA031S-2	TSIA031S-1	TSIA031S-0
0X0C4	:FE	TSIA041C-7	TSIA041C-6	TSIA041C-5	TSIA041C-4	TSIA041C-3	TSIA041C-2	TSIA041C-1	TSIA041C-0
continued	:00	TSIA041N-1	TSIA041N-0	TSIA041S-5	TSIA041S-4	TSIA041S-3	TSIA041S-2	TSIA041S-1	TSIA041S-0
0X0C5	:FE	TSIA051C-7	TSIA051C-6	TSIA051C-5	TSIA051C-4	TSIA051C-3	TSIA051C-2	TSIA051C-1	TSIA051C-0
continued	:00	TSIA051N-1	TSIA051N-0	TSIA051S-5	TSIA051S-4	TSIA051S-3	TSIA051S-2	TSIA051S-1	TSIA051S-0
0X0C6	:FE	TSIA061C-7	TSIA061C-6	TSIA061C-5	TSIA061C-4	TSIA061C-3	TSIA061C-2	TSIA061C-1	TSIA061C-0
continued	:00	TSIA061N-1	TSIA061N-0	TSIA061S-5	TSIA061S-4	TSIA061S-3	TSIA061S-2	TSIA061S-1	TSIA061S-0
0X0C7	:FE	TSIA071C-7	TSIA071C-6	TSIA071C-5	TSIA071C-4	TSIA071C-3	TSIA071C-2	TSIA071C-1	TSIA071C-0
continued	:00	TSIA071N-1	TSIA071N-0	TSIA071S-5	TSIA071S-4	TSIA071S-3	TSIA071S-2	TSIA071S-1	TSIA071S-0
0X0C8	:FE	TSIA081C-7	TSIA081C-6	TSIA081C-5	TSIA081C-4	TSIA081C-3	TSIA081C-2	TSIA081C-1	TSIA081C-0
continued	:00	TSIA081N-1	TSIA081N-0	TSIA081S-5	TSIA081S-4	TSIA081S-3	TSIA081S-2	TSIA081S-1	TSIA081S-0
0X0C9	:FE	TSIA091C-7	TSIA091C-6	TSIA091C-5	TSIA091C-4	TSIA091C-3	TSIA091C-2	TSIA091C-1	TSIA091C-0
continued	:00	TSIA091N-1	TSIA091N-0	TSIA091S-5	TSIA091S-4	TSIA091S-3	TSIA091S-2	TSIA091S-1	TSIA091S-0
0X0CA	:FE	TSIA101C-7	TSIA101C-6	TSIA101C-5	TSIA101C-4	TSIA101C-3	TSIA101C-2	TSIA101C-1	TSIA101C-0
continued	:00	TSIA101N-1	TSIA101N-0	TSIA101S-5	TSIA101S-4	TSIA101S-3	TSIA101S-2	TSIA101S-1	TSIA101S-0
0X0CB	:FE	TSIA111C-7	TSIA111C-6	TSIA111C-5	TSIA111C-4	TSIA111C-3	TSIA111C-2	TSIA111C-1	TSIA111C-0
continued	:00	TSIA111N-1	TSIA111N-0	TSIA111S-5	TSIA111S-4	TSIA111S-3	TSIA111S-2	TSIA111S-1	TSIA111S-0
0X0CC	:FE	TSIA121C-7	TSIA121C-6	TSIA121C-5	TSIA121C-4	TSIA121C-3	TSIA121C-2	TSIA121C-1	TSIA121C-0
continued	:00	TSIA121N-1	TSIA121N-0	TSIA121S-5	TSIA121S-4	TSIA121S-3	TSIA121S-2	TSIA121S-1	TSIA121S-0
0X0CD	:FE	TSIA131C-7	TSIA131C-6	TSIA131C-5	TSIA131C-4	TSIA131C-3	TSIA131C-2	TSIA131C-1	TSIA131C-0
continued	:00	TSIA131N-1	TSIA131N-0	TSIA131S-5	TSIA131S-4	TSIA131S-3	TSIA131S-2	TSIA131S-1	TSIA131S-0
0X0CE	:FE	TSIA141C-7	TSIA141C-6	TSIA141C-5	TSIA141C-4	TSIA141C-3	TSIA141C-2	TSIA141C-1	TSIA141C-0
continued	:00	TSIA141N-1	TSIA141N-0	TSIA141S-5	TSIA141S-4	TSIA141S-3	TSIA141S-2	TSIA141S-1	TSIA141S-0
0X0CF	:FE	TSIA151C-7	TSIA151C-6	TSIA151C-5	TSIA151C-4	TSIA151C-3	TSIA151C-2	TSIA151C-1	TSIA151C-0
continued	:00	TSIA151N-1	TSIA151N-0	TSIA151S-5	TSIA151S-4	TSIA151S-3	TSIA151S-2	TSIA151S-1	TSIA151S-0
0X0D0	:FE	TSIA161C-7	TSIA161C-6	TSIA161C-5	TSIA161C-4	TSIA161C-3	TSIA161C-2	TSIA161C-1	TSIA161C-0
continued	:00	TSIA161N-1	TSIA161N-0	TSIA161S-5	TSIA161S-4	TSIA161S-3	TSIA161S-2	TSIA161S-1	TSIA161S-0
0X0D1	:FE	TSIA171C-7	TSIA171C-6	TSIA171C-5	TSIA171C-4	TSIA171C-3	TSIA171C-2	TSIA171C-1	TSIA171C-0
continued	:00	TSIA171N-1	TSIA171N-0	TSIA171S-5	TSIA171S-4	TSIA171S-3	TSIA171S-2	TSIA171S-1	TSIA171S-0
0X0D2	:FE	TSIA181C-7	TSIA181C-6	TSIA181C-5	TSIA181C-4	TSIA181C-3	TSIA181C-2	TSIA181C-1	TSIA181C-0
continued	:00	TSIA181N-1	TSIA181N-0	TSIA181S-5	TSIA181S-4	TSIA181S-3	TSIA181S-2	TSIA181S-1	TSIA181S-0
0X0D3	:FE	TSIA191C-7	TSIA191C-6	TSIA191C-5	TSIA191C-4	TSIA191C-3	TSIA191C-2	TSIA191C-1	TSIA191C-0
continued	:00	TSIA191N-1	TSIA191N-0	TSIA191S-5	TSIA191S-4	TSIA191S-3	TSIA191S-2	TSIA191S-1	TSIA191S-0
0X0D4	:FE	TSIA201C-7	TSIA201C-6	TSIA201C-5	TSIA201C-4	TSIA201C-3	TSIA201C-2	TSIA201C-1	TSIA201C-0
continued	:00	TSIA201N-1	TSIA201N-0	TSIA201S-5	TSIA201S-4	TSIA201S-3	TSIA201S-2	TSIA201S-1	TSIA201S-0
0X0D5	:FE	TSIA211C-7	TSIA211C-6	TSIA211C-5	TSIA211C-4	TSIA211C-3	TSIA211C-2	TSIA211C-1	TSIA211C-0
continued	:00	TSIA211N-1	TSIA211N-0	TSIA211S-5	TSIA211S-4	TSIA211S-3	TSIA211S-2	TSIA211S-1	TSIA211S-0
0X0D6	:FE	TSIA221C-7	TSIA221C-6	TSIA221C-5	TSIA221C-4	TSIA221C-3	TSIA221C-2	TSIA221C-1	TSIA221C-0
continued	:00	TSIA221N-1	TSIA221N-0	TSIA221S-5	TSIA221S-4	TSIA221S-3	TSIA221S-2	TSIA221S-1	TSIA221S-0
0X0D7	:FE	TSIA231C-7	TSIA231C-6	TSIA231C-5	TSIA231C-4	TSIA231C-3	TSIA231C-2	TSIA231C-1	TSIA231C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA231N-1	TSIA231N-0	TSIA231S-5	TSIA231S-4	TSIA231S-3	TSIA231S-2	TSIA231S-1	TSIA231S-0
0X0D8	:FE	TSIA241C-7	TSIA241C-6	TSIA241C-5	TSIA241C-4	TSIA241C-3	TSIA241C-2	TSIA241C-1	TSIA241C-0
continued	:00	TSIA241N-1	TSIA241N-0	TSIA241S-5	TSIA241S-4	TSIA241S-3	TSIA241S-2	TSIA241S-1	TSIA241S-0
0X0D9	:FE	TSIA251C-7	TSIA251C-6	TSIA251C-5	TSIA251C-4	TSIA251C-3	TSIA251C-2	TSIA251C-1	TSIA251C-0
continued	:00	TSIA251N-1	TSIA251N-0	TSIA251S-5	TSIA251S-4	TSIA251S-3	TSIA251S-2	TSIA251S-1	TSIA251S-0
0X0DA	:FE	TSIA261C-7	TSIA261C-6	TSIA261C-5	TSIA261C-4	TSIA261C-3	TSIA261C-2	TSIA261C-1	TSIA261C-0
continued	:00	TSIA261N-1	TSIA261N-0	TSIA261S-5	TSIA261S-4	TSIA261S-3	TSIA261S-2	TSIA261S-1	TSIA261S-0
0X0DB	:FE	TSIA271C-7	TSIA271C-6	TSIA271C-5	TSIA271C-4	TSIA271C-3	TSIA271C-2	TSIA271C-1	TSIA271C-0
continued	:00	TSIA271N-1	TSIA271N-0	TSIA271S-5	TSIA271S-4	TSIA271S-3	TSIA271S-2	TSIA271S-1	TSIA271S-0
0X0DC	:FE	TSIA281C-7	TSIA281C-6	TSIA281C-5	TSIA281C-4	TSIA281C-3	TSIA281C-2	TSIA281C-1	TSIA281C-0
continued	:00	TSIA281N-1	TSIA281N-0	TSIA281S-5	TSIA281S-4	TSIA281S-3	TSIA281S-2	TSIA281S-1	TSIA281S-0
0X0DD	:FE	TSIA291C-7	TSIA291C-6	TSIA291C-5	TSIA291C-4	TSIA291C-3	TSIA291C-2	TSIA291C-1	TSIA291C-0
continued	:00	TSIA291N-1	TSIA291N-0	TSIA291S-5	TSIA291S-4	TSIA291S-3	TSIA291S-2	TSIA291S-1	TSIA291S-0
0X0DE	:FE	TSIA301C-7	TSIA301C-6	TSIA301C-5	TSIA301C-4	TSIA301C-3	TSIA301C-2	TSIA301C-1	TSIA301C-0
continued	:00	TSIA301N-1	TSIA301N-0	TSIA301S-5	TSIA301S-4	TSIA301S-3	TSIA301S-2	TSIA301S-1	TSIA301S-0
0X0DF	:FE	TSIA311C-7	TSIA311C-6	TSIA311C-5	TSIA311C-4	TSIA311C-3	TSIA311C-2	TSIA311C-1	TSIA311C-0
continued	:00	TSIA311N-1	TSIA311N-0	TSIA311S-5	TSIA311S-4	TSIA311S-3	TSIA311S-2	TSIA311S-1	TSIA311S-0
0X0E0	:FE	TSIA321C-7	TSIA321C-6	TSIA321C-5	TSIA321C-4	TSIA321C-3	TSIA321C-2	TSIA321C-1	TSIA321C-0
continued	:00	TSIA321N-1	TSIA321N-0	TSIA321S-5	TSIA321S-4	TSIA321S-3	TSIA321S-2	TSIA321S-1	TSIA321S-0
0X0E1	:FE	TSIA331C-7	TSIA331C-6	TSIA331C-5	TSIA331C-4	TSIA331C-3	TSIA331C-2	TSIA331C-1	TSIA331C-0
continued	:00	TSIA331N-1	TSIA331N-0	TSIA331S-5	TSIA331S-4	TSIA331S-3	TSIA331S-2	TSIA331S-1	TSIA331S-0
0X0E2	:FE	TSIA341C-7	TSIA341C-6	TSIA341C-5	TSIA341C-4	TSIA341C-3	TSIA341C-2	TSIA341C-1	TSIA341C-0
continued	:00	TSIA341N-1	TSIA341N-0	TSIA341S-5	TSIA341S-4	TSIA341S-3	TSIA341S-2	TSIA341S-1	TSIA341S-0
0X0E3	:FE	TSIA351C-7	TSIA351C-6	TSIA351C-5	TSIA351C-4	TSIA351C-3	TSIA351C-2	TSIA351C-1	TSIA351C-0
continued	:00	TSIA351N-1	TSIA351N-0	TSIA351S-5	TSIA351S-4	TSIA351S-3	TSIA351S-2	TSIA351S-1	TSIA351S-0
0X0E4	:FE	TSIA361C-7	TSIA361C-6	TSIA361C-5	TSIA361C-4	TSIA361C-3	TSIA361C-2	TSIA361C-1	TSIA361C-0
continued	:00	TSIA361N-1	TSIA361N-0	TSIA361S-5	TSIA361S-4	TSIA361S-3	TSIA361S-2	TSIA361S-1	TSIA361S-0
0X0E5	:FE	TSIA371C-7	TSIA371C-6	TSIA371C-5	TSIA371C-4	TSIA371C-3	TSIA371C-2	TSIA371C-1	TSIA371C-0
continued	:00	TSIA371N-1	TSIA371N-0	TSIA371S-5	TSIA371S-4	TSIA371S-3	TSIA371S-2	TSIA371S-1	TSIA371S-0
0X0E6	:FE	TSIA381C-7	TSIA381C-6	TSIA381C-5	TSIA381C-4	TSIA381C-3	TSIA381C-2	TSIA381C-1	TSIA381C-0
continued	:00	TSIA381N-1	TSIA381N-0	TSIA381S-5	TSIA381S-4	TSIA381S-3	TSIA381S-2	TSIA381S-1	TSIA381S-0
0X0E7	:FE	TSIA391C-7	TSIA391C-6	TSIA391C-5	TSIA391C-4	TSIA391C-3	TSIA391C-2	TSIA391C-1	TSIA391C-0
continued	:00	TSIA391N-1	TSIA391N-0	TSIA391S-5	TSIA391S-4	TSIA391S-3	TSIA391S-2	TSIA391S-1	TSIA391S-0
0X0E8	:FE	TSIA401C-7	TSIA401C-6	TSIA401C-5	TSIA401C-4	TSIA401C-3	TSIA401C-2	TSIA401C-1	TSIA401C-0
continued	:00	TSIA401N-1	TSIA401N-0	TSIA401S-5	TSIA401S-4	TSIA401S-3	TSIA401S-2	TSIA401S-1	TSIA401S-0
0X0E9	:FE	TSIA411C-7	TSIA411C-6	TSIA411C-5	TSIA411C-4	TSIA411C-3	TSIA411C-2	TSIA411C-1	TSIA411C-0
continued	:00	TSIA411N-1	TSIA411N-0	TSIA411S-5	TSIA411S-4	TSIA411S-3	TSIA411S-2	TSIA411S-1	TSIA411S-0
0X0EA	:FE	TSIA421C-7	TSIA421C-6	TSIA421C-5	TSIA421C-4	TSIA421C-3	TSIA421C-2	TSIA421C-1	TSIA421C-0
continued	:00	TSIA421N-1	TSIA421N-0	TSIA421S-5	TSIA421S-4	TSIA421S-3	TSIA421S-2	TSIA421S-1	TSIA421S-0
0X0EB	:FE	TSIA431C-7	TSIA431C-6	TSIA431C-5	TSIA431C-4	TSIA431C-3	TSIA431C-2	TSIA431C-1	TSIA431C-0
continued	:00	TSIA431N-1	TSIA431N-0	TSIA431S-5	TSIA431S-4	TSIA431S-3	TSIA431S-2	TSIA431S-1	TSIA431S-0
0X0EC	:FE	TSIA441C-7	TSIA441C-6	TSIA441C-5	TSIA441C-4	TSIA441C-3	TSIA441C-2	TSIA441C-1	TSIA441C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA441N-1	TSIA441N-0	TSIA441S-5	TSIA441S-4	TSIA441S-3	TSIA441S-2	TSIA441S-1	TSIA441S-0
0X0ED	:FE	TSIA451C-7	TSIA451C-6	TSIA451C-5	TSIA451C-4	TSIA451C-3	TSIA451C-2	TSIA451C-1	TSIA451C-0
continued	:00	TSIA451N-1	TSIA451N-0	TSIA451S-5	TSIA451S-4	TSIA451S-3	TSIA451S-2	TSIA451S-1	TSIA451S-0
0X0EE	:FE	TSIA461C-7	TSIA461C-6	TSIA461C-5	TSIA461C-4	TSIA461C-3	TSIA461C-2	TSIA461C-1	TSIA461C-0
continued	:00	TSIA461N-1	TSIA461N-0	TSIA461S-5	TSIA461S-4	TSIA461S-3	TSIA461S-2	TSIA461S-1	TSIA461S-0
0X0EF	:FE	TSIA471C-7	TSIA471C-6	TSIA471C-5	TSIA471C-4	TSIA471C-3	TSIA471C-2	TSIA471C-1	TSIA471C-0
continued	:00	TSIA471N-1	TSIA471N-0	TSIA471S-5	TSIA471S-4	TSIA471S-3	TSIA471S-2	TSIA471S-1	TSIA471S-0
TSI Bank 1 STATUS (R/O), DELTA (R/O) and MASK (R/W) Bits									
0x0F0	:00	0	0	0	0	0	0	0	0
continued	:7E	0	PARERR1LOC-5	PARERR1LOC-4	PARERR1LOC-3	PARERR1LOC-2	PARERR1LOC-1	PARERR1LOC-0	MEMPARERR1
0x0F1	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRD1
0x0F2	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRM1
0x0F3	:FF	TSIA151P	TSIA141P	TSIA131P	TSIA121P	TSIA111P	TSIA101P	TSIA091P	TSIA081P
continued	:FF	TSIA071P	TSIA061P	TSIA051P	TSIA041P	TSIA031P	TSIA021P	TSIA1011P	TSIA001P
0x0F4	:FF	TSIA311P	TSIA301P	TSIA291P	TSIA281P	TSIA271P	TSIA261P	TSIA251P	TSIA241P
continued	:FF	TSIA231P	TSIA221P	TSIA211P	TSIA201P	TSIA191P	TSIA181P	TSIA171P	TSIA161P
0x0F5	:FF	TSIA471P	TSIA461P	TSIA451P	TSIA441P	TSIA431P	TSIA421P	TSIA411P	TSIA401P
continued	:FF	TSIA391P	TSIA381P	TSIA371P	TSIA361P	TSIA351P	TSIA341P	TSIA331P	TSIA321P
(invalid addresses)									
0x0F6-0X0FF	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Standby Connection Map, Bank 2 (R/W)									
0x100	:FE	TSIS002C-7	TSIS002C-6	TSIS002C-5	TSIS002C-4	TSIS002C-3	TSIS002C-2	TSIS002C-1	TSIS002C-0
continued	:00	TSIS002N-1	TSIS002N-0	TSIS002S-5	TSIS002S-4	TSIS002S-3	TSIS002S-2	TSIS002S-1	TSIS002S-0
0x101	:FE	TSIS012C-7	TSIS012C-6	TSIS012C-5	TSIS012C-4	TSIS012C-3	TSIS012C-2	TSIS012C-1	TSIS012C-0
continued	:00	TSIS012N-1	TSIS012N-0	TSIS012S-5	TSIS012S-4	TSIS012S-3	TSIS012S-2	TSIS012S-1	TSIS012S-0
0X102	:FE	TSIS022C-7	TSIS022C-6	TSIS022C-5	TSIS022C-4	TSIS022C-3	TSIS022C-2	TSIS022C-1	TSIS022C-0
continued	:00	TSIS022N-1	TSIS022N-0	TSIS022S-5	TSIS022S-4	TSIS022S-3	TSIS022S-2	TSIS022S-1	TSIS022S-0
0X103	:FE	TSIS032C-7	TSIS032C-6	TSIS032C-5	TSIS032C-4	TSIS032C-3	TSIS032C-2	TSIS032C-1	TSIS032C-0
continued	:00	TSIS032N-1	TSIS032N-0	TSIS032S-5	TSIS032S-4	TSIS032S-3	TSIS032S-2	TSIS032S-1	TSIS032S-0
0X104	:FE	TSIS042C-7	TSIS042C-6	TSIS042C-5	TSIS042C-4	TSIS042C-3	TSIS042C-2	TSIS042C-1	TSIS042C-0
continued	:00	TSIS042N-1	TSIS042N-0	TSIS042S-5	TSIS042S-4	TSIS042S-3	TSIS042S-2	TSIS042S-1	TSIS042S-0
0X105	:FE	TSIS052C-7	TSIS052C-6	TSIS052C-5	TSIS052C-4	TSIS052C-3	TSIS052C-2	TSIS052C-1	TSIS052C-0
continued	:00	TSIS052N-1	TSIS052N-0	TSIS052S-5	TSIS052S-4	TSIS052S-3	TSIS052S-2	TSIS052S-1	TSIS052S-0
0X106	:FE	TSIS062C-7	TSIS062C-6	TSIS062C-5	TSIS062C-4	TSIS062C-3	TSIS062C-2	TSIS062C-1	TSIS062C-0
continued	:00	TSIS062N-1	TSIS062N-0	TSIS062S-5	TSIS062S-4	TSIS062S-3	TSIS062S-2	TSIS062S-1	TSIS062S-0
0X107	:FE	TSIS072C-7	TSIS072C-6	TSIS072C-5	TSIS072C-4	TSIS072C-3	TSIS072C-2	TSIS072C-1	TSIS072C-0
continued	:00	TSIS072N-1	TSIS072N-0	TSIS072S-5	TSIS072S-4	TSIS072S-3	TSIS072S-2	TSIS072S-1	TSIS072S-0
0X108	:FE	TSIS082C-7	TSIS082C-6	TSIS082C-5	TSIS082C-4	TSIS082C-3	TSIS082C-2	TSIS082C-1	TSIS082C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS082N-1	TSIS082N-0	TSIS082S-5	TSIS082S-4	TSIS082S-3	TSIS082S-2	TSIS082S-1	TSIS082S-0
0X109	:FE	TSIS092C-7	TSIS092C-6	TSIS092C-5	TSIS092C-4	TSIS092C-3	TSIS092C-2	TSIS092C-1	TSIS092C-0
continued	:00	TSIS092N-1	TSIS092N-0	TSIS092S-5	TSIS092S-4	TSIS092S-3	TSIS092S-2	TSIS092S-1	TSIS092S-0
0X10A	:FE	TSIS102C-7	TSIS102C-6	TSIS102C-5	TSIS102C-4	TSIS102C-3	TSIS102C-2	TSIS102C-1	TSIS102C-0
continued	:00	TSIS102N-1	TSIS102N-0	TSIS102S-5	TSIS102S-4	TSIS102S-3	TSIS102S-2	TSIS102S-1	TSIS102S-0
0X10B	:FE	TSIS112C-7	TSIS112C-6	TSIS112C-5	TSIS112C-4	TSIS112C-3	TSIS112C-2	TSIS112C-1	TSIS112C-0
continued	:00	TSIS112N-1	TSIS112N-0	TSIS112S-5	TSIS112S-4	TSIS112S-3	TSIS112S-2	TSIS112S-1	TSIS112S-0
0X10C	:FE	TSIS122C-7	TSIS122C-6	TSIS122C-5	TSIS122C-4	TSIS122C-3	TSIS122C-2	TSIS122C-1	TSIS122C-0
continued	:00	TSIS122N-1	TSIS122N-0	TSIS122S-5	TSIS122S-4	TSIS122S-3	TSIS122S-2	TSIS122S-1	TSIS122S-0
0X10D	:FE	TSIS132C-7	TSIS132C-6	TSIS132C-5	TSIS132C-4	TSIS132C-3	TSIS132C-2	TSIS132C-1	TSIS132C-0
continued	:00	TSIS132N-1	TSIS132N-0	TSIS132S-5	TSIS132S-4	TSIS132S-3	TSIS132S-2	TSIS132S-1	TSIS132S-0
0X10E	:FE	TSIS142C-7	TSIS142C-6	TSIS142C-5	TSIS142C-4	TSIS142C-3	TSIS142C-2	TSIS142C-1	TSIS142C-0
continued	:00	TSIS142N-1	TSIS142N-0	TSIS142S-5	TSIS142S-4	TSIS142S-3	TSIS142S-2	TSIS142S-1	TSIS142S-0
0X10F	:FE	TSIS152C-7	TSIS152C-6	TSIS152C-5	TSIS152C-4	TSIS152C-3	TSIS152C-2	TSIS152C-1	TSIS152C-0
continued	:00	TSIS152N-1	TSIS152N-0	TSIS152S-5	TSIS152S-4	TSIS152S-3	TSIS152S-2	TSIS152S-1	TSIS152S-0
0X110	:FE	TSIS162C-7	TSIS162C-6	TSIS162C-5	TSIS162C-4	TSIS162C-3	TSIS162C-2	TSIS162C-1	TSIS162C-0
continued	:00	TSIS162N-1	TSIS162N-0	TSIS162S-5	TSIS162S-4	TSIS162S-3	TSIS162S-2	TSIS162S-1	TSIS162S-0
0X111	:FE	TSIS172C-7	TSIS172C-6	TSIS172C-5	TSIS172C-4	TSIS172C-3	TSIS172C-2	TSIS172C-1	TSIS172C-0
continued	:00	TSIS172N-1	TSIS172N-0	TSIS172S-5	TSIS172S-4	TSIS172S-3	TSIS172S-2	TSIS172S-1	TSIS172S-0
0X112	:FE	TSIS182C-7	TSIS182C-6	TSIS182C-5	TSIS182C-4	TSIS182C-3	TSIS182C-2	TSIS182C-1	TSIS182C-0
continued	:00	TSIS182N-1	TSIS182N-0	TSIS182S-5	TSIS182S-4	TSIS182S-3	TSIS182S-2	TSIS182S-1	TSIS182S-0
0X113	:FE	TSIS192C-7	TSIS192C-6	TSIS192C-5	TSIS192C-4	TSIS192C-3	TSIS192C-2	TSIS192C-1	TSIS192C-0
continued	:00	TSIS192N-1	TSIS192N-0	TSIS192S-5	TSIS192S-4	TSIS192S-3	TSIS192S-2	TSIS192S-1	TSIS192S-0
0X114	:FE	TSIS202C-7	TSIS202C-6	TSIS202C-5	TSIS202C-4	TSIS202C-3	TSIS202C-2	TSIS202C-1	TSIS202C-0
continued	:00	TSIS202N-1	TSIS202N-0	TSIS202S-5	TSIS202S-4	TSIS202S-3	TSIS202S-2	TSIS202S-1	TSIS202S-0
0X115	:FE	TSIS212C-7	TSIS212C-6	TSIS212C-5	TSIS212C-4	TSIS212C-3	TSIS212C-2	TSIS212C-1	TSIS212C-0
continued	:00	TSIS212N-1	TSIS212N-0	TSIS212S-5	TSIS212S-4	TSIS212S-3	TSIS212S-2	TSIS212S-1	TSIS212S-0
0X116	:FE	TSIS222C-7	TSIS222C-6	TSIS222C-5	TSIS222C-4	TSIS222C-3	TSIS222C-2	TSIS222C-1	TSIS222C-0
continued	:00	TSIS222N-1	TSIS222N-0	TSIS222S-5	TSIS222S-4	TSIS222S-3	TSIS222S-2	TSIS222S-1	TSIS222S-0
0X117	:FE	TSIS232C-7	TSIS232C-6	TSIS232C-5	TSIS232C-4	TSIS232C-3	TSIS232C-2	TSIS232C-1	TSIS232C-0
continued	:00	TSIS232N-1	TSIS232N-0	TSIS232S-5	TSIS232S-4	TSIS232S-3	TSIS232S-2	TSIS232S-1	TSIS232S-0
0X118	:FE	TSIS242C-7	TSIS242C-6	TSIS242C-5	TSIS242C-4	TSIS242C-3	TSIS242C-2	TSIS242C-1	TSIS242C-0
continued	:00	TSIS242N-1	TSIS242N-0	TSIS242S-5	TSIS242S-4	TSIS242S-3	TSIS242S-2	TSIS242S-1	TSIS242S-0
0X119	:FE	TSIS252C-7	TSIS252C-6	TSIS252C-5	TSIS252C-4	TSIS252C-3	TSIS252C-2	TSIS252C-1	TSIS252C-0
continued	:00	TSIS252N-1	TSIS252N-0	TSIS252S-5	TSIS252S-4	TSIS252S-3	TSIS252S-2	TSIS252S-1	TSIS252S-0
0X11A	:FE	TSIS262C-7	TSIS262C-6	TSIS262C-5	TSIS262C-4	TSIS262C-3	TSIS262C-2	TSIS262C-1	TSIS262C-0
continued	:00	TSIS262N-1	TSIS262N-0	TSIS262S-5	TSIS262S-4	TSIS262S-3	TSIS262S-2	TSIS262S-1	TSIS262S-0
0X11B	:FE	TSIS272C-7	TSIS272C-6	TSIS272C-5	TSIS272C-4	TSIS272C-3	TSIS272C-2	TSIS272C-1	TSIS272C-0
continued	:00	TSIS272N-1	TSIS272N-0	TSIS272S-5	TSIS272S-4	TSIS272S-3	TSIS272S-2	TSIS272S-1	TSIS272S-0
0X11C	:FE	TSIS282C-7	TSIS282C-6	TSIS282C-5	TSIS282C-4	TSIS282C-3	TSIS282C-2	TSIS282C-1	TSIS282C-0
continued	:00	TSIS282N-1	TSIS282N-0	TSIS282S-5	TSIS282S-4	TSIS282S-3	TSIS282S-2	TSIS282S-1	TSIS282S-0
0X11D	:FE	TSIS292C-7	TSIS292C-6	TSIS292C-5	TSIS292C-4	TSIS292C-3	TSIS292C-2	TSIS292C-1	TSIS292C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS292N-1	TSIS292N-0	TSIS292S-5	TSIS292S-4	TSIS292S-3	TSIS292S-2	TSIS292S-1	TSIS292S-0
0X11E	:FE	TSIS302C-7	TSIS302C-6	TSIS302C-5	TSIS302C-4	TSIS302C-3	TSIS302C-2	TSIS302C-1	TSIS302C-0
continued	:00	TSIS302N-1	TSIS302N-0	TSIS302S-5	TSIS302S-4	TSIS302S-3	TSIS302S-2	TSIS302S-1	TSIS302S-0
0X11F	:FE	TSIS312C-7	TSIS312C-6	TSIS312C-5	TSIS312C-4	TSIS312C-3	TSIS312C-2	TSIS312C-1	TSIS312C-0
continued	:00	TSIS312N-1	TSIS312N-0	TSIS312S-5	TSIS312S-4	TSIS312S-3	TSIS312S-2	TSIS312S-1	TSIS312S-0
0X120	:FE	TSIS322C-7	TSIS322C-6	TSIS322C-5	TSIS322C-4	TSIS322C-3	TSIS322C-2	TSIS322C-1	TSIS322C-0
continued	:00	TSIS322N-1	TSIS322N-0	TSIS322S-5	TSIS322S-4	TSIS322S-3	TSIS322S-2	TSIS322S-1	TSIS322S-0
0X121	:FE	TSIS332C-7	TSIS332C-6	TSIS332C-5	TSIS332C-4	TSIS332C-3	TSIS332C-2	TSIS332C-1	TSIS332C-0
continued	:00	TSIS332N-1	TSIS332N-0	TSIS332S-5	TSIS332S-4	TSIS332S-3	TSIS332S-2	TSIS332S-1	TSIS332S-0
0X122	:FE	TSIS342C-7	TSIS342C-6	TSIS342C-5	TSIS342C-4	TSIS342C-3	TSIS342C-2	TSIS342C-1	TSIS342C-0
continued	:00	TSIS342N-1	TSIS342N-0	TSIS342S-5	TSIS342S-4	TSIS342S-3	TSIS342S-2	TSIS342S-1	TSIS342S-0
0X123	:FE	TSIS352C-7	TSIS352C-6	TSIS352C-5	TSIS352C-4	TSIS352C-3	TSIS352C-2	TSIS352C-1	TSIS352C-0
continued	:00	TSIS352N-1	TSIS352N-0	TSIS352S-5	TSIS352S-4	TSIS352S-3	TSIS352S-2	TSIS352S-1	TSIS352S-0
0X124	:FE	TSIS362C-7	TSIS362C-6	TSIS362C-5	TSIS362C-4	TSIS362C-3	TSIS362C-2	TSIS362C-1	TSIS362C-0
continued	:00	TSIS362N-1	TSIS362N-0	TSIS362S-5	TSIS362S-4	TSIS362S-3	TSIS362S-2	TSIS362S-1	TSIS362S-0
0X125	:FE	TSIS372C-7	TSIS372C-6	TSIS372C-5	TSIS372C-4	TSIS372C-3	TSIS372C-2	TSIS372C-1	TSIS372C-0
continued	:00	TSIS372N-1	TSIS372N-0	TSIS372S-5	TSIS372S-4	TSIS372S-3	TSIS372S-2	TSIS372S-1	TSIS372S-0
0X126	:FE	TSIS382C-7	TSIS382C-6	TSIS382C-5	TSIS382C-4	TSIS382C-3	TSIS382C-2	TSIS382C-1	TSIS382C-0
continued	:00	TSIS382N-1	TSIS382N-0	TSIS382S-5	TSIS382S-4	TSIS382S-3	TSIS382S-2	TSIS382S-1	TSIS382S-0
0X127	:FE	TSIS392C-7	TSIS392C-6	TSIS392C-5	TSIS392C-4	TSIS392C-3	TSIS392C-2	TSIS392C-1	TSIS392C-0
continued	:00	TSIS392N-1	TSIS392N-0	TSIS392S-5	TSIS392S-4	TSIS392S-3	TSIS392S-2	TSIS392S-1	TSIS392S-0
0X128	:FE	TSIS402C-7	TSIS402C-6	TSIS402C-5	TSIS402C-4	TSIS402C-3	TSIS402C-2	TSIS402C-1	TSIS402C-0
continued	:00	TSIS402N-1	TSIS402N-0	TSIS402S-5	TSIS402S-4	TSIS402S-3	TSIS402S-2	TSIS402S-1	TSIS402S-0
0X129	:FE	TSIS412C-7	TSIS412C-6	TSIS412C-5	TSIS412C-4	TSIS412C-3	TSIS412C-2	TSIS412C-1	TSIS412C-0
continued	:00	TSIS412N-1	TSIS412N-0	TSIS412S-5	TSIS412S-4	TSIS412S-3	TSIS412S-2	TSIS412S-1	TSIS412S-0
0X12A	:FE	TSIS422C-7	TSIS422C-6	TSIS422C-5	TSIS422C-4	TSIS422C-3	TSIS422C-2	TSIS422C-1	TSIS422C-0
continued	:00	TSIS422N-1	TSIS422N-0	TSIS422S-5	TSIS422S-4	TSIS422S-3	TSIS422S-2	TSIS422S-1	TSIS422S-0
0X12B	:FE	TSIS432C-7	TSIS432C-6	TSIS432C-5	TSIS432C-4	TSIS432C-3	TSIS432C-2	TSIS432C-1	TSIS432C-0
continued	:00	TSIS432N-1	TSIS432N-0	TSIS432S-5	TSIS432S-4	TSIS432S-3	TSIS432S-2	TSIS432S-1	TSIS432S-0
0X12C	:FE	TSIS442C-7	TSIS442C-6	TSIS442C-5	TSIS442C-4	TSIS442C-3	TSIS442C-2	TSIS442C-1	TSIS442C-0
continued	:00	TSIS442N-1	TSIS442N-0	TSIS442S-5	TSIS442S-4	TSIS442S-3	TSIS442S-2	TSIS442S-1	TSIS442S-0
0X12D	:FE	TSIS452C-7	TSIS452C-6	TSIS452C-5	TSIS452C-4	TSIS452C-3	TSIS452C-2	TSIS452C-1	TSIS452C-0
continued	:00	TSIS452N-1	TSIS452N-0	TSIS452S-5	TSIS452S-4	TSIS452S-3	TSIS452S-2	TSIS452S-1	TSIS452S-0
0X12E	:FE	TSIS462C-7	TSIS462C-6	TSIS462C-5	TSIS462C-4	TSIS462C-3	TSIS462C-2	TSIS462C-1	TSIS462C-0
continued	:00	TSIS462N-1	TSIS462N-0	TSIS462S-5	TSIS462S-4	TSIS462S-3	TSIS462S-2	TSIS462S-1	TSIS462S-0
0X12F	:FE	TSIS472C-7	TSIS472C-6	TSIS472C-5	TSIS472C-4	TSIS472C-3	TSIS472C-2	TSIS472C-1	TSIS472C-0
continued	:00	TSIS472N-1	TSIS472N-0	TSIS472S-5	TSIS472S-4	TSIS472S-3	TSIS472S-2	TSIS472S-1	TSIS472S-0
Invalid Addresses									
0x130-0X13F	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
Standby Connection Map, Bank 3 (R/W)									
0X140	:FE	TSIS003C-7	TSIS003C-6	TSIS003C-5	TSIS003C-4	TSIS003C-3	TSIS003C-2	TSIS003C-1	TSIS003C-0
continued	:00	TSIS003N-1	TSIS003N-0	TSIS003S-5	TSIS003S-4	TSIS003S-3	TSIS003S-2	TSIS003S-1	TSIS003S-0
0X141	:FE	TSIS013C-7	TSIS013C-6	TSIS013C-5	TSIS013C-4	TSIS013C-3	TSIS013C-2	TSIS013C-1	TSIS013C-0
continued	:00	TSIS013N-1	TSIS013N-0	TSIS013S-5	TSIS013S-4	TSIS013S-3	TSIS013S-2	TSIS013S-1	TSIS013S-0
0X142	:FE	TSIS023C-7	TSIS023C-6	TSIS023C-5	TSIS023C-4	TSIS023C-3	TSIS023C-2	TSIS023C-1	TSIS023C-0
continued	:00	TSIS023N-1	TSIS023N-0	TSIS023S-5	TSIS023S-4	TSIS023S-3	TSIS023S-2	TSIS023S-1	TSIS023S-0
0X143	:FE	TSIS033C-7	TSIS033C-6	TSIS033C-5	TSIS033C-4	TSIS033C-3	TSIS033C-2	TSIS033C-1	TSIS033C-0
continued	:00	TSIS033N-1	TSIS033N-0	TSIS033S-5	TSIS033S-4	TSIS033S-3	TSIS033S-2	TSIS033S-1	TSIS033S-0
0X144	:FE	TSIS043C-7	TSIS043C-6	TSIS043C-5	TSIS043C-4	TSIS043C-3	TSIS043C-2	TSIS043C-1	TSIS043C-0
continued	:00	TSIS043N-1	TSIS043N-0	TSIS043S-5	TSIS043S-4	TSIS043S-3	TSIS043S-2	TSIS043S-1	TSIS043S-0
0X145	:FE	TSIS053C-7	TSIS053C-6	TSIS053C-5	TSIS053C-4	TSIS053C-3	TSIS053C-2	TSIS053C-1	TSIS053C-0
continued	:00	TSIS053N-1	TSIS053N-0	TSIS053S-5	TSIS053S-4	TSIS053S-3	TSIS053S-2	TSIS053S-1	TSIS053S-0
0X146	:FE	TSIS063C-7	TSIS063C-6	TSIS063C-5	TSIS063C-4	TSIS063C-3	TSIS063C-2	TSIS063C-1	TSIS063C-0
continued	:00	TSIS063N-1	TSIS063N-0	TSIS063S-5	TSIS063S-4	TSIS063S-3	TSIS063S-2	TSIS063S-1	TSIS063S-0
0X147	:FE	TSIS073C-7	TSIS073C-6	TSIS073C-5	TSIS073C-4	TSIS073C-3	TSIS073C-2	TSIS073C-1	TSIS073C-0
continued	:00	TSIS073N-1	TSIS073N-0	TSIS073S-5	TSIS073S-4	TSIS073S-3	TSIS073S-2	TSIS073S-1	TSIS073S-0
0X148	:FE	TSIS083C-7	TSIS083C-6	TSIS083C-5	TSIS083C-4	TSIS083C-3	TSIS083C-2	TSIS083C-1	TSIS083C-0
continued	:00	TSIS083N-1	TSIS083N-0	TSIS083S-5	TSIS083S-4	TSIS083S-3	TSIS083S-2	TSIS083S-1	TSIS083S-0
0X149	:FE	TSIS093C-7	TSIS093C-6	TSIS093C-5	TSIS093C-4	TSIS093C-3	TSIS093C-2	TSIS093C-1	TSIS093C-0
continued	:00	TSIS093N-1	TSIS093N-0	TSIS093S-5	TSIS093S-4	TSIS093S-3	TSIS093S-2	TSIS093S-1	TSIS093S-0
0X14A	:FE	TSIS103C-7	TSIS103C-6	TSIS103C-5	TSIS103C-4	TSIS103C-3	TSIS103C-2	TSIS103C-1	TSIS103C-0
continued	:00	TSIS103N-1	TSIS103N-0	TSIS103S-5	TSIS103S-4	TSIS103S-3	TSIS103S-2	TSIS103S-1	TSIS103S-0
0X14B	:FE	TSIS113C-7	TSIS113C-6	TSIS113C-5	TSIS113C-4	TSIS113C-3	TSIS113C-2	TSIS113C-1	TSIS113C-0
continued	:00	TSIS113N-1	TSIS113N-0	TSIS113S-5	TSIS113S-4	TSIS113S-3	TSIS113S-2	TSIS113S-1	TSIS113S-0
0X14C	:FE	TSIS123C-7	TSIS123C-6	TSIS123C-5	TSIS123C-4	TSIS123C-3	TSIS123C-2	TSIS123C-1	TSIS123C-0
continued	:00	TSIS123N-1	TSIS123N-0	TSIS123S-5	TSIS123S-4	TSIS123S-3	TSIS123S-2	TSIS123S-1	TSIS123S-0
0X14D	:FE	TSIS133C-7	TSIS133C-6	TSIS133C-5	TSIS133C-4	TSIS133C-3	TSIS133C-2	TSIS133C-1	TSIS133C-0
continued	:00	TSIS133N-1	TSIS133N-0	TSIS133S-5	TSIS133S-4	TSIS133S-3	TSIS133S-2	TSIS133S-1	TSIS133S-0
0X14E	:FE	TSIS143C-7	TSIS143C-6	TSIS143C-5	TSIS143C-4	TSIS143C-3	TSIS143C-2	TSIS143C-1	TSIS143C-0
continued	:00	TSIS143N-1	TSIS143N-0	TSIS143S-5	TSIS143S-4	TSIS143S-3	TSIS143S-2	TSIS143S-1	TSIS143S-0
0X14F	:FE	TSIS153C-7	TSIS153C-6	TSIS153C-5	TSIS153C-4	TSIS153C-3	TSIS153C-2	TSIS153C-1	TSIS153C-0
continued	:00	TSIS153N-1	TSIS153N-0	TSIS153S-5	TSIS153S-4	TSIS153S-3	TSIS153S-2	TSIS153S-1	TSIS153S-0
0X150	:FE	TSIS163C-7	TSIS163C-6	TSIS163C-5	TSIS163C-4	TSIS163C-3	TSIS163C-2	TSIS163C-1	TSIS163C-0
continued	:00	TSIS163N-1	TSIS163N-0	TSIS163S-5	TSIS163S-4	TSIS163S-3	TSIS163S-2	TSIS163S-1	TSIS163S-0
0X151	:FE	TSIS173C-7	TSIS173C-6	TSIS173C-5	TSIS173C-4	TSIS173C-3	TSIS173C-2	TSIS173C-1	TSIS173C-0
continued	:00	TSIS173N-1	TSIS173N-0	TSIS173S-5	TSIS173S-4	TSIS173S-3	TSIS173S-2	TSIS173S-1	TSIS173S-0
0X152	:FE	TSIS183C-7	TSIS183C-6	TSIS183C-5	TSIS183C-4	TSIS183C-3	TSIS183C-2	TSIS183C-1	TSIS183C-0
continued	:00	TSIS183N-1	TSIS183N-0	TSIS183S-5	TSIS183S-4	TSIS183S-3	TSIS183S-2	TSIS183S-1	TSIS183S-0
0X153	:FE	TSIS193C-7	TSIS193C-6	TSIS193C-5	TSIS193C-4	TSIS193C-3	TSIS193C-2	TSIS193C-1	TSIS193C-0
continued	:00	TSIS193N-1	TSIS193N-0	TSIS193S-5	TSIS193S-4	TSIS193S-3	TSIS193S-2	TSIS193S-1	TSIS193S-0
0X154	:FE	TSIS203C-7	TSIS203C-6	TSIS203C-5	TSIS203C-4	TSIS203C-3	TSIS203C-2	TSIS203C-1	TSIS203C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS203N-1	TSIS203N-0	TSIS203S-5	TSIS203S-4	TSIS203S-3	TSIS203S-2	TSIS203S-1	TSIS203S-0
0X155	:FE	TSIS213C-7	TSIS213C-6	TSIS213C-5	TSIS213C-4	TSIS213C-3	TSIS213C-2	TSIS213C-1	TSIS213C-0
continued	:00	TSIS213N-1	TSIS213N-0	TSIS213S-5	TSIS213S-4	TSIS213S-3	TSIS213S-2	TSIS213S-1	TSIS213S-0
0X156	:FE	TSIS223C-7	TSIS223C-6	TSIS223C-5	TSIS223C-4	TSIS223C-3	TSIS223C-2	TSIS223C-1	TSIS223C-0
continued	:00	TSIS223N-1	TSIS223N-0	TSIS223S-5	TSIS223S-4	TSIS223S-3	TSIS223S-2	TSIS223S-1	TSIS223S-0
0X157	:FE	TSIS233C-7	TSIS233C-6	TSIS233C-5	TSIS233C-4	TSIS233C-3	TSIS233C-2	TSIS233C-1	TSIS233C-0
continued	:00	TSIS233N-1	TSIS233N-0	TSIS233S-5	TSIS233S-4	TSIS233S-3	TSIS233S-2	TSIS233S-1	TSIS233S-0
0X158	:FE	TSIS243C-7	TSIS243C-6	TSIS243C-5	TSIS243C-4	TSIS243C-3	TSIS243C-2	TSIS243C-1	TSIS243C-0
continued	:00	TSIS243N-1	TSIS243N-0	TSIS243S-5	TSIS243S-4	TSIS243S-3	TSIS243S-2	TSIS243S-1	TSIS243S-0
0X159	:FE	TSIS253C-7	TSIS253C-6	TSIS253C-5	TSIS253C-4	TSIS253C-3	TSIS253C-2	TSIS253C-1	TSIS253C-0
continued	:00	TSIS253N-1	TSIS253N-0	TSIS253S-5	TSIS253S-4	TSIS253S-3	TSIS253S-2	TSIS253S-1	TSIS253S-0
0X15A	:FE	TSIS263C-7	TSIS263C-6	TSIS263C-5	TSIS263C-4	TSIS263C-3	TSIS263C-2	TSIS263C-1	TSIS263C-0
continued	:00	TSIS263N-1	TSIS263N-0	TSIS263S-5	TSIS263S-4	TSIS263S-3	TSIS263S-2	TSIS263S-1	TSIS263S-0
0X15B	:FE	TSIS273C-7	TSIS273C-6	TSIS273C-5	TSIS273C-4	TSIS273C-3	TSIS273C-2	TSIS273C-1	TSIS273C-0
continued	:00	TSIS273N-1	TSIS273N-0	TSIS273S-5	TSIS273S-4	TSIS273S-3	TSIS273S-2	TSIS273S-1	TSIS273S-0
0X15C	:FE	TSIS283C-7	TSIS283C-6	TSIS283C-5	TSIS283C-4	TSIS283C-3	TSIS283C-2	TSIS283C-1	TSIS283C-0
continued	:00	TSIS283N-1	TSIS283N-0	TSIS283S-5	TSIS283S-4	TSIS283S-3	TSIS283S-2	TSIS283S-1	TSIS283S-0
0X15D	:FE	TSIS293C-7	TSIS293C-6	TSIS293C-5	TSIS293C-4	TSIS293C-3	TSIS293C-2	TSIS293C-1	TSIS293C-0
continued	:00	TSIS293N-1	TSIS293N-0	TSIS293S-5	TSIS293S-4	TSIS293S-3	TSIS293S-2	TSIS293S-1	TSIS293S-0
0X15E	:FE	TSIS303C-7	TSIS303C-6	TSIS303C-5	TSIS303C-4	TSIS303C-3	TSIS303C-2	TSIS303C-1	TSIS303C-0
continued	:00	TSIS303N-1	TSIS303N-0	TSIS303S-5	TSIS303S-4	TSIS303S-3	TSIS303S-2	TSIS303S-1	TSIS303S-0
0X15F	:FE	TSIS313C-7	TSIS313C-6	TSIS313C-5	TSIS313C-4	TSIS313C-3	TSIS313C-2	TSIS313C-1	TSIS313C-0
continued	:00	TSIS313N-1	TSIS313N-0	TSIS313S-5	TSIS313S-4	TSIS313S-3	TSIS313S-2	TSIS313S-1	TSIS313S-0
0X160	:FE	TSIS323C-7	TSIS323C-6	TSIS323C-5	TSIS323C-4	TSIS323C-3	TSIS323C-2	TSIS323C-1	TSIS323C-0
continued	:00	TSIS323N-1	TSIS323N-0	TSIS323S-5	TSIS323S-4	TSIS323S-3	TSIS323S-2	TSIS323S-1	TSIS323S-0
0X161	:FE	TSIS333C-7	TSIS333C-6	TSIS333C-5	TSIS333C-4	TSIS333C-3	TSIS333C-2	TSIS333C-1	TSIS333C-0
continued	:00	TSIS333N-1	TSIS333N-0	TSIS333S-5	TSIS333S-4	TSIS333S-3	TSIS333S-2	TSIS333S-1	TSIS333S-0
0X162	:FE	TSIS343C-7	TSIS343C-6	TSIS343C-5	TSIS343C-4	TSIS343C-3	TSIS343C-2	TSIS343C-1	TSIS343C-0
continued	:00	TSIS343N-1	TSIS343N-0	TSIS343S-5	TSIS343S-4	TSIS343S-3	TSIS343S-2	TSIS343S-1	TSIS343S-0
0X163	:FE	TSIS353C-7	TSIS353C-6	TSIS353C-5	TSIS353C-4	TSIS353C-3	TSIS353C-2	TSIS353C-1	TSIS353C-0
continued	:00	TSIS353N-1	TSIS353N-0	TSIS353S-5	TSIS353S-4	TSIS353S-3	TSIS353S-2	TSIS353S-1	TSIS353S-0
0X164	:FE	TSIS363C-7	TSIS363C-6	TSIS363C-5	TSIS363C-4	TSIS363C-3	TSIS363C-2	TSIS363C-1	TSIS363C-0
continued	:00	TSIS363N-1	TSIS363N-0	TSIS363S-5	TSIS363S-4	TSIS363S-3	TSIS363S-2	TSIS363S-1	TSIS363S-0
0X165	:FE	TSIS373C-7	TSIS373C-6	TSIS373C-5	TSIS373C-4	TSIS373C-3	TSIS373C-2	TSIS373C-1	TSIS373C-0
continued	:00	TSIS373N-1	TSIS373N-0	TSIS373S-5	TSIS373S-4	TSIS373S-3	TSIS373S-2	TSIS373S-1	TSIS373S-0
0X166	:FE	TSIS383C-7	TSIS383C-6	TSIS383C-5	TSIS383C-4	TSIS383C-3	TSIS383C-2	TSIS383C-1	TSIS383C-0
continued	:00	TSIS383N-1	TSIS383N-0	TSIS383S-5	TSIS383S-4	TSIS383S-3	TSIS383S-2	TSIS383S-1	TSIS383S-0
0X167	:FE	TSIS393C-7	TSIS393C-6	TSIS393C-5	TSIS393C-4	TSIS393C-3	TSIS393C-2	TSIS393C-1	TSIS393C-0
continued	:00	TSIS393N-1	TSIS393N-0	TSIS393S-5	TSIS393S-4	TSIS393S-3	TSIS393S-2	TSIS393S-1	TSIS393S-0
0X168	:FE	TSIS403C-7	TSIS403C-6	TSIS403C-5	TSIS403C-4	TSIS403C-3	TSIS403C-2	TSIS403C-1	TSIS403C-0
continued	:00	TSIS403N-1	TSIS403N-0	TSIS403S-5	TSIS403S-4	TSIS403S-3	TSIS403S-2	TSIS403S-1	TSIS403S-0
0X169	:FE	TSIS413C-7	TSIS413C-6	TSIS413C-5	TSIS413C-4	TSIS413C-3	TSIS413C-2	TSIS413C-1	TSIS413C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIS413N-1	TSIS413N-0	TSIS413S-5	TSIS413S-4	TSIS413S-3	TSIS413S-2	TSIS413S-1	TSIS413S-0
0X16A	:FE	TSIS423C-7	TSIS423C-6	TSIS423C-5	TSIS423C-4	TSIS423C-3	TSIS423C-2	TSIS423C-1	TSIS423C-0
continued	:00	TSIS423N-1	TSIS423N-0	TSIS423S-5	TSIS423S-4	TSIS423S-3	TSIS423S-2	TSIS423S-1	TSIS423S-0
0X16B	:FE	TSIS433C-7	TSIS433C-6	TSIS433C-5	TSIS433C-4	TSIS433C-3	TSIS433C-2	TSIS433C-1	TSIS433C-0
continued	:00	TSIS433N-1	TSIS433N-0	TSIS433S-5	TSIS433S-4	TSIS433S-3	TSIS433S-2	TSIS433S-1	TSIS433S-0
0X16C	:FE	TSIS443C-7	TSIS443C-6	TSIS443C-5	TSIS443C-4	TSIS443C-3	TSIS443C-2	TSIS443C-1	TSIS443C-0
continued	:00	TSIS443N-1	TSIS443N-0	TSIS443S-5	TSIS443S-4	TSIS443S-3	TSIS443S-2	TSIS443S-1	TSIS443S-0
0X16D	:FE	TSIS453C-7	TSIS453C-6	TSIS453C-5	TSIS453C-4	TSIS453C-3	TSIS453C-2	TSIS453C-1	TSIS453C-0
continued	:00	TSIS453N-1	TSIS453N-0	TSIS453S-5	TSIS453S-4	TSIS453S-3	TSIS453S-2	TSIS453S-1	TSIS453S-0
0X16E	:FE	TSIS463C-7	TSIS463C-6	TSIS463C-5	TSIS463C-4	TSIS463C-3	TSIS463C-2	TSIS463C-1	TSIS463C-0
continued	:00	TSIS463N-1	TSIS463N-0	TSIS463S-5	TSIS463S-4	TSIS463S-3	TSIS463S-2	TSIS463S-1	TSIS463S-0
0X16F	:FE	TSIS473C-7	TSIS473C-6	TSIS473C-5	TSIS473C-4	TSIS473C-3	TSIS473C-2	TSIS473C-1	TSIS473C-0
continued	:00	TSIS473N-1	TSIS473N-0	TSIS473S-5	TSIS473S-4	TSIS473S-3	TSIS473S-2	TSIS473S-1	TSIS473S-0
Miscellaneous Control Bits									
0X170	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	TSITRNSPNT1
0X171	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	DOMAIN1
Invalid Addresses									
0X172-0X17F	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Active Connection Map, Bank 2 (R/O)									
0X180	:FE	TSIA002C-7	TSIA002C-6	TSIA002C-5	TSIA002C-4	TSIA002C-3	TSIA002C-2	TSIA002C-1	TSIA002C-0
continued	:00	TSIA002N-1	TSIA002N-0	TSIA002S-5	TSIA002S-4	TSIA002S-3	TSIA002S-2	TSIA002S-1	TSIA002S-0
0X181	:FE	TSIA012C-7	TSIA012C-6	TSIA012C-5	TSIA012C-4	TSIA012C-3	TSIA012C-2	TSIA012C-1	TSIA012C-0
continued	:00	TSIA012N-1	TSIA012N-0	TSIA012S-5	TSIA012S-4	TSIA012S-3	TSIA012S-2	TSIA012S-1	TSIA012S-0
0X182	:FE	TSIA022C-7	TSIA022C-6	TSIA022C-5	TSIA022C-4	TSIA022C-3	TSIA022C-2	TSIA022C-1	TSIA022C-0
continued	:00	TSIA022N-1	TSIA022N-0	TSIA022S-5	TSIA022S-4	TSIA022S-3	TSIA022S-2	TSIA022S-1	TSIA022S-0
0X183	:FE	TSIA032C-7	TSIA032C-6	TSIA032C-5	TSIA032C-4	TSIA032C-3	TSIA032C-2	TSIA032C-1	TSIA032C-0
continued	:00	TSIA032N-1	TSIA032N-0	TSIA032S-5	TSIA032S-4	TSIA032S-3	TSIA032S-2	TSIA032S-1	TSIA032S-0
0X184	:FE	TSIA042C-7	TSIA042C-6	TSIA042C-5	TSIA042C-4	TSIA042C-3	TSIA042C-2	TSIA042C-1	TSIA042C-0
continued	:00	TSIA042N-1	TSIA042N-0	TSIA042S-5	TSIA042S-4	TSIA042S-3	TSIA042S-2	TSIA042S-1	TSIA042S-0
0X185	:FE	TSIA052C-7	TSIA052C-6	TSIA052C-5	TSIA052C-4	TSIA052C-3	TSIA052C-2	TSIA052C-1	TSIA052C-0
continued	:00	TSIA052N-1	TSIA052N-0	TSIA052S-5	TSIA052S-4	TSIA052S-3	TSIA052S-2	TSIA052S-1	TSIA052S-0
0X186	:FE	TSIA062C-7	TSIA062C-6	TSIA062C-5	TSIA062C-4	TSIA062C-3	TSIA062C-2	TSIA062C-1	TSIA062C-0
continued	:00	TSIA062N-1	TSIA062N-0	TSIA062S-5	TSIA062S-4	TSIA062S-3	TSIA062S-2	TSIA062S-1	TSIA062S-0
0X187	:FE	TSIA072C-7	TSIA072C-6	TSIA072C-5	TSIA072C-4	TSIA072C-3	TSIA072C-2	TSIA072C-1	TSIA072C-0
continued	:00	TSIA072N-1	TSIA072N-0	TSIA072S-5	TSIA072S-4	TSIA072S-3	TSIA072S-2	TSIA072S-1	TSIA072S-0
0X188	:FE	TSIA082C-7	TSIA082C-6	TSIA082C-5	TSIA082C-4	TSIA082C-3	TSIA082C-2	TSIA082C-1	TSIA082C-0
continued	:00	TSIA082N-1	TSIA082N-0	TSIA082S-5	TSIA082S-4	TSIA082S-3	TSIA082S-2	TSIA082S-1	TSIA082S-0
0X189	:FE	TSIA092C-7	TSIA092C-6	TSIA092C-5	TSIA092C-4	TSIA092C-3	TSIA092C-2	TSIA092C-1	TSIA092C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA092N-1	TSIA092N-0	TSIA092S-5	TSIA092S-4	TSIA092S-3	TSIA092S-2	TSIA092S-1	TSIA092S-0
0X18A	:FE	TSIA102C-7	TSIA102C-6	TSIA102C-5	TSIA102C-4	TSIA102C-3	TSIA102C-2	TSIA102C-1	TSIA102C-0
continued	:00	TSIA102N-1	TSIA102N-0	TSIA102S-5	TSIA102S-4	TSIA102S-3	TSIA102S-2	TSIA102S-1	TSIA102S-0
0X18B	:FE	TSIA112C-7	TSIA112C-6	TSIA112C-5	TSIA112C-4	TSIA112C-3	TSIA112C-2	TSIA112C-1	TSIA112C-0
continued	:00	TSIA112N-1	TSIA112N-0	TSIA112S-5	TSIA112S-4	TSIA112S-3	TSIA112S-2	TSIA112S-1	TSIA112S-0
0X18C	:FE	TSIA122C-7	TSIA122C-6	TSIA122C-5	TSIA122C-4	TSIA122C-3	TSIA122C-2	TSIA122C-1	TSIA122C-0
continued	:00	TSIA122N-1	TSIA122N-0	TSIA122S-5	TSIA122S-4	TSIA122S-3	TSIA122S-2	TSIA122S-1	TSIA122S-0
0X18D	:FE	TSIA132C-7	TSIA132C-6	TSIA132C-5	TSIA132C-4	TSIA132C-3	TSIA132C-2	TSIA132C-1	TSIA132C-0
continued	:00	TSIA132N-1	TSIA132N-0	TSIA132S-5	TSIA132S-4	TSIA132S-3	TSIA132S-2	TSIA132S-1	TSIA132S-0
0X18E	:FE	TSIA142C-7	TSIA142C-6	TSIA142C-5	TSIA142C-4	TSIA142C-3	TSIA142C-2	TSIA142C-1	TSIA142C-0
continued	:00	TSIA142N-1	TSIA142N-0	TSIA142S-5	TSIA142S-4	TSIA142S-3	TSIA142S-2	TSIA142S-1	TSIA142S-0
0X18F	:FE	TSIA152C-7	TSIA152C-6	TSIA152C-5	TSIA152C-4	TSIA152C-3	TSIA152C-2	TSIA152C-1	TSIA152C-0
continued	:00	TSIA152N-1	TSIA152N-0	TSIA152S-5	TSIA152S-4	TSIA152S-3	TSIA152S-2	TSIA152S-1	TSIA152S-0
0X190	:FE	TSIA162C-7	TSIA162C-6	TSIA162C-5	TSIA162C-4	TSIA162C-3	TSIA162C-2	TSIA162C-1	TSIA162C-0
continued	:00	TSIA162N-1	TSIA162N-0	TSIA162S-5	TSIA162S-4	TSIA162S-3	TSIA162S-2	TSIA162S-1	TSIA162S-0
0X191	:FE	TSIA172C-7	TSIA172C-6	TSIA172C-5	TSIA172C-4	TSIA172C-3	TSIA172C-2	TSIA172C-1	TSIA172C-0
continued	:00	TSIA172N-1	TSIA172N-0	TSIA172S-5	TSIA172S-4	TSIA172S-3	TSIA172S-2	TSIA172S-1	TSIA172S-0
0X192	:FE	TSIA182C-7	TSIA182C-6	TSIA182C-5	TSIA182C-4	TSIA182C-3	TSIA182C-2	TSIA182C-1	TSIA182C-0
continued	:00	TSIA182N-1	TSIA182N-0	TSIA182S-5	TSIA182S-4	TSIA182S-3	TSIA182S-2	TSIA182S-1	TSIA182S-0
0X193	:FE	TSIA192C-7	TSIA192C-6	TSIA192C-5	TSIA192C-4	TSIA192C-3	TSIA192C-2	TSIA192C-1	TSIA192C-0
continued	:00	TSIA192N-1	TSIA192N-0	TSIA192S-5	TSIA192S-4	TSIA192S-3	TSIA192S-2	TSIA192S-1	TSIA192S-0
0X194	:FE	TSIA202C-7	TSIA202C-6	TSIA202C-5	TSIA202C-4	TSIA202C-3	TSIA202C-2	TSIA202C-1	TSIA202C-0
continued	:00	TSIA202N-1	TSIA202N-0	TSIA202S-5	TSIA202S-4	TSIA202S-3	TSIA202S-2	TSIA202S-1	TSIA202S-0
0X195	:FE	TSIA212C-7	TSIA212C-6	TSIA212C-5	TSIA212C-4	TSIA212C-3	TSIA212C-2	TSIA212C-1	TSIA212C-0
continued	:00	TSIA212N-1	TSIA212N-0	TSIA212S-5	TSIA212S-4	TSIA212S-3	TSIA212S-2	TSIA212S-1	TSIA212S-0
0X196	:FE	TSIA222C-7	TSIA222C-6	TSIA222C-5	TSIA222C-4	TSIA222C-3	TSIA222C-2	TSIA222C-1	TSIA222C-0
continued	:00	TSIA222N-1	TSIA222N-0	TSIA222S-5	TSIA222S-4	TSIA222S-3	TSIA222S-2	TSIA222S-1	TSIA222S-0
0X197	:FE	TSIA232C-7	TSIA232C-6	TSIA232C-5	TSIA232C-4	TSIA232C-3	TSIA232C-2	TSIA232C-1	TSIA232C-0
continued	:00	TSIA232N-1	TSIA232N-0	TSIA232S-5	TSIA232S-4	TSIA232S-3	TSIA232S-2	TSIA232S-1	TSIA232S-0
0X198	:FE	TSIA242C-7	TSIA242C-6	TSIA242C-5	TSIA242C-4	TSIA242C-3	TSIA242C-2	TSIA242C-1	TSIA242C-0
continued	:00	TSIA242N-1	TSIA242N-0	TSIA242S-5	TSIA242S-4	TSIA242S-3	TSIA242S-2	TSIA242S-1	TSIA242S-0
0X199	:FE	TSIA252C-7	TSIA252C-6	TSIA252C-5	TSIA252C-4	TSIA252C-3	TSIA252C-2	TSIA252C-1	TSIA252C-0
continued	:00	TSIA252N-1	TSIA252N-0	TSIA252S-5	TSIA252S-4	TSIA252S-3	TSIA252S-2	TSIA252S-1	TSIA252S-0
0X19A	:FE	TSIA262C-7	TSIA262C-6	TSIA262C-5	TSIA262C-4	TSIA262C-3	TSIA262C-2	TSIA262C-1	TSIA262C-0
continued	:00	TSIA262N-1	TSIA262N-0	TSIA262S-5	TSIA262S-4	TSIA262S-3	TSIA262S-2	TSIA262S-1	TSIA262S-0
0X19B	:FE	TSIA272C-7	TSIA272C-6	TSIA272C-5	TSIA272C-4	TSIA272C-3	TSIA272C-2	TSIA272C-1	TSIA272C-0
continued	:00	TSIA272N-1	TSIA272N-0	TSIA272S-5	TSIA272S-4	TSIA272S-3	TSIA272S-2	TSIA272S-1	TSIA272S-0
0X19C	:FE	TSIA282C-7	TSIA282C-6	TSIA282C-5	TSIA282C-4	TSIA282C-3	TSIA282C-2	TSIA282C-1	TSIA282C-0
continued	:00	TSIA282N-1	TSIA282N-0	TSIA282S-5	TSIA282S-4	TSIA282S-3	TSIA282S-2	TSIA282S-1	TSIA282S-0
0X19D	:FE	TSIA292C-7	TSIA292C-6	TSIA292C-5	TSIA292C-4	TSIA292C-3	TSIA292C-2	TSIA292C-1	TSIA292C-0
continued	:00	TSIA292N-1	TSIA292N-0	TSIA292S-5	TSIA292S-4	TSIA292S-3	TSIA292S-2	TSIA292S-1	TSIA292S-0
0X19E	:FE	TSIA302C-7	TSIA302C-6	TSIA302C-5	TSIA302C-4	TSIA302C-3	TSIA302C-2	TSIA302C-1	TSIA302C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA302N-1	TSIA302N-0	TSIA302S-5	TSIA302S-4	TSIA302S-3	TSIA302S-2	TSIA302S-1	TSIA302S-0
0X19F	:FE	TSIA312C-7	TSIA312C-6	TSIA312C-5	TSIA312C-4	TSIA312C-3	TSIA312C-2	TSIA312C-1	TSIA312C-0
continued	:00	TSIA312N-1	TSIA312N-0	TSIA312S-5	TSIA312S-4	TSIA312S-3	TSIA312S-2	TSIA312S-1	TSIA312S-0
0X1A0	:FE	TSIA322C-7	TSIA322C-6	TSIA322C-5	TSIA322C-4	TSIA322C-3	TSIA322C-2	TSIA322C-1	TSIA322C-0
continued	:00	TSIA322N-1	TSIA322N-0	TSIA322S-5	TSIA322S-4	TSIA322S-3	TSIA322S-2	TSIA322S-1	TSIA322S-0
0X1A1	:FE	TSIA332C-7	TSIA332C-6	TSIA332C-5	TSIA332C-4	TSIA332C-3	TSIA332C-2	TSIA332C-1	TSIA332C-0
continued	:00	TSIA332N-1	TSIA332N-0	TSIA332S-5	TSIA332S-4	TSIA332S-3	TSIA332S-2	TSIA332S-1	TSIA332S-0
0X1A2	:FE	TSIA342C-7	TSIA342C-6	TSIA342C-5	TSIA342C-4	TSIA342C-3	TSIA342C-2	TSIA342C-1	TSIA342C-0
continued	:00	TSIA342N-1	TSIA342N-0	TSIA342S-5	TSIA342S-4	TSIA342S-3	TSIA342S-2	TSIA342S-1	TSIA342S-0
0X1A3	:FE	TSIA352C-7	TSIA352C-6	TSIA352C-5	TSIA352C-4	TSIA352C-3	TSIA352C-2	TSIA352C-1	TSIA352C-0
continued	:00	TSIA352N-1	TSIA352N-0	TSIA352S-5	TSIA352S-4	TSIA352S-3	TSIA352S-2	TSIA352S-1	TSIA352S-0
0X1A4	:FE	TSIA362C-7	TSIA362C-6	TSIA362C-5	TSIA362C-4	TSIA362C-3	TSIA362C-2	TSIA362C-1	TSIA362C-0
continued	:00	TSIA362N-1	TSIA362N-0	TSIA362S-5	TSIA362S-4	TSIA362S-3	TSIA362S-2	TSIA362S-1	TSIA362S-0
0X1A5	:FE	TSIA372C-7	TSIA372C-6	TSIA372C-5	TSIA372C-4	TSIA372C-3	TSIA372C-2	TSIA372C-1	TSIA372C-0
continued	:00	TSIA372N-1	TSIA372N-0	TSIA372S-5	TSIA372S-4	TSIA372S-3	TSIA372S-2	TSIA372S-1	TSIA372S-0
0X1A6	:FE	TSIA382C-7	TSIA382C-6	TSIA382C-5	TSIA382C-4	TSIA382C-3	TSIA382C-2	TSIA382C-1	TSIA382C-0
continued	:00	TSIA382N-1	TSIA382N-0	TSIA382S-5	TSIA382S-4	TSIA382S-3	TSIA382S-2	TSIA382S-1	TSIA382S-0
0X1A7	:FE	TSIA392C-7	TSIA392C-6	TSIA392C-5	TSIA392C-4	TSIA392C-3	TSIA392C-2	TSIA392C-1	TSIA392C-0
continued	:00	TSIA392N-1	TSIA392N-0	TSIA392S-5	TSIA392S-4	TSIA392S-3	TSIA392S-2	TSIA392S-1	TSIA392S-0
0X1A8	:FE	TSIA402C-7	TSIA402C-6	TSIA402C-5	TSIA402C-4	TSIA402C-3	TSIA402C-2	TSIA402C-1	TSIA402C-0
continued	:00	TSIA402N-1	TSIA402N-0	TSIA402S-5	TSIA402S-4	TSIA402S-3	TSIA402S-2	TSIA402S-1	TSIA402S-0
0X1A9	:FE	TSIA412C-7	TSIA412C-6	TSIA412C-5	TSIA412C-4	TSIA412C-3	TSIA412C-2	TSIA412C-1	TSIA412C-0
continued	:00	TSIA412N-1	TSIA412N-0	TSIA412S-5	TSIA412S-4	TSIA412S-3	TSIA412S-2	TSIA412S-1	TSIA412S-0
0X1AA	:FE	TSIA422C-7	TSIA422C-6	TSIA422C-5	TSIA422C-4	TSIA422C-3	TSIA422C-2	TSIA422C-1	TSIA422C-0
continued	:00	TSIA422N-1	TSIA422N-0	TSIA422S-5	TSIA422S-4	TSIA422S-3	TSIA422S-2	TSIA422S-1	TSIA422S-0
0X1AB	:FE	TSIA432C-7	TSIA432C-6	TSIA432C-5	TSIA432C-4	TSIA432C-3	TSIA432C-2	TSIA432C-1	TSIA432C-0
continued	:00	TSIA432N-1	TSIA432N-0	TSIA432S-5	TSIA432S-4	TSIA432S-3	TSIA432S-2	TSIA432S-1	TSIA432S-0
0X1AC	:FE	TSIA442C-7	TSIA442C-6	TSIA442C-5	TSIA442C-4	TSIA442C-3	TSIA442C-2	TSIA442C-1	TSIA442C-0
continued	:00	TSIA442N-1	TSIA442N-0	TSIA442S-5	TSIA442S-4	TSIA442S-3	TSIA442S-2	TSIA442S-1	TSIA442S-0
0X1AD	:FE	TSIA452C-7	TSIA452C-6	TSIA452C-5	TSIA452C-4	TSIA452C-3	TSIA452C-2	TSIA452C-1	TSIA452C-0
continued	:00	TSIA452N-1	TSIA452N-0	TSIA452S-5	TSIA452S-4	TSIA452S-3	TSIA452S-2	TSIA452S-1	TSIA452S-0
0X1AE	:FE	TSIA462C-7	TSIA462C-6	TSIA462C-5	TSIA462C-4	TSIA462C-3	TSIA462C-2	TSIA462C-1	TSIA462C-0
continued	:00	TSIA462N-1	TSIA462N-0	TSIA462S-5	TSIA462S-4	TSIA462S-3	TSIA462S-2	TSIA462S-1	TSIA462S-0
0X1AF	:FE	TSIA472C-7	TSIA472C-6	TSIA472C-5	TSIA472C-4	TSIA472C-3	TSIA472C-2	TSIA472C-1	TSIA472C-0
continued	:00	TSIA472N-1	TSIA472N-0	TSIA472S-5	TSIA472S-4	TSIA472S-3	TSIA472S-2	TSIA472S-1	TSIA472S-0
TSI Bank 2 Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0X1B0	:00	0	0	0	0	0	0	0	0
continued	:7E	0	PARERR2LOC-5	PARERR2LOC-4	PARERR2LOC-3	PARERR2LOC-2	PARERR2LOC-1	PARERR2LOC-0	MEMPARERR2
0X1B1	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRD2
0X1B2	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRM2

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
0X1B3	:FF	TSIA152P	TSIA142P	TSIA132P	TSIA122P	TSIA112P	TSIA102P	TSIA092P	TSIA082P
continued	:FF	TSIA072P	TSIA062P	TSIA052P	TSIA042P	TSIA032P	TSIA022P	TSIA1012P	TSIA002P
0X1B4	:FF	TSIA312P	TSIA302P	TSIA292P	TSIA282P	TSIA272P	TSIA262P	TSIA252P	TSIA242P
continued	:FF	TSIA232P	TSIA222P	TSIA212P	TSIA202P	TSIA192P	TSIA182P	TSIA172P	TSIA162P
0X1B5	:FF	TSIA472P	TSIA462P	TSIA452P	TSIA442P	TSIA432P	TSIA422P	TSIA412P	TSIA402P
continued	:FF	TSIA392P	TSIA382P	TSIA372P	TSIA362P	TSIA352P	TSIA342P	TSIA332P	TSIA322P
Invalid Addresses									
0X1B6-0X1BF	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1
Active Connection Map, Bank 3 (R/O)									
0X1C0	:FE	TSIA003C-7	TSIA003C-6	TSIA003C-5	TSIA003C-4	TSIA003C-3	TSIA003C-2	TSIA003C-1	TSIA003C-0
continued	:00	TSIA003N-1	TSIA003N-0	TSIA003S-5	TSIA003S-4	TSIA003S-3	TSIA003S-2	TSIA003S-1	TSIA003S-0
0X1C1	:FE	TSIA013C-7	TSIA013C-6	TSIA013C-5	TSIA013C-4	TSIA013C-3	TSIA013C-2	TSIA013C-1	TSIA013C-0
continued	:00	TSIA013N-1	TSIA013N-0	TSIA013S-5	TSIA013S-4	TSIA013S-3	TSIA013S-2	TSIA013S-1	TSIA013S-0
0X1C2	:FE	TSIA023C-7	TSIA023C-6	TSIA023C-5	TSIA023C-4	TSIA023C-3	TSIA023C-2	TSIA023C-1	TSIA023C-0
continued	:00	TSIA023N-1	TSIA023N-0	TSIA023S-5	TSIA023S-4	TSIA023S-3	TSIA023S-2	TSIA023S-1	TSIA023S-0
0X1C3	:FE	TSIA033C-7	TSIA033C-6	TSIA033C-5	TSIA033C-4	TSIA033C-3	TSIA033C-2	TSIA033C-1	TSIA033C-0
continued	:00	TSIA033N-1	TSIA033N-0	TSIA033S-5	TSIA033S-4	TSIA033S-3	TSIA033S-2	TSIA033S-1	TSIA033S-0
0X1C4	:FE	TSIA043C-7	TSIA043C-6	TSIA043C-5	TSIA043C-4	TSIA043C-3	TSIA043C-2	TSIA043C-1	TSIA043C-0
continued	:00	TSIA043N-1	TSIA043N-0	TSIA043S-5	TSIA043S-4	TSIA043S-3	TSIA043S-2	TSIA043S-1	TSIA043S-0
0X1C5	:FE	TSIA053C-7	TSIA053C-6	TSIA053C-5	TSIA053C-4	TSIA053C-3	TSIA053C-2	TSIA053C-1	TSIA053C-0
continued	:00	TSIA053N-1	TSIA053N-0	TSIA053S-5	TSIA053S-4	TSIA053S-3	TSIA053S-2	TSIA053S-1	TSIA053S-0
0X1C6	:FE	TSIA063C-7	TSIA063C-6	TSIA063C-5	TSIA063C-4	TSIA063C-3	TSIA063C-2	TSIA063C-1	TSIA063C-0
continued	:00	TSIA063N-1	TSIA063N-0	TSIA063S-5	TSIA063S-4	TSIA063S-3	TSIA063S-2	TSIA063S-1	TSIA063S-0
0X1C7	:FE	TSIA073C-7	TSIA073C-6	TSIA073C-5	TSIA073C-4	TSIA073C-3	TSIA073C-2	TSIA073C-1	TSIA073C-0
continued	:00	TSIA073N-1	TSIA073N-0	TSIA073S-5	TSIA073S-4	TSIA073S-3	TSIA073S-2	TSIA073S-1	TSIA073S-0
0X1C8	:FE	TSIA083C-7	TSIA083C-6	TSIA083C-5	TSIA083C-4	TSIA083C-3	TSIA083C-2	TSIA083C-1	TSIA083C-0
continued	:00	TSIA083N-1	TSIA083N-0	TSIA083S-5	TSIA083S-4	TSIA083S-3	TSIA083S-2	TSIA083S-1	TSIA083S-0
0X1C9	:FE	TSIA093C-7	TSIA093C-6	TSIA093C-5	TSIA093C-4	TSIA093C-3	TSIA093C-2	TSIA093C-1	TSIA093C-0
continued	:00	TSIA093N-1	TSIA093N-0	TSIA093S-5	TSIA093S-4	TSIA093S-3	TSIA093S-2	TSIA093S-1	TSIA093S-0
0X1CA	:FE	TSIA103C-7	TSIA103C-6	TSIA103C-5	TSIA103C-4	TSIA103C-3	TSIA103C-2	TSIA103C-1	TSIA103C-0
continued	:00	TSIA103N-1	TSIA103N-0	TSIA103S-5	TSIA103S-4	TSIA103S-3	TSIA103S-2	TSIA103S-1	TSIA103S-0
0X1CB	:FE	TSIA113C-7	TSIA113C-6	TSIA113C-5	TSIA113C-4	TSIA113C-3	TSIA113C-2	TSIA113C-1	TSIA113C-0
continued	:00	TSIA113N-1	TSIA113N-0	TSIA113S-5	TSIA113S-4	TSIA113S-3	TSIA113S-2	TSIA113S-1	TSIA113S-0
0X1CC	:FE	TSIA123C-7	TSIA123C-6	TSIA123C-5	TSIA123C-4	TSIA123C-3	TSIA123C-2	TSIA123C-1	TSIA123C-0
continued	:00	TSIA123N-1	TSIA123N-0	TSIA123S-5	TSIA123S-4	TSIA123S-3	TSIA123S-2	TSIA123S-1	TSIA123S-0
0X1CD	:FE	TSIA133C-7	TSIA133C-6	TSIA133C-5	TSIA133C-4	TSIA133C-3	TSIA133C-2	TSIA133C-1	TSIA133C-0
continued	:00	TSIA133N-1	TSIA133N-0	TSIA133S-5	TSIA133S-4	TSIA133S-3	TSIA133S-2	TSIA133S-1	TSIA133S-0
0X1CE	:FE	TSIA143C-7	TSIA143C-6	TSIA143C-5	TSIA143C-4	TSIA143C-3	TSIA143C-2	TSIA143C-1	TSIA143C-0
continued	:00	TSIA143N-1	TSIA143N-0	TSIA143S-5	TSIA143S-4	TSIA143S-3	TSIA143S-2	TSIA143S-1	TSIA143S-0
0X1CF	:FE	TSIA153C-7	TSIA153C-6	TSIA153C-5	TSIA153C-4	TSIA153C-3	TSIA153C-2	TSIA153C-1	TSIA153C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA153N-1	TSIA153N-0	TSIA153S-5	TSIA153S-4	TSIA153S-3	TSIA153S-2	TSIA153S-1	TSIA153S-0
0X1D0	:FE	TSIA163C-7	TSIA163C-6	TSIA163C-5	TSIA163C-4	TSIA163C-3	TSIA163C-2	TSIA163C-1	TSIA163C-0
continued	:00	TSIA163N-1	TSIA163N-0	TSIA163S-5	TSIA163S-4	TSIA163S-3	TSIA163S-2	TSIA163S-1	TSIA163S-0
0X1D1	:FE	TSIA173C-7	TSIA173C-6	TSIA173C-5	TSIA173C-4	TSIA173C-3	TSIA173C-2	TSIA173C-1	TSIA173C-0
continued	:00	TSIA173N-1	TSIA173N-0	TSIA173S-5	TSIA173S-4	TSIA173S-3	TSIA173S-2	TSIA173S-1	TSIA173S-0
0X1D2	:FE	TSIA183C-7	TSIA183C-6	TSIA183C-5	TSIA183C-4	TSIA183C-3	TSIA183C-2	TSIA183C-1	TSIA183C-0
continued	:00	TSIA183N-1	TSIA183N-0	TSIA183S-5	TSIA183S-4	TSIA183S-3	TSIA183S-2	TSIA183S-1	TSIA183S-0
0X1D3	:FE	TSIA193C-7	TSIA193C-6	TSIA193C-5	TSIA193C-4	TSIA193C-3	TSIA193C-2	TSIA193C-1	TSIA193C-0
continued	:00	TSIA193N-1	TSIA193N-0	TSIA193S-5	TSIA193S-4	TSIA193S-3	TSIA193S-2	TSIA193S-1	TSIA193S-0
0X1D4	:FE	TSIA203C-7	TSIA203C-6	TSIA203C-5	TSIA203C-4	TSIA203C-3	TSIA203C-2	TSIA203C-1	TSIA203C-0
continued	:00	TSIA203N-1	TSIA203N-0	TSIA203S-5	TSIA203S-4	TSIA203S-3	TSIA203S-2	TSIA203S-1	TSIA203S-0
0X1D5	:FE	TSIA213C-7	TSIA213C-6	TSIA213C-5	TSIA213C-4	TSIA213C-3	TSIA213C-2	TSIA213C-1	TSIA213C-0
continued	:00	TSIA213N-1	TSIA213N-0	TSIA213S-5	TSIA213S-4	TSIA213S-3	TSIA213S-2	TSIA213S-1	TSIA213S-0
0X1D6	:FE	TSIA223C-7	TSIA223C-6	TSIA223C-5	TSIA223C-4	TSIA223C-3	TSIA223C-2	TSIA223C-1	TSIA223C-0
continued	:00	TSIA223N-1	TSIA223N-0	TSIA223S-5	TSIA223S-4	TSIA223S-3	TSIA223S-2	TSIA223S-1	TSIA223S-0
0X1D7	:FE	TSIA233C-7	TSIA233C-6	TSIA233C-5	TSIA233C-4	TSIA233C-3	TSIA233C-2	TSIA233C-1	TSIA233C-0
continued	:00	TSIA233N-1	TSIA233N-0	TSIA233S-5	TSIA233S-4	TSIA233S-3	TSIA233S-2	TSIA233S-1	TSIA233S-0
0X1D8	:FE	TSIA243C-7	TSIA243C-6	TSIA243C-5	TSIA243C-4	TSIA243C-3	TSIA243C-2	TSIA243C-1	TSIA243C-0
continued	:00	TSIA243N-1	TSIA243N-0	TSIA243S-5	TSIA243S-4	TSIA243S-3	TSIA243S-2	TSIA243S-1	TSIA243S-0
0X1D9	:FE	TSIA253C-7	TSIA253C-6	TSIA253C-5	TSIA253C-4	TSIA253C-3	TSIA253C-2	TSIA253C-1	TSIA253C-0
continued	:00	TSIA253N-1	TSIA253N-0	TSIA253S-5	TSIA253S-4	TSIA253S-3	TSIA253S-2	TSIA253S-1	TSIA253S-0
0X1DA	:FE	TSIA263C-7	TSIA263C-6	TSIA263C-5	TSIA263C-4	TSIA263C-3	TSIA263C-2	TSIA263C-1	TSIA263C-0
continued	:00	TSIA263N-1	TSIA263N-0	TSIA263S-5	TSIA263S-4	TSIA263S-3	TSIA263S-2	TSIA263S-1	TSIA263S-0
0X1DB	:FE	TSIA273C-7	TSIA273C-6	TSIA273C-5	TSIA273C-4	TSIA273C-3	TSIA273C-2	TSIA273C-1	TSIA273C-0
continued	:00	TSIA273N-1	TSIA273N-0	TSIA273S-5	TSIA273S-4	TSIA273S-3	TSIA273S-2	TSIA273S-1	TSIA273S-0
0X1DC	:FE	TSIA283C-7	TSIA283C-6	TSIA283C-5	TSIA283C-4	TSIA283C-3	TSIA283C-2	TSIA283C-1	TSIA283C-0
continued	:00	TSIA283N-1	TSIA283N-0	TSIA283S-5	TSIA283S-4	TSIA283S-3	TSIA283S-2	TSIA283S-1	TSIA283S-0
0X1DD	:FE	TSIA293C-7	TSIA293C-6	TSIA293C-5	TSIA293C-4	TSIA293C-3	TSIA293C-2	TSIA293C-1	TSIA293C-0
continued	:00	TSIA293N-1	TSIA293N-0	TSIA293S-5	TSIA293S-4	TSIA293S-3	TSIA293S-2	TSIA293S-1	TSIA293S-0
0X1DE	:FE	TSIA303C-7	TSIA303C-6	TSIA303C-5	TSIA303C-4	TSIA303C-3	TSIA303C-2	TSIA303C-1	TSIA303C-0
continued	:00	TSIA303N-1	TSIA303N-0	TSIA303S-5	TSIA303S-4	TSIA303S-3	TSIA303S-2	TSIA303S-1	TSIA303S-0
0X1DF	:FE	TSIA313C-7	TSIA313C-6	TSIA313C-5	TSIA313C-4	TSIA313C-3	TSIA313C-2	TSIA313C-1	TSIA313C-0
continued	:00	TSIA313N-1	TSIA313N-0	TSIA313S-5	TSIA313S-4	TSIA313S-3	TSIA313S-2	TSIA313S-1	TSIA313S-0
0X1E0	:FE	TSIA323C-7	TSIA323C-6	TSIA323C-5	TSIA323C-4	TSIA323C-3	TSIA323C-2	TSIA323C-1	TSIA323C-0
continued	:00	TSIA323N-1	TSIA323N-0	TSIA323S-5	TSIA323S-4	TSIA323S-3	TSIA323S-2	TSIA323S-1	TSIA323S-0
0X1E1	:FE	TSIA333C-7	TSIA333C-6	TSIA333C-5	TSIA333C-4	TSIA333C-3	TSIA333C-2	TSIA333C-1	TSIA333C-0
continued	:00	TSIA333N-1	TSIA333N-0	TSIA333S-5	TSIA333S-4	TSIA333S-3	TSIA333S-2	TSIA333S-1	TSIA333S-0
0X1E2	:FE	TSIA343C-7	TSIA343C-6	TSIA343C-5	TSIA343C-4	TSIA343C-3	TSIA343C-2	TSIA343C-1	TSIA343C-0
continued	:00	TSIA343N-1	TSIA343N-0	TSIA343S-5	TSIA343S-4	TSIA343S-3	TSIA343S-2	TSIA343S-1	TSIA343S-0
0X1E3	:FE	TSIA353C-7	TSIA353C-6	TSIA353C-5	TSIA353C-4	TSIA353C-3	TSIA353C-2	TSIA353C-1	TSIA353C-0
continued	:00	TSIA353N-1	TSIA353N-0	TSIA353S-5	TSIA353S-4	TSIA353S-3	TSIA353S-2	TSIA353S-1	TSIA353S-0
0X1E4	:FE	TSIA363C-7	TSIA363C-6	TSIA363C-5	TSIA363C-4	TSIA363C-3	TSIA363C-2	TSIA363C-1	TSIA363C-0

Table 20. TSI Register Map *(continued)*

Address Offset	Initial Value (8MSb)	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-8
Continued	Initial Value (8LSb)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	TSIA363N-1	TSIA363N-0	TSIA363S-5	TSIA363S-4	TSIA363S-3	TSIA363S-2	TSIA363S-1	TSIA363S-0
0X1E5	:FE	TSIA373C-7	TSIA373C-6	TSIA373C-5	TSIA373C-4	TSIA373C-3	TSIA373C-2	TSIA373C-1	TSIA373C-0
continued	:00	TSIA373N-1	TSIA373N-0	TSIA373S-5	TSIA373S-4	TSIA373S-3	TSIA373S-2	TSIA373S-1	TSIA373S-0
0X1E6	:FE	TSIA383C-7	TSIA383C-6	TSIA383C-5	TSIA383C-4	TSIA383C-3	TSIA383C-2	TSIA383C-1	TSIA383C-0
continued	:00	TSIA383N-1	TSIA383N-0	TSIA383S-5	TSIA383S-4	TSIA383S-3	TSIA383S-2	TSIA383S-1	TSIA383S-0
0X1E7	:FE	TSIA393C-7	TSIA393C-6	TSIA393C-5	TSIA393C-4	TSIA393C-3	TSIA393C-2	TSIA393C-1	TSIA393C-0
continued	:00	TSIA393N-1	TSIA393N-0	TSIA393S-5	TSIA393S-4	TSIA393S-3	TSIA393S-2	TSIA393S-1	TSIA393S-0
0X1E8	:FE	TSIA403C-7	TSIA403C-6	TSIA403C-5	TSIA403C-4	TSIA403C-3	TSIA403C-2	TSIA403C-1	TSIA403C-0
continued	:00	TSIA403N-1	TSIA403N-0	TSIA403S-5	TSIA403S-4	TSIA403S-3	TSIA403S-2	TSIA403S-1	TSIA403S-0
0X1E9	:FE	TSIA413C-7	TSIA413C-6	TSIA413C-5	TSIA413C-4	TSIA413C-3	TSIA413C-2	TSIA413C-1	TSIA413C-0
continued	:00	TSIA413N-1	TSIA413N-0	TSIA413S-5	TSIA413S-4	TSIA413S-3	TSIA413S-2	TSIA413S-1	TSIA413S-0
0X1EA	:FE	TSIA423C-7	TSIA423C-6	TSIA423C-5	TSIA423C-4	TSIA423C-3	TSIA423C-2	TSIA423C-1	TSIA423C-0
continued	:00	TSIA423N-1	TSIA423N-0	TSIA423S-5	TSIA423S-4	TSIA423S-3	TSIA423S-2	TSIA423S-1	TSIA423S-0
0X1EB	:FE	TSIA433C-7	TSIA433C-6	TSIA433C-5	TSIA433C-4	TSIA433C-3	TSIA433C-2	TSIA433C-1	TSIA433C-0
continued	:00	TSIA433N-1	TSIA433N-0	TSIA433S-5	TSIA433S-4	TSIA433S-3	TSIA433S-2	TSIA433S-1	TSIA433S-0
0X1EC	:FE	TSIA443C-7	TSIA443C-6	TSIA443C-5	TSIA443C-4	TSIA443C-3	TSIA443C-2	TSIA443C-1	TSIA443C-0
continued	:00	TSIA443N-1	TSIA443N-0	TSIA443S-5	TSIA443S-4	TSIA443S-3	TSIA443S-2	TSIA443S-1	TSIA443S-0
0X1ED	:FE	TSIA453C-7	TSIA453C-6	TSIA453C-5	TSIA453C-4	TSIA453C-3	TSIA453C-2	TSIA453C-1	TSIA453C-0
continued	:00	TSIA453N-1	TSIA453N-0	TSIA453S-5	TSIA453S-4	TSIA453S-3	TSIA453S-2	TSIA453S-1	TSIA453S-0
0X1EE	:FE	TSIA463C-7	TSIA463C-6	TSIA463C-5	TSIA463C-4	TSIA463C-3	TSIA463C-2	TSIA463C-1	TSIA463C-0
continued	:00	TSIA463N-1	TSIA463N-0	TSIA463S-5	TSIA463S-4	TSIA463S-3	TSIA463S-2	TSIA463S-1	TSIA463S-0
0X1EF	:FE	TSIA473C-7	TSIA473C-6	TSIA473C-5	TSIA473C-4	TSIA473C-3	TSIA473C-2	TSIA473C-1	TSIA473C-0
continued	:00	TSIA473N-1	TSIA473N-0	TSIA473S-5	TSIA473S-4	TSIA473S-3	TSIA473S-2	TSIA473S-1	TSIA473S-0
TSI Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0X1F0	:00	0	0	0	0	0	0	0	0
continued	:7E	0	PARERR3LOC-5	PARERR3LOC-4	PARERR3LOC-3	PARERR3LOC-2	PARERR3LOC-1	PARERR3LOC-0	MEMPARERR3
0X1F1	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRD3
0X1F2	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	MEMPARERRM3
0X1F3	:FF	TSIA153P	TSIA143P	TSIA133P	TSIA123P	TSIA113P	TSIA103P	TSIA093P	TSIA083P
continued	:FF	TSIA073P	TSIA063P	TSIA053P	TSIA043P	TSIA033P	TSIA023P	TSIA1013P	TSIA003P
0X1F4	:Ff	TSIA313P	TSIA303P	TSIA293P	TSIA283P	TSIA273P	TSIA263P	TSIA253P	TSIA243P
continued	:FF	TSIA233P	TSIA223P	TSIA213P	TSIA203P	TSIA193P	TSIA183P	TSIA173P	TSIA163P
0X1F5	:FF	TSIA473P	TSIA463P	TSIA453P	TSIA443P	TSIA433P	TSIA423P	TSIA413P	TSIA403P
continued	:FF	TSIA393P	TSIA383P	TSIA373P	TSIA363P	TSIA353P	TSIA343P	TSIA333P	TSIA323P
Invalid Addresses									
0X1F6-0X1FF	:NA	1	1	1	1	1	1	1	1
continued	:NA	1	1	1	1	1	1	1	1

Table 21. TSI Register Map Signals

Signal Name	Description	Bit Width
Control Bits (R/W)		
TSISxxyC	For time slot xx, bank y, the physical channel (0-135) or special frame code where its data is obtained after the next configuration update. TSIS000C is the only word used in transparent mode.	8
TSISxxyS	For time slot xx, bank y, the time slot (0-47) where its data is obtained after the next configuration update.	6
TSISxxyN	For time slot xx, bank y, the nibble or bit pair where its data is obtained after the next configuration update.	2
TSITRNSPNT0	Transparent mode control for output 0. TSITRNSPNT0 = 0, normal Time Slot Interchange is enabled. TSITRNSPNT0 = 1, Time Slot Interchange is disabled and all data from the input selected by TSIA000C is routed to dout0.	1
TSITRNSPNT1	Transparent mode control for output 1. Valid only in HFBS1, HFBS2, and FFBS1 modes. TSITRNSPNT1 = 0, normal Time Slot Interchange is enabled. TSITRNSPNT1 = 1, Time Slot Interchange is disabled and all data from the input selected by TSIA002C is routed to dout 1.	1
DOMAIN0	Frame Domain mode control for output 0. DOMAIN0 = 0, use fsynci0 and new_cfg0 for controlling transfer between standby and active registers. DOMAIN0 = 1, use fsynci1 and new_cfg1 for controlling transfer between standby and active registers.	1
DOMAIN1	Frame Domain mode control for output 1. Valid only in HFBS1, HFBS2, and FFBS1 modes. DOMAIN1 = 0, use fsynci0 and new_cfg0 for controlling transfer between standby and active registers. DOMAIN1 = 1, use fsynci1 and new_cfg1 for controlling transfer between standby and active registers.	1
Status Bits (R/O)		
TSIAxxyC	For time slot xx, bank y, the physical channel (0-135) or special frame code where its data is obtained. TSIA000C is the only word used in transparent mode.	8
TSIAxxyS	For time slot xx, bank y, the time slot (0-47) where its data is obtained.	6
TSIAxxyN	For time slot xx, bank y, the nibble or bit-pair where its data is obtained.	1
TSIAxxyP	For time slot xx, bank y, the even parity of the word formed by TSIAxxyC, TSIAxxyS, TSIAxxyN.	1
MEMPARERR0	Indicates a memory parity error has occurred within the active configuration map bank 0.	1
MEMPARERR1	Indicated a memory parity error has occurred within the active configuration map bank 1.	1
MEMPARERR2	Indicates a memory parity error has occurred within the active configuration map bank 2.	1
MEMPARERR3	Indicated a memory parity error has occurred within the active configuration map bank 3.	1
PARERR0LOC[5:0]	Indicates the location (time slot) at which an error occurred. The contents are invalid when MEMPARERR0 = 0.	6
PARERR1LOC[5:0]	Indicates the location (time slot) at which an error occurred. The contents are invalid when MEMPARERR1 = 0.	6
PARERR2LOC[5:0]	Indicates the location time slot) at which an error occurred. The contents are invalid when MEMPARERR2 = 0.	6
PARERR3LOC[5:0]	Indicates the location (time slot) at which an error occurred. The contents are invalid when MEMPARERR3 = 0.	6
Delta Bits (R/O, Clear on R)		
MEMPARERRD0	Indicates a change in MEMPARERR0.	1
MEMPARERRD1	Indicated a change in MEMPARERR1.	1
MEMPARERRD2	Indicates a change in MEMPARERR2.	1

Table 21. TSI Register Map Signals *(continued)*

Signal Name	Description	Bit Width
MEMPARERRD3	Indicated a change in MEMPARERR3.	1
Event Bits (R/O, Clear on R)		
(none)		
Mask Bits (R/W)		
MEMPARERRM0	Mask bit for MEMPARERRD0.	
MEMPARERRM1	Mask bit for MEMPARERRD1.	
MEMPARERRM2	Mask bit for MEMPARERRD2.	
MEMPARERRM3	Mask bit for MEMPARERRD3.	

3.3 BPRx Register Map

BPRx has a 64-word address space. Unused bits (labeled 0) are not implemented in hardware.

Table 22. BPRx Register Map

Address Offset	Initial Value (8MSB	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-0
Continued	Initial Value (8LSB)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
(R/W - Control Bits)									
BPRX Controls									
0x00	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	BENAB	BENAA	FM_SEL	FRMDELTSTMOD	FIFORESET	SOFTRESET
0x01	:00	0	0	0	0	0	0	0	0
continued	:00	0	FSYNC_SEL	LOSTXCNT1	LOSTXCNT0	BPDSCRINH	BPAISINH	BPRXTRNSPNT	BPRXTHRU
0x02	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	STS12SEL	QFR	UNEQ	FBPAIS
0x03	:00	0	0	0	0	0	B1FRMCNT-4	B1FRMCNT-3	B1FRMCNT-2
continued	:00	B1FRMCNT-1	B1FRMCNT-0	B1ERRTH-5	B1ERRTH-4	B1ERRTH-3	B1ERRTH-2	B1ERRTH-1	B1ERRTH-0
Overhead Monitor Controls									
0x04	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	BPIROW-3	BPIROW-2	BPIROW-1	BPIROW-0	BPICOL-1	BPICOL-0
0X05	:00	0	0	0	0	XBI_TS(0)-5	XBI_TS(0)-4	XBI_TS(0)-3	XBI_TS(0)-2
continued	:00	XBI_TS(0)-1	XBI_TS(0)-0	XBI_ROW(0)-3	XBI_ROW(0)-2	XBI_ROW(0)-1	XBI_ROW(0)-0	XBI_COL(0)-1	XBI_COL(0)-0
0X06	:00	0	0	0	0	XBI_TS(1)-5	XBI_TS(1)-4	XBI_TS(1)-3	XBI_TS(1)-2
continued	:00	XBI_TS(1)-1	XBI_TS(1)-0	XBI_ROW(1)-3	XBI_ROW(1)-2	XBI_ROW(1)-1	XBI_ROW(1)-0	XBI_COL(1)-1	XBI_COL(1)-0
0X07	:00	0	0	0	0	XBI_TS(2)-5	XBI_TS(2)-4	XBI_TS(2)-3	XBI_TS(2)-2
continued	:00	XBI_TS(2)-1	XBI_TS(2)-0	XBI_ROW(2)-3	XBI_ROW(2)-2	XBI_ROW(2)-1	XBI_ROW(2)-0	XBI_COL(2)-1	XBI_COL(2)-0
0X08	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI_TS(0)-1	XXBI_TS(0)-0	XXBI_ROW(0)-3	XXBI_ROW(0)-2	XXBI_ROW(0)-1	XXBI_ROW(0)-0	XXBI_COL(0)-1	XXBI_COL(0)-0
0X09	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI_TS(1)-1	XXBI_TS(1)-0	XXBI_ROW(1)-3	XXBI_ROW(1)-2	XXBI_ROW(1)-1	XXBI_ROW(1)-0	XXBI_COL(1)-1	XXBI_COL(1)-0
0X0A	:00	0	0	0	0	0	0	0	0

Table 22. BPRx Register Map *(continued)*

Address Offset	Initial Value (8MSB	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-0
Continued	Initial Value (8LSB)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	XXBI_TS(2)-1	XXBI_TS(2)-0	XXBI_ROW(2)-3	XXBI_ROW(2)-2	XXBI_ROW(2)-1	XXBI_ROW(2)-0	XXBI_COL(2)-1	XXBI_COL(2)-0
HSIRX Controls									
0X0B	:00	0	0	0	0	0	0	0	0
continued	:00	RXGPC-7	RXGPC-6	RXGPC-5	RXGPC-4	RXGPC-3	RXGPC-2	RXGPC-1	RXGPC-0
0X0C	:00	0	0	0	0	0	0	RXREFSEL-1	RXREFSEL-0
continued	:00	RXLOSTH-1	RXLOSTH-0	RXPWROFF	RXTERMCTL	RXEQCTRL-3	RXEQCTRL-2	RXEQCTRL-1	RXEQCTRL-0
BPRx Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0X0D	:00	BPSYNCDIFF-15	BPSYNCDIFF-14	BPSYNCDIFF-13	BPSYNCDIFF-12	BPSYNCDIFF-11	BPSYNCDIFF-10	BPSYNCDIFF-9	BPSYNCDIFF-8
continued	:00	BPSYNCDIFF-7	BPSYNCDIFF-6	BPSYNCDIFF-5	BPSYNCDIFF-4	BPSYNCDIFF-3	BPSYNCDIFF-2	BPSYNCDIFF-1	BPSYNCDIFF-0
0x0E	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOF
0x0F	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOFD
0x10	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOFM
0x11	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOA
0x12	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOAD
0x13	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	OOAM
0x14	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	LOS
0x15	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	LOSD
0x16	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	LOSM
0x17	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESOFLOW
0x18	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESOFLOWD
0x19	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESOFLOWM
0x1A	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESUFLOW
0x1B	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESUFLOWD
0x1C	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	ESUFLOWM
0x1D	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	B1ERRE
0x1E	:00	0	0	0	0	0	0	0	0

Table 22. BPRx Register Map *(continued)*

Address Offset	Initial Value (8MSB	MSb Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSb Microprocessor bit-0
Continued	Initial Value (8LSB)	MSb Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSb Microprocessor bit-0
continued	:00	0	0	0	0	0	0	0	B1ERRD
0x1F	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	B1ERRM
HSIRx Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0x20	:NA	ELSTC_ENDFLG	ELSTC_RAM_FM	RAM_ENDFLG	RAM_FM	RXGPS-7	RXGPS-6	RXGPS-5	RXGPS-4
continued	:NA	RXGPS-3	RXGPS-2	RXGPS-1	RXGPS-0	RXNOREF	RXLOLHI	RXLOLLO	RXLOL
0x21	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	RXLOLD
0x22	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	RXLOLM
0x23	:NA	0	0	0	0	0	0	0	0
continued	:NA	0	0	0	0	0	0	0	RXLOS
0x24	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	RXLOSD
0x25	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	RXLOSM
Invalid Addresses									
0X26-0x3F	:NA	0	0	0	0	0	0	0	0
continued	:NA	0	0	0	0	0	0	0	0

Table 23. BPRx Register Map Signals

Signal Name	Description	Bit Width
BPTX Control Bits (R/W)		
QFR	QFR is used to indicate a quick framing sequence. If QFR = 0, the framer takes 2 consecutive good frames (with correct framing patterns) to go in-frame and 5 bad frames to go out-of-frame (OOF). If QFR = 1, the framer takes 1 good frame to go In-frame and 1 bad frame to go OOF.	1
UNEQ	Unequipped port. If UNEQ = 0, the current port will not zero fill. If UNEQ = 1, the current port will zero fill the payload (except A1 and A2 bytes), H2 and H3 replace the payload with zeros, and insert 68h in the H1 bytes.	1
BPDSCRINH	Descramble-inhibit. Bit used to inhibit descrambling on the input data at BPRX. When BPDSCRINH = 0, data on all ports of a group is descrambled. When BPDSCRINH = 1, data on all ports of a group is not descrambled.	1
BPAISINH	BP-AIS-inhibit. Bit inhibits the automatic insertion of AIS on the port When BPAISINH = 0, automatic AIS insertion is enabled. When BPAISINH = 1, automatic AIS insertion is inhibited.	1
FBPAIS	Force-BP-AIS. Bit forces the insertion of AIS in the port. FBPAISn has priority over BPAISINH. When FBPAIS = 0, force AIS insertion is disabled. When FBPAIS = 1, force AIS insertion is enabled.	1
B1ERRTH[5:0]	B1 error threshold. Number of B1 errors allowed in a selected number of frames before a B1 event is triggered.	6

Table 23. BPRx Register Map Signals *(continued)*

Signal Name	Description	Bit Width
B1FRMCNT[4:0]	Number of frames over which B1 errors are accumulated. 1 to 32 frames.	5
LOSTXCNT[1:0]	Set consecutive transitionless bit count which is required if declaring an LOS due to lack of transitions. 00: 256 bits 01: 512 bits 10: 1024 bits 11: Unused	2
BPRXTRNSPNT	Enable Transparent mode. 0: Transparent mode is off (default) 1: Transparent mode is on	1
BPRXTHRU	Enable Total Transparent mode. 0: Through mode is off 1: Through mode is on and data will not be aligned or framed	1
STS12SEL	Enable STS12 operation mode. 0: STS48 mode 1: STS12 mode	1
FIFORESET	Force an elastic store FIFO reset. 0: Normal operation 1: Output FIFO is held in reset	1
SOFTRESET	Force reset of all flip-flops in the block. 0: Normal operation 1: All flip-flops held in reset	1
FRMDELTSTMOD	Vitesse use only. Leave at a value of 0.	1
FSYNC_SEL	Select Frame Sync domain. 0: frm_sync_l (lower) 1: frm_sync_u (upper)	1
Overhead Monitor Control Bits (R/W)		
BPIROW[3:0]	1-9: Row location for capture of 48 contiguous overhead bytes.	4
BPICOL[1:0]	1-3: Column location for capture of 48 contiguous overhead bytes.	2
XBIx_ROW[3:0], x = 1,2,3	1-9: Row location for capture of additional byte x.	4
XBIx_COL[1:0], x = 1,2,3	1-3: Column location for capture of additional byte x.	2
XBIx_TS[1:0], x = 1,2,3	0-47: Time slot location for capture of additional byte x.	6
XXBIx_ROW[3:0], x = 1,2,3	1-9: Row location for capture of extra additional byte group xx.	4
XXBIx_COL[1:0], x = 1,2,3	1-3: Column location for capture of extra additional byte group xx.	2
XXBIx_TS[1:0], x = 1,2,3	0-2: Group of 16 (first, second, third) for capture of extra additional byte group xx.	6
HSIRX Control Bits (R/W)		
RXPWROFF	Power off associated HSIRx block.	1
RXEQCTRL[3:0]	Equalization setting for HSIRx input cell.	4
RXLOSTH[1:0]	Loss of signal threshold for HSIRx input cell.	2
RXTERMCTL	Termination mode control for HSIRx input cell.	1
RXREFSEL[1:0]	Vitesse use only. Leave at a value of 00.	2
RXGPC[7:0]	General purpose control bits to HSIRx (reserved for Vitesse use only).	8

Table 23. BPRx Register Map Signals *(continued)*

Signal Name	Description	Bit Width
BPRX Status Bits (R/O)		
OOF	Out of frame indication.	1
OOA	Out of alignment indication.	1
LOS	Composite result of RXLOS and transition detector (no transitions in 32 consecutive bytes before descrambling).	1
ESOFLOW	Elastic store overflow alarm.	1
ESUFLOW	Elastic store underflow alarm.	1
BPSYNCDIFF[15:0]	Indicates difference in core clock cycles between internal frame sync and frame sync extracted from incoming data.	16
RXGPS[7:0]	General purpose status bits from HSIRx (reserved for Vitesse use only).	8
HSIRX Status Bits (R/O)		
RXLOL	Indicates loss of lock from HSITx clock multiplier PLL (HSITx internally ORs TXLOLHI and TXLOLLO).	1
RXLOLHI	Indicates loss of lock, frequency out of range high, from HSITx clock multiplier PLL.	1
RXLOLLO	Indicates loss of lock, frequency out of range low, from HSITx clock multiplier PLL.	1
RXLOS	Indicates input signal strength below threshold set by LOSTH.	1
RXNOREF	Indicates invalid reference frequency applied or selected. This triggers an RXLOL, so there are no delta or mask bits.	1
Delta Bits (R/O, clear on read)		
RXLOLD	Delta bit to indicate change in status of RXLOL.	1
RXLOSD	Delta bit to indicate change in status of RXLOS.	1
LOSD	Delta bit to indicate change in status of LOS.	1
OOFD	Delta bit to indicate change in status of OOF.	1
OOAD	Delta bit to indicate change in status of OOA.	1
ESOFLOWD	Elastic store overflow alarm delta bit.	1
ESUFLOWD	Elastic store underflow alarm delta bit.	1
B1ERRD	B1 error event delta bit.	1
Event Bits (R/O, clear on read)		
B1ERRE	B1 error indication event bits are used for B1 error tracking. B1ERRE[n] = 0, indicates no errors were detected. B1ERRE[n] = 1, indicates the B1 error threshold was exceeded in the selected number of frames.	1
Mask Bits (R/W)		
RXLOLM	Interrupt mask bit for RXLOLD.	1
RXLOSM	Interrupt mask bit for RXLOSD.	1
LOSM	Interrupt mask bit for LOSD.	1
OOFM	Interrupt mask bit for OOFD.	1
OOAM	Interrupt mask bit for OOAD.	1
B1ERRM	Interrupt mask bit for B1ERRD.	1
ESOFLOWM	Interrupt mask bit for ESOFLOW.	1
ESUFLOWM	Interrupt mask bit for ESUFLOW.	1

3.4 BPTx Register Map

BPTx has a 128-word address space. See the register map for the base addresses of BPTx blocks.

Table 24. BPTx Register Map

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
R/W Control Bits									
BPTX Controls (R/W)									
0x00	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	BENAB(1)	BENAA(1)	FM_SEL(1)	FIFORESET	SOFTRESET
0x01	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	BPSCRAMB	A1A2ERRINS	B1ERRINS	B1CALCB	BPTXTRNSPNT	RDIE
0x02	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	STS12SEL	TFI_FIVEB	AISINS
BPTX Provisionable Overhead Byte Insertion Controls (R/W)									
0x03	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	BPIROW-3	BPIROW-2	BPIROW-1	BPIROW-0	BPICOL-1	BPICOL-0
0x04	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	XXBI_MODE	XBI_MODE	BPI_MODE
0X05	:00	0	0	0	0	XBI_TS(0)-5	XBI_TS(0)-4	XBI_TS(0)-3	XBI_TS(0)-2
continued	:00	XBI_TS(0)-1	XBI_TS(0)-0	XBI_ROW(0)-3	XBI_ROW(0)-2	XBI_ROW(0)-1	XBI_ROW(0)-0	XBI_COL(0)-1	XBI_COL(0)-0
0X06	:00	0	0	0	0	XBI_TS(1)-5	XBI_TS(1)-4	XBI_TS(1)-3	XBI_TS(1)-2
continued	:00	XBI_TS(1)-1	XBI_TS(1)-0	XBI_ROW(1)-3	XBI_ROW(1)-2	XBI_ROW(1)-1	XBI_ROW(1)-0	XBI_COL(1)-1	XBI_COL(1)-0
0X07	:00	0	0	0	0	XBI_TS(2)-5	XBI_TS(2)-4	XBI_TS(2)-3	XBI_TS(2)-2
continued	:00	XBI_TS(2)-1	XBI_TS(2)-0	XBI_ROW(2)-3	XBI_ROW(2)-2	XBI_ROW(2)-1	XBI_ROW(2)-0	XBI_COL(2)-1	XBI_COL(2)-0
0X08	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI_TS(0)-1	XXBI_TS(0)-0	XXBI_ROW(0)-3	XXBI_ROW(0)-2	XXBI_ROW(0)-1	XXBI_ROW(0)-0	XXBI_COL(0)-1	XXBI_COL(0)-0
0X09	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI_TS(1)-1	XXBI_TS(1)-0	XXBI_ROW(1)-3	XXBI_ROW(1)-2	XXBI_ROW(1)-1	XXBI_ROW(1)-0	XXBI_COL(1)-1	XXBI_COL(1)-0
0X0A	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI_TS(2)-1	XXBI_TS(2)-0	XXBI_ROW(2)-3	XXBI_ROW(2)-2	XXBI_ROW(2)-1	XXBI_ROW(2)-0	XXBI_COL(2)-1	XXBI_COL(2)-0
BPTX Provisionable Overhead Bytes (R/W)									
0X0B	:00	0	0	0	0	0	0	0	0
continued	:00	XBI(0)-7	XBI(0)-6	XBI(0)-5	XBI(0)-4	XBI(0)-3	XBI(0)-2	XBI(0)-1	XBI(0)-0
0X0C	:00	0	0	0	0	0	0	0	0
continued	:00	XBI(1)-7	XBI(1)-6	XBI(1)-5	XBI(1)-4	XBI(1)-3	XBI(1)-2	XBI(1)-1	XBI(1)-0
0X0D	:00	0	0	0	0	0	0	0	0
continued	:00	XBI(2)-7	XBI(2)-6	XBI(2)-5	XBI(2)-4	XBI(2)-3	XBI(2)-2	XBI(2)-1	XBI(2)-0
0X0E	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-0-7	XXBI(0)-0-6	XXBI(0)-0-5	XXBI(0)-0-4	XXBI(0)-0-3	XXBI(0)-0-2	XXBI(0)-0-1	XXBI(0)-0-0
0X0F	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-1-7	XXBI(0)-1-6	XXBI(0)-1-5	XXBI(0)-1-4	XXBI(0)-1-3	XXBI(0)-1-2	XXBI(0)-1-1	XXBI(0)-1-0
0X10	:00	0	0	0	0	0	0	0	0

Table 24. BPTx Register Map *(continued)*

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
continued	:00	XXBI(0)-2-7	XXBI(0)-2-6	XXBI(0)-2-5	XXBI(0)-2-4	XXBI(0)-2-3	XXBI(0)-2-2	XXBI(0)-2-1	XXBI(0)-2-0
0X11	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-3-7	XXBI(0)-3-6	XXBI(0)-3-5	XXBI(0)-3-4	XXBI(0)-3-3	XXBI(0)-3-2	XXBI(0)-3-1	XXBI(0)-3-0
0X12	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-4-7	XXBI(0)-4-6	XXBI(0)-4-5	XXBI(0)-4-4	XXBI(0)-4-3	XXBI(0)-4-2	XXBI(0)-4-1	XXBI(0)-4-0
0X13	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-5-7	XXBI(0)-5-6	XXBI(0)-5-5	XXBI(0)-5-4	XXBI(0)-5-3	XXBI(0)-5-2	XXBI(0)-5-1	XXBI(0)-5-0
0X14	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-6-7	XXBI(0)-6-6	XXBI(0)-6-5	XXBI(0)-6-4	XXBI(0)-6-3	XXBI(0)-6-2	XXBI(0)-6-1	XXBI(0)-6-0
0X15	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-7-7	XXBI(0)-7-6	XXBI(0)-7-5	XXBI(0)-7-4	XXBI(0)-7-3	XXBI(0)-7-2	XXBI(0)-7-1	XXBI(0)-7-0
0X16	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-8-7	XXBI(0)-8-6	XXBI(0)-8-5	XXBI(0)-8-4	XXBI(0)-8-3	XXBI(0)-8-2	XXBI(0)-8-1	XXBI(0)-8-0
0X17	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-9-7	XXBI(0)-9-6	XXBI(0)-9-5	XXBI(0)-9-4	XXBI(0)-9-3	XXBI(0)-9-2	XXBI(0)-9-1	XXBI(0)-9-0
0X18	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-10-7	XXBI(0)-10-6	XXBI(0)-10-5	XXBI(0)-10-4	XXBI(0)-10-3	XXBI(0)-10-2	XXBI(0)-10-1	XXBI(0)-10-0
0X19	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-11-7	XXBI(0)-11-6	XXBI(0)-11-5	XXBI(0)-11-4	XXBI(0)-11-3	XXBI(0)-11-2	XXBI(0)-11-1	XXBI(0)-11-0
0X1a	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-12-7	XXBI(0)-12-6	XXBI(0)-12-5	XXBI(0)-12-4	XXBI(0)-12-3	XXBI(0)-12-2	XXBI(0)-12-1	XXBI(0)-12-0
0X1b	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-13-7	XXBI(0)-13-6	XXBI(0)-13-5	XXBI(0)-13-4	XXBI(0)-13-3	XXBI(0)-13-2	XXBI(0)-13-1	XXBI(0)-13-0
0X1c	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-14-7	XXBI(0)-14-6	XXBI(0)-14-5	XXBI(0)-14-4	XXBI(0)-14-3	XXBI(0)-14-2	XXBI(0)-14-1	XXBI(0)-14-0
0X1d	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(0)-15-7	XXBI(0)-15-6	XXBI(0)-15-5	XXBI(0)-15-4	XXBI(0)-15-3	XXBI(0)-15-2	XXBI(0)-15-1	XXBI(0)-15-0
0X1E	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-0-7	XXBI(1)-0-6	XXBI(1)-0-5	XXBI(1)-0-4	XXBI(1)-0-3	XXBI(1)-0-2	XXBI(1)-0-1	XXBI(1)-0-0
0X1f	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-1-7	XXBI(1)-1-6	XXBI(1)-1-5	XXBI(1)-1-4	XXBI(1)-1-3	XXBI(1)-1-2	XXBI(1)-1-1	XXBI(1)-1-0
0X20	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-2-7	XXBI(1)-2-6	XXBI(1)-2-5	XXBI(1)-2-4	XXBI(1)-2-3	XXBI(1)-2-2	XXBI(1)-2-1	XXBI(1)-2-0
0X21	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-3-7	XXBI(1)-3-6	XXBI(1)-3-5	XXBI(1)-3-4	XXBI(1)-3-3	XXBI(1)-3-2	XXBI(1)-3-1	XXBI(1)-3-0
0X22	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-4-7	XXBI(1)-4-6	XXBI(1)-4-5	XXBI(1)-4-4	XXBI(1)-4-3	XXBI(1)-4-2	XXBI(1)-4-1	XXBI(1)-4-0
0X23	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-5-7	XXBI(1)-5-6	XXBI(1)-5-5	XXBI(1)-5-4	XXBI(1)-5-3	XXBI(1)-5-2	XXBI(1)-5-1	XXBI(1)-5-0
0X24	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-6-7	XXBI(1)-6-6	XXBI(1)-6-5	XXBI(1)-6-4	XXBI(1)-6-3	XXBI(1)-6-2	XXBI(1)-6-1	XXBI(1)-6-0
0X25	:00	0	0	0	0	0	0	0	0

Table 24. BPTx Register Map *(continued)*

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
continued	:00	XXBI(1)-7-7	XXBI(1)-7-6	XXBI(1)-7-5	XXBI(1)-7-4	XXBI(1)-7-3	XXBI(1)-7-2	XXBI(1)-7-1	XXBI(1)-7-0
0X26	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-8-7	XXBI(1)-8-6	XXBI(1)-8-5	XXBI(1)-8-4	XXBI(1)-8-3	XXBI(1)-8-2	XXBI(1)-8-1	XXBI(1)-8-0
0X27	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-9-7	XXBI(1)-9-6	XXBI(1)-9-5	XXBI(1)-9-4	XXBI(1)-9-3	XXBI(1)-9-2	XXBI(1)-9-1	XXBI(1)-9-0
0X28	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-10-7	XXBI(1)-10-6	XXBI(1)-10-5	XXBI(1)-10-4	XXBI(1)-10-3	XXBI(1)-10-2	XXBI(1)-10-1	XXBI(1)-10-0
0X29	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-11-7	XXBI(1)-11-6	XXBI(1)-11-5	XXBI(1)-11-4	XXBI(1)-11-3	XXBI(1)-11-2	XXBI(1)-11-1	XXBI(1)-11-0
0X2a	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-12-7	XXBI(1)-12-6	XXBI(1)-12-5	XXBI(1)-12-4	XXBI(1)-12-3	XXBI(1)-12-2	XXBI(1)-12-1	XXBI(1)-12-0
0X2B	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-13-7	XXBI(1)-13-6	XXBI(1)-13-5	XXBI(1)-13-4	XXBI(1)-13-3	XXBI(1)-13-2	XXBI(1)-13-1	XXBI(1)-13-0
0X2C	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-14-7	XXBI(1)-14-6	XXBI(1)-14-5	XXBI(1)-14-4	XXBI(1)-14-3	XXBI(1)-14-2	XXBI(1)-14-1	XXBI(1)-14-0
0X2d	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(1)-15-7	XXBI(1)-15-6	XXBI(1)-15-5	XXBI(1)-15-4	XXBI(1)-15-3	XXBI(1)-15-2	XXBI(1)-15-1	XXBI(1)-15-0
0X2e	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-0-7	XXBI(2)-0-6	XXBI(2)-0-5	XXBI(2)-0-4	XXBI(2)-0-3	XXBI(2)-0-2	XXBI(2)-0-1	XXBI(2)-0-0
0X2f	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-1-7	XXBI(2)-1-6	XXBI(2)-1-5	XXBI(2)-1-4	XXBI(2)-1-3	XXBI(2)-1-2	XXBI(2)-1-1	XXBI(2)-1-0
0X30	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-2-7	XXBI(2)-2-6	XXBI(2)-2-5	XXBI(2)-2-4	XXBI(2)-2-3	XXBI(2)-2-2	XXBI(2)-2-1	XXBI(2)-2-0
0X31	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-3-7	XXBI(2)-3-6	XXBI(2)-3-5	XXBI(2)-3-4	XXBI(2)-3-3	XXBI(2)-3-2	XXBI(2)-3-1	XXBI(2)-3-0
0X32	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-4-7	XXBI(2)-4-6	XXBI(2)-4-5	XXBI(2)-4-4	XXBI(2)-4-3	XXBI(2)-4-2	XXBI(2)-4-1	XXBI(2)-4-0
0X33	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-5-7	XXBI(2)-5-6	XXBI(2)-5-5	XXBI(2)-5-4	XXBI(2)-5-3	XXBI(2)-5-2	XXBI(2)-5-1	XXBI(2)-5-0
0X34	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-6-7	XXBI(2)-6-6	XXBI(2)-6-5	XXBI(2)-6-4	XXBI(2)-6-3	XXBI(2)-6-2	XXBI(2)-6-1	XXBI(2)-6-0
0X35	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-7-7	XXBI(2)-7-6	XXBI(2)-7-5	XXBI(2)-7-4	XXBI(2)-7-3	XXBI(2)-7-2	XXBI(2)-7-1	XXBI(2)-7-0
0X36	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-8-7	XXBI(2)-8-6	XXBI(2)-8-5	XXBI(2)-8-4	XXBI(2)-8-3	XXBI(2)-8-2	XXBI(2)-8-1	XXBI(2)-8-0
0X37	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-9-7	XXBI(2)-9-6	XXBI(2)-9-5	XXBI(2)-9-4	XXBI(2)-9-3	XXBI(2)-9-2	XXBI(2)-9-1	XXBI(2)-9-0
0X38	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-10-7	XXBI(2)-10-6	XXBI(2)-10-5	XXBI(2)-10-4	XXBI(2)-10-3	XXBI(2)-10-2	XXBI(2)-10-1	XXBI(2)-10-0
0X39	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-11-7	XXBI(2)-11-6	XXBI(2)-11-5	XXBI(2)-11-4	XXBI(2)-11-3	XXBI(2)-11-2	XXBI(2)-11-1	XXBI(2)-11-0
0X3A	:00	0	0	0	0	0	0	0	0

Table 24. BPTx Register Map *(continued)*

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
continued	:00	XXBI(2)-12-7	XXBI(2)-12-6	XXBI(2)-12-5	XXBI(2)-12-4	XXBI(2)-12-3	XXBI(2)-12-2	XXBI(2)-12-1	XXBI(2)-12-0
0X3B	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-13-7	XXBI(2)-13-6	XXBI(2)-13-5	XXBI(2)-13-4	XXBI(2)-13-3	XXBI(2)-13-2	XXBI(2)-13-1	XXBI(2)-13-0
0X3C	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-14-7	XXBI(2)-14-6	XXBI(2)-14-5	XXBI(2)-14-4	XXBI(2)-14-3	XXBI(2)-14-2	XXBI(2)-14-1	XXBI(2)-14-0
0X3D	:00	0	0	0	0	0	0	0	0
continued	:00	XXBI(2)-15-7	XXBI(2)-15-6	XXBI(2)-15-5	XXBI(2)-15-4	XXBI(2)-15-3	XXBI(2)-15-2	XXBI(2)-15-1	XXBI(2)-15-0
0x3E	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB0-7	BPIB0-6	BPIB0-5	BPIB0-4	BPIB0-3	BPIB0-2	BPIB0-1	BPIB0-0
0x3F	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB1-7	BPIB1-6	BPIB1-5	BPIB1-4	BPIB1-3	BPIB1-2	BPIB1-1	BPIB1-0
0x40	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB2-7	BPIB2-6	BPIB2-5	BPIB2-4	BPIB2-3	BPIB2-2	BPIB2-1	BPIB2-0
0x41	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB3-7	BPIB3-6	BPIB3-5	BPIB3-4	BPIB3-3	BPIB3-2	BPIB3-1	BPIB3-0
0x42	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB4-7	BPIB4-6	BPIB4-5	BPIB4-4	BPIB4-3	BPIB4-2	BPIB4-1	BPIB4-0
0x43	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB5-7	BPIB5-6	BPIB5-5	BPIB5-4	BPIB5-3	BPIB5-2	BPIB5-1	BPIB5-0
0x44	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB6-7	BPIB6-6	BPIB6-5	BPIB6-4	BPIB6-3	BPIB6-2	BPIB6-1	BPIB6-0
0x45	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB7-7	BPIB7-6	BPIB7-5	BPIB7-4	BPIB7-3	BPIB7-2	BPIB7-1	BPIB7-0
0x46	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB8-7	BPIB8-6	BPIB8-5	BPIB8-4	BPIB8-3	BPIB8-2	BPIB8-1	BPIB8-0
0x47	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB9-7	BPIB9-6	BPIB9-5	BPIB9-4	BPIB9-3	BPIB9-2	BPIB9-1	BPIB9-0
0x48	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB10-7	BPIB10-6	BPIB10-5	BPIB10-4	BPIB10-3	BPIB10-2	BPIB10-1	BPIB10-0
0x49	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB11-7	BPIB11-6	BPIB11-5	BPIB11-4	BPIB11-3	BPIB11-2	BPIB11-1	BPIB11-0
0x4A	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB12-7	BPIB12-6	BPIB12-5	BPIB12-4	BPIB12-3	BPIB12-2	BPIB12-1	BPIB12-0
0x4B	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB13-7	BPIB13-6	BPIB13-5	BPIB13-4	BPIB13-3	BPIB13-2	BPIB13-1	BPIB13-0
0x4C	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB14-7	BPIB14-6	BPIB14-5	BPIB14-4	BPIB14-3	BPIB14-2	BPIB14-1	BPIB14-0
0x4D	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB15-7	BPIB15-6	BPIB15-5	BPIB15-4	BPIB15-3	BPIB15-2	BPIB15-1	BPIB15-0
0x4E	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB16-7	BPIB16-6	BPIB16-5	BPIB16-4	BPIB16-3	BPIB16-2	BPIB16-1	BPIB16-0
0x4F	:00	0	0	0	0	0	0	0	0

Table 24. BPTx Register Map *(continued)*

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
continued	:00	BPIB17-7	BPIB17-6	BPIB17-5	BPIB17-4	BPIB17-3	BPIB17-2	BPIB17-1	BPIB17-0
0x50	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB18-7	BPIB18-6	BPIB18-5	BPIB18-4	BPIB18-3	BPIB18-2	BPIB18-1	BPIB18-0
0x51	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB19-7	BPIB19-6	BPIB19-5	BPIB19-4	BPIB19-3	BPIB19-2	BPIB19-1	BPIB19-0
0x52	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB20-7	BPIB20-6	BPIB20-5	BPIB20-4	BPIB20-3	BPIB20-2	BPIB20-1	BPIB20-0
0x53	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB21-7	BPIB21-6	BPIB21-5	BPIB21-4	BPIB21-3	BPIB21-2	BPIB21-1	BPIB21-0
0x54	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB22-7	BPIB22-6	BPIB22-5	BPIB22-4	BPIB22-3	BPIB22-2	BPIB22-1	BPIB22-0
0x55	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB23-7	BPIB23-6	BPIB23-5	BPIB23-4	BPIB23-3	BPIB23-2	BPIB23-1	BPIB23-0
0x56	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB24-7	BPIB24-6	BPIB24-5	BPIB24-4	BPIB24-3	BPIB24-2	BPIB24-1	BPIB24-0
0x57	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB25-7	BPIB25-6	BPIB25-5	BPIB25-4	BPIB25-3	BPIB25-2	BPIB25-1	BPIB25-0
0x58	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB26-7	BPIB26-6	BPIB26-5	BPIB26-4	BPIB26-3	BPIB26-2	BPIB26-1	BPIB26-0
0x59	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB27-7	BPIB27-6	BPIB27-5	BPIB27-4	BPIB27-3	BPIB27-2	BPIB27-1	BPIB27-0
0x5A	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB28-7	BPIB28-6	BPIB28-5	BPIB28-4	BPIB28-3	BPIB28-2	BPIB28-1	BPIB28-0
0x5B	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB29-7	BPIB29-6	BPIB29-5	BPIB29-4	BPIB29-3	BPIB29-2	BPIB29-1	BPIB29-0
0x5C	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB30-7	BPIB30-6	BPIB30-5	BPIB30-4	BPIB30-3	BPIB30-2	BPIB30-1	BPIB30-0
0x5D	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB31-7	BPIB31-6	BPIB31-5	BPIB31-4	BPIB31-3	BPIB31-2	BPIB31-1	BPIB31-0
0x5E	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB32-7	BPIB32-6	BPIB32-5	BPIB32-4	BPIB32-3	BPIB32-2	BPIB32-1	BPIB32-0
0x5F	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB33-7	BPIB33-6	BPIB33-5	BPIB33-4	BPIB33-3	BPIB33-2	BPIB33-1	BPIB33-0
0x60	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB34-7	BPIB34-6	BPIB34-5	BPIB34-4	BPIB34-3	BPIB34-2	BPIB34-1	BPIB34-0
0x61	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB35-7	BPIB35-6	BPIB35-5	BPIB35-4	BPIB35-3	BPIB35-2	BPIB35-1	BPIB35-0
0x62	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB36-7	BPIB36-6	BPIB36-5	BPIB36-4	BPIB36-3	BPIB36-2	BPIB36-1	BPIB36-0
0x63	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB37-7	BPIB37-6	BPIB37-5	BPIB37-4	BPIB37-3	BPIB37-2	BPIB37-1	BPIB37-0
0x64	:00	0	0	0	0	0	0	0	0

Table 24. BPTx Register Map *(continued)*

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
continued	:00	BPIB38-7	BPIB38-6	BPIB38-5	BPIB38-4	BPIB38-3	BPIB38-2	BPIB38-1	BPIB38-0
0x65	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB39-7	BPIB39-6	BPIB39-5	BPIB39-4	BPIB39-3	BPIB39-2	BPIB39-1	BPIB39-0
0x66	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB40-7	BPIB40-6	BPIB40-5	BPIB40-4	BPIB40-3	BPIB40-2	BPIB40-1	BPIB40-0
0x67	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB41-7	BPIB41-6	BPIB41-5	BPIB41-4	BPIB41-3	BPIB41-2	BPIB41-1	BPIB41-0
0x68	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB42-7	BPIB42-6	BPIB42-5	BPIB42-4	BPIB42-3	BPIB42-2	BPIB42-1	BPIB42-0
0x69	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB43-7	BPIB43-6	BPIB43-5	BPIB43-4	BPIB43-3	BPIB43-2	BPIB43-1	BPIB43-0
0x6A	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB44-7	BPIB44-6	BPIB44-5	BPIB44-4	BPIB44-3	BPIB44-2	BPIB44-1	BPIB44-0
0x6B	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB45-7	BPIB45-6	BPIB45-5	BPIB45-4	BPIB45-3	BPIB45-2	BPIB45-1	BPIB45-0
0x6C	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB46-7	BPIB46-6	BPIB46-5	BPIB46-4	BPIB46-3	BPIB46-2	BPIB46-1	BPIB46-0
0x6D	:00	0	0	0	0	0	0	0	0
continued	:00	BPIB47-7	BPIB47-6	BPIB47-5	BPIB47-4	BPIB47-3	BPIB47-2	BPIB47-1	BPIB47-0
Invalid Address									
0X6E	:NA	0	0	0	0	0	0	0	0
continued	:NA	0	0	0	0	0	0	0	0
HSITX Controls (R/W)									
0X6F	:00	0	0	0	TXGPC-7	TXGPC-6	TXGPC-5	TXGPC-4	TXGPC-3
continued	:00	TXGPC-2	TXGPC-1	TXGPC-0	BPTXDATINH	TXDRIVE	TXEQCTRL-2	TXEQCTRL-1	TXEQCTRL-0
HSITx Status (R/O), Delta (R/O), and Mask (R/W) Bits									
0x70	:NA	0	0	0	ram_endflg(1)	ram_fm(1)	TXGPS-7	TXGPS-6	TXGPS-5
continued	:NA	TXGPS-4	TXGPS-3	TXGPS-2	TXGPS-1	TXGPS-0	TXLOLHI	TXLOLLO	TXLOL
0x71	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	TXLOLi
0x72	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	TXLOLe
Invalid Addresses									
0X73-0x7F	:NA	0	0	0	0	0	0	0	0
continued	:NA	0	0	0	0	0	0	0	0

1. These bits are used for Vitesse manufacturing test purposes.

Table 25. BPTx Register Map Signals

Signal Name	Description	Bit Width
BPTX Control Bits (R/W)		

Table 25. BPTx Register Map Signals *(continued)*

Signal Name	Description	Bit Width
BPSCRAMB	Disable or enable scrambling of the TFI-5 Tx stream. 0: Allow scrambling 1: Inhibit scrambling	1
A1ERRINS	Insert A1A2 error. 0: No A1A2 errors are inserted 1: 1-bit A1A2 error is inserted	1
B1ERRINS	Insert B1 error. 0: No B1 errors are inserted 1: 1-bit B1 error is inserted	1
B1CALCB	B1 insertion inhibit. 0: Insert B1 parity byte 1: Inhibit B1 parity byte insertion	1
TFI_FIVEB	TFI-5 mode. 0: Insert A1/A2 using the TFI-5 mode standard (3A1s,3A2s) 1: Insert all 48 A1s and A2s	1
STS12SEL	Enable STS12 mode of operation. 0: STS48 mode 1: STS12 mode	1
AISINS	Insert AIS. 0: No AIS inserted 1: Insert AIS (All 1s in payload and overhead except A1,A2 and the counting pattern in J0/Z0)	1
BPTXTRNSPNT	Enable Transparent mode. 0: Transparent mode is off (default) 1: Transparent mode is on	1
BPIROW[3:0]	1-9: Row location for each of the 48 provisionable overhead bytes.	4
BPICOL[1:0]	1-3: Column location for each of the 48 provisionable overhead bytes.	2
BPIBx-[7:0] x = 0 to 47	0x00-0xFF: Byte value for each of the 48 provisionable overhead bytes.	8
BPI_MODE	Provisionable overhead bytes insertion mode. 1: Use OHMon data 0: Enable CPU access	1
XBI_MODE	Extended overhead byte insertion mode. 1: Use OHMon data 0: Enable CPU access	1
XBIx_ROW[3:0] x = 0:2	1-9: Row location for each of the 3 extended overhead bytes.	4
XBIx_COL[1:0] x = 0:2	1-3: Column location for each of the 3 extended overhead bytes.	2
XBIx_TS[5:0] x = 0:2	0-47: Timeslot location for each of the 3 extended overhead bytes.	6
XBIx-[7:0] x = 0 to 2	0x00-0xFF: Byte value for each of the 3 extended overhead bytes.	8
XXBI_MODE	Extra extended overhead byte insertion mode. 1: Use OHMon data 0: Enable CPU access	1
XXBIx_ROW[3:0] x = 0:2	1-9: Row location for each of the 3 groups of extra extended overhead bytes.	4
XXBIx_COL[1:0] x = 0:2	1-3: Column location for each of the 3 groups of extra extended overhead bytes.	2
XXBIx_TS[1:0] x = 0:2	0-2: Group location (first, second, or third group of 16) for each of the 3 groups of extra extended overhead bytes.	2
XXBI0-x-[7:0] x = 0 to 15	0x00-0xFF: Byte value for each of the extra extended overhead bytes in group 0.	8
XXBI1-x-[7:0] x = 0 to 15	0x00-0xFF: Byte value for each of the extra extended overhead bytes in group 1.	8
XXBI2-x-[7:0] x = 0 to 15	0x00-0xFF: Byte value for each of the extra extended overhead bytes in group 2.	8

Table 25. BPTx Register Map Signals *(continued)*

Signal Name	Description	Bit Width
FIFORESET	Force a FIFO reset. 0: Normal operation 1: Output FIFO is held in reset	1
SOFTRESET	Force a reset of all flip-flops in the block. 0: Normal operation 1: All flip-flops in the block are held in reset	1
RDIE	Enable insertion of RDI_L bits in K2 byte when rdi_on is asserted.	1
HSITX Control Bits (R/W)		
BPTXDATINH	Inhibit data transmission by powering off the associated HSITx block. 1: Inhibit (power off) 0: Normal operation	1
TXEQCTRL[2:0]	Equalization setting for the HSITx output driver.	3
TXDRIVE	Combined with TXEQCTRL to set the output drive and pre-emphasis. For more information, see Table 18, page 70.	1
TXGPC[7:0]	General purpose control bits to HSITx (reserved for Vitesse use only).	8
Status Bits (R/O)		
TXLOL	Indicates loss of lock from HSITx Clock multiplier PLL (HSITx internally ORs TXLOLHI and TXLOLLO).	1
TXLOLHI	Indicates loss of lock, frequency out of range high, from HSITx Clock multiplier PLL.	1
TXLOLLO	Indicates loss of lock, frequency out of range low, from HSITx Clock multiplier PLL.	1
TXGPS[7:0]	General purpose status bits from HSITx (reserved for Vitesse use only).	8
Delta Bits (R/O, clear on read)		
TXLOLD	Delta bit to indicate change in status of TXLOL.	1
Mask Bits (R/W)		
TXLOLM	Interrupt mask bit for TXLOLD.	1
Event Bits (RO, clear on R/W		
(none)		

3.5 SFG Register Map

Each SFG block has an 8-word address space located at the base address specified in the master memory map.

Table 26. SFG Register Map

Address Offset	Initial Value (8MSB)	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-8
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Configuration Bits									
0x0	:00	0	0	0	0	0	0	0	0
continued	:01	0	0	0	Patlen-3	Patlen-2	Patlen-1	Patlen-0	Patsel
0x1	:00	USERPAT-15	USERPAT-14	USERPAT-13	USERPAT-12	USERPAT-11	USERPAT-10	USERPAT-9	USERPAT-8
continued	:00	USERPAT-7	USERPAT-6	USERPAT-5	USERPAT-4	USERPAT-3	USERPAT-2	USERPAT-1	USERPAT-0
0x2	:00	USERPAT-31	USERPAT-30	USERPAT-29	USERPAT-28	USERPAT-27	USERPAT-26	USERPAT-25	USERPAT-24
continued	:00	USERPAT-23	USERPAT-22	USERPAT-21	USERPAT-20	USERPAT-19	USERPAT-18	USERPAT-17	USERPAT-16
0x3	:00	USERPAT-47	USERPAT-46	USERPAT-45	USERPAT-44	USERPAT-43	USERPAT-42	USERPAT-41	USERPAT-40
continued	:00	USERPAT-39	USERPAT-38	USERPAT-37	USERPAT-36	USERPAT-35	USERPAT-34	USERPAT-33	USERPAT-32
0x4	:00	USERPAT-63	USERPAT-62	USERPAT-61	USERPAT-60	USERPAT-59	USERPAT-58	USERPAT-57	USERPAT-56
continued	:00	USERPAT-55	USERPAT-54	USERPAT-53	USERPAT-52	USERPAT-51	USERPAT-50	USERPAT-49	USERPAT-48
0x5	:00	USERPAT-79	USERPAT-78	USERPAT-77	USERPAT-76	USERPAT-75	USERPAT-74	USERPAT-73	USERPAT-72
continued	:00	USERPAT-71	USERPAT-70	USERPAT-69	USERPAT-68	USERPAT-67	USERPAT-66	USERPAT-65	USERPAT-64
0x6	:00	USERPAT-95	USERPAT-94	USERPAT-93	USERPAT-92	USERPAT-91	USERPAT-90	USERPAT-89	USERPAT-88
continued	:00	USERPAT-87	USERPAT-86	USERPAT-85	USERPAT-84	USERPAT-83	USERPAT-82	USERPAT-81	USERPAT-80
0x7	:NA	KEY-15	KEY-14	KEY-13	KEY-12	KEY-11	KEY-10	KEY-9	KEY-8
continued	:NA	KEY-7	KEY-6	KEY-5	KEY-4	KEY-3	KEY-2	KEY-1	KEY-0

Table 27. SFG Register Map R/W Control Bits

Signal Name	Description	Bit Width
PATSEL0	PRBS/User pattern select for TEST data 0. PATSEL0 = 0, user pattern selected PATSEL0 = 1, PRBS pattern selected	1
PATLEN0	Length of user pattern in bytes. Values greater than 11 are assumed to be 11.	4
USERPAT0	User pattern.	96
PATSEL1	PRBS/User pattern select for TEST data 1. PATSEL = 0, user pattern selected PATSEL = 1, PRBS pattern selected	1
PATLEN1	Length of user pattern in bytes. Values greater than 11 will be assumed to be 11.	4
USERPAT1	User pattern.	96
KEY	Special register for Vitesse use only.	16

3.6 SyncMan Register Map

SyncMan has an 8-word address space.

Unused bits (labeled 0) are not implemented in the hardware. The interface to the internal read data bus should set these bits to zero when driving the bus.

Table 28. SyncMan Register Map

Address Offset	Initial Value (8MS	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LS	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
(R/W - control bits)									
BP Sync OFFSET and Frame Sync Select Controls									
0x00	:00	0	0	0	0	0	0	0	0
continued	:00	BPSYNCWIN-3	BPSYNCWIN-2	BPSYNCWIN-1	BPSYNCWIN-0	BPSYNCSPLIT	BPSYNCINH	BPSYNCx-1	BPSYNCx-0
0x01	:00	BPOFFSETL-15	BPOFFSETL-14	BPOFFSETL-13	BPOFFSETL-12	BPOFFSETL-11	BPOFFSETL-10	BPOFFSETL-9	BPOFFSETL-8
continued	:00	BPOFFSETL-7	BPOFFSETL-6	BPOFFSETL-5	BPOFFSETL-4	BPOFFSETL-3	BPOFFSETL-2	BPOFFSETL-1	BPOFFSETL-0
0x02	:00	BPOFFSETU-15	BPOFFSETU-14	BPOFFSETU-13	BPOFFSETU-12	BPOFFSETU-11	BPOFFSETU-10	BPOFFSETU-9	BPOFFSETU-8
continued	:00	BPOFFSETU-7	BPOFFSETU-6	BPOFFSETU-5	BPOFFSETU-4	BPOFFSETU-3	BPOFFSETU-2	BPOFFSETU-1	BPOFFSETU-0
BP Sync Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0x03	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	BPSYNC
0x04	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	BPSYNCD
0x05	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	BPSYNCM
Invalid Addresses									
0x06-0X07	:NA	0	0	0	0	0	0	0	0
continued	:NA	0	0	0	0	0	0	0	0

The register map signals that correspond to the frame synchronous filter are updated each time the frame is synchronized.

Table 29. SyncMan Register Map Signals

Signal Name	Description	Bit Width
Control Bits (R/W)		
BPOFFSETL[15:0]	This gives the offset for the frame sync, selected by BPSYNCSEL, for the lower channel frame domain.	16
BPOFFSETU[15:0]	This gives offset for the frame sync, selected by BPSYNCSEL, for the lower channel frame domain.	16
BPSYNCX[1:0]	Number of framepulse misses or hits before the Out-of-Sync or In-Sync state is achieved. 00 = 1 miss or hit 01 = 2 misses or hits 10 = 3 misses or hits 11 = 4 misses or hits	2

Table 29. SyncMan Register Map Signals *(continued)*

Signal Name	Description	Bit Width
BPSYNCINH	Backplane Sync Inhibits. This bit inhibits the flywheel. If BPSYNCINH = 1, the flywheel maintains its current sync frame If BPSYNCINH = 0, the flywheel is enabled to accept a new sync pulse	1
BPSYNCPLIT	Backplane SyncSplit. If BPSYNCINH = 0, only the value of BPOFFSETL[15:0] is used to control the offset of both on-chip frame syncs If BPSYNCINH = 1, the two on-chip frame syncs can have independent offsets	1
BPSYNCWIN[3:0]	Backplane sync tolerance window. This is the amount of jitter or shift tolerated on the external sync. 0000 = ± 0 byte clock cycle 0001 = ± 1 byte clock cycle 0010 = ± 2 byte clock cycles * * * * * * * * * 1101 = ± 13 byte clock cycles 1110 = ± 14 byte clock cycles 1111 = ± 15 byte clock cycles	4
Status Bits (R/O)		
BPSYNC	Backplane status sync is a bit register, which indicates the frame pulse status for the backplane side signals. If BpSync = 1, then the device is in-sync If BpSync = 0, then the device is out-of-sync	1
Delta Bits (R/O, Clear on R)		
BPSYNCD	Backplane status sync delta bit monitor is set high when the corresponding bit in BpSync changes state.	1
Event Bits (R/O, Clear on R)		
(none)		
Mask Bits (R/W)		
BPSYNCM	Backplane status sync mask bit enables the contribution of the BPSYNC delta toward the generation of an interrupt. When BPSYNCM = 0, BPSYNC delta does not contribute towards the interrupt. When BPSYNCM = 1, BPSYNC delta contributes towards the interrupt.	1

3.7 Master Control Register Map

The Master Control Page Registers have a 32-word address space. Unused bits (labeled 0) are not implemented in hardware, and will return logic 0 if read. Unused bits (labeled 0) are not implemented in hardware. The interface to the internal read data bus should set these bits to zero when driving the bus.

Table 30. PLL Controls Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
R/W Control Bit									
PLL Controls									
0x00	:3C	PLL_LBW9	PLL_LBW8	PLL_LBW7	PLL_LBW6	PLL_LBW5	PLL_LBW4	PLL_LBW3	PLL_LBW2
continued	:44	PLL_LBW1	PLL_LBW0	PLLDIVCORE-2	PLLDIVCORE-1	PLLDIVCORE-0	PLLDIVREF-2	PLLDIVREF-1	PLLDIVREF-0

Table 31. PLL Controls Register Map Signals

Signal Name	Description	Bit Width
Control Bits (R/W)		
PLL_LBW[9:0]	Bits to control loop bandwidth of Tx and Rx PLLs. The currently assigned functions are: PLL_LBW[9:8] = Tx PLL filter adjust (rr), default is 00. PLL_LBW[7:6] = Tx PLL current adjust (i), default is 11. PLL_LBW[5:4] = Rx PLL filter adjust (rr), default is 11. PLL_LBW[3:2] = Rx PLL current adjust (i0), default is 00, only bit 2 is currently used. PLL_LBW[1:0] = Rx PLL pulse width adjust (pw), default is 01 and only bit 1 is currently used.	10
PLLDIVCORE[2:0]	Not used.	3
PLLDIVREF[2:0]	Ratio of external reference to internal VCO frequency (VCO is normally running at 2.5GHz). If PLLDIVREF = 000, expected reference is 311 MHz. If PLLDIVREF = 001, expected reference is 155 MHz. If PLLDIVREF = 010, expected reference is 78 MHz. If PLLDIVREF = 100, the state of external pins refsel[2:0] are used instead of the contents of PLLDIVREF[2:0].	3

Table 32. PLL Status Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
PLL Status (R/O), Delta (R/O) and Mask (R/W) Bits									
0x01	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLOL
0x02	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLOLd
0x03	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLOLM
0x04	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLOR
0x05	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLORD
0x06	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	PLLLORM

Table 33. PLL Status Register Map Signals

Signal Name	Description	Bit Width
Status Bits (R/O)		
PLLLOL	Indicates the lock status of the clock multiplier PLL. If PLLLOL = 0, then the PLL is locked. If PLLLOL = 1, then the PLL is NOT locked.	1
PLLLOR	Indicates whether the clock multiplier PLL is receiving a valid reference signal. If PLLLOR = 0, then the PLL is receiving a valid reference. If PLLLOL = 1, then the PLL is NOT receiving a valid reference.	1
Delta Bits (R/O, Clear on R)		
PLLLOLD	The PLL lock delta bit monitors PLLLOL and is set high when PLLLOL changes state.	1
PLLLORD	The PLL loss of reference delta bit monitors PLLLOL and is set high when PLLLOL changes state.	1
Mask Bits (R/W)		
PLLLOLM	The PLL lock mask bit enables the contribution of the PLLLOL delta towards the generation of an interrupt. When PLLLOLM = 0, PLLLOL delta does not contribute towards the interrupt. When PLLLOLM = 1, PLLLOL delta contributes towards the interrupt.	1
PLLLORM	The PLL loss of reference mask bit enables the contribution of the PLLLOR delta towards the generation of an interrupt. When PLLLORM = 0, PLLLOR delta does not contribute towards the interrupt. When PLLLORM = 1, PLLLOR delta contributes towards the interrupt.	1

Table 34. Test Control Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Test Control Registers (R/W)									
0x07	:00	TSTCTRL1-7	TSTCTRL1-6	TSTCTRL1-5	TSTCTRL1-4	TSTCTRL1-3	TSTCTRL1-2	TSTCTRL1-1	TSTCTRL1-0
continued	:00	TSTCTRL0-7	TSTCTRL0-6	TSTCTRL0-5	TSTCTRL0-4	TSTCTRL0-3	TSTCTRL0-2	TSTCTRL0-1	TSTCTRL0-0
0x08	:00	TSTCTRL3-7	TSTCTRL3-6	TSTCTRL3-5	TSTCTRL3-4	TSTCTRL3-3	TSTCTRL3-2	TSTCTRL3-1	TSTCTRL3-0
continued	:00	TSTCTRL2-7	TSTCTRL2-6	TSTCTRL2-5	TSTCTRL2-4	TSTCTRL2-3	TSTCTRL2-2	TSTCTRL2-1	TSTCTRL2-0
0x09	:00	TSTCTRL5-7	TSTCTRL5-6	TSTCTRL5-5	TSTCTRL5-4	TSTCTRL5-3	TSTCTRL5-2	TSTCTRL5-1	TSTCTRL5-0
continued	:00	TSTCTRL4-7	TSTCTRL4-6	TSTCTRL4-5	TSTCTRL4-4	TSTCTRL4-3	TSTCTRL4-2	TSTCTRL4-1	TSTCTRL4-0
0x0A	:00	TSTCTRL7-7	TSTCTRL7-6	TSTCTRL7-5	TSTCTRL7-4	TSTCTRL7-3	TSTCTRL7-2	TSTCTRL7-1	TSTCTRL7-0
continued	:00	TSTCTRL6-7	TSTCTRL6-6	TSTCTRL6-5	TSTCTRL6-4	TSTCTRL6-3	TSTCTRL6-2	TSTCTRL6-1	TSTCTRL6-0
0x0B	:00	TSTCTRL9-7	TSTCTRL9-6	TSTCTRL9-5	TSTCTRL9-4	TSTCTRL9-3	TSTCTRL9-2	TSTCTRL9-1	TSTCTRL9-0
continued	:00	TSTCTRL8-7	TSTCTRL8-6	TSTCTRL8-5	TSTCTRL8-4	TSTCTRL8-3	TSTCTRL8-2	TSTCTRL8-1	TSTCTRL8-0
0x0C	:00	TSTCTRL11-7	TSTCTRL11-6	TSTCTRL11-5	TSTCTRL11-4	TSTCTRL11-3	TSTCTRL11-2	TSTCTRL11-1	TSTCTRL11-0
continued	:00	TSTCTRL10-7	TSTCTRL10-6	TSTCTRL10-5	TSTCTRL10-4	TSTCTRL10-3	TSTCTRL10-2	TSTCTRL10-1	TSTCTRL10-0
0x0D	:00	TSTCTRL13-7	TSTCTRL13-6	TSTCTRL13-5	TSTCTRL13-4	TSTCTRL13-3	TSTCTRL13-2	TSTCTRL13-1	TSTCTRL13-0
continued	:00	TSTCTRL12-7	TSTCTRL12-6	TSTCTRL12-5	TSTCTRL12-4	TSTCTRL12-3	TSTCTRL12-2	TSTCTRL12-1	TSTCTRL12-0
0x0E	:00	TSTCTRL15-7	TSTCTRL15-6	TSTCTRL15-5	TSTCTRL15-4	TSTCTRL15-3	TSTCTRL15-2	TSTCTRL15-1	TSTCTRL15-0
continued	:00	TSTCTRL14-7	TSTCTRL14-6	TSTCTRL14-5	TSTCTRL14-4	TSTCTRL14-3	TSTCTRL14-2	TSTCTRL14-1	TSTCTRL14-0
0x0F	:00	TSTCTRL17-7	TSTCTRL17-6	TSTCTRL17-5	TSTCTRL17-4	TSTCTRL17-3	TSTCTRL17-2	TSTCTRL17-1	TSTCTRL17-0
continued	:00	TSTCTRL16-7	TSTCTRL16-6	TSTCTRL16-5	TSTCTRL16-4	TSTCTRL16-3	TSTCTRL16-2	TSTCTRL16-1	TSTCTRL16-0
0x10	:00	TSTCTRL19-7	TSTCTRL19-6	TSTCTRL19-5	TSTCTRL19-4	TSTCTRL19-3	TSTCTRL19-2	TSTCTRL19-1	TSTCTRL19-0
continued	:00	TSTCTRL18-7	TSTCTRL18-6	TSTCTRL18-5	TSTCTRL18-4	TSTCTRL18-3	TSTCTRL18-2	TSTCTRL18-1	TSTCTRL18-0
0x11	:00	TSTCTRL21-7	TSTCTRL21-6	TSTCTRL21-5	TSTCTRL21-4	TSTCTRL21-3	TSTCTRL21-2	TSTCTRL21-1	TSTCTRL21-0
continued	:00	TSTCTRL20-7	TSTCTRL20-6	TSTCTRL20-5	TSTCTRL20-4	TSTCTRL20-3	TSTCTRL20-2	TSTCTRL20-1	TSTCTRL20-0
0x12	:00	TSTCTRL23-7	TSTCTRL23-6	TSTCTRL23-5	TSTCTRL23-4	TSTCTRL23-3	TSTCTRL23-2	TSTCTRL23-1	TSTCTRL23-0
continued	:00	TSTCTRL22-7	TSTCTRL22-6	TSTCTRL22-5	TSTCTRL22-4	TSTCTRL22-3	TSTCTRL22-2	TSTCTRL22-1	TSTCTRL22-0
0x13	:00	TSTCTRL25-7	TSTCTRL25-6	TSTCTRL25-5	TSTCTRL25-4	TSTCTRL25-3	TSTCTRL25-2	TSTCTRL25-1	TSTCTRL25-0
continued	:00	TSTCTRL24-7	TSTCTRL24-6	TSTCTRL24-5	TSTCTRL24-4	TSTCTRL24-3	TSTCTRL24-2	TSTCTRL24-1	TSTCTRL24-0
0x14	:00	TSTCTRL27-7	TSTCTRL27-6	TSTCTRL27-5	TSTCTRL27-4	TSTCTRL27-3	TSTCTRL27-2	TSTCTRL27-1	TSTCTRL27-0
continued	:00	TSTCTRL26-7	TSTCTRL26-6	TSTCTRL26-5	TSTCTRL26-4	TSTCTRL26-3	TSTCTRL26-2	TSTCTRL26-1	TSTCTRL26-0
0x15	:00	TSTCTRL29-7	TSTCTRL29-6	TSTCTRL29-5	TSTCTRL29-4	TSTCTRL29-3	TSTCTRL29-2	TSTCTRL29-1	TSTCTRL29-0
continued	:00	TSTCTRL28-7	TSTCTRL28-6	TSTCTRL28-5	TSTCTRL28-4	TSTCTRL28-3	TSTCTRL28-2	TSTCTRL28-1	TSTCTRL28-0
0x16	:00	TSTCTRL31-7	TSTCTRL31-6	TSTCTRL31-5	TSTCTRL31-4	TSTCTRL31-3	TSTCTRL31-2	TSTCTRL31-1	TSTCTRL31-0
continued	:00	TSTCTRL30-7	TSTCTRL30-6	TSTCTRL30-5	TSTCTRL30-4	TSTCTRL30-3	TSTCTRL30-2	TSTCTRL30-1	TSTCTRL30-0

Table 35. Test Control Register Map Signals

Signal Name	Description	Bit Width
Control Bits (R/W)		
TSTCTRL[31:0][7:0]	32 8-bit words used to address blocks for each of 32 scan chains. The contents will set which block within the group of blocks on each chain is currently being tested.	256

Table 36. Revision ID Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Revision ID Code (R/O)									
0X17	:00	0	0	0	0	0	0	0	0
continued	:AA	REVID-7	REVID-6	REVID-5	REVID-4	REVID-3	REVID-2	REVID-1	REVID-0

Table 37. Revision ID Register Map Signals

Signal Name	Description	Bit Width
Status Bits (R/O)		
REVID[7:0]	Revision code of the silicon. 0xAA for revision A silicon, 0xAB for revision B silicon, and so forth. Some software, such as the Vitesse GUI, may just use the bottom nibble, thereby giving only A or B.	8

Table 38. Interrupt Composite States Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Interrupt Composite States (R/O)									
0x18	:NA	INTSRC0-15	INTSRC0-14	INTSRC0-13	INTSRC0-12	INTSRC0-11	INTSRC0-10	INTSRC0-9	INTSRC0-8
continued	:NA	INTSRC0-7	INTSRC0-6	INTSRC0-5	INTSRC0-4	INTSRC0-3	INTSRC0-2	INTSRC0-1	INTSRC0-0
0X19	:NA	INTSRC1-15	INTSRC1-14	INTSRC1-13	INTSRC1-12	INTSRC1-11	INTSRC1-10	INTSRC1-9	INTSRC1-8
continued	:NA	INTSRC1-7	INTSRC1-6	INTSRC1-5	INTSRC1-4	INTSRC1-3	INTSRC1-2	INTSRC1-1	INTSRC1-0

Table 39. Interrupt Composite States Register Map Signals

Signal Name	Description	Bit Width
Status Bits (R/O)		
INTSRC0[15:0]	Status of first 16 interrupt composite bits, from intci[15:0]. For more information, see Table 38.	16
INTSRC1[15:0]	Status of second 16 interrupt composite bits, from intci[31:16]. For more information, see Table 38.	16

Table 40. Software Reset Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Software Reset									
0x1A	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	SFTRST

Table 41. Software Reset Register Map Signals

Signal Name	Description	Bit Width
Software Reset Bits (R/W)		
SFTRST	Soft reset bit to control device master reset. 1: Put all flip-flops in the reset state. 0: Resume normal operation of these circuits.	1

Table 42. Software Configuration Command Register Map

Address Offset	Initial Value (8MSB	MSB Microprocessor bit-15	Microprocessor bit-14	Microprocessor bit-13	Microprocessor bit-12	Microprocessor bit-11	Microprocessor bit-10	Microprocessor bit-9	LSB Microprocessor bit-0
Continued	Initial Value (8LSB)	Microprocessor bit-7	Microprocessor bit-6	Microprocessor bit-5	Microprocessor bit-4	Microprocessor bit-3	Microprocessor bit-2	Microprocessor bit-1	LSB Microprocessor bit-0
Software Configuration Command									
0x1B	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	NEWCFGHOLD	NEWCFGLOCK	NEWCFGBUSYM	NEWCFGM
0x1C	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	NEWCFGD
0x1D	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	NEWCFGBUSY	NEWCFGBUSYD
Software Configuration Command (One-shot, W/O)									
0x1E	:00	0	0	0	0	0	0	0	0
continued	:00	0	0	0	0	0	0	0	NEWCFG

Table 43. Software Configuration Command Register Map Signals

Signal Name	Description	Bit Width
Control Bits (R/W)		
NEWCFGLOCK	When high, prevents NEWCFG bit or new_cfg_in pin from causing a new_cfg_out pulse while NEWCFGD continues to work.	1
NEWCFGBUSYM	The new_cfg busy mask bit enables the contribution of the NEWCFGBUSY delta towards the generation of an interrupt. When NEWCFGBUSYM = 0, NEWCFGBUSY delta does not contribute towards the interrupt. When NEWCFGBUSYM = 1, NEWCFGBUSY delta contributes towards the interrupt.	1
NEWCFGM	The new_cfg mask bit enables the contribution of the NEWCFG delta towards the generation of an interrupt. When NEWCFGM = 0, NEWCFG delta does not contribute towards the interrupt. When NEWCFGM = 1, NEWCFG delta contributes towards the interrupt.	1
NEWCFGD	The new_cfg delta bit monitors activity on the new_cfg pin and NEWCFG register bit and is set high when a configuration update has been requested.	1
NEWCFGBUSY	Indicates that a new configuration pulse has been issued to the core, but the frame boundary has not yet occurred in the core.	1
NEWCFGBUSYD	The new_cfg busy delta bit monitors activity on the NEWCFGBUSY bit and is set high when NEWCFGBUSY goes to 0.	1
One-Shot Bits (W/O to Create One-Shot Signal)		
NEWCFG	Writing to this bit initiates a request to transfer the standby TSI switch configuration maps to the active maps at the next frame boundary.	1

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC9295 device.

4.1 DC Characteristics

The following sections contain the DC specifications for the VSC9295 device.

4.1.1 TFI-5 Data Signals and LVCMOS Signals

There are two sets of I/O levels. They are listed here:

- TFI-5 signals are characterized by minimum and maximum values of ΔV_{IN}, V_{OCM}, R_O, V_{ICM}, and R_{IN}. The TFI-5 levels hold when a high-speed port is configured for STS-12 operation.
- 2.5 V TTL or CMOS signals are characterized by minimum and maximum values of V_{OH},V_{OL},V_{IH},V_{IL}, I_{IH}, I_{IL}, and I_{OZ}.

Specifications for these I/O levels are shown in the following tables and illustrations.

Table 44. High-Speed (TFI-5 Data) Signal DC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{DDAP}	Power supply voltage for high-speed I/O cells	1.14	1.26	V	
V_{ICM}	Receiver common mode range	0.75	V_{DDAP} + 0.26	V	
ΔV_{IN}	Receiver input sensitivity range	75	800	mV	Within valid range of V_{ICM} (single-ended swing).
R_{IN}	Input termination impedance	85	115	Ω	To V_{DDAP} each side.
I_{XCI}	Input short-circuit current that the pin can sustain without damage	–30	30	mA	Device supply at 0 V, input driven from TFI-5 output driver.
ΔV_{OUT_LD}	Output differential voltage, low drive	250	500	mV	Far-end terminated 50 Ω to V_{DDAP} each side (single-ended swing).
ΔV_{OUT_HD}	Output differential voltage, high drive	400	800	mV	Far-end terminated 50 Ω to V_{DDAP} each side (single-ended swing).
V_{OCM_CML}	Output offset voltage (output termination to V_{DDH})	V_{DDAP} – 0.4	V_{DDAP} – 0.1	V	Far-end terminated 50 Ω to V_{DDAP} each side.
R_O	DC output impedance, single-ended	40	60	Ω	
I_{XCO}	Output short-circuit current that the pin can sustain without damage	–30	30	mA	To any voltage between V_{DDH} and GND, powered and unpowered.

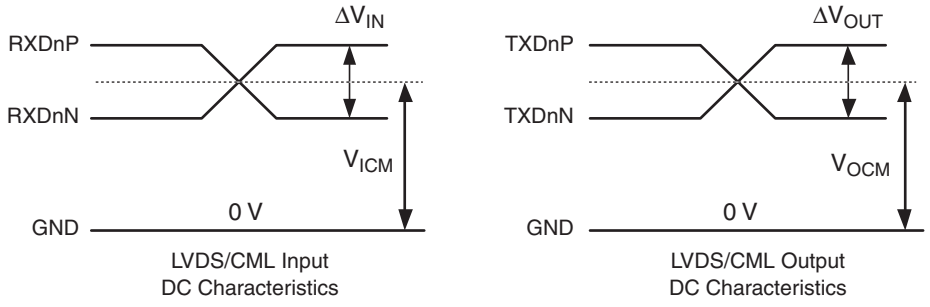


Figure 35. High-Speed Level Definitions

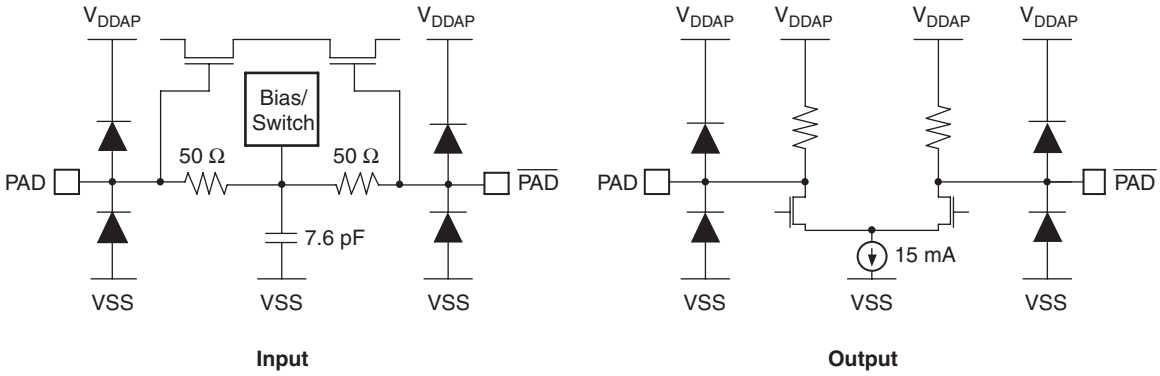


Figure 36. High-Speed I/O Equivalent Circuits

Table 45. LVCMOS DC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{DD_IO}	Power supply voltage for CMOS I/O cells	2.375	3.465	V	Recommended 2.5 V
V_{IL}	Input low (CMOS)	–0.2	0.75	V	
V_{IH}	Input high (CMOS)	V_{DD_IO} – 0.8	V_{DD_IO} + 0.2	V	
I_{IL}	Input low input leakage	–40	40	µA	$0 < V_{IN} < V_{IL}$
I_{IH}	Input high input leakage	–40	40	µA	$V_{IH} < V_{IN} < V_{DD\_IO}$
V_{OH}	Output voltage high (CMOS)	V_{DD_IO} – 0.4	V_{DD_IO}	V	Sourcing 2.0 mA into load
V_{OL}	Output voltage low (CMOS)	0	0.4	V	Sinking 2.0 mA from load
I_{OZ}	Tri-state output leakage current	–50	40	µA	$0 < V_{OUT} < V_{DD\_IO}$
R_{PD}	Input pull-down impedance	40 k	1 M	Ω	Pull-down impedance of open input

4.1.2 Power Supply Voltages and Currents

The VSC9295 operates with a core voltage of 1.2 V ± 5%, with an additional supply of 1.8 V ± 5% or 2.5 V ± 5% for some of the analog components. The TTL/CMOS I/O will also operate with a 2.5 V ± 5% power supply, which can optionally be set at 3.3 V ± 5% for compatibility purposes to provide three power supply voltages, if desired.

There is no need to sequence these power supplies; they can be allowed to come up in any order. The estimated current draw for the power supplies is shown in the following tables.

Table 46. Core Power Supply Voltages and Currents

Symbol	Parameter	Voltage	Maximum DC Currents	Maximum Allowed Ripple
V_{DD}	Positive power supply to core digital standard cells	1.2 V	11 A	60 mV p-p
V_{SS}	Ground to core digital standard cells	0	11 A	

Table 47. CMOS I/O Power Supply Voltages and Currents

Symbol	Parameter	Voltage	Maximum DC Currents	Maximum Allowed Ripple
V_{DDIO}	Positive power supply to CMOS I/O	3.3 V / 2.5 V	165 mA(1)	125 mV p-p
V_{SSIO}	Ground to CMOS I/O	0	165 mA(1)	

1. Based on driving 20 pF loads on every CMOS output with typical activity, with maximum V_{DDIO} voltage.

Table 48. High-Speed Interface Power Supply Voltages and Currents

Symbol	Parameter	Voltage	Maximum DC Currents	Maximum Allowed Ripple
V_{DDAP}	Positive power supply to high-speed digital circuitry in the high-speed interface	1.2 V	9.0 A	25 mV p-p
V_{DD18}	High voltage power supply to the high-speed interface	2.5 V / 1.8 V	1.5 A	25 mV p-p

4.2 AC Characteristics

The following sections contain the AC specifications for the VSC9295 device.

4.2.1 CPU interface

The CPU interface supports three operational modes:

- Intel mode with separate address and data bus (Intel non-multiplexed)
- Intel mode where the data bus is used to transmit address followed by data in sequence, delineated by the ale pin
- Motorola mode for separate address and data buses

The mode and the resulting meaning of the external control signals is set by the cpu_mode pin.

Figure 37 shows the csn-to-ds-wrn timing for the device, which is common to each of the modes described in the list of operational modes. For detailed information about the CPU interface and its modes of operation, see "CPU Interface," page 29. The timing diagrams for each of the operational modes are shown in Figure 38, page 126 through Figure 43, page 129. These diagrams are followed by the master timing parameters in Table 49, page 129.

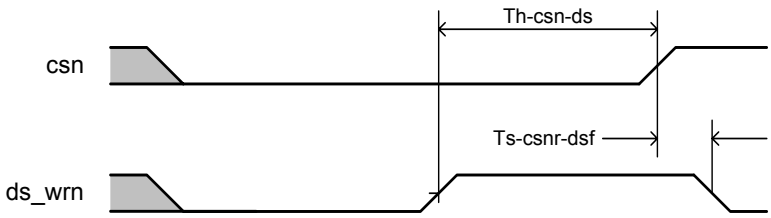


Figure 37. csn-to-ds_wrn Timing in All Modes

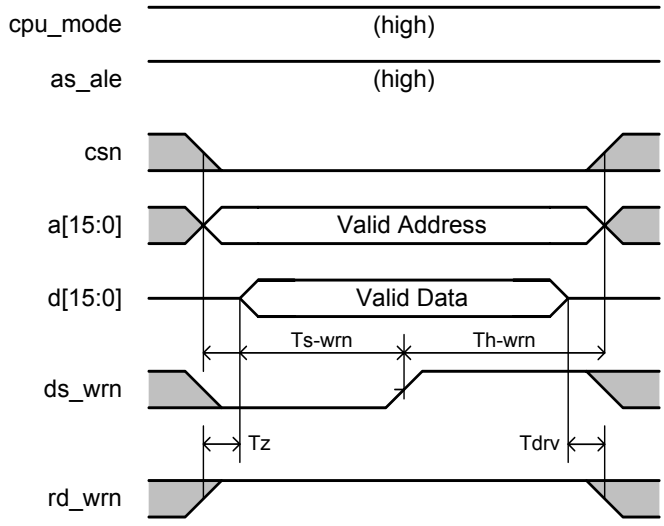


Figure 38. Non-Multiplexed Intel Mode Write Timing

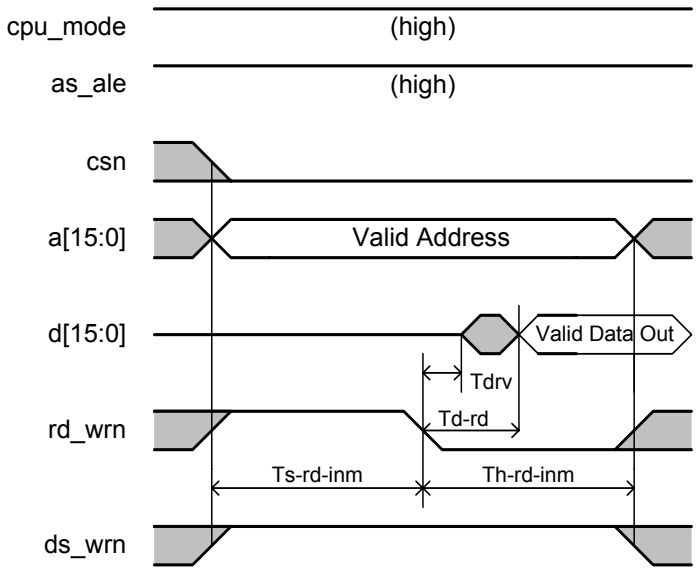


Figure 39. Non-Multiplexed Intel Mode Read Timing

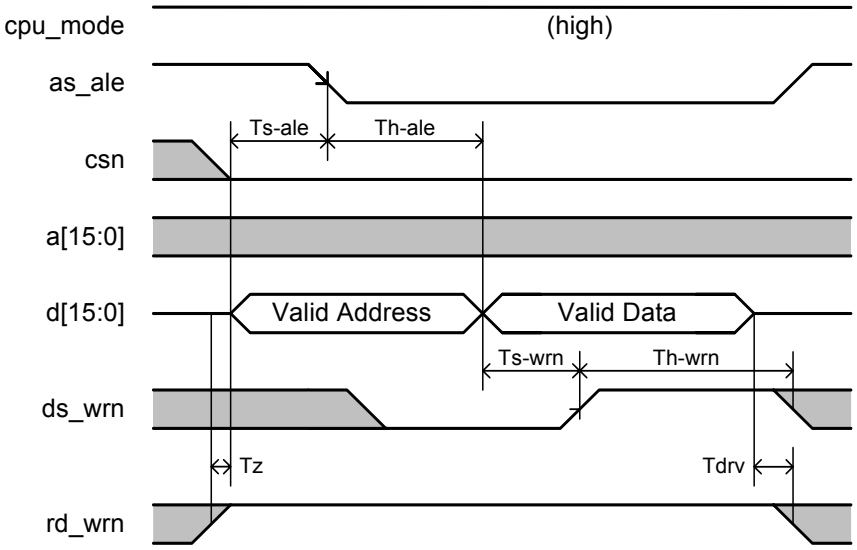


Figure 40. Multiplexed Intel Mode Write Timing

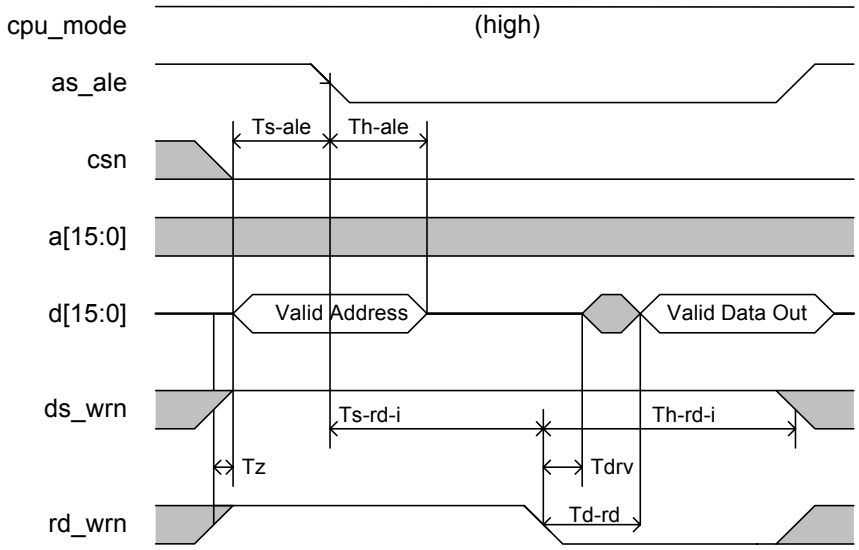


Figure 41. Multiplexed Intel Mode Read Timing

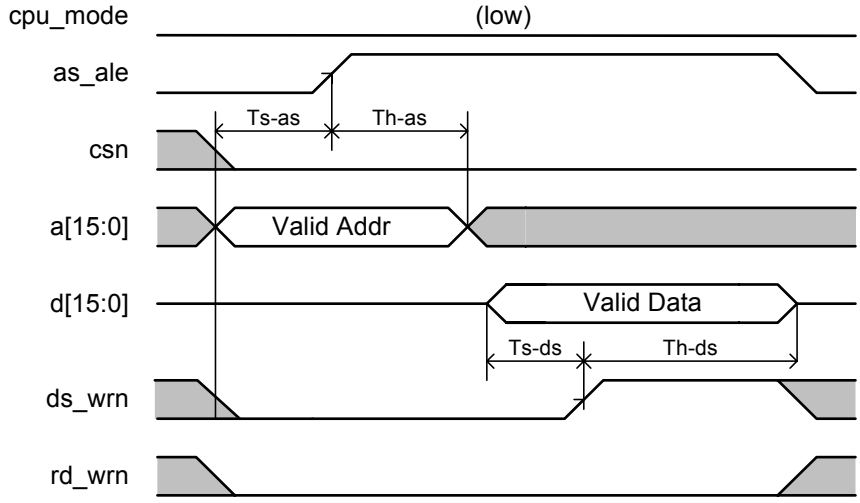


Figure 42. Motorola Mode Write Timing

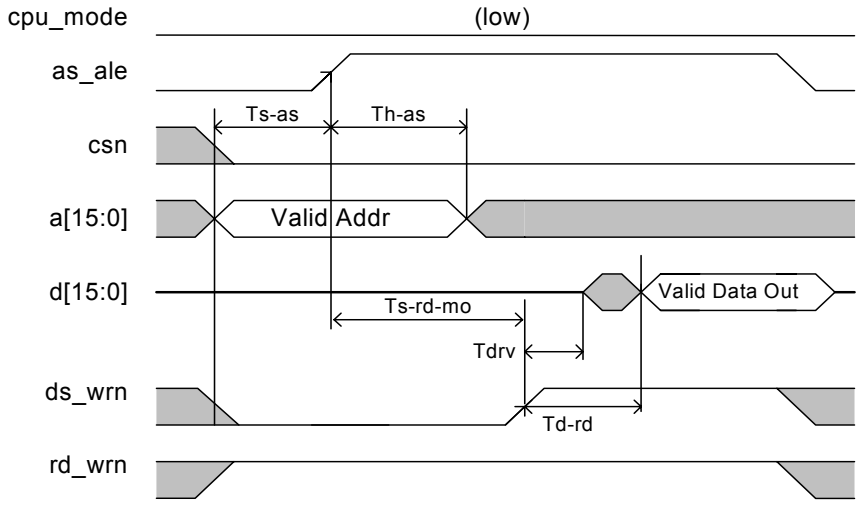


Figure 43. Motorola Mode Read Timing

Table 49. CPU Interface Timing Variable Definitions

Symbol	Mode	Operation	Parameter	Minimum	Maximum	Unit
Td-rd	Non-mux Intel	Read	Delay from rdb falling to valid data on d, with ds_wrn high	3	63	ns
	Motorola	Read	Delay from ds_wrn rising to valid data on d, with rd_wrn high			
Tdrv	Non-mux Intel	Write	Time for d to be driven instead of tri-state after falling edge of rd_wrn	1	2	ns
	Mux Intel	Write	Time for d to be driven instead of tri-state after falling edge of rd_wrn			
	Mux Intel	Read	Time for d to be driven instead of tri-state after falling edge of rd_wrn			
	Motorola	Read	Time for d to be driven instead of tri-state after rising edge of ds_wrn			
Th-ale	Mux Intel	Write	Hold time of d after as_alen falling	6		ns
	Mux Intel	Read	Hold time of d after as_alen falling			
	Motorola	Read	Hold time of a after as_alen rising			
Th-as	Motorola	Write	Hold time of a after as_alen rising	5		ns
Th-ds	Motorola	Write	Hold time of d or csn after ds_wrn rising	6.5		ns
Th-rd-l	Mux Intel	Read	Hold time of csn and ds_wrn after rd_wrn falling	25		ns
Th-wrn	Non-mux Intel	Write	Hold time of a or d after the rising edge of ds_wrn	6.5[1]		ns
	Mux Intel	Write	Hold time of d after ds_wrn rising			
Ts-ds	Motorola	Write	Setup time of d to ds_wrn rising			

Table 49. CPU Interface Timing Variable Definitions *(continued)*

Symbol	Mode	Operation	Parameter	Minimum	Maximum	Unit
Ts-ale	Mux Intel	Write	Setup time of d to as_alen falling	6.5		ns
	Mux Intel	Read	Setup time of d to as_alen falling			
	Motorola	Read	Setup time of a changing or csn falling to as_alen rising			
Ts-as	Motorola	Write	Setup time of a changing, ds_wrn falling, or csn falling to as_alen rising			
Ts-rd-I	Mux Intel	Read	Setup time from as_alen falling to rd_wrn falling	12.5		ns
Ts-rd-inm	Non-mux Intel	Read	Setup time from the latest of a changing or csn falling to falling edge of rd_wrn			
Ts-rd-mo	Motorola	Read	Setup time from as_ale rising to ds_wrn rising			
Ts-wrn	Non-mux Intel	Write	Setup time from the latest of a or d changing or csn falling to rising edge of ds_wrn	12.5		ns
	Mux Intel	Write	Setup time of d to ds_wrn rising			
Tz	Non-mux Intel	Write	Time for d to go tri-state after rising edge of rd_wrn	1	2	ns
	Mux Intel	Write	Time for d to go tri-state after rising edge of rd_wrn			
	Mux Intel	Read	Time for d to go tri-state after rising edge of rd_wrn			
Ts-csnr-dsf	All Modes	Write	Setup time of csn rising before falling edge of ds_wrn	1	2	ns
Th-csn-ds	All Modes	Read/Write	Hold time of csn after the rising edge of ds_wrn	6.5(1)		ns

1. When CPU access for overhead insertion in the BPTx is enabled, these numbers must be increased by 9.6 ns.

4.2.2 Overhead Monitor Interface

The overhead monitor interface clocks out ohdataouta/b and captures ohdataina/b on the rising edge of ohpclkoa/b. The signal ohpdva/b is raised on the rising edge of ohpclkoa/b that clocks out the first byte of each frame's data. The following illustration shows the overhead monitor interface timing diagram. The table provides the timing variable definitions for the overhead monitor interface.

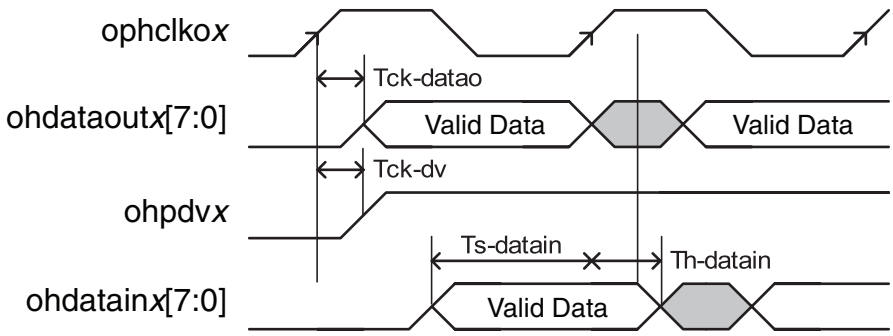


Figure 44. Overhead Monitor Interface Timing

In the following table, all timing is measured at the package balls.

Table 50. Overhead Interface Timing Variable Definitions

Symbol	Parameter	Minimum	Maximum	Unit
Tck-datao	Delay from rising edge of ohpclkoa/b to valid data on ohdataouta/b	0.09(1)	5.0(1)	ns
Tck-dv	Delay from rising edge of ohpclkoa/b to valid data on ohdataouta/b	0.02(1)	5.0(1)	ns
DCohpclko	Duty cycle of ohpclkoa/b	45	55	%
Ts-datain	Setup time from data valid on ohdataina/b to rising edge of ohpclkoa/b	4.35 + 0.075*C_{LD}(2)		ns
Th-datain	Hold time from data valid on ohdataina/b to rising edge of ohpclkoa/b	0		ns
C_{in}	Input capacitance of ohdatain pins		3.3	pF

1. Any significant difference in loading between ohpclkoa/b and the associated ohdataout and ohpdv alters these numbers by 0.075 ns per pF.

2. C_{LD} is the pin load seen by the ohpclkoa/b output measured in pF.

4.2.3 High-Speed Interface

The high-speed interfaces receive and transmit serial data with TFI-5 electrical specifications at 2.488 Gbps and 622.08 Mbps. Signal data rates must be an exact multiple (8x, 16x or 32x) of the reference frequency provided on tfi_refclk. Inputs can tolerate a combined wander and skew of ± 140 ns. There is no fixed phase relationship required or implied between any high-speed input or output and the reference clock (tfi_refclk).

The input receivers and output drivers incorporate programmable equalization to reduce the effects of signal degradation from copper media. For more information, see "HSIRx Control and Monitoring," page 59. The input receivers also incorporate a signal-strength-based loss-of-signal detection with programmable threshold. The output drivers can be programmed to one of two drive levels.

The AC specifications of the high-speed interface are shown in the following table. All timing is measured at the package balls, and all minimum and maximum values are given for the recommended operating conditions.

Table 51. High-Speed Interface Receiver Side AC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
f_{RxD}	Data transmission rate, full speed (nominally 2.488 Gbps for TFI-5 operation)	0.622 – 100 ppm	2.488 + 100 ppm	Gbps
f_{RxDQ}	Quarter-speed data transmission rate (for STS-12 mode)	0.622 – 100 ppm	2.488 + 100 ppm	Gbps
f_{RefClk}	tfi_refclk ± clock frequency	f_{RxD}/32, f_{RxD}/16, f_{RxD}/8	f_{RxD}/32, f_{RxD}/16, f_{RxD}/8	MHz
T_r and T_f	Rise time and fall time of incoming signal for 2.488 Gbps		200	ps
RL_{in}	Input return loss, 10 MHz to 1.875 GHz	9		dB
S_{RxD}	Skew across all 136 TFI-5 ports (earliest to latest, with no wander)(1)		300	ns
T_{CID}	Maximum run length of consecutive identical digits allowed in the data to maintain the specified jitter tolerance		72	UI

1. Wander and skew are handled by the elastic store. The sum of peak-to-peak wander and skew must not exceed S_{RXD}.

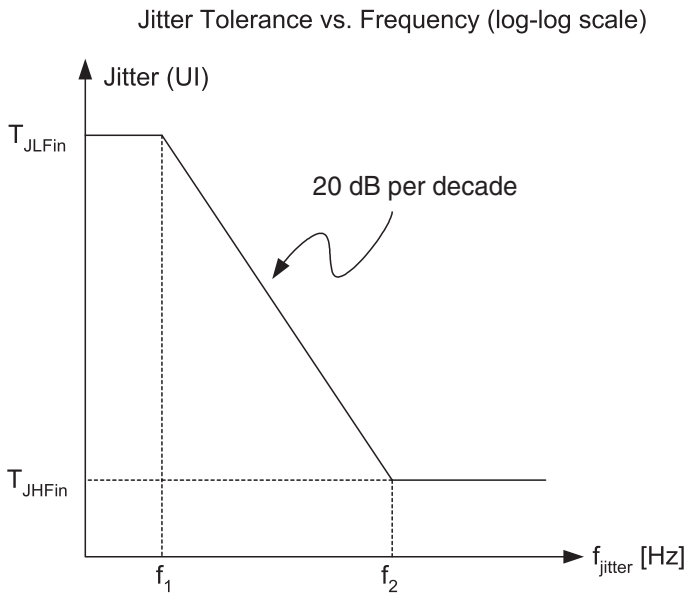


Figure 45. Receive Jitter Tolerance Mask

The following table shows the values when using default CRU loop bandwidth settings. Jitter tolerance can be increased by adjusting the loop bandwidth parameters. For more information, contact Vitesse.

Table 52. Receiver Jitter Tolerance Mask Definitions

Symbol	Parameter	Maximum	Unit	Condition
f_1	First corner frequency of jitter tolerance mask.	440	Hz	See Table 51.
f_2	Second corner frequency of jitter tolerance mask.	1.0	MHz	See Table 51.
T_{JLFin}	Input peak-to-peak jitter or wander below f_1 in jitter tolerance mask	750	UI	
T_{JHFin1}	Input peak-to-peak jitter (random + deterministic + sinusoidal) above f_2 with input equalization enabled	0.7	UI	
T_{JHFin2}	Input peak-to-peak jitter (random + deterministic + sinusoidal) above f_2 with input equalization disabled	0.33	UI	

The following table shows the AC characteristics for the high-speed interface transmitter side.

Table 53. High-Speed Interface Transmitter Side AC Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
f_{TxD}	TxD transmission rate, full speed (nominally 2.488 Gbps for TFI-5)	0.622 – 100 ppm	2.488 + 100 ppm	Gbps
f_{TxDQ}	Quarter-speed data transmission rate (for STS-12 mode)	0.622 – 100 ppm	2.488 + 100 ppm	Gbps
T_r and T_f	TxD[135:0] + rise time and fall time	60	140	ps
RL_{out}	Output return loss, 10 MHz to 1.875 GHz	7.5		dB
S_{TxD}	Skew across data TxD[135:0] channels.	–200	200	ps
T_{Jotot}	Output jitter (random + deterministic) unfiltered		120	ps
T_{Jorand}	Output jitter (random) unfiltered peak-to-peak at 1e-12 BER		84	ps

The reference clock provided on tfi_refclkp and tfi_refclkn must comply with the jitter values contained in Table 54, page 133 for the high-speed interfaces to meet the specifications in Table 52, page 132 and Table 53, page 132.

Table 54. Reference Clock Jitter Tolerance

Symbol	Parameter	Maximum	Unit	Condition
T_{JLFin}	RMS value of the random and sinusoidal jitter in the frequency range 12 kHz to 10 MHz	1.5	ps	RMS
T_{JHFin}	RMS value of the random and sinusoidal jitter in the frequency range above 10 MHz	7.5	ps	RMS

4.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC9295 device.

Table 55. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage to core digital standard cells	1.14	1.2	1.26	V
V_{DDAP}	Power supply voltage to high-speed digital circuitry in the high-speed interface	1.14	1.2	1.26	V
V_{DD18}	Power supply voltage to high-speed interface	1.71		2.625	V
V_{DDIO}	Power supply voltage to CMOS I/O	2.375		3.46	V
T	Operating temperature(1)	–10		110	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

4.4 Stress Ratings

This section contains the stress ratings for the VSC9295 device.

Table 56. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage, potential to GND	–0.5	1.32	V
V_{DDAP}	Power supply voltage, potential to GND	–0.5	1.32	V
V_{DD18}	Power supply voltage, potential to GND	–0.5	2.75	V
V_{DDIO}	Power supply voltage, potential to GND	–0.5	3.6	V
V_{IN_TTL}	DC input voltage applied (TTL/CMOS pins)	–0.5	5.5	V
V_{IN_CML}	DC input voltage applied (TFI-5/CML pins)	–0.5	1.32	V
I_{OUT}	Output current on any signal pin	–50	50	mA
T_S	Storage temperature	–40	125	°C
V_{ESD_HBM}	Electrostatic discharge voltage, human body model	–500	500	V
V_{ESD_CDM}	Electrostatic discharge voltage, charged device model	–100	100	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

5 Pin Descriptions

This section provides the pin diagram and descriptions for the VSC9295 device.

5.1 Pin Diagrams

The following two illustrations show the pin diagrams for the VSC9295 device. For more information about the abbreviations used in the pin diagrams, see "Pins by Number," page 140.

AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	U	
						odoa3	odoa4	odoa5	odoa6	odoa7	bs4	bs3	bs2	bs1	bs0	bs5	bs6	34
					rp0	rp2	rp4	rp7	rp10	rp13	rp16	rp19	rp22	rp25	rp28	rp31	rp34	33
				odoa2	rn0	rn2	rn4	rn7	rn10	rn13	rn16	rn19	rn22	rn25	rn28	rn31	rn34	32
			odia7	odoa1	rp1	rp3	rp5	rp8	rp11	rp14	rp17	rp20	rp23	rp26	rp29	rp32	rp35	31
		odia5	odia6	odoa0	rn1	rn3	rn5	rn8	rn11	rn14	rn17	rn20	rn23	rn26	rn29	rn32	rn35	30
	tp1	tn1	tp0	tn0	vdd18	vddio	rp6	rp9	rp12	rp15	rp18	rp21	rp24	rp27	rp30	rp33	rp36	29
odia4	tp3	tn3	tp2	tn2	vdda	vddio	rn6	rn9	rn12	rn15	rn18	rn21	rn24	rn27	rn30	rn33	rn36	28
odia3	tp6	tn6	tp5	tn5	tp4	tn4	vdd18	**vss**	**vss**	vdd18	vdda	**vss**	**vss**	vdd18	vdda	**vss**	**vss**	27
odia2	tp9	tn9	tp8	tn8	tp7	tn7	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	26
odia1	tp12	tn12	tp11	tn11	tp10	tn10	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	25
odia0	tp15	tn15	tp14	tn14	tp13	tn13	vddp	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	24
ohdva	tp18	tn18	tp17	tn17	tp16	tn16	vdd18	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	23
ohcka	tp21	tn21	tp20	tn20	tp19	tn19	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	22
odisa	tp24	tn24	tp23	tn23	tp22	tn22	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	21
chsz0	tp27	tn27	tp26	tn26	tp25	tn25	vddp	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	20
chsz1	tp30	tn30	tp29	tn29	tp28	tn28	vdd18	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	19
chsz2	tp33	tn33	tp32	tn32	tp31	tn31	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	18
adr15	tp36	tn36	tp35	tn35	tp34	tn34	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	17
adr14	tp39	tn39	tp38	tn38	tp37	tn37	vddp	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	16
adr13	tp42	tn42	tp41	tn41	tp40	tn40	vdd18	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	15
adr12	tp45	tn45	tp44	tn44	tp43	tn43	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	14
adr11	tp48	tn48	tp47	tn47	tp46	tn46	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	13
adr10	tp51	tn51	tp50	tn50	tp49	tn49	vddp	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	12
adr9	tp54	tn54	tp53	tn53	tp52	tn52	vdd18	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	11
adr8	tp57	tn57	tp56	tn56	tp55	tn55	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	10
adr7	tp60	tn60	tp59	tn59	tp58	tn58	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	9
adr6	tp63	tn63	tp62	tn62	tp61	tn61	vdd18	**vss**	**vss**	vddp	vdd18	**vss**	**vss**	vddp	vdd18	**vss**	**vss**	8
adr5	tp65	tn65	tp64	tn64	adr4	vddio	rn72	rn75	rn78	rn81	rn84	rn87	rn90	rn93	rn96	rn99	rn102	7
	tp67	tn67	tp66	tn66	adr3	vddio	rp72	rp75	rp78	rp81	rp84	rp87	rp90	rp93	rp96	rp99	rp102	6
		adr0	adr1	adr2	rn68	rn70	rn73	rn76	rn79	rn82	rn85	rn88	rn91	rn94	rn97	rn100	rn103	5
			dat15	dat14	rp68	rp70	rp73	rp76	rp79	rp82	rp85	rp88	rp91	rp94	rp97	rp100	rp103	4
				dat13	rn69	rn71	rn74	rn77	rn80	rn83	rn86	rn89	rn92	rn95	rn98	rn101	rn104	3
					rp69	rp71	rp74	rp77	rp80	rp83	rp86	rp89	rp92	rp95	rp98	rp101	rp104	2
						dat12	dat11	dat10	dat9	dat8	dat7	dat6	dat5	dat4	dat3	dat2	dat1	1

Figure 46. Pin Diagram (Left Half of Bottom View)

T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
bs7	tck	tdi	tdo	tms	trstb	tsckn	tsckp	xio5	t8krf							34
rp37	rp40	rp43	rp46	rp49	rp52	rp55	rp58	rp61	rp64	rp66						33
rn37	rn40	rn43	rn46	rn49	rn52	rn55	rn58	rn61	rn64	rn66	rfsl0					32
rp38	rp41	rp44	rp47	rp50	rp53	rp56	rp59	rp62	rp65	rp67	rfckp	rfsl1				31
rn38	rn41	rn44	rn47	rn50	rn53	rn56	rn59	rn62	rn65	rn67	xio8	rfckn	rfsl2			30
rp39	rp42	rp45	rp48	rp51	rp54	rp57	rp60	rp63	vddio	vdd18	tn69	tp69	tn68	tp68		29
rn39	rn42	rn45	rn48	rn51	rn54	rn57	rn60	rn63	vddio	vdda	tn71	tp71	tn70	tp70	plock	28
vdd18	vdda	**vss**	**vss**	vdd18	vdda	**vss**	**vss**	vdd18	tn74	tp74	tn73	tp73	tn72	tp72	xio13	27
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn77	tp77	tn76	tp76	tn75	tp75	xio9	26
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn80	tp80	tn79	tp79	tn78	tp78	shtfm	25
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd18	tn83	tp83	tn82	tp82	tn81	tp81	txpmd	24
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdda	tn86	tp86	tn85	tp85	tn84	tp84	isce	23
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn89	tp89	tn88	tp88	tn87	tp87	pbyp	22
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn92	tp92	tn91	tp91	tn90	tp90	tssns	21
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd18	tn95	tp95	tn94	tp94	tn93	tp93	tsdrv	20
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdda	tn98	tp98	tn97	tp97	tn96	tp96	xio10	19
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn101	tp101	tn100	tp100	tn99	tp99	cpumd	18
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn104	tp104	tn103	tp103	tn102	tp102	odisb	17
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd18	tn107	tp107	tn106	tp106	tn105	tp105	ohckb	16
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdda	tn110	tp110	tn109	tp109	tn108	tp108	ohdvb	15
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn113	tp113	tn112	tp112	tn111	tp111	odib0	14
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn116	tp116	tn115	tp115	tn114	tp114	odib1	13
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdd18	tn119	tp119	tn118	tp118	tn117	tp117	odib2	12
vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	**vss**	vdda	tn122	tp122	tn121	tp121	tn120	tp120	odib3	11
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn125	tp125	tn124	tp124	tn123	tp123	odib4	10
vss	**vss**	vdd	vdd	**vss**	**vss**	vdd	vdd	**vss**	tn128	tp128	tn127	tp127	tn126	tp126	odib5	9
vddp	vdd18	**vss**	**vss**	vddp	vdd18	**vss**	**vss**	vdd18	tn131	tp131	tn130	tp130	tn129	tp129	odib6	8
rn105	rn108	rn111	rn114	rn117	rn120	rn123	rn126	rn129	vddio	vdd18	tn133	tp133	tn132	tp132	odib7	7
rp105	rp108	rp111	rp114	rp117	rp120	rp123	rp126	rp129	vddio	vdda	tn135	tp135	tn134	tp134		6
rn106	rn109	rn112	rn115	rn118	rn121	rn124	rn127	rn130	rn132	rn134	odob5	odob2	odob0			5
rp106	rp109	rp112	rp115	rp118	rp121	rp124	rp127	rp130	rp132	rp134	odob4	odob1				4
rn107	rn110	rn113	rn116	rn119	rn122	rn125	rn128	rn131	rn133	rn135	odob3					3
rp107	rp110	rp113	rp116	rp119	rp122	rp125	rp128	rp131	rp133	rp135						2
dat0	dswrn	rdwrn	asale	csn	intn	nwcfg	rstn	odob7	odob6							1

Figure 47. Pin Diagram (Right Half of Bottom View)

5.2 Pins by Function

This section contains the functional pin descriptions for the VSC9295 device.

5.2.1 External Signal Descriptions

External signal pins for the VSC9295 are defined in the following tables. The signal pins are divided according to function.

Table 57. Data Traffic Signals

Signal Name	Description	I/O	Level	Frequency
rxdp[135:0]	High-speed receive serial data, true	I	TFI-5	0.622 Gbps to 2.488 Gbps
rxdn[135:0]	High-speed receive serial data, complement	I	TFI-5	0.622 Gbps to 2.488 Gbps
txdp[135:0]	High-speed transmit serial data, true	O	TFI-5	0.622 Gbps to 2.488 Gbps
txdn[135:0]	High-speed receive serial data, complement	O	TFI-5	0.622 Gbps to 2.488 Gbps

Table 58. CPU Interface Signals

Signal Name	Description	I/O	Level	Frequency
addr[15:0]	Address bits	I	LVCMOS	53 MWps
data[15:0]	Data bits (bidirectional)	B	LVCMOS	53 MWps
csn	Device select (active low)	I	LVCMOS	<16.5 MHz
ds_wrn	Data strobe (Motorola mode), write bar (Intel mode)	I	LVCMOS	53 MHz
rd_wrn	Read/write bar (Motorola mode), read bar (Intel mode)	I	LVCMOS	53 MHz
as_ale	Address strobe (Motorola mode), address latch enable (Intel mode)	I	LVCMOS	53 MHz
intn	Interrupt (active low)	O	LVCMOS	Async
rstn	Master hardware reset (active low)	I	LVCMOS	Async
cpu_mode	CPU mode selection (0 = Motorola, 1 = Intel)	I	LVCMOS	Static
newcfg	Request to update active connection maps (active high)	I	LVCMOS	Async

Table 59. Frame Synchronization Signals

Signal Name	Description	I/O	Level	Frequency
tfi_8kref	External frame sync (TFI8KREF) (rising edge, duty cycle 0.01% to 55%)	I	LVCMOS	8 kHz

Table 60. Overhead Monitor Interface Signals

Signal Name	Description	I/O	Level	Frequency
ohdataouta[7:0]	Dropped overhead bytes, port A (for inputs rxd0-67)	O	LVCMOS	78 MWps
ohdataina[7:0]	Overhead bytes to be added, port A (for outputs txd0-67)	I	LVCMOS	78 MWps
ohpclkoa	Clock to external FPGA, port A	O	LVCMOS	78 MHz

Table 60. Overhead Monitor Interface Signals *(continued)*

Signal Name	Description	I/O	Level	Frequency
ohpdva	Data valid pulse to external FPGA, port A	O	LVCMOS	8 kHz
ohpdisablea	Disables operation of the overhead monitor interface, port A (high to disable)	I	LVCMOS	Static
ohdataoutb[7:0]	Dropped overhead bytes, port B (for inputs rxd68-135)	O	LVCMOS	78 MWps
ohdatainb[7:0]	Overhead bytes to be added, port B (for outputs txd68-135)	I	LVCMOS	78 MWps
ohpclkob	Clock to external FPGA, port B	O	LVCMOS	78 MHz
ohpdvb	Data valid pulse to external FPGA, port B	O	LVCMOS	8 kHz
ohpdisableb	Disables operation of the overhead monitor interface, port B (high to disable)	I	LVCMOS	Static

Table 61. JTAG Interface Signals

Signal Name	Description	I/O	Level	Frequency
tdi	Test data In (ignored when trstb = 0)	I	LVCMOS	10 MHz
tdo	Test data out (high impedance in normal operation)	O	LVCMOS	10 MHz
tms	Test mode select (ignored when trstb = 0)	I	LVCMOS	10 MHz
tck	Test clock (ignored when trstb = 0)	I	LVCMOS	10 MHz
tstrstb	Test reset bar (low for normal device operation)	I	LVCMOS	10 MHz

Table 62. CMU Signals

Signal Name	Description	I/O	Level	Frequency
tfi_refclkn	Reference clock for framed data, complement (internally terminated, internally biased)	I	TFI-5 / AC	78 MHz to 311 MHz
tfi_refclkp	Reference clock for framed data, true (internally terminated, internally biased)	I	TFI-5 / AC	78 MHz to 311 MHz
refsel[2:0]	Reference clock divide ratio selection (see Table 30, page 116	I	LVCMOS	Static
plock	CMU PLL lock indicator (high when PLL locked)	O	LVCMOS	Async
testclkp	Test clock output, true (leave open if unused)	O	TFI-5	311 MHz
testclkn	Test clock output, complement (leave open if unused)	O	TFI-5	311 MHz

Table 63. Miscellaneous Signals

Signal Name	Description	I/O	Level	Frequency
bitslice[7:0]	Bitslicing mode controls For more information, see "Bitslicing and Sizing," page 22 and "Bitslicing Modes and Bit Pair Select Mode," page 42.	I	LVCMOS	Static
chipsize[2:0]	Global channel configuration	I	LVCMOS	Static
trnspntmod	Forces entire device into Transparent mode if high	I	LVCMOS	Static
xio9,xio10,xio13	VCO range controls (tie high for normal operation)	I	LVCMOS	Static
xio5, xio8	Test outputs (Vitesse use only, leave open)			

Table 64. Test Mode Signals

Signal Name	Description	I/O	Level	Frequency
tstdrv	Drive port test input (Vitesse use only, tie low)	I	LCMOS	10 MHz
tstsns	Sense port test output (Vitesse use only, leave open)	O	LCMOS	10 MHz
isce	Forces core and I/O to full scan test mode (Vitesse use only, tie low)	I	LVCMOS	Static
pllbyp	Forces PLL to pass reference clock as VCO clock for functional test (Vitesse use only, tie low)	I	LVCMOS	Static
shortfrm	Forces the device to use short frames (see SyncMan requirements, tie low if unused)	I	LVCMOS	Static

5.2.2 External Power Descriptions

The following tables contain the external power descriptions.

Table 65. Core Power

Signal Name	Description	Voltage
VDD	Positive power supply to core digital standard cells	1.2 V
VSS	Ground to core digital standard cells	0

Table 66. CMOS I/O Power

Signal Name	Description	Voltage
VDDIO	Positive power supply to CMOS I/O	3.3 V / 2.5 V
VSSIO	Ground to CMOS I/O	0

Table 67. High-Speed Interface Power

Signal Name	Description	Voltage
VDDA/P	Positive power supply to high-speed digital circuitry in HSI	1.2 V
VDD18	High voltage supply to HSI	2.5 V / 1.8 V

5.3 Pins by Number

This section provides a numerical list of the VSC9295 pins.

Table 68. Pins by Number

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
A7	ohdatainb7	odib7	B26	txdp75	tp75
A8	ohdatainb6	odib6	B27	txdp72	tp72
A9	ohdatainb5	odib5	B28	txdp70	tp70
A10	ohdatainb4	odib4	B29	txdp68	tp68
A11	ohdatainb3	odib3	C5	ohdataoutb0	odob0
A12	ohdatainb2	odib2	C6	txdn134	tn134
A13	ohdatainb1	odib1	C7	txdn132	tn132
A14	ohdatainb0	odib0	C8	txdn129	tn129
A15	ohpdvb	ohdvb	C9	txdn126	tn126
A16	ohpclkob	ohckb	C10	txdn123	tn123
A17	ohpdisableb	odisb	C11	txdn120	tn120
A18	cpu_mode	cpumd	C12	txdn117	tn117
A19	xio10	xio10	C13	txdn114	tn114
A20	tstdrv	tsdrv	C14	txdn111	tn111
A21	tstsns	tssns	C15	txdn108	tn108
A22	pllbyp	pbyp	C16	txdn105	tn105
A23	isce	isce	C17	txdn102	tn102
A24	trnspntmod	txpmd	C18	txdn99	tn99
A25	shortfrm	shtfm	C19	txdn96	tn96
A26	xio9	xio9	C20	txdn93	tn93
A27	xio13	xio13	C21	txdn90	tn90
A28	plock	plock	C22	txdn87	tn87
B6	txdp134	tp134	C23	txdn84	tn84
B7	txdp132	tp132	C24	txdn81	tn81
B8	txdp129	tp129	C25	txdn78	tn78
B9	txdp126	tp126	C26	txdn75	tn75
B10	txdp123	tp123	C27	txdn72	tn72
B11	txdp120	tp120	C28	txdn70	tn70
B12	txdp117	tp117	C29	txdn68	tn68
B13	txdp114	tp114	C30	refsel2	rfsl2
B14	txdp111	tp111	D4	ohdataoutb1	odob1
B15	txdp108	tp108	D5	ohdataoutb2	odob2
B16	txdp105	tp105	D6	txdp135	tp135
B17	txdp102	tp102	D7	txdp133	tp133
B18	txdp99	tp99	D8	txdp130	tp130
B19	txdp96	tp96	D9	txdp127	tp127
B20	txdp93	tp93	D10	txdp124	tp124
B21	txdp90	tp90	D11	txdp121	tp121
B22	txdp87	tp87	D12	txdp118	tp118
B23	txdp84	tp84	D13	txdp115	tp115
B24	txdp81	tp81	D14	txdp112	tp112

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
B25	txdp78	tp78	D15	txdp109	tp109
D16	txdp106	tp106	E32	refsel0	rfsl0
D17	txdp103	tp103	F2	rxdp135	rp135
D18	txdp100	tp100	F3	rxdn135	rn135
D19	txdp97	tp97	F4	rxdp134	rp134
D20	txdp94	tp94	F5	rxdn134	rn134
D21	txdp91	tp91	F6	vddapp	vddap
D22	txdp88	tp88	F7	vdd18	vdd18
D23	txdp85	tp85	F8	txdp131	tp131
D24	txdp82	tp82	F9	txdp128	tp128
D25	txdp79	tp79	F10	txdp125	tp125
D26	txdp76	tp76	F11	txdp122	tp122
D27	txdp73	tp73	F12	txdp119	tp119
D28	txdp71	tp71	F13	txdp116	tp116
D29	txdp69	tp69	F14	txdp113	tp113
D30	tfi_refclkn	rfckn	F15	txdp110	tp110
D31	refsel1	rfsl1	F16	txdp107	tp107
E3	ohdataoutb3	odob3	F17	txdp104	tp104
E4	ohdataoutb4	odob4	F18	txdp101	tp101
E5	ohdataoutb5	odob5	F19	txdp98	tp98
E6	txdn135	tn135	F20	txdp95	tp95
E7	txdn133	tn133	F21	txdp92	tp92
E8	txdn130	tn130	F22	txdp89	tp89
E9	txdn127	tn127	F23	txdp86	tp86
E10	txdn124	tn124	F24	txdp83	tp83
E11	txdn121	tn121	F25	txdp80	tp80
E12	txdn118	tn118	F26	txdp77	tp77
E13	txdn115	tn115	F27	txdp74	tp74
E14	txdn112	tn112	F28	vddap	vdda
E15	txdn109	tn109	F29	vdd18	vdd18
E16	txdn106	tn106	F30	rxdn67	rn67
E17	txdn103	tn103	F31	rxdp67	rp67
E18	txdn100	tn100	F32	rxdn66	rn66
E19	txdn97	tn97	F33	rxdp66	rp66
E20	txdn94	tn94	G1	ohdataoutb6	odob6
E21	txdn91	tn91	G2	rxdp133	rp133
E22	txdn88	tn88	G3	rxdn133	rn133
E23	txdn85	tn85	G4	rxdp132	rp132
E24	txdn82	tn82	G5	rxdn132	rn132
E25	txdn79	tn79	G6	vddio	vddio
E26	txdn76	tn76	G7	vddio	vddio
E27	txdn73	tn73	G8	txdn131	tn131
E28	txdn71	tn71	G9	txdn128	tn128
E29	txdn69	tn69	G10	txdn125	tn125
E30	xio8	xio8	G11	txdn122	tn122

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
E31	tfi_refclkp	rfckp	G12	txdn119	tn119
G13	txdn116	tn116	H24	vdd18	vdd18
G14	txdn113	tn113	H25	vss	vss
G15	txdn110	tn110	H26	vss	vss
G16	txdn107	tn107	H27	vdd18	vdd18
G17	txdn104	tn104	H28	rxdn63	rn63
G18	txdn101	tn101	H29	rxdp63	rp63
G19	txdn98	tn98	H30	rxdn62	rn62
G20	txdn95	tn95	H31	rxdp62	rp62
G21	txdn92	tn92	H32	rxdn61	rn61
G22	txdn89	tn89	H33	rxdp61	rp61
G23	txdn86	tn86	H34	xio5	xio5
G24	txdn83	tn83	J1	rstn	rstn
G25	txdn80	tn80	J2	rxdp128	rp128
G26	txdn77	tn77	J3	rxdn128	rn128
G27	txdn74	tn74	J4	rxdp127	rp127
G28	vddio	vddio	J5	rxdn127	rn127
G29	vddio	vddio	J6	rxdp126	rp126
G30	rxdn65	rn65	J7	rxdn126	rn126
G31	rxdp65	rp65	J8	vss	vss
G32	rxdn64	rn64	J9	vdd	vdd
G33	rxdp64	rp64	J10	vdd	vdd
G34	tfi_8kref	t8krf	J11	vss	vss
H1	ohdataoutb7	odob7	J12	vss	vss
H2	rxdp131	rp131	J13	vdd	vdd
H3	rxdn131	rn131	J14	vdd	vdd
H4	rxdp130	rp130	J15	vss	vss
H5	rxdn130	rn130	J16	vss	vss
H6	rxdp129	rp129	J17	vdd	vdd
H7	rxdn129	rn129	J18	vdd	vdd
H8	vdd18	vdd18	J19	vss	vss
H9	vss	vss	J20	vss	vss
H10	vss	vss	J21	vdd	vdd
H11	vddap	vdda	J22	vdd	vdd
H12	vdd18	vdd18	J23	vss	vss
H13	vss	vss	J24	vss	vss
H14	vss	vss	J25	vdd	vdd
H15	vddap	vdda	J26	vdd	vdd
H16	vdd18	vdd18	J27	vss	vss
H17	vss	vss	J28	rxdn60	rn60
H18	vss	vss	J29	rxdp60	rp60
H19	vddap	vdda	J30	rxdn59	rn59
H20	vdd18	vdd18	J31	rxdp59	rp59
H21	vss	vss	J32	rxdn58	rn58
H22	vss	vss	J33	rxdp58	rp58

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
H23	vddap	vdda	J34	testclkp	tsckp
K1	newcfg	nwcfg	L12	vdd	vdd
K2	rxdp125	rp125	L13	vss	vss
K3	rxdn125	rn125	L14	vss	vss
K4	rxdp124	rp124	L15	vdd	vdd
K5	rxdn124	rn124	L16	vdd	vdd
K6	rxdp123	rp123	L17	vss	vss
K7	rxdn123	rn123	L18	vss	vss
K8	vss	vss	L19	vdd	vdd
K9	vdd	vdd	L20	vdd	vdd
K10	vdd	vdd	L21	vss	vss
K11	vss	vss	L22	vss	vss
K12	vss	vss	L23	vdd	vdd
K13	vdd	vdd	L24	vdd	vdd
K14	vdd	vdd	L25	vss	vss
K15	vss	vss	L26	vss	vss
K16	vss	vss	L27	vddap	vdda
K17	vdd	vdd	L28	rxdn54	rn54
K18	vdd	vdd	L29	rxdp54	rp54
K19	vss	vss	L30	rxdn53	rn53
K20	vss	vss	L31	rxdp53	rp53
K21	vdd	vdd	L32	rxdn52	rn52
K22	vdd	vdd	L33	rxdp52	rp52
K23	vss	vss	L34	tstrstb	trstb
K24	vss	vss	M1	csn	csn
K25	vdd	vdd	M2	rxdp119	rp119
K26	vdd	vdd	M3	rxdn119	rn119
K27	vss	vss	M4	rxdp118	rp118
K28	rxdn57	rn57	M5	rxdn118	rn118
K29	rxdp57	rp57	M6	rxdp117	rp117
K30	rxdn56	rn56	M7	rxdn117	rn117
K31	rxdp56	rp56	M8	vddap	vddp
K32	rxdn55	rn55	M9	vss	vss
K33	rxdp55	rp55	M10	vss	vss
K34	testclkn	tsckn	M11	vdd	vdd
L1	intn	intn	M12	vdd	vdd
L2	rxdp122	rp122	M13	vss	vss
L3	rxdn122	rn122	M14	vss	vss
L4	rxdp121	rp121	M15	vdd	vdd
L5	rxdn121	rn121	M16	vdd	vdd
L6	rxdp120	rp120	M17	vss	vss
L7	rxdn120	rn120	M18	vss	vss
L8	vdd18	vdd18	M19	vdd	vdd
L9	vss	vss	M20	vdd	vdd
L10	vss	vss	M21	vss	vss

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
L11	vdd	vdd	M22	vss	vss
M23	vdd	vdd	N34	tdo	tdo
M24	vdd	vdd	P1	rd_wrn	rdwrn
M25	vss	vss	P2	rxdp113	rp113
M26	vss	vss	P3	rxdn113	rn113
M27	vdd18	vdd18	P4	rxdp112	rp112
M28	rxdn51	rn51	P5	rxdn112	rn112
M29	rxdp51	rp51	P6	rxdp111	rp111
M30	rxdn50	rn50	P7	rxdn111	rn111
M31	rxdp50	rp50	P8	vss	vss
M32	rxdn49	rn49	P9	vdd	vdd
M33	rxdp49	rp49	P10	vdd	vdd
M34	tms	tms	P11	vss	vss
N1	as_ale	asale	P12	vss	vss
N2	rxdp116	rp116	P13	vdd	vdd
N3	rxdn116	rn116	P14	vdd	vdd
N4	rxdp115	rp115	P15	vss	vss
N5	rxdn115	rn115	P16	vss	vss
N6	rxdp114	rp114	P17	vdd	vdd
N7	rxdn114	rn114	P18	vdd	vdd
N8	vss	vss	P19	vss	vss
N9	vdd	vdd	P20	vss	vss
N10	vdd	vdd	P21	vdd	vdd
N11	vss	vss	P22	vdd	vdd
N12	vss	vss	P23	vss	vss
N13	vdd	vdd	P24	vss	vss
N14	vdd	vdd	P25	vdd	vdd
N15	vss	vss	P26	vdd	vdd
N16	vss	vss	P27	vss	vss
N17	vdd	vdd	P28	rxdn45	rn45
N18	vdd	vdd	P29	rxdp45	rp45
N19	vss	vss	P30	rxdn44	rn44
N20	vss	vss	P31	rxdp44	rp44
N21	vdd	vdd	P32	rxdn43	rn43
N22	vdd	vdd	P33	rxdp43	rp43
N23	vss	vss	P34	tdi	tdi
N24	vss	vss	R1	ds_wrn	dswrn
N25	vdd	vdd	R2	rxdp110	rp110
N26	vdd	vdd	R3	rxdn110	rn110
N27	vss	vss	R4	rxdp109	rp109
N28	rxdn48	rn48	R5	rxdn109	rn109
N29	rxdp48	rp48	R6	rxdp108	rp108
N30	rxdn47	rn47	R7	rxdn108	rn108
N31	rxdp47	rp47	R8	vdd18	vdd18
N32	rxdn46	rn46	R9	vss	vss

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
N33	rxdp46	rp46	R10	vss	vss
R11	vdd	vdd	T22	vss	vss
R12	vdd	vdd	T23	vdd	vdd
R13	vss	vss	T24	vdd	vdd
R14	vss	vss	T25	vss	vss
R15	vdd	vdd	T26	vss	vss
R16	vdd	vdd	T27	vdd18	vdd18
R17	vss	vss	T28	rxdn39	rn39
R18	vss	vss	T29	rxdp39	rp39
R19	vdd	vdd	T30	rxdn38	rn38
R20	vdd	vdd	T31	rxdp38	rp38
R21	vss	vss	T32	rxdn37	rn37
R22	vss	vss	T33	rxdp37	rp37
R23	vdd	vdd	T34	bitslice7	bs7
R24	vdd	vdd	U1	data1	dat1
R25	vss	vss	U2	rxdp104	rp104
R26	vss	vss	U3	rxdn104	rn104
R27	vddap	vdda	U4	rxdp103	rp103
R28	rxdn42	rn42	U5	rxdn103	rn103
R29	rxdp42	rp42	U6	rxdp102	rp102
R30	rxdn41	rn41	U7	rxdn102	rn102
R31	rxdp41	rp41	U8	vss	vss
R32	rxdn40	rn40	U9	vdd	vdd
R33	rxdp40	rp40	U10	vdd	vdd
R34	tck	tck	U11	vss	vss
T1	data0	dat0	U12	vss	vss
T2	rxdp107	rp107	U13	vdd	vdd
T3	rxdn107	rn107	U14	vdd	vdd
T4	rxdp106	rp106	U15	vss	vss
T5	rxdn106	rn106	U16	vss	vss
T6	rxdp105	rp105	U17	vdd	vdd
T7	rxdn105	rn105	U18	vdd	vdd
T8	vddap	vddp	U19	vss	vss
T9	vss	vss	U20	vss	vss
T10	vss	vss	U21	vdd	vdd
T11	vdd	vdd	U22	vdd	vdd
T12	vdd	vdd	U23	vss	vss
T13	vss	vss	U24	vss	vss
T14	vss	vss	U25	vdd	vdd
T15	vdd	vdd	U26	vdd	vdd
T16	vdd	vdd	U27	vss	vss
T17	vss	vss	U28	rxdn36	rn36
T18	vss	vss	U29	rxdp36	rp36
T19	vdd	vdd	U30	rxdn35	rn35
T20	vdd	vdd	U31	rxdp35	rp35

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
T21	vss	vss	U32	rxdn34	rn34
U33	rxdp34	rp34	W10	vss	vss
U34	bitslice6	bs6	W11	vdd	vdd
V1	data2	dat2	W12	vdd	vdd
V2	rxdp101	rp101	W13	vss	vss
V3	rxdn101	rn101	W14	vss	vss
V4	rxdp100	rp100	W15	vdd	vdd
V5	rxdn100	rn100	W16	vdd	vdd
V6	rxdp99	rp99	W17	vss	vss
V7	rxdn99	m99	W18	vss	vss
V8	vss	vss	W19	vdd	vdd
V9	vdd	vdd	W20	vdd	vdd
V10	vdd	vdd	W21	vss	vss
V11	vss	vss	W22	vss	vss
V12	vss	vss	W23	vdd	vdd
V13	vdd	vdd	W24	vdd	vdd
V14	vdd	vdd	W25	vss	vss
V15	vss	vss	W26	vss	vss
V16	vss	vss	W27	vddap	vdda
V17	vdd	vdd	W28	rxdn30	rn30
V18	vdd	vdd	W29	rxdp30	rp30
V19	vss	vss	W30	rxdn29	rn29
V20	vss	vss	W31	rxdp29	rp29
V21	vdd	vdd	W32	rxdn28	rn28
V22	vdd	vdd	W33	rxdp28	rp28
V23	vss	vss	W34	bitslice0	bs0
V24	vss	vss	Y1	data4	dat4
V25	vdd	vdd	Y2	rxdp95	rp95
V26	vdd	vdd	Y3	rxdn95	rn95
V27	vss	vss	Y4	rxdp94	rp94
V28	rxdn33	rn33	Y5	rxdn94	rn94
V29	rxdp33	rp33	Y6	rxdp93	rp93
V30	rxdn32	rn32	Y7	rxdn93	rn93
V31	rxdp32	rp32	Y8	vddap	vddp
V32	rxdn31	rn31	Y9	vss	vss
V33	rxdp31	rp31	Y10	vss	vss
V34	bitslice5	bs5	Y11	vdd	vdd
W1	data3	dat3	Y12	vdd	vdd
W2	rxdp98	rp98	Y13	vss	vss
W3	rxdn98	rn98	Y14	vss	vss
W4	rxdp97	rp97	Y15	vdd	vdd
W5	rxdn97	rn97	Y16	vdd	vdd
W6	rxdp96	rp96	Y17	vss	vss
W7	rxdn96	rn96	Y18	vss	vss
W8	vdd18	vdd18	Y19	vdd	vdd

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
W9	vss	vss	Y20	vdd	vdd
Y21	vss	vss	AA32	rxdn22	rn22
Y22	vss	vss	AA33	rxdp22	rp22
Y23	vdd	vdd	AA34	bitslice2	bs2
Y24	vdd	vdd	AB1	data6	dat6
Y25	vss	vss	AB2	rxdp89	rp89
Y26	vss	vss	AB3	rxdn89	rn89
Y27	vdd18	vdd18	AB4	rxdp88	rp88
Y28	rxdn27	rn27	AB5	rxdn88	rn88
Y29	rxdp27	rp27	AB6	rxdp87	rp87
Y30	rxdn26	rn26	AB7	rxdn87	rn87
Y31	rxdp26	rp26	AB8	vss	vss
Y32	rxdn25	rn25	AB9	vdd	vdd
Y33	rxdp25	rp25	AB10	vdd	vdd
Y34	bitslice1	bs1	AB11	vss	vss
AA1	data5	dat5	AB12	vss	vss
AA2	rxdp92	rp92	AB13	vdd	vdd
AA3	rxdn92	rn92	AB14	vdd	vdd
AA4	rxdp91	rp91	AB15	vss	vss
AA5	rxdn91	rn91	AB16	vss	vss
AA6	rxdp90	rp90	AB17	vdd	vdd
AA7	rxdn90	rn90	AB18	vdd	vdd
AA8	vss	vss	AB19	vss	vss
AA9	vdd	vdd	AB20	vss	vss
AA10	vdd	vdd	AB21	vdd	vdd
AA11	vss	vss	AB22	vdd	vdd
AA12	vss	vss	AB23	vss	vss
AA13	vdd	vdd	AB24	vss	vss
AA14	vdd	vdd	AB25	vdd	vdd
AA15	vss	vss	AB26	vdd	vdd
AA16	vss	vss	AB27	vss	vss
AA17	vdd	vdd	AB28	rxdn21	rn21
AA18	vdd	vdd	AB29	rxdp21	rp21
AA19	vss	vss	AB30	rxdn20	rn20
AA20	vss	vss	AB31	rxdp20	rp20
AA21	vdd	vdd	AB32	rxdn19	rn19
AA22	vdd	vdd	AB33	rxdp19	rp19
AA23	vss	vss	AB34	bitslice3	bs3
AA24	vss	vss	AC1	data7	dat7
AA25	vdd	vdd	AC2	rxdp86	rp86
AA26	vdd	vdd	AC3	rxdn86	rn86
AA27	vss	vss	AC4	rxdp85	rp85
AA28	rxdn24	rn24	AC5	rxdn85	rn85
AA29	rxdp24	rp24	AC6	rxdp84	rp84
AA30	rxdn23	rn23	AC7	rxdn84	rn84

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
AA31	rxdp23	rp23	AC8	vdd18	vdd18
AC9	vss	vss	AD20	vdd	vdd
AC10	vss	vss	AD21	vss	vss
AC11	vdd	vdd	AD22	vss	vss
AC12	vdd	vdd	AD23	vdd	vdd
AC13	vss	vss	AD24	vdd	vdd
AC14	vss	vss	AD25	vss	vss
AC15	vdd	vdd	AD26	vss	vss
AC16	vdd	vdd	AD27	vdd18	vdd18
AC17	vss	vss	AD28	rxdn15	rn15
AC18	vss	vss	AD29	rxdp15	rp15
AC19	vdd	vdd	AD30	rxdn14	rn14
AC20	vdd	vdd	AD31	rxdp14	rp14
AC21	vss	vss	AD32	rxdn13	rn13
AC22	vss	vss	AD33	rxdp13	rp13
AC23	vdd	vdd	AD34	ohdataouta7	odoa7
AC24	vdd	vdd	AE1	data9	dat9
AC25	vss	vss	AE2	rxdp80	rp80
AC26	vss	vss	AE3	rxdn80	rn80
AC27	vddap	vdda	AE4	rxdp79	rp79
AC28	rxdn18	rn18	AE5	rxdn79	rn79
AC29	rxdp18	rp18	AE6	rxdp78	rp78
AC30	rxdn17	rn17	AE7	rxdn78	rn78
AC31	rxdp17	rp17	AE8	vss	vss
AC32	rxdn16	rn16	AE9	vdd	vdd
AC33	rxdp16	rp16	AE10	vdd	vdd
AC34	bitslice4	bs4	AE11	vss	vss
AD1	data8	dat8	AE12	vss	vss
AD2	rxdp83	rp83	AE13	vdd	vdd
AD3	rxdn83	rn83	AE14	vdd	vdd
AD4	rxdp82	rp82	AE15	vss	vss
AD5	rxdn82	rn82	AE16	vss	vss
AD6	rxdp81	rp81	AE17	vdd	vdd
AD7	rxdn81	rn81	AE18	vdd	vdd
AD8	vddap	vddp	AE19	vss	vss
AD9	vss	vss	AE20	vss	vss
AD10	vss	vss	AE21	vdd	vdd
AD11	vdd	vdd	AE22	vdd	vdd
AD12	vdd	vdd	AE23	vss	vss
AD13	vss	vss	AE24	vss	vss
AD14	vss	vss	AE25	vdd	vdd
AD15	vdd	vdd	AE26	vdd	vdd
AD16	vdd	vdd	AE27	vss	vss
AD17	vss	vss	AE28	rxdn12	rn12
AD18	vss	vss	AE29	rxdp12	rp12

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
AD19	vdd	vdd	AE30	rxdn11	rn11
AE31	rxdp11	rp11	AG8	vdd18	vdd18
AE32	rxdn10	rn10	AG9	vss	vss
AE33	rxdp10	rp10	AG10	vss	vss
AE34	ohdataouta6	odoa6	AG11	vdd18	vdd18
AF1	data10	dat10	AG12	vddap	vddp
AF2	rxdp77	rp77	AG13	vss	vss
AF3	rxdn77	rn77	AG14	vss	vss
AF4	rxdp76	rp76	AG15	vdd18	vdd18
AF5	rxdn76	rn76	AG16	vddap	vddp
AF6	rxdp75	rp75	AG17	vss	vss
AF7	rxdn75	rn75	AG18	vss	vss
AF8	vss	vss	AG19	vdd18	vdd18
AF9	vdd	vdd	AG20	vddap	vddap
AF10	vdd	vdd	AG21	vss	vss
AF11	vss	vss	AG22	vss	vss
AF12	vss	vss	AG23	vdd18	vdd18
AF13	vdd	vdd	AG24	vddap	vddp
AF14	vdd	vdd	AG25	vss	vss
AF15	vss	vss	AG26	vss	vss
AF16	vss	vss	AG27	vdd18	vdd18
AF17	vdd	vdd	AG28	rxdn6	rn6
AF18	vdd	vdd	AG29	rxdp6	rp6
AF19	vss	vss	AG30	rxdn5	rn5
AF20	vss	vss	AG31	rxdp5	rp5
AF21	vdd	vdd	AG32	rxdn4	rn4
AF22	vdd	vdd	AG33	rxdp4	rp4
AF23	vss	vss	AG34	ohdataouta4	odoa4
AF24	vss	vss	AH1	data12	dat12
AF25	vdd	vdd	AH2	rxdp71	rp71
AF26	vdd	vdd	AH3	rxdn71	rn71
AF27	vss	vss	AH4	rxdp70	rp70
AF28	rxdn9	rn9	AH5	rxdn70	rn70
AF29	rxdp9	rp9	AH6	vddio	vddio
AF30	rxdn8	rn8	AH7	vddio	vddio
AF31	rxdp8	rp8	AH8	txdn61	tn61
AF32	rxdn7	rn7	AH9	txdn58	tn58
AF33	rxdp7	rp7	AH10	txdn55	tn55
AF34	ohdataouta5	odoa5	AH11	txdn52	tn52
AG1	data11	dat11	AH12	txdn49	tn49
AG2	rxdp74	rp74	AH13	txdn46	tn46
AG3	rxdn74	rn74	AH14	txdn43	tn43
AG4	rxdp73	rp73	AH15	txdn40	tn40
AG5	rxdn73	rn73	AH16	txdn37	tn37
AG6	rxdp72	rp72	AH17	txdn34	tn34

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
AG7	rxdn72	rn72	AH18	txdn31	tn31
AH19	txdn28	tn28	AJ31	rxdp1	rp1
AH20	txdn25	tn25	AJ32	rxdn0	rn0
AH21	txdn22	tn22	AJ33	rxdp0	rp0
AH22	txdn19	tn19	AK3	data13	dat13
AH23	txdn16	tn16	AK4	data14	dat14
AH24	txdn13	tn13	AK5	addr2	adr2
AH25	txdn10	tn10	AK6	txdn66	tn66
AH26	txdn7	tn7	AK7	txdn64	tn64
AH27	txdn4	tn4	AK8	txdn62	tn62
AH28	vddio	vddio	AK9	txdn59	tn59
AH29	vddio	vddio	AK10	txdn56	tn56
AH30	rxdn3	rn3	AK11	txdn53	tn53
AH31	rxdp3	rp3	AK12	txdn50	tn50
AH32	rxdn2	rn2	AK13	txdn47	tn47
AH33	rxdp2	rp2	AK14	txdn44	tn44
AH34	ohdataouta3	odoa3	AK15	txdn41	tn41
AJ2	rxdp69	rp69	AK16	txdn38	tn38
AJ3	rxdn69	rn69	AK17	txdn35	tn35
AJ4	rxdp68	rp68	AK18	txdn32	tn32
AJ5	rxdn68	rn68	AK19	txdn29	tn29
AJ6	addr3	adr3	AK20	txdn26	tn26
AJ7	addr4	adr4	AK21	txdn23	tn23
AJ8	txdp61	tp61	AK22	txdn20	tn20
AJ9	txdp58	tp58	AK23	txdn17	tn17
AJ10	txdp55	tp55	AK24	txdn14	tn14
AJ11	txdp52	tp52	AK25	txdn11	tn11
AJ12	txdp49	tp49	AK26	txdn8	tn8
AJ13	txdp46	tp46	AK27	txdn5	tn5
AJ14	txdp43	tp43	AK28	txdn2	tn2
AJ15	txdp40	tp40	AK29	txdn0	tn0
AJ16	txdp37	tp37	AK30	ohdataouta0	odoa0
AJ17	txdp34	tp34	AK31	ohdataouta1	odoa1
AJ18	txdp31	tp31	AK32	ohdataouta2	odoa2
AJ19	txdp28	tp28	AL4	data15	dat15
AJ20	txdp25	tp25	AL5	addr1	adr1
AJ21	txdp22	tp22	AL6	txdp66	tp66
AJ22	txdp19	tp19	AL7	txdp64	tp64
AJ23	txdp16	tp16	AL8	txdp62	tp62
AJ24	txdp13	tp13	AL9	txdp59	tp59
AJ25	txdp10	tp10	AL10	txdp56	tp56
AJ26	txdp7	tp7	AL11	txdp53	tp53
AJ27	txdp4	tp4	AL12	txdp50	tp50
AJ28	vddap	vdda	AL13	txdp47	tp47
AJ29	vdd18	vdd18	AL14	txdp44	tp44

Table 68. Pins by Number *(continued)*

Ball	Signal	Signal Abbreviation	Ball	Signal	Signal Abbreviation
AJ30	rxdn1	rn1	AL15	txdp41	tp41
AL16	txdp38	tp38	AN8	txdp63	tp63
AL17	txdp35	tp35	AN9	txdp60	tp60
AL18	txdp32	tp32	AN10	txdp57	tp57
AL19	txdp29	tp29	AN11	txdp54	tp54
AL20	txdp26	tp26	AN12	txdp51	tp51
AL21	txdp23	tp23	AN13	txdp48	tp48
AL22	txdp20	tp20	AN14	txdp45	tp45
AL23	txdp17	tp17	AN15	txdp42	tp42
AL24	txdp14	tp14	AN16	txdp39	tp39
AL25	txdp11	tp11	AN17	txdp36	tp36
AL26	txdp8	tp8	AN18	txdp33	tp33
AL27	txdp5	tp5	AN19	txdp30	tp30
AL28	txdp2	tp2	AN20	txdp27	tp27
AL29	txdp0	tp0	AN21	txdp24	tp24
AL30	ohdataina6	odia6	AN22	txdp21	tp21
AL31	ohdataina7	odia7	AN23	txdp18	tp18
AM5	addr0	adr0	AN24	txdp15	tp15
AM6	txdn67	tn67	AN25	txdp12	tp12
AM7	txdn65	tn65	AN26	txdp9	tp9
AM8	txdn63	tn63	AN27	txdp6	tp6
AM9	txdn60	tn60	AN28	txdp3	tp3
AM10	txdn57	tn57	AN29	txdp1	tp1
AM11	txdn54	tn54	AP7	addr5	adr5
AM12	txdn51	tn51	AP8	addr6	adr6
AM13	txdn48	tn48	AP9	addr7	adr7
AM14	txdn45	tn45	AP10	addr8	adr8
AM15	txdn42	tn42	AP11	addr9	adr9
AM16	txdn39	tn39	AP12	addr10	adr10
AM17	txdn36	tn36	AP13	addr11	adr11
AM18	txdn33	tn33	AP14	addr12	adr12
AM19	txdn30	tn30	AP15	addr13	adr13
AM20	txdn27	tn27	AP16	addr14	adr14
AM21	txdn24	tn24	AP17	addr15	adr15
AM22	txdn21	tn21	AP18	chipsize2	chsz2
AM23	txdn18	tn18	AP19	chipsize1	chsz1
AM24	txdn15	tn15	AP20	chipsize0	chsz0
AM25	txdn12	tn12	AP21	ohpdisablea	odisa
AM26	txdn9	tn9	AP22	ohpclkoa	ohcka
AM27	txdn6	tn6	AP23	ohpdva	ohdva
AM28	txdn3	tn3	AP24	ohdataina0	odia0
AM29	txdn1	tn1	AP25	ohdataina1	odia1
AM30	ohdataina5	odia5	AP26	ohdataina2	odia2
AN6	txdp67	tp67	AP27	ohdataina3	odia3
AN7	txdp65	tp65	AP28	ohdataina4	odia4

6 Package Information

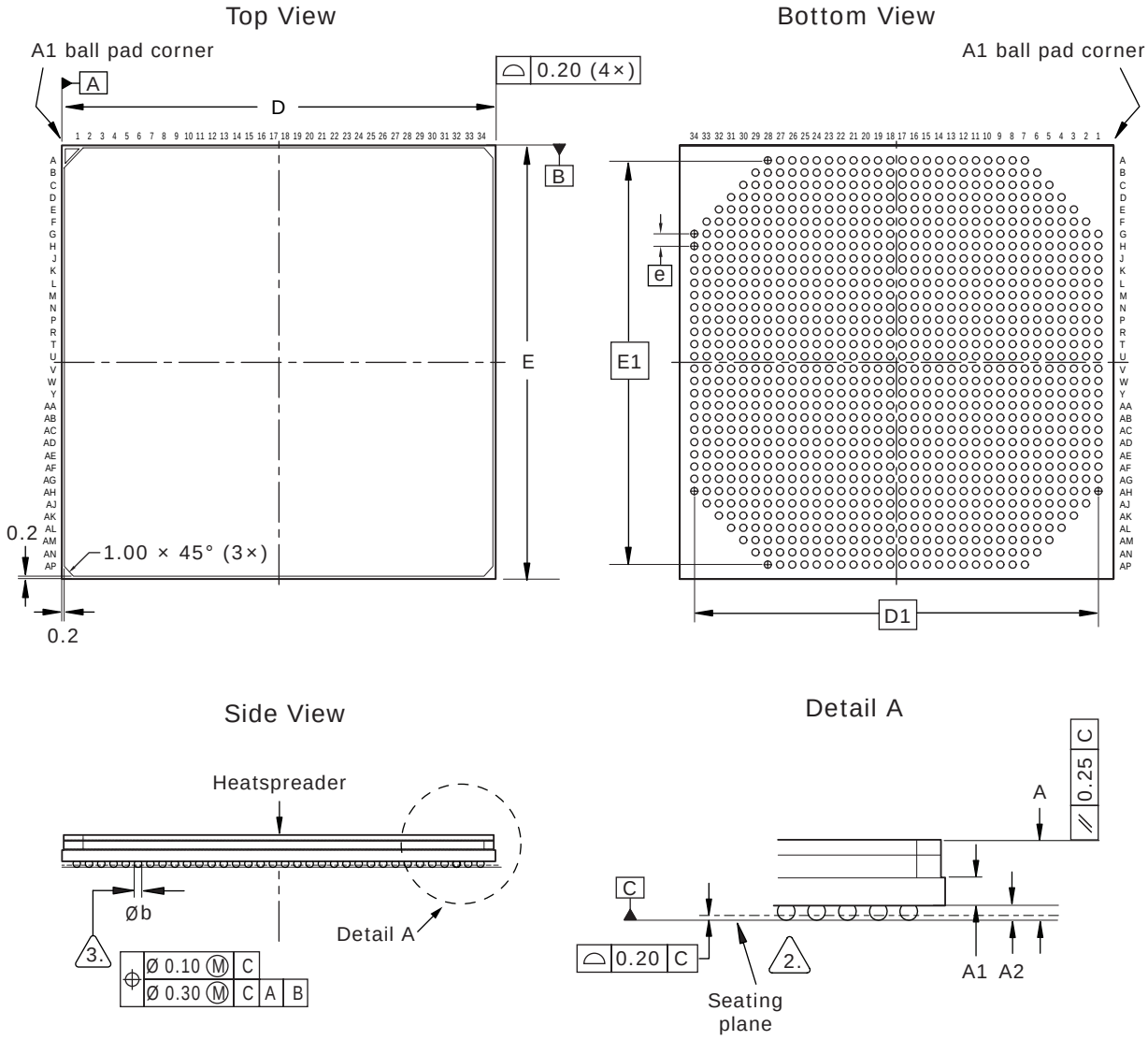
The VSC9295 device is available in two package types. VSC9295SM is a 1072-pin, flip chip ball grid array (FCBGA) with a 45 mm × 45 mm body size, 1.27 mm pin pitch, and 3.4 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC9295XSM.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing and moisture sensitivity rating for the VSC9295 device.

6.1 Package Drawing

The following illustration shows the package drawing for the VSC9295 device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Radial true position is represented by typical values.

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			3.40
A1	0.99	1.09	1.19
A2	0.50	0.60	0.70
D	44.80	45.00	45.20
E	44.80	45.00	45.20
D1		41.91 BSC	
E1		41.91 BSC	
e		1.27 BSC	
b	0.60	0.75	0.90

Figure 48. Package Drawing

6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 69. Thermal Resistances

		θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	**0**	**100**	**200**
VSC9295SM	0.22	10.4	7	5.5
VSC9295XSM	0.22	10.4	7	5.5

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

7 Ordering Information

The VSC9295 device is available in two package types. VSC9295SM is a 1072-pin, flip chip ball grid array (FCBGA) with a 45 mm × 45 mm body size, 1.27 mm pin pitch, and 3.4 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC9295XSM.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC9295 device.

Table 70. Ordering Information

Part Order Number	Description
VSC9295SM	1072-pin FCBGA, 45 mm × 45 mm body size, 1.27 mm pin pitch, and 3.4 mm maximum height
VSC9295XSM	Lead(Pb)-free (second-level interconnect only),1072-pin FCBGA, 45 mm × 45 mm body size, 1.27 mm pin pitch, and 3.4 mm maximum height

CORPORATE HEADQUARTERS
Vitesse Semiconductor Corporation
741 Calle Plano
Camarillo, CA 93012
Tel: 1-800-VITESSE • FAX:1-(805) 987-5896

For application support, latest technical literature, and locations of sales offices,
please visit our web site at
www.vitesse.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:
VSC9295XSM