UPD350

Highly Integrated Small Form Factor USB Type-C™ Power Delivery 3.0 Port Controller

Highlights

- Small Form Factor QFN Package
- Integrated Analog Discrete Components Reduce Bill of Materials and Design Footprint
- USB Power Delivery 3.0 Compliant MAC
- USB Type-C (1) Connector Support with Connection Detection and Control
- I^2C/SPI (2) Interface for CPU/SoC Communication
- USB Type-C™ Alternate Mode Support
- Dual Role Port (DRP) and Fast Role Swap (FRS) Support with DRP offload mode

Target Applications

- Notebook Computers
- All-in-One/Desktop PCs
- Smartphones
- Tablets
- Monitors
- Docking Stations
- HDTVs
- Printers
- Automotive Breakout Boxes
- Multi-port Chargers

Key Benefits

- Integrated Analog Discrete Components
  - VCONN FETs with Rp/Rd Switching
  - Dead Battery Rd termination
  - Programmable Current Sense for Overcurrent Conditions
  - Voltage Sense for Overvoltage Conditions
- Integrated 3.3V Power Switch
  - Provides Dead Battery Support (2)
  - Automatically Switch between VBUS and Main +3.3V
- USB Power Delivery MAC
  - Compliant with USB Power Delivery Specification Revision 3.0
  - Power Delivery Packet Framing
  - CRC Checking/Generation
  - 4B/5B Encoding/Decoding
  - BMC Encoding/Decoding
  - EOP/SOP Generation for PD Frames
  - SOP Detection and SOP Header Processing
  - Separate RX/TX FIFOs
  - Automatic GoodCRC Message Generation
  - Automatic Retry Generation
  - Error Handling
  - Low Standby Power Support
- USB Type-C Cable Detect Logic
  - Auto Cable Attach & Orientation Detection
  - Routes Baseband Communication to Respective CC Pin per Detected Orientation
  - VCONN Supply Control for Active Cable
  - Configurable Downstream Facing Port (DFP) and Upstream Facing Port (UFP) Modes
  - Charging Current Capability Detection
  - Detection of Debug Accessory Mode, Audio Adapter Accessory Mode
- I^2C/SPI Interface Supports Communication/Configuration via Microchip USB Power Delivery hub or supported embedded controller (2)
- Alternate Mode Support
  - DisplayPort™ and other Major Protocols
- **CFG_SEL** Pin for Selection of Device Mode and I^2C addresses (2)
- Power and I/Os
  - Integrated 1.8V Voltage Regulator
  - 10 Configurable General Purpose I/O Pins
- Package
  - 28-QFN (4.0mm x 4.0mm)
- Environmental Product Options
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)
  - Automotive AEC-Q100 Grade 3 (-40°C to +85°C)

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2. *Available only in select UPD350 configurations.*

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1.0 PREFACE

1.1 Glossary of Terms

TABLE 1-1: GLOSSARY OF TERMS

Term	Definition
ADC	Analog to Digital Converter
AFE	Analog Front End
BCI	Baseband CC Interface
Billboard	USB Billboard Device. A required USB device class for UFPs which support Alternate Modes in order to provide product information to the USB Host.
BIST	Built-In Self Test
BMC	Bi-phase Mark Coding
Byte	8-bits
CC	Generic reference to USB Type-C™ Cable / Connector CC1/CC2 pins
CSR	Control and Status Register
DB	Dead Battery
DFP	Downstream Facing Port (USB Type-C™ Specification definition)
DP	DisplayPort (a VESA standard interface)
DPM	Device Policy Manager (PD Specification definition)
DRP	Dual Role Power (USB Type-C™ Specification definition)
DWORD	32-bits
EC	Embedded Controller
EP	USB Endpoint
FIFO	First In First Out buffer
FW	Firmware
FS	Full-Speed
Host	External system (Includes processor, application software, etc.)
HPD	Hot-Plug Detect functionality as defined by DisplayPort and DisplayPort Alternate Mode specifications
HS	High-Speed
HW	Hardware (Refers to function implemented by the device)
IC	Integrated Circuit
IFC	InterFrame Gap
LDO	Linear Drop-Out regulator
MAC	Media Access Controller
Microchip	Microchip Technology Incorporated
N/A	Not Applicable
OCS	Over-Current Sense
PCS	Physical Coding Sublayer
PD / UPD	USB Power Delivery
PIO	General Purpose I/O
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PRBS	Pseudo Random Binary Sequence
QWORD	64-bits
SA	Source Address

TABLE 1-1: GLOSSARY OF TERMS (CONTINUED)

Term	Definition
SBU	SideBand Use
SCSR	System Control and Status Register
SPM	System Policy Manager (PD Specification definition)
SS	SuperSpeed
SVDM	Standard/Vendor Defined Message (PD Specification definition)
SVID	Standard/Vendor IDentity (PD Specification definition)
TCPC	USB Type-C Port Controller
UFP	Upstream Facing Port (USB Type-C™ Specification definition)
USB	Universal Serial Bus
USB Type-C	USB Type-C Cable / Connector
VDO	Vendor-defined Object (PD Specification definition)
VSM	Vendor Specific Messaging
WORD	16-bits
ZLP	Zero Length USB Packet

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
IS	Schmitt-triggered input
I2C	I^2C interface
O8	Output with 8 mA sink and 8 mA source
OD8	Open-drain output with 8 mA sink
PU	70k (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
AIO	Analog bidirectional
P	Power pin

Note: Digital signals are not 5V tolerant unless specified.

Note: Refer to Section 14.5, "DC Characteristics," on page 53 for the electrical characteristics of the various buffers.

1.3 Register Nomenclature

TABLE 1-3: REGISTER NOMENCLATURE

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
RS	**Read to Set:** This bit is set on read.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WC	**Write Anything to Clear:** Writing anything clears the value.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents are self-cleared after the being set. Writes of zero have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** Bits with this attribute will stay high until the bit is read. After it is read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read, the bit will remain high regardless of a change to the high condition.
NASR	**Not Affected by Software Reset.** The state of NASR bits do not change on assertion of a software reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

1.4 References

- NXP I^2C-Bus Specification (UM10204, April 4, 2014): www.nxp.com/documents/user_manual/UM10204.pdf
- USB Power Delivery and USB Type-C™ Specifications: http://www.usb.org/developers/docs/usb_31_102015.zip
- VESA DisplayPort Alternate Mode Specification 1.0: http://www.vesa.org

2.0 INTRODUCTION

2.1 General Description

The UPD350 is a highly integrated, small form factor USB Type-C™ Power Delivery (PD) Port Controller designed to adhere to the *USB Type-C™ Cable and Connector Specification* and *USB Power Delivery 3.0 Specification*. The UPD350 provides cable plug orientation and detection for a USB Type-C receptacle and implements baseband communication with a partner USB Type-C device via the integrated USB Power Delivery 3.0 MAC. The device can function in Standalone UFP modes, or utilize the integrated I^2C/SPI interface to connect to a companion CPU/SoC (dependent on device version, see Section 2.2, "UPD350 Family Differences Summary").

Additionally, the UPD350 integrates many of the analog discrete components required for USB Type-C PD applications, including two VCONN FETs with Rp/Rd switching, a power switch, and current and voltage sense circuitry for over-voltage/current detection. By integrating many of the analog discrete components required for USB Type-C PD applications, the UPD350 provides a low cost, low power, small footprint solution for consumer (notebooks, desktop PCs, smartphones, tablets, monitors, docking stations) applications.

To enable the UPD350 to efficiently support dead battery use cases, an integrated power switch is provided to select between two external 3.3V supplies (VBUS and main). This effectively allows connection detection and system wakeup without external processor intervention (external processor in sleep mode).

The UPD350 is also capable of negotiating alternate modes over USB Type-C connectors using the Power Delivery 3.0 protocol. DisplayPort operation over USB Type-C connectors is supported in addition to other major protocols.

A system diagram utilizing the UPD350 is shown in Figure 2-1. An internal block diagram of the UPD350 is shown in Figure 2-2.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM

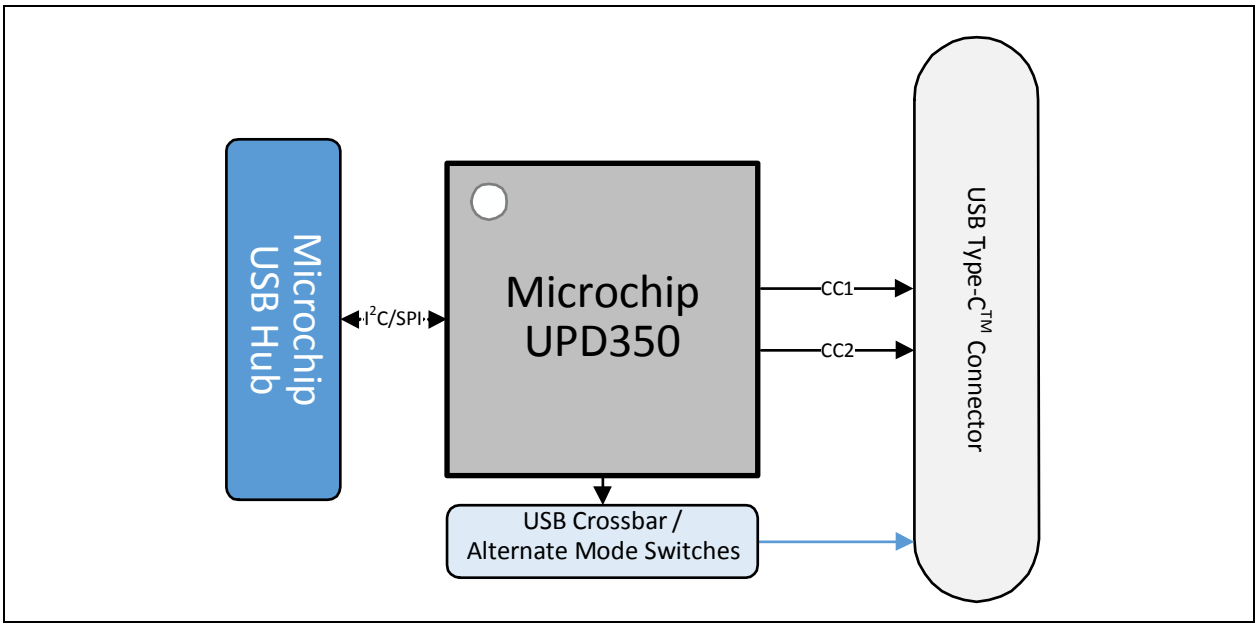
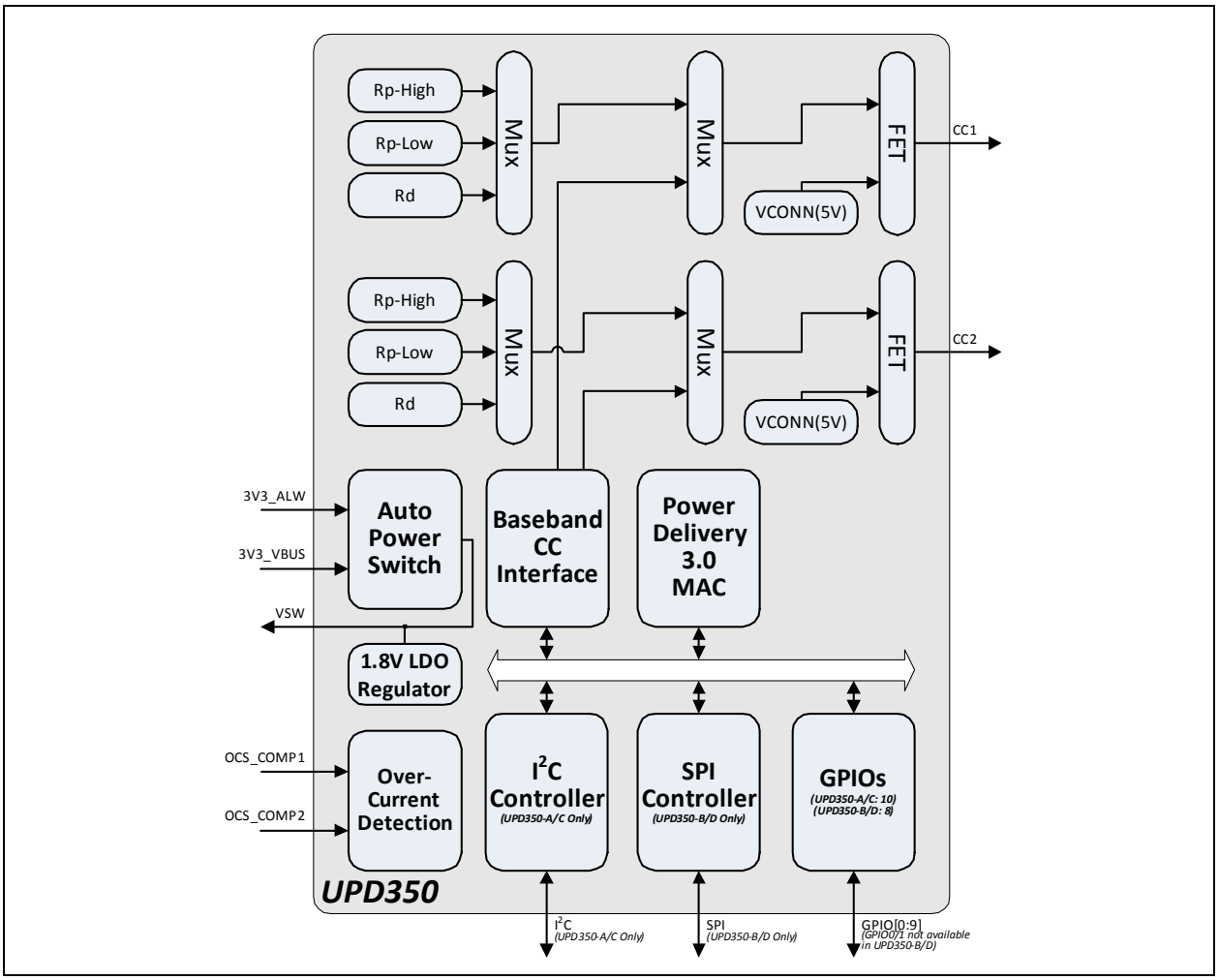


FIGURE 2-2: INTERNAL BLOCK DIAGRAM



2.2 UPD350 Family Differences Summary

The UPD350 is available in four versions:

- UPD350-A
- UPD350-B
- UPD350-C
- UPD350-D

A summary of the differences between these versions is provided in Table 2-1. Device specific features that do no pertain to the entire UPD350 family are called out independently throughout this document. For ordering information, refer to the Product Identification System on page 62.

TABLE 2-1: UPD350 FAMILY DIFFERENCES

Device	+1.8V-3.3V I^2C Interface	SPI Interface	Standalone UFP Mode	Dead Battery Support
UPD350-A	X		X	X
UPD350-B		X		X
UPD350-C	X		X	
UPD350-D		X		

3.0 PIN DESCRIPTIONS AND CONFIGURATION

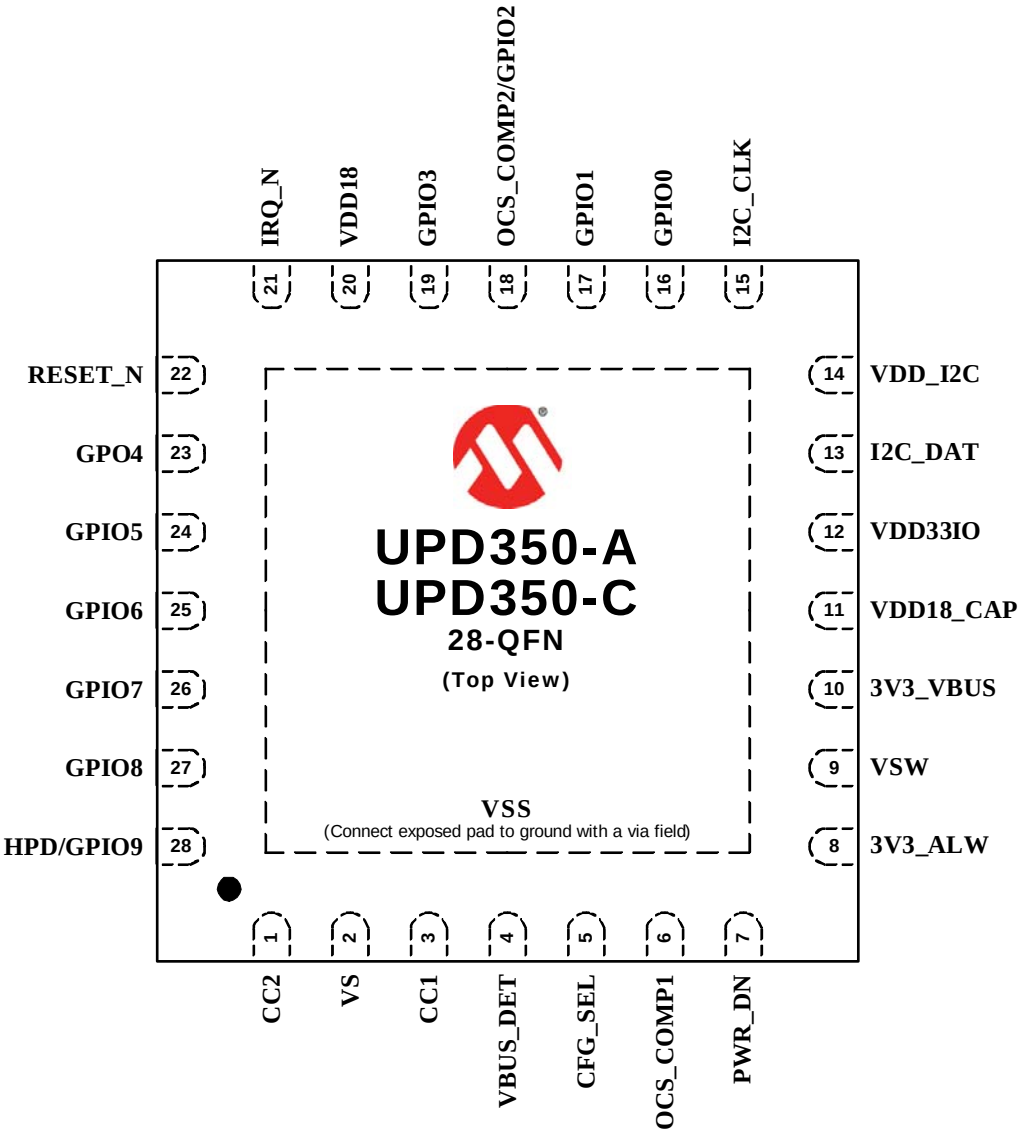
3.1 Pin Assignments

The pin assignments for the UPD350-A / UPD350-C are detailed in Section 3.1.1, "UPD350-A / UPD350-C Pin Assignments," on page 9. The pin assignments for the UPD350-B / UPD350-D are detailed in Section 3.1.2, "UPD350-B / UPD350-D Pin Assignments," on page 11. For information on the differences between the UPD350 family of devices, refer to Section 2.2, "UPD350 Family Differences Summary," on page 8.

3.1.1 UPD350-A / UPD350-C PIN ASSIGNMENTS

The pin assignments of the UPD350-A and UPD350-C devices are identical. The device pin diagram for the UPD350-A / UPD350-C can be seen in Figure 3-1. Table 3-1 provides a UPD350-A / UPD350-C pin assignment table. Pin descriptions are provided in Section 3.2, "Pin Descriptions".

FIGURE 3-1: UPD350-A / UPD350-C PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad (**VSS**) on bottom of package must be connected to ground with a via field.

TABLE 3-1: UPD350-A / UPD350-C PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name
1	CC2	15	I2C_CLK
2	VS	16	GPIO0(Note 3-1)
3	CC1	17	GPIO1(Note 3-1)
4	VBUS_DET	18	OCS_COMP2/GPIO2(Note 3-1)
5	CFG_SEL	19	GPIO3(Note 3-1)
6	OCS_COMP1	20	VDD18
7	PWR_DN	21	IRQ_N
8	3V3_ALW	22	RESET_N
9	VSW	23	GPO4
10	3V3_VBUS	24	GPIO5(Note 3-1)
11	VDD18_CAP	25	GPIO6(Note 3-1)
12	VDD33IO	26	GPIO7(Note 3-1)
13	I2C_DAT	27	GPIO8(Note 3-1)
14	VDD_I2C	28	HPD/GPIO9(Note 3-1)

Note 3-1 This pin provides alternate functions when in Standalone UFP Mode. Refer to Section 3.1.1.1, "UPD350-A / UPD350-C GPIO Functions in Standalone UFP Modes" for additional information.

3.1.1.1 UPD350-A / UPD350-C GPIO Functions in Standalone UFP Modes

When the UPD350-A / UPD350-C is configured in Standalone UFP mode, the following GPIO pins are assigned specific alternate functions, as detailed in Table 3-2.

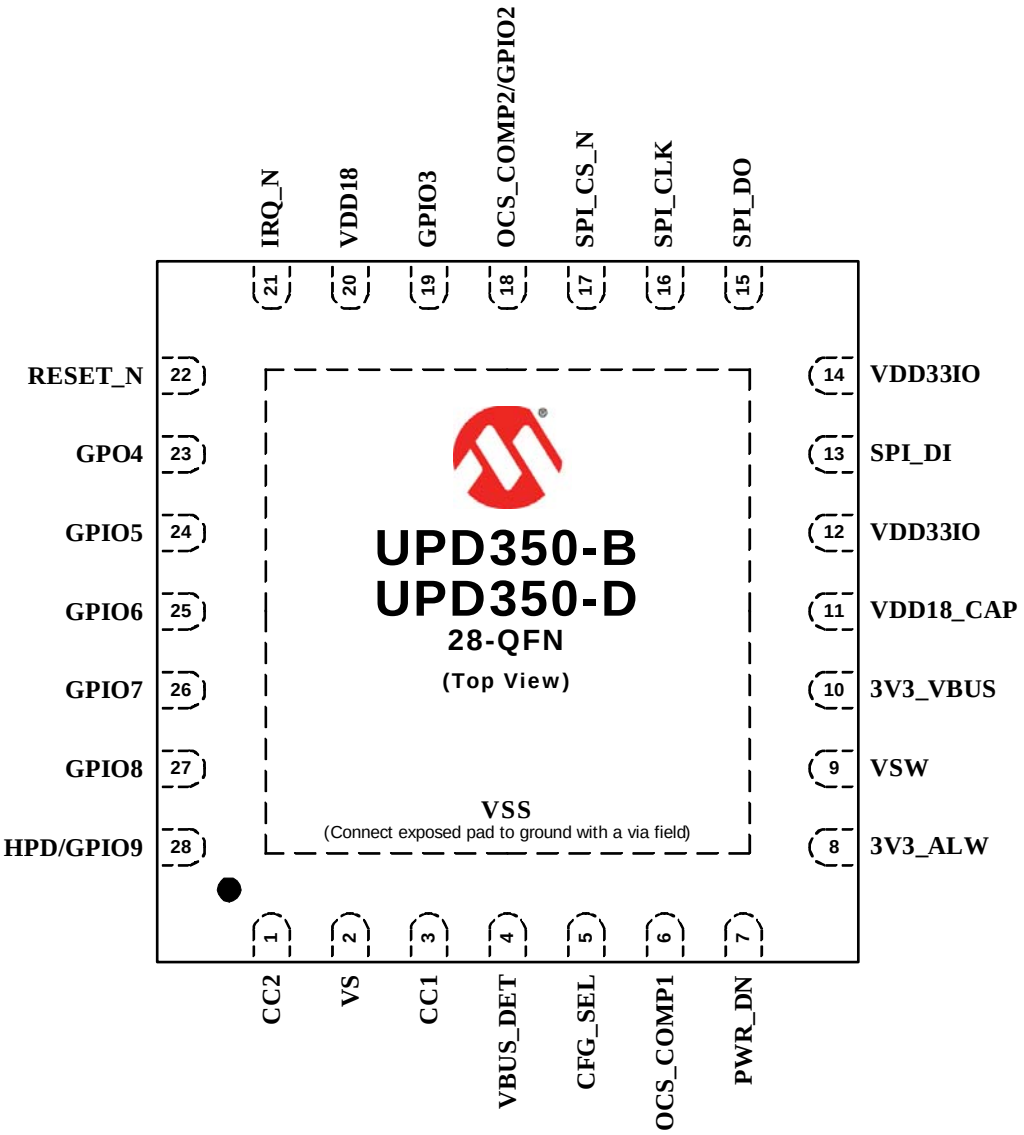
TABLE 3-2: UPD350-A / UPD350-C ALTERNATE GPIO FUNCTIONS IN STANDALONE UFP MODE

Pin	I^2C Companion Mode	Standalone UFP Mode
16	GPIO0	GPIO0
17	GPIO1	GPIO1
18	GPIO2	ORIENTATION
19	GPIO3	ATTACH
23	GPO4	GPO4
24	GPIO5	GPIO5
25	GPIO6	SINK_5V_LEGACY_N
26	GPIO7	SINK_5V_1A5_N
27	GPIO8	SINK_5V_3A0_N
28	GPIO9	GPIO9

3.1.2 UPD350-B / UPD350-D PIN ASSIGNMENTS

The pin assignments of the UPD350-B and UPD350-D devices are identical. The device pin diagram for the UPD350-B / UPD350-D can be seen in Figure 3-2. Table 3-3 provides a UPD350-B / UPD350-D pin assignment table. Pin descriptions are provided in Section 3.2, "Pin Descriptions".

FIGURE 3-2: UPD350-B / UPD350-D PIN ASSIGNMENTS (TOP VIEW)



Note: Exposed pad **(VSS)** on bottom of package must be connected to ground with a via field.

TABLE 3-3: UPD350-B / UPD350-D PIN ASSIGNMENTS

Pin	Pin Name	Pin	Pin Name
1	**CC2**	15	**SPI_DO**
2	**VS**	16	**SPI_CLK**
3	**CC1**	17	**SPI_CS_N**
4	**VBUS_DET**	18	**OCS_COMP2/GPIO2**
5	**CFG_SEL**	19	**GPIO3**
6	**OCS_COMP1**	20	**VDD18**
7	**PWR_DN**	21	**IRQ_N**
8	**3V3_ALW**	22	**RESET_N**
9	**VSW**	23	**GPO4**
10	**3V3_VBUS**	24	**GPIO5**
11	**VDD18_CAP**	25	**GPIO6**
12	**VDD33IO**	26	**GPIO7**
13	**SPI_DI**	27	**GPIO8**
14	**VDD33IO**	28	**HPD/GPIO9**

3.2 Pin Descriptions

This sections details the functions of the various device signals.

TABLE 3-4: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB Type-C™			
Configuration Channel 1	**CC1**	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Configuration Channel 2	**CC2**	AIO	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
I^2C Interface *(UPD350-A / UPD350-C Only)*			
I^2C Clock	**I2C_CLK**	I2C	+1.8/3.3V I^2C clock signal
I^2C Data	**I2C_DAT**	I2C	+1.8/3.3V I^2C data signal
SPI Interface *(UPD350-B / UPD350-D Only)*			
SPI Clock	**SPI_CLK**	IS	SPI clock. The maximum supported SPI clock frequency is 25 MHz.
SPI Data Out	**SPI_DO**	O8	SPI output data.
SPI Data In	**SPI_DI**	IS	SPI input data.
SPI Chip Enable	**SPI_CS_N**	IS	Active low SPI chip enable input.
Power Delivery Control			
Hot Plug Detect	**HPD**	IS/O8	DisplayPort Hot Plug Detection.
VBUS Discharge	**DISCHARGE**	O8	VBUS discharge. **Note:** This signal is not available in the UPD350-B / UPD350-D.
Type-C Attach	**ATTACH**	O8	In the Standalone UFP mode *(UPD350-A / UPD350-C only)*, this signal indicates that the USB Type-C receptacles at the near and far end of the cable both have a plug-in. 0b: Nothing attached 1b: USB Type-C port has an end-end attached **Note:** Float this signal when unused. **Note:** This signal is not available in the UPD350-B / UPD350-D.
Type-C Orientation	**ORIENTATION**	O8	In the Standalone UFP mode *(UPD350-A / UPD350-C only)*, this signal is used to indicate which CC pin is terminated by the attached device. 0b: **CC1** pin is pulled to a higher voltage than **CC2**. 1b: **CC2** pin is pulled to a higher voltage than **CC1**. **Note:** Float this signal when unused. **Note:** This signal is not available in the UPD350-B / UPD350-D.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Sink Legacy Current	**SINK_5V_LEGACY_N**	OD8	In the Standalone UFP mode *(UPD350-A / UPD350-C only)*, this pin asserts autonomously when a source has been detected that provides legacy USB current. **Note:** Float this signal when unused. **Note:** This signal is not available in the UPD350-B / UPD350-D.
Sink 1.5A Current	**SINK_5V_1A5_N**	OD8	In the Standalone UFP mode *(UPD350-A / UPD350-C only)*, this pin asserts autonomously when a source has been detected that provides 1.5A USB current. **Note:** Float this signal when unused. **Note:** This signal is not available in the UPD350-B / UPD350-D.
Sink 3A Current	**SINK_5V_3A0_N**	OD8	In the Standalone UFP mode *(UPD350-A / UPD350-C only)*, this pin asserts autonomously when a source has been detected that provides 3.0A USB current. **Note:** Float this signal when unused. **Note:** This signal is not available in the UPD350-B / UPD350-D.
Miscellaneous			
Interrupt	**IRQ_N**	OD8	Active low interrupt signal. **Note:** Float this signal when unused.
VBUS Detection	**VBUS_DET**	AIO	Scaled down version of VBUS. Tie this signal to VBUS via a resistor divider.
Configuration Select	**CFG_SEL**	AIO	This multi-level configuration signal is sampled after a system reset to select the device's default mode of operation based on the connected 1% precision resistor value. **Note:** This pin is used to determine the default I^2C slave address and operating mode in the UPD350-A / UPD350-C. For the UPD350-B / UPD350-D, this pin can be used for customer specific purposes to provide a discrete value (0-15) based upon the attached resistor value.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
General Purpose I/O 0-9	**GPIO0**, **GPIO1**, **GPIO2**, **GPIO3**, **GPO4**, **GPIO5**, **GPIO6**, **GPIO7**, **GPIO8**, **GPIO9**	IS/O8/ OD8 (PU)	The general purpose I/O signals are fully programmable as either a push-pull output, an open-drain output, or a Schmitt-triggered input (except **GPO4**). A programmable pull-up may optionally be enabled. **Note:** The functionality of these GPIOs is defined and controlled by USB Power Delivery firmware executed external to the UPD350 (in the Microchip USB hub or embedded controller). **Note:** **The GPO4 general purpose signal can only function as an output and must be pulled up externally.** **Note:** Tie these signals to ground when unused. **Note:** External pull-ups and pull-downs shall be placed on GPIO pins to ensure that when in the reset state the inputs to external devices are driven to a valid state. **Note:** **GPIO0** and **GPIO1** are not available in the UPD350-B / UPD350-D. **Note:** In Standalone UFP mode *(UPD350-A / UPD350-C only)*, select GPIOs have alternate dedicated functions, as defined in Section 3.1.1.1, "UPD350-A / UPD350-C GPIO Functions in Standalone UFP Modes," on page 10.
System Reset	**RESET_N**	IS	Active low system reset. **Note:** If this signal is unused, it must be pulled up to **VDD33IO**.
Power Down	**PWR_DN**	AI	When asserted, this signal places the device into the power-down state. **Note:** Tie this signal to ground when unused.
Over-Current Sense Comparator 1	**OCS_COMP1**	AI	This pin is used by the integrated OCS comparator to detect for error conditions. **Note:** Tie this signal to ground when unused.
Over-Current Sense Comparator 2	**OCS_COMP2**	AI	This pin is used by the integrated OCS comparator to detect for error conditions. **Note:** Tie this signal to ground when unused.
Power/Ground			
+3.3V Voltage Switch Supply	**VSW**	P	+3.3V power supply output from the integrated power switch. **Note:** This pin also provides capacitance for the integrated power switch and must be connected to a 1 uF (<100 Mohm ESR) capacitor to ground.
+3.3V VBUS Supply	**3V3_VBUS**	P	+3.3V main power supply input derived from VBUS to the integrated power switch. **Note:** The 2.2 uF capacitor is only required for the UPD350-A and UPD350-B.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+3.3V Always Supply	**3V3_ALW**	P	+3.3V main power supply input to the integrated power switch. **Note:** This pin must be connect to a 2.2 uF capacitor to ground.
+3.3V I/O Power Supply Input	**VDD33IO**	P	+3.3V I/O power supply input.
+3.3/1.8V I^2C Power Supply Input	**VDD_I2C**	P	+3.3/1.8V I^2C power supply input. Tie this pin to **VDD33IO** for +3.3V I^2C interfaces. Tie this pin to **VDD18** for +1.8V I^2C interfaces. **Note:** This pin is not available in the UPD350-B / UPD350-D.
+1.8V Core Voltage Power Supply Input	**VDD18**	P	+1.8V core voltage power supply input.
+1.8V Digital Core Power Supply Capacitor	**VDD18_CAP**	P	+1.8V digital core power supply capacitor. This signal must be connected to a 1uF capacitor to ground for proper operation.
+5V VS Power Supply Input	**VS**	P	+5V VCONN FET power source.
Ground	**VSS**	P	Ground pins.

4.0 I²C SLAVE CONTROLLER *(UPD350-A/UPD350-C ONLY)*

This chapter details the integrated I²C slave controller (**I2C_DAT** and **I2C_CLK**) available in the UPD350-A and UPD350-C. The I²C slave controller can be used for Host CPU serial management and data transfer, and allows host access to all device Configuration and Status Registers.

4.1 I²C Overview

I²C is a bi-directional 2-wire data protocol. A device that is currently sending data is defined as the “transmitter” and a device that is currently receiving data is defined as the “receiver”. The bus is controlled by a master which generates the SCL clock, controls bus access, and generates the start and stop conditions. The master and slave will operate as transmitter or receiver, bit-by-bit, as determined by the master. Since the device I²C controller is a slave only, the terms “host” and “master” are synonymous, both referring to the external side of the interface.

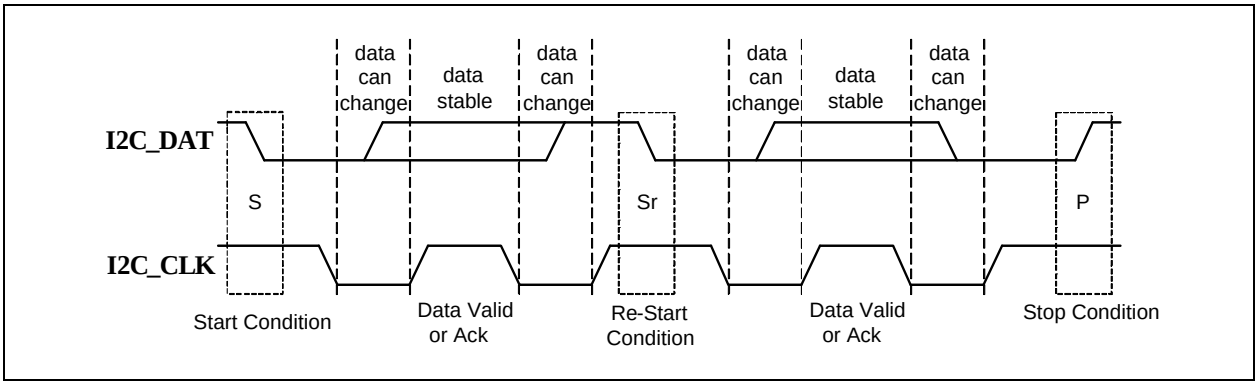
Both the clock (SCL) and data (SDA) signals have analog input filters that reject pulses that are less than 50 ns. The data pin is driven low when either interface sends a low, emulating the wired-AND function of the I²C bus. Since the slave interface never drives the clock pin, the wired-AND is not necessary.

The following bus states exist:

- **Idle:** Both **I2C_DAT** and **I2C_CLK** are high when the bus is idle.
- **Start & Stop Conditions:** A start condition (S) is defined as a high to low transition on the SDA line while SCL is high. A stop condition (P) is defined as a low to high transition on the SDA line while SCL is high. The bus is considered to be busy following a start condition and is considered free 4.7 µs / 1.3 µs / 0.5µs (for 100 kHz / 400 kHz / 1MHz operation, respectively) following a stop condition. The bus stays busy following a repeated start condition (Sr) in the absence of a stop condition. Stop/start sequences and repeated starts are otherwise functionally equivalent.
- **Data Valid:** Data is valid, following the start condition, when SDA is stable while SCL is high. Data can only be changed while the clock is low. There is one valid bit per clock pulse. Every byte must be 8 bits long and is transmitted MSB first.
- **Acknowledge:** Each byte of data is followed by an acknowledge bit. The master generates a ninth clock pulse for this bit, and the transmitter releases SDA (high). To provide a positive “acknowledge” (ACK), the receiver drives SDA low so that it remains valid during the high period of the clock, taking into account the setup and hold times. To provide a negative “no-acknowledge” (NACK or ACK), the receiver will allow the line to remain high during this bit time. The receiver may be the master or the slave depending on the direction of the data. Typically the receiver acknowledges each byte. If the master is the receiver, it does not generate an acknowledge on the last byte of a transfer. This informs the slave to not drive the next byte of data, freeing SDA so that the master may generate a stop or repeated start condition.

Figure 4-1 displays the various bus states of a typical I²C cycle.

FIGURE 4-1: I²C CYCLES



4.2 I²C Slave Operation

The I²C slave serial interface consists of a data wire (**I2C_DAT**) and a serial clock (**I2C_CLK**). The serial clock is driven by the master, while the data wire is bi-directional. Both signals are open-drain and require external pull-up resistors.

The I²C slave controller implements the low level I²C slave serial interface (start and stop condition detection, data bit transmission/reception and acknowledge generation/reception), handles the slave command protocol and performs system register reads and writes. It tolerates and also provides clock stretching, in particular for supporting a transparent Wake on Host Access (see Section 6.3, "Asynchronous I2C Wakeup (UPD350-A/UPD350-C Only)," on page 28).

The I²C slave controller conforms to the NXP *I²C-Bus Specification* (UM10204, April 4, 2014), and supports traffic as defined therein for the following modes:

- Standard-mode (Sm, 100 kbit/s)
- Fast-mode (Fm, 400 kbit/s)
- Fast-mode Plus (Fm+, 1 Mbit/s)

Refer to Section 14.6.2, "I2C Slave Interface (UPD350-A/UPD350-C only)," on page 55 for timing information.

4.2.1 I²C SLAVE COMMAND FORMAT

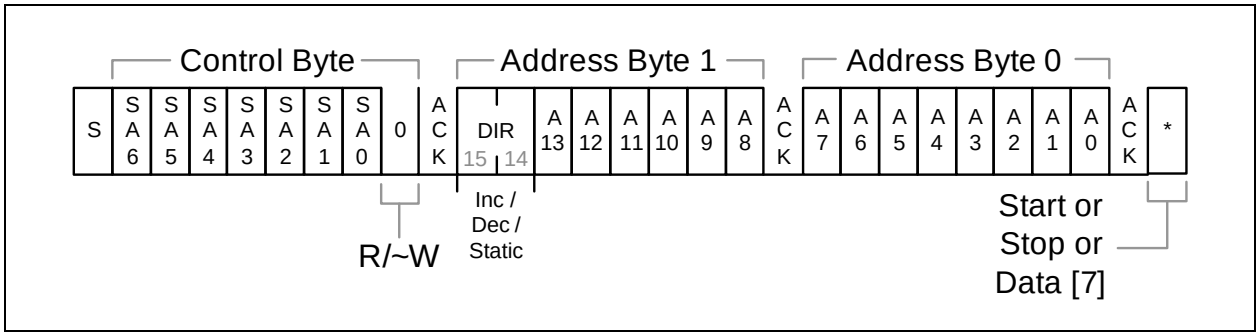
The I²C slave serial interface supports single register and multiple register Read and Write commands. A Read or Write command is started by the master first sending a Start condition, followed by a Control byte. The Control byte consists of a 7-bit slave address and a 1-bit Read/Write indication (R/~W). The default slave address used by the device is selected via the CFG_SEL configuration strap. Assuming the slave address in the Control byte matches this address, the Control byte is acknowledged by the device. Otherwise, the entire sequence is ignored until the next Start condition. The I²C slave controller also supports the General Call Address. The I²C command formats can be seen in Figure 4-2, Figure 4-4, and Figure 4-5.

If the read/write indication (R/~W) in the Control byte is a 0 (Write), the next two bytes sent by the master are a register address, and these two bytes are mandatory. The upper (first) two bits of the address field are a Direction control (DIR), which indicates whether multi-byte accesses will increment, decrement, or fix (as static) the issued address (Section 4.2.2). After the address bytes are acknowledged by the device, the master may send data bytes, which will be written to successive registers starting at this address. It may instead send another Start condition (to start the reading of data) or a Stop condition (only setting the address). The latter two will terminate the current Write before writing any data, but will have the effect of setting the internal register address which will be used for subsequent Reads.

If the read/write indication (R/~W) in the Control byte is a 1 (Read), the device will start sending data following the Control byte acknowledge bit. Read commands cannot designate an address by themselves, but may optionally be prefixed with a Write command to set it (see Figure 4-4, prefixes in gray). If however the Read immediately follows a Multiple Register Write or Read, the address may have been incremented or decremented internally according to its DIR field, so this Read will start its access at the next successive byte address. Also, regardless of the previous access, a multiple-byte Read will continue the Increment/Decrement internally, as determined by the previously-issued DIR field (Section 4.2.2).

The length of the register address field is always two full bytes. Some high-order bits are don't-care. Don't-care register address bits should be sent as '0' always, for upward compatibility.

FIGURE 4-2: I²C SLAVE ADDRESSING



Note:	Within bytes (address and data), the bits are transferred most-significant bit first. Addresses are transferred Most-Significant Byte first. All registers are accessed in units of bytes, and register data is transferred in increasing byte address order. Refer to the device register layout to determine the effect of this on the significance order of any multi-byte value.

4.2.2 MULTIPLE-BYTE REGISTER ADDRESS SEQUENCING

The DIR subfield in Address field bits [15:14] determines how multiple-byte sequences will be interpreted. This field is held internally whenever issued with an address, but is not applied in I^2C except in multiple-byte transfers, Read or Write. The DIR field definitions are as follows:

- **DIR = 00b:** Selects auto-incrementing of the internally-held register address for subsequent byte accesses in a multiple-byte packet.
- **DIR = 10b:** Selects auto-decrementing of the internally-held register address for subsequent byte accesses in a multiple-byte packet.
- **DIR = 11b:** Select a fixed address. No modification of the internal register address will occur, meaning that all subsequent accesses, single- or multiple-byte, are made to the same register.
- **DIR = 01b:** Reserved for future use.

Note that the DIR field is altered only by issuing an address. It remains, affecting any subsequent multiple-byte Read packets, until altered.

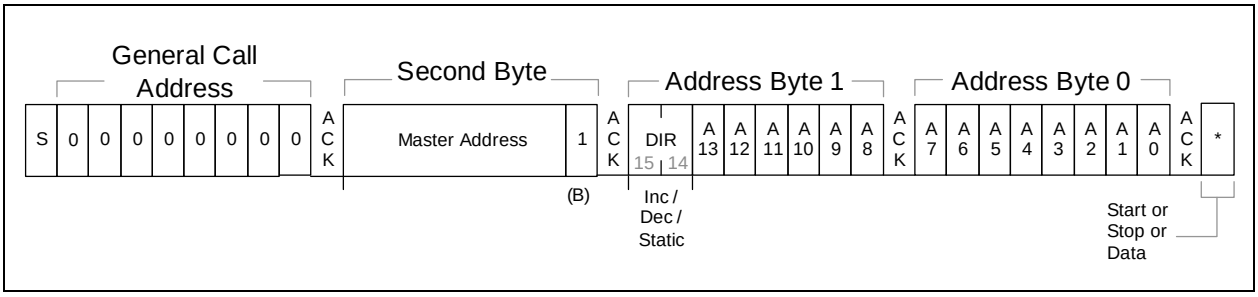
4.2.3 GENERAL CALL ADDRESS

The device supports the I^2C General Call Address. The intent of this feature is to enable global I^2C writes to topologies that have multiple UPD350 slaves. This minimizes the I^2C transactions for device reset, as well as for various common configuration registers. This mode of operation is intended for topologies that consist solely of UPD350 slaves. This mode of operation may not be compatible with non-UPD350 slaves coexisting on the I^2C bus.

Only the case where the least significant bit, “B”, of the General Call address is set to one is supported. The device will ignore the case when the least significant bit, “B”, of the General Call address is set to zero. For the latter case, the device will ACK the first byte, General call address. The device will ignore and silently discard all subsequent bytes and not acknowledge them. The second byte of the General Call address is also ignored and not acknowledged by the device.

Figure 4-3 illustrates the supported General Call Address format.

FIGURE 4-3: I^2C GENERAL CALL ADDRESS



4.2.4 DEVICE INITIALIZATION

Until the device has initialized itself to the point where the various configuration inputs are valid, the I^2C slave interface will not respond to or be affected by any external pin activity. The device should not be accessed by the master in this state. If, however, it is necessary to do so, this state will appear externally as a NACK (high) in the ACK bit time of the Control Byte, and of any further bytes transmitted by the master. The device will continue to act in this manner until the first Start condition is received after it is initialized internally. A Read transaction should not be attempted until an Address Write has been completed successfully (Figure 4-2), since the value(s) read may be unpredictable otherwise. Alternatively, an **IRQ_N** pin assertion can be used to indicate the device is ready.

4.2.5 ACCESS DURING AND FOLLOWING POWER MANAGEMENT

During low-power modes, a Start condition will trigger the device to wake, and the device will also stretch the I2C clock low until its internal clocks are running and locked. It will then release the I2C clock, and process the incoming packet.

It performs these steps before receiving the Slave Address bits, meaning that if there are multiple devices of this type asleep on the same I2C bus segment then they will all stretch the clock, and they will all wake, regardless of whether they were actually addressed. In the event that the slave address of the I2C transaction does not match the value specified in the I2C Slave Address Register (I2C_ADDR) (UPD350-A/UPD350-C Only), the device will power-down automatically.

4.2.6 I2C SLAVE READ SEQUENCE

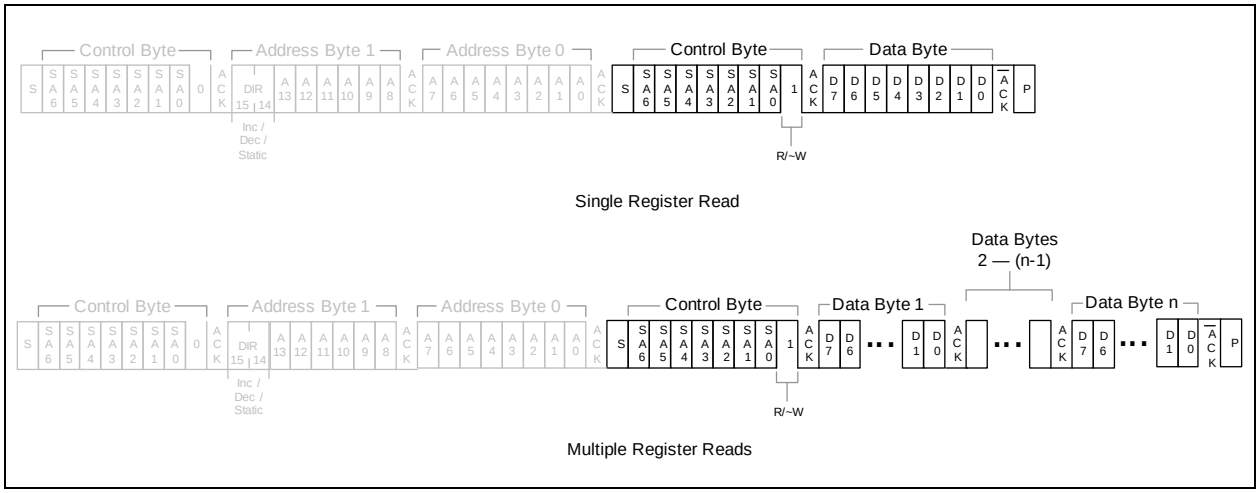
Following the device addressing, as detailed in Section 4.2.1, a register is read from the device when the master sends a Start condition and Control byte with the R/~W bit set to '1'. Assuming the slave address in the Control byte matches the device address, the Control byte is acknowledged by the device. Otherwise, the entire sequence is ignored until the next Start condition. Following the acknowledge, the device sends 1 or more bytes of data, from successive register addresses according to the last-issued DIR address subfield (Section 4.2.2), until the master sends a no-acknowledge followed by the Stop condition. The no-acknowledge informs the device not to send any further bytes.

The internal register address is unchanged if only a single register byte is read, otherwise (a Multiple Register Read) the internal register address may be incremented or decremented (Section 4.2.2) after each byte including the final one. If the internal address reaches its maximum, it rolls over to 0.

If the master sends an unexpected start or stop condition, the device will stop sending immediately and will respond to the next sequence as needed.

Figure 4-4 illustrates a typical single and multiple register read. An optional Write of an address is allowed to occur first, shown in gray. Note that this example shows an abbreviated case, where the Write does not have a Stop condition before the Read transfer's Starts. in this case, the Stop is still allowed, but not required.

FIGURE 4-4: I2C SLAVE READS



4.2.7 I2C SLAVE WRITE SEQUENCE

Following the device addressing, as detailed in Section 4.2.1, a register value is written to the device when the master continues to send data bytes. Each byte is acknowledged by the device. Following any data byte, after the acknowledge, the master may either send another start condition or halt the sequence with a stop condition. The internal register address is unchanged following a single-byte write.

Multiple writes are performed when the master sends additional data bytes following the first. The internal address is automatically incremented and the next register is written. Once the internal address reaches its maximum value, it rolls over to 0. The multiple write is concluded when the master sends another start or stop condition. In performing a multiple write, the internal register address may be incremented or decremented (Section 4.2.2) for each write including the final.

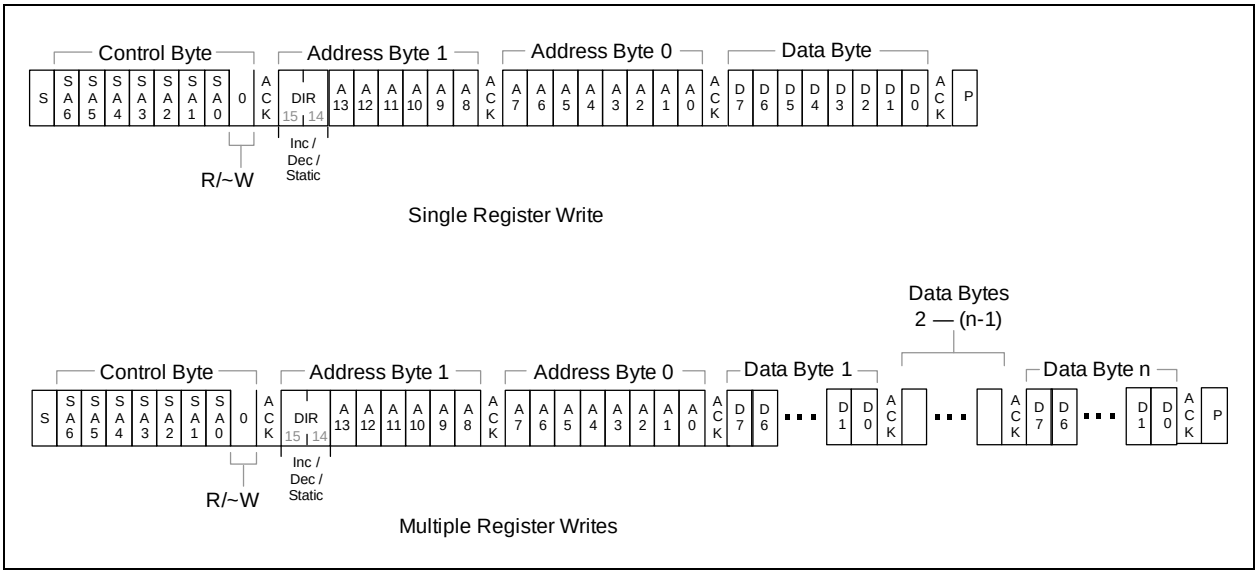
This is not relevant for subsequent writes after a new Start condition, since a new register address (with its DIR subfield) must then be included. However, this would affect the address used by any subsequent read without first resetting the register address.

For both single and multiple writes, if the master sends an unexpected start or stop condition, the device will stop immediately and will respond to the next sequence as needed.

The data write to a multi-byte register may be delayed until after all bits are input. In the event that the full register is not written (master sends a start or a stop condition occurs unexpectedly), the write may be considered invalid and the register not affected. Multiple registers may be written in a multiple write cycle, each one being written in sequence. I^2C writes must not be performed to unused register addresses.

Figure 4-5 illustrates a typical single and multiple register write.

FIGURE 4-5: I^2C SLAVE WRITES



4.2.8 SPECIAL CSR HANDLING

4.2.8.1 Live Bits

Register values are latched (registered) at the beginning of each register read to prevent the host from reading a changing value. The latching occurs individually per register in a multiple register read sequence.

4.2.8.2 Change-on-Read Registers and FIFOs

Any single-byte register that triggers a side-effect from a read operation (for example, containing “clear on read” bits, or advancing a FIFO structure) triggers only after the host has begun accessing the value. The value seen by the master will always be the original value and never the updated result of the side-effect.

For a multiple-byte register that is considered a single unit, the change may be delayed until all bytes of the register have been read. In the event that the host sends a no-acknowledge on one of the first bytes of a multi-byte register, or a start or stop condition occurs unexpectedly before the acknowledge of the full register, the read may be considered invalid and the side-effect not triggered.

4.2.8.3 Live Bits that are also Change-on-Read

As described above, the current value from a register with live bits (as is the case of any register) is captured and latched as output data, and Change on Read bits are then changed in the original register. To prevent loss of a hardware event that occurs following the data capture but before the Change on Read, these hardware events are held pending until after the read action and after any change due to the read. This sequence also ensures an edge in the bit due to the hardware event.

5.0 SPI SLAVE CONTROLLER *(UPD350-B/UPD350-D ONLY)*

This chapter details the integrated SPI slave controller (**SPI_DI**, **SPI_DO**, **SPI_CLK**, and **SPI_CS_N**) available in the UPD350-B and UPD350-D. The SPI slave controller can be used for Host CPU serial management and data transfer, and allows host access to all device Configuration and Status Registers.

5.1 SPI Overview

The SPI Slave module provides a low pin count synchronous slave interface that facilitates communication between the device and a host system. The SPI slave allows access to the System CSRs and internal FIFOs and memories. It supports single and multiple register read and write commands with incrementing, decrementing and static addressing. Only a Single bit lane is supported in SPI mode at up to 25 MHz.

The following is an overview of the functions provided by the SPI Slave:

- **Fast Read:** 4-wire (clock, select, data in and data out) reads. Serial command, address and data. This is called “Fast” Read for historical reasons, and is the only Read command supported. There is a single Dummy byte required for first access. Single and multiple register reads with incrementing, decrementing or static addressing.
- **Write:** 4-wire (clock, select, data in and data out) writes at up to 25 MHz. Serial command, address and data. Single and multiple register writes with incrementing, decrementing or static addressing.

5.2 SPI Slave Operation

A SPI frame starts on the falling edge of **SPI_CS_N**, and ends with **SPI_CS_N** rising. At the edges of **SPI_CS_N**, the **SPI_CLK** clock may be at its reset state of either low (Mode 0) or high (Mode 3), at the option of the Master.

Input data on the **SPI_DI** pin (often called “MOSI”) is sampled on the rising edge of the **SPI_CLK** input clock. Output data is launched on the **SPI_DO** pin (often called “MISO”) with the falling edge of the clock. While the **SPI_CS_N** chip select input is high, the **SPI_DI** and **SPI_CLK** inputs are ignored and the **SPI_DO** output is floating.

Each frame starts with an 8-bit instruction byte, transmitted by the Master, and it is accepted on **SPI_DI** starting at the first rising edge of the input clock after **SPI_CS_N** goes active.

For both Write and (Fast) Read instructions, two address bytes follow the instruction byte. The address field expresses a byte address. Fourteen address bits specify the address. The remaining two bits [15:14] constitute the DIR subfield of the address field, which specifies whether the address is Auto-Incremented (00b) or Auto-Decremented (10b) for consecutive data bytes in the frame. A special Static address coding (11b) keeps the address static throughout the frame of data, causing a single byte address to be accessed repeatedly if multiple bytes are transferred in the frame. DIR subfield encoding 01b is reserved and should be decoded in implementation to be the same as 00b, for the sake of minimizing the effect of a software error that increments beyond the address space.

For the Fast Read instruction, one dummy byte follows the address bytes. The dummy byte occupies 8 bits, one per clock.

The device will normally not drive **SPI_DO** during the Instruction, Address or Dummy byte cycles, but see Section 5.2.2, "Access During and Following Power Management," on page 23 for a special case.

For Fast Read instructions, one or more 8-bit data fields follow the dummy byte. For Write instructions, they immediately follow the address bytes.

Individual bytes in instruction, address and data fields are transferred with the most-significant bit (msb) first. The two-byte Address field is transferred with the most-significant byte (MSB) first. Multi-byte data values are transferred in the order specified by the DIR subfield of the Address field (bits [15:14]), and so their order can be effectively selected by using Increment mode (starting from the lowest byte address) or Decrement mode (starting from the highest byte address).

The SPI interface supports a minimum time of 50ns between successive commands (a minimum **SPI_CS_N** inactive time of 50ns).

The instructions supported by the SPI slave controller are listed in Table 5-1. Unsupported instructions are reserved and must not be used.

TABLE 5-1: SPI INSTRUCTIONS

Instruction	Description	Bus Bit Width	Inst. Code	Address Bytes	Dummy Bytes	Data bytes	Max Freq.
Read							
FASTREAD	Read, higher speed format	1	0Bh	2	1	1 to ∞	25 MHz
Write							
WRITE	Write	1	02h	2	0	1 to ∞	25 MHz

5.2.1 DEVICE INITIALIZATION

Until the device has been initialized to the point where the various configuration inputs are valid, the SPI interface will not respond to or be affected by any external pin activity.

Once device initialization completes, the SPI interface will ignore the pins until a rising edge of **SPI_CS_N** is detected.

If the device initialization completes during an active cycle (**SPI_CS_N** low), the trailing end of the frame must be seen (**SPI_CS_N** returning high) before any internal registers are affected or the state of the SPI interface changes.

The first SPI access after device initialization must always be a dummy read to the SPI Test Register (SPI_TEST) (UPD350-B/UPD350-D Only).

5.2.1.1 SPI Slave Read Polling for Initialization Complete

With an external weak pull-up resistor present on **SPI_DO**, a value of FFh will appear to have been read from any internal register while the device is uninitialized. By verifying the SPI Test Register (SPI_TEST) (UPD350-B/UPD350-D Only) has at least one “0” bit in it, it is possible to tell when the device is initialized.

5.2.2 ACCESS DURING AND FOLLOWING POWER MANAGEMENT

The Wake event on SPI traffic is local to the specific device, and does not affect the states of other devices even on the same SPI bus. Until waking is complete, the SPI interface holds the **SPI_DO** pin low for the duration of the **SPI_CS_N** low time.

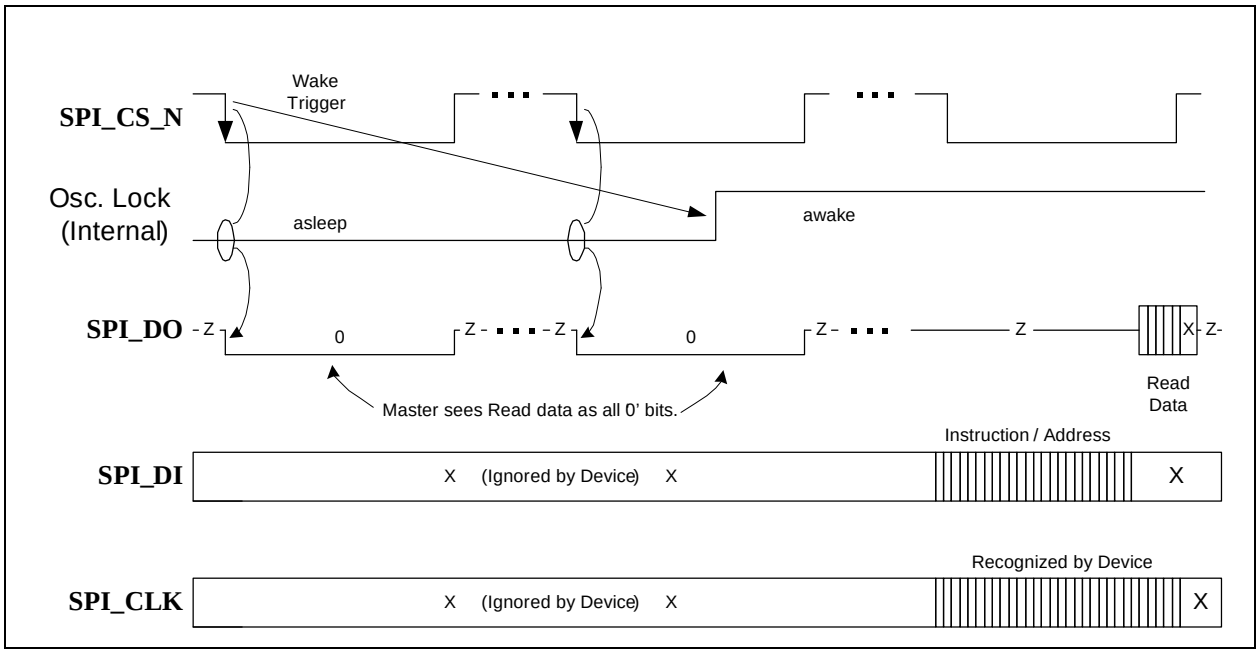
Until the device is awake, then, any Read access performed by the Master will appear to have returned all “1” bits. To determine when the device is awake and the SPI interface functional, the SPI Test Register (SPI_TEST) (UPD350-B/UPD350-D Only) should be repeatedly polled by the Master in separate frames (**SPI_CS_N** low then high). Once a correct, non-zero value is read, the interface can be considered functional. As an alternative to polling, an **IRQ_N** pin assertion can be used to indicate the device is ready.

Once the power management mode changes back to ACTIVE, the SPI interface will still ignore the **SPI_CLK** and **SPI_DI** pins, following **SPI_CS_N** low with **SPI_DO** low, until **SPI_CS_N** is seen high. At the next **SPI_CS_N** falling edge, SPI communication will continue normally.

At any time after performing SPI traffic, the device will not go back to a non-communicating power state until explicitly allowed to do so by a command from the SPI Master.

Figure 5-1 illustrates the sequence of waking from SPI traffic.

FIGURE 5-1: POWER MANAGEMENT WAKE ON SPI TRAFFIC



5.2.3 SPI READ COMMAND (FAST READ)

The Fast Read command is supported by the SPI slave. A single byte, or multiple bytes, may be read in a single frame (**SPI_CS_N** low).

Fast Read is the only form of Read access supported by the device. The instruction inputs the instruction code, the address and a dummy byte on **SPI_DI**, and outputs the data one bit per clock on **SPI_DO**.

The SPI slave interface is selected by first bringing **SPI_CS_N** active. The 8-bit FASTREAD instruction, 0Bh, is input into the **SPI_DI** pin, followed by the two address bytes and 1 dummy byte. The address bytes specify a Byte register address within the device, and also specify how addresses are sequenced for successive bytes in a Multiple Byte Read (below). The contents of the dummy byte are don't-care.

On the falling clock edge following the rising edge of the last dummy bit, the **SPI_DO** pin is driven starting with the most significant bit of the selected register byte. The remaining register bits are shifted out on subsequent falling clock edges.

The **SPI_CS_N** input is brought inactive to conclude the cycle. The **SPI_DO** pin is floated by the device in response.

5.2.3.1 Multiple Byte Reads

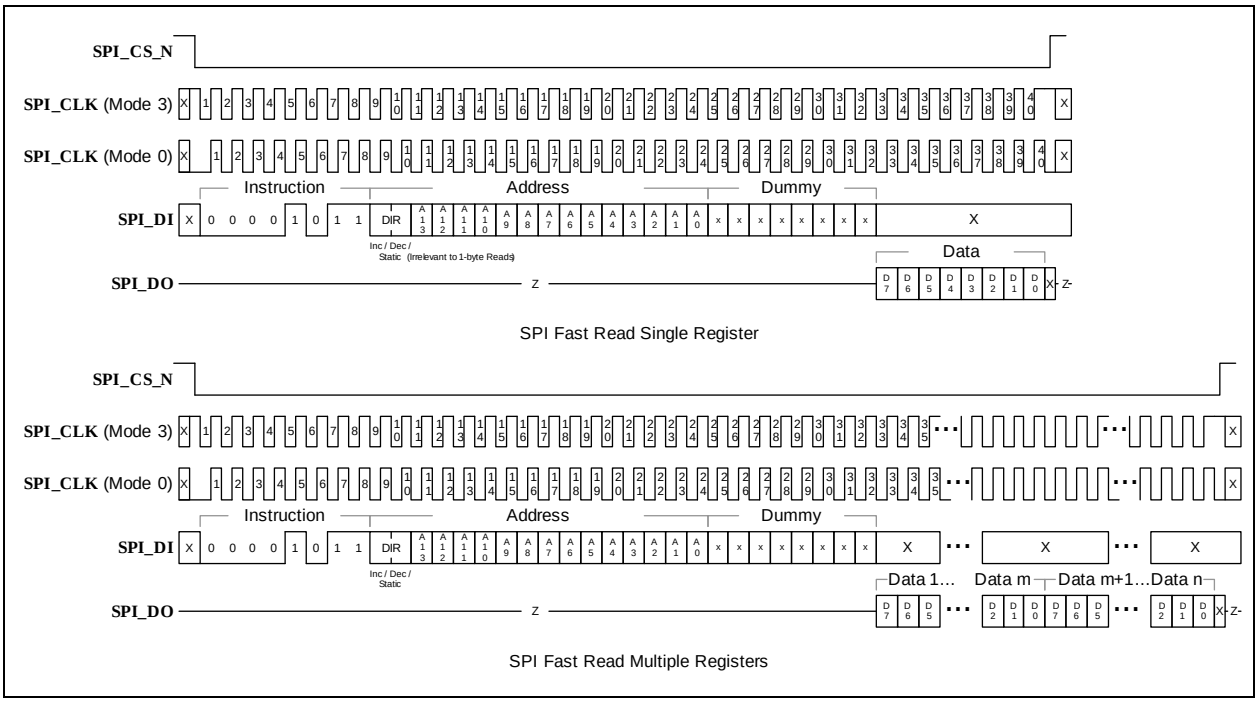
Additional byte reads beyond the first are performed by the Master by continuing the clock pulses while **SPI_CS_N** is active. The upper two bits [15:14] (DIR subfield) of the address specify Auto-Incrementing (DIR=00b) or Auto-Decrementing (DIR=10b) or Static (fixed) (DIR=11b) for successive bytes read. Maintaining a Static internal address is provided for FIFO Read/Write or low-level register polling within a single frame, if the Master supports it.

Towards the end of the current one-byte output shift the address is incremented or decremented, if appropriate, and another synchronized capture sequence is done.

5.2.3.2 Fast Read

Figure 5-2 illustrates a typical single and multiple register fast read for SPI mode.

FIGURE 5-2: SPI FAST READ



5.2.4 SPI WRITE COMMANDS

The following write commands are supported by the SPI slave controller:

- Write
- Multiple Writes

5.2.4.1 Write

The Write instruction provides the instruction code and address and data bytes on the **SPI_DI** pin, one bit per clock.

The SPI transfer is started by the Master first driving **SPI_CS_N** active. The 8-bit WRITE instruction, 02h, is given on the **SPI_DI** pin, followed by the two address bytes. The address bytes specify a byte address within the device, and a Direction control subfield (DIR).

The data immediately follows the address bytes on the **SPI_DI** pin, starting with the most significant bit of the first byte. The data is input from the **SPI_DI** pin by the device, shifted in on each subsequent rising clock edge.

5.2.4.2 Multiple Writes

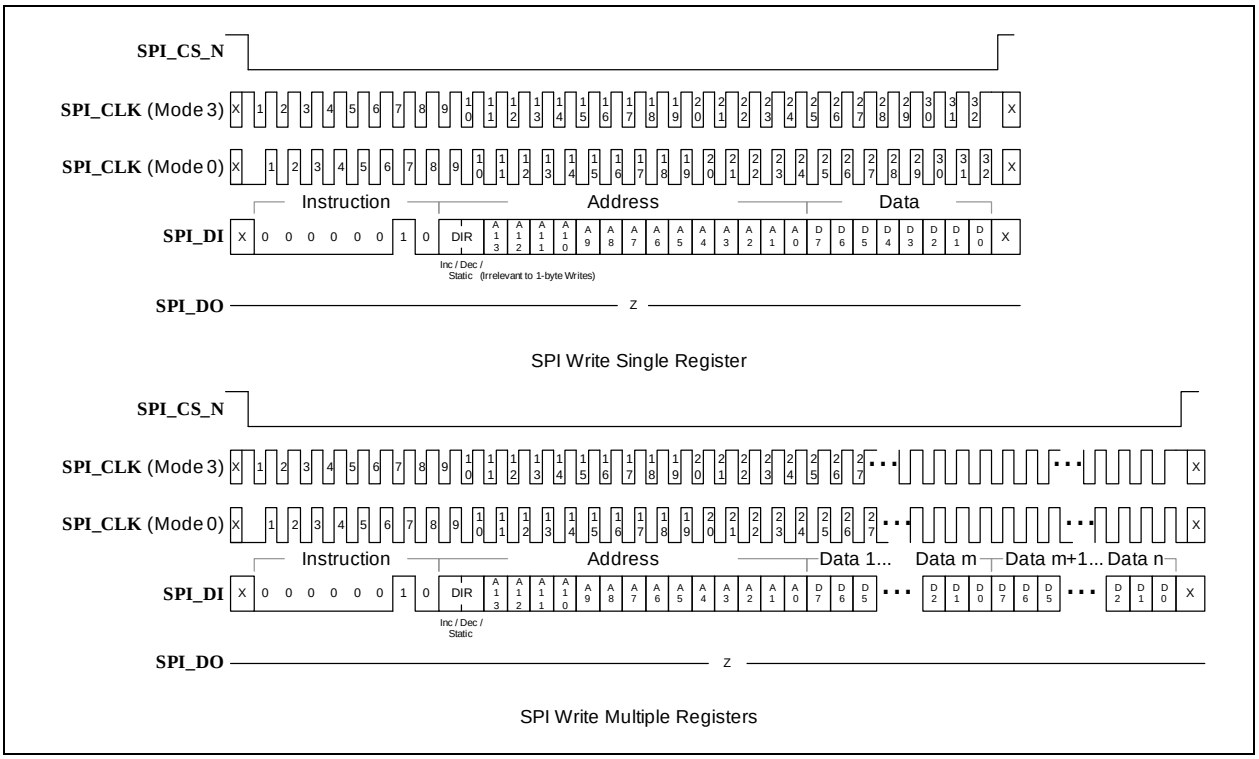
Multiple writes are performed by the Master by continuing the clock pulses and **SPI_DI** data while **SPI_CS_N** remains active. The upper two bits [15:14] of the address constitute the DIR subfield, and specify auto-incrementing (DIR=00b) or auto-decrementing (DIR=10b) or Static addressing. The internal Byte address is incremented, decremented, or kept fixed (Static) based on these bits. Maintaining a fixed internal address may be useful for FIFO access, register “bit-banging” or other repeated activity.

The data write to the register occurs after the full register contents are input: this depends on the defined size of the register. In the event that the full register is not written when **SPI_CS_N** is returned high, the write is considered invalid and the register is not affected.

The **SPI_CS_N** input is then brought inactive to conclude the cycle.

Figure 5-3 illustrates a typical SPI single and multiple register write.

FIGURE 5-3: SPI WRITE



5.2.5 SPECIAL CSR HANDLING

5.2.5.1 Live Bits

Register values are latched (registered) at the beginning of each register read to prevent the host from reading a changing value. The latching occurs individually per register in a multiple register read sequence.

5.2.5.2 Change-on-Read Registers and FIFOs

Any single-byte register that triggers a side-effect from a read operation (for example, containing “clear on read” bits, or advancing a FIFO structure) triggers only after the host has begun accessing the value. The value seen by the master will always be the original value and never the updated result of the side-effect.

For a multiple-byte register that is considered a single unit, the change may be delayed until all bytes of the register have been read. In the event that the host sends a no-acknowledge on one of the first bytes of a multi-byte register, or a start or stop condition occurs unexpectedly before the acknowledge of the full register, the read may be considered invalid and the side-effect not triggered.

Registers read in multiple-register read access will trigger multiple side-effects, occurring as they are read.

5.2.5.3 Live Bits that are also Change-on-Read

As described above, the current value from a register with live bits (as is the case of any register) is captured and latched as output data, and Change on Read bits are then changed in the original register. To prevent loss of a hardware event that occurs following the data capture but before the Change on Read, these hardware events are held pending until after the read action and after any change due to the read. This sequence also ensures an edge in the bit due to the hardware event.

6.0 CLOCKS, RESETS, AND POWER MANAGEMENT

This section details the various clocks, resets, and power managements states of the device:

6.1 Clocks

The following internal clocks are generated by the device:

- **48 MHz Relaxation Oscillator**
- **20 KHz Keep Alive Oscillator**
- **Ring Oscillator**

These oscillators can be manually enabled/disabled via software.

6.2 Power States

The device supports the following power states, as defined in their respective sub-sections:

- SLEEP
- HIBERNATE
- STANDBY
- ATTACHED IDLE (FRS Enabled)
- ATTACHED IDLE (FRS Disabled)
- ACTIVE

6.2.1 SLEEP

This is the lowest power state of the device. The SLEEP state is entered via assertion of the **PWR_DN** pin. Virtually all of the device is powered off in this mode with minimal circuity in the 3.3V domain to detect deassertion of **PWR_DN**.

This mode is intended to minimize power consumption when the device is not being used in battery powered applications. In these applications, a wake up event such as a button press, can cause the host CPU to deassert **PWR_DN**.

6.2.2 HIBERNATE

In this state, the port is disabled by the USB PD firmware and the **PWR_DN** pin is low. Attach detection is disabled due to CC terminations in the high-impedance state.

6.2.3 STANDBY

STANDBY is the lowest power functional state of the device. The majority of the device is powered off in this state. The internal CC comparator and 20 KHz oscillator are enabled in this state as well as requisite analog components (1.8V LDO, PORs, Biases, etc).

The CC lines are constantly monitored for an attach condition which shall result in an interrupt assertion to the host. If an attachment has been made, this state can detect a change in the partner's advertisement as well as a detach.

STANDBY is the power state that the UPD350 device will be in when in USB Type-C™ Unattached.SRC/SNK.

6.2.4 ATTACHED IDLE (FRS ENABLED)

In this state, a USB Type-C™ device is connected and the USB PD bus is idle (no USB packets in transit). The CC signals are constantly being monitored for packet transmission and Fast Role Swap (FRS) signal detection is enabled.

6.2.5 ATTACHED IDLE (FRS DISABLED)

In this state, a USB Type-C™ device is connected and the USB PD bus is idle (no USB packets in transit). The CC signals are constantly being monitored for packet transmission and Fast Role Swap (FRS) signal detection is disabled.

6.2.6 ACTIVE

This state defines the condition of the device after an attachment occurred. In this state, Power Delivery communication is supported. This state is also used for any condition in which the 48 MHz Relaxation Oscillator must be enabled, such as when it is desired to debounce a GPIO within the micro-second range.

When transmitting a Power Delivery packet, an additional 5 mA may be consumed. Additional power consumption results from enabling the OCS comparator, VBUS comparator and other modules. When VCONN FETs are enabled, there is an additional 70 mW of power consumption.

6.3 Asynchronous I2C Wakeup *(UPD350-A/UPD350-C Only)*

The device supports asynchronous wakes on the I2C slave interface. Via clock stretching, the I2C transaction that caused the wakeup will not be lost and does not have to be repeated by the host. The device will not clock stretch for more than 3 us.

The following steps illustrate the I2C wake function. Initially the Ring Oscillator and 48 MHz Oscillator are disabled.

1. The Host initiates an I2C transaction to the device.
2. The device asynchronously detects reception of the Start Bit and enables clock stretching by pulling-down **I2C_CLK** after the host drives SCL low. The Ring Oscillator is asynchronously enabled and used as a clock source for the power management logic.
3. After a delay of approximately 5 us the oscillator stabilizes and clocks the I2C controller.
4. Clock stretching is disabled and the I2C controller is enabled and begins processing the pending transaction.
5. The I2C transaction completes.
6. The Host checks the device status to see if there are any pending transactions. The I2C transaction may have initiated a PD transmission or conversely a coincident PD transaction may be in the process of being received.
7. After host confirms the device has no pending transactions, it power downs the device by disabling the Ring Oscillator and 48 MHz Relaxation Oscillator.
8. The device is ready to accept future asynchronous I2C wake event.

6.4 Asynchronous SPI Wakeup *(UPD350-B/UPD350-D Only)*

UPD350 supports asynchronous wakes on the SPI interface. The SPI protocol for this device is defined such that there is no requirement that the SPI transaction must be repeated.

The following steps illustrate the SPI wake function. Initially the Ring Oscillator and 48 MHz Oscillator are disabled.

1. The device is powered down.
2. The Host initiates an SPI transaction to the SPI Test Register (SPI_TEST) (UPD350-B/UPD350-D Only) which, when the device is operational, returns a non-zero value. The device drives **SPI_DO** to 0b while in power-down.
3. The device detects reception of an SPI message. The Ring Oscillator is asynchronously enabled and used as a clock source for the power management logic.
4. After a delay of approximately 5 us the oscillator stabilizes and clocks the SPI controller.
5. The device processes the next received SPI transaction.
6. The SPI transaction(s) complete(s).
7. The Host checks the device status to see if there are any pending transactions. The SPI transaction may have initiated a PD transmission or conversely a coincident PD transaction may be in the process of being received.
8. After the Host confirms the device has no pending transactions, it powers down the device by disabling the Ring Oscillator, and 48 MHz Relaxation Oscillator.
9. The device drives **SPI_DO** to 0b and awaits an asynchronous SPI wake.

6.5 Power Delivery MAC Wakeup

The PD MAC is capable of asynchronous wakeup upon reception of a PD packet. This enables the device to be placed in STANDBY mode and minimize power consumption.

The following steps illustrate the RX PD MAC wake function. Initially the Ring Oscillator and the 48 MHz Relaxation Oscillator are disabled. The 20 KHz Keep Alive Oscillator is enabled, but not used in the wake process.

1. In order to receive a PD message, the RX AFE is enabled via software and the trip point is set.
2. The PD MAC is configured and enabled via software.
3. The device is powered down. Software disables the 48 MHz Relaxation Oscillator, and Ring Oscillator if enabled.
4. After some time elapses, the device receives a PD message from the attached partner.
5. The PD MAC asynchronously detects preamble activity on the CC line and enables the 48 MHz Relaxation Oscillator.
6. The oscillator is operational in approximately 5 us, at which point the PD MAC is operational.
7. The PD MAC receives the remainder of the preamble and stores the message into the RX FIFO, and in accordance with the PD protocol, responds with GoodCRC as required.
8. An interrupt is issued via assertion of the **IRQ_N** pin.
9. Software services the interrupt via I^2C, reads the PD message, and responds as required.
10. The device is then powered down. Software disables the 48 MHz Relaxation Oscillator and Ring Oscillator.
11. The device remains powered down until the next PD message is received.

6.6 Interrupt Assertion from STANDBY

When the device is in STANDBY it is able to detect a number of events that may be configured to assert the **IRQ_N** pin upon being appropriately programmed via software. The logic detecting such events operates off of the 20 KHz Keep Alive Oscillator.

Upon the occurrence of an event, which is programmed to assert **IRQ_N**, the 48 MHz Relaxation Oscillator and Ring Oscillator are enabled. Upon synchronization, the **IRQ_N** pin shall assert.

After software services the source interrupt(s), it should disable the 48 MHz Relaxation Oscillator and Ring Oscillator to place the part back in STANDBY.

The following example sequence illustrates the steps for configuring the device to detect an OCS event on the **OCS_COMP1** pin while in STANDBY.

1. Software enables the OCS Compare Interrupt.
2. Software enables OCS detection, as defined in Section 7.2, "External Over-current Detection", to sample the **OCS_COMP1** pin.
3. Software disables the 48 MHz Relaxation Oscillator and 1 MHz Ring Oscillator.
4. An OCS event occurs and is detected on **OCS_COMP1**.
5. The Ring Oscillator is enabled and is used to as the device's operational clock.
6. The device enables the 48 MHz oscillator and waits about 5 us for the oscillator to stabilize.
7. The 48 MHz oscillator is stable.
8. After synchronization is complete, the **IRQ_N** pin is asserted.
9. Software detects **IRQ_N** assertion and services the interrupt.
10. Software disables the 48 MHz Relaxation Oscillator and Ring Oscillator.

6.7 Reset Operation

The following chip-level resets are supported by the device:

- Power-On-Reset (POR)
- Pin Reset (**RESET_N**)
- Software Reset (SRESET bit in Hardware Control Register (HW_CTL))
- Watchdog Timer (WDT_STS)

Chip-level resets trigger the sampling of the **CFG_SEL** configuration strap (see Section 8.9.1, "Configuration Selection," on page 43 for additional information). Chip-level reset completion can be determined by assertion of the RDY_INT bit in the Interrupt Enable Register (INT_EN) and assertion of the **IRQ_N** pin.

The following is s summary of steps that occur after a chip-level reset.

1. System level reset event (POR, **RESET_N**, SRESET, WDT_STS) occurs.
2. The device enables the 20 KHz Keep Alive Oscillator, 48 MHz Relaxation Oscillator, and 1MHz Ring Oscillator.
3. The device samples the **CFG_SEL** pin.
4. The device configures itself in accordance with the **CFG_SEL** pin and settings.
5. The device is enabled, the RDY_INT bit in the Interrupt Enable Register (INT_EN) asserts, the **IRQ_N** pin asserts.
6. The device disables the 48 MHz Relaxation Oscillator and the Ring Oscillator.

7.0 SYSTEM CONTROL

This section details the following system controls:

- General Purpose I/O
- External Over-current Detection
- System Control Registers

7.1 General Purpose I/O

A key function of the UPD350 is to manage external devices via up to ten PIOs. Usually this is accomplished via host software programming of the PIOs.

In some cases the UPD350 must automatically override the PIO state in response to an error condition. Features have been incorporated into the design to enable such operation. This is required in cases where the latency introduced by reliance on software to affect PIO state is either or too long or not deterministic.

Note:	**GPIO0** and **GPIO1** are not available in the UPD350-B / UPD350-D.

Note:	In Standalone UFP mode *(UPD350-A/UPD350-C only)*, certain GPIOs have alternate dedicated functions, as defined in Section 3.1.1.1, "UPD350-A / UPD350-C GPIO Functions in Standalone UFP Modes," on page 10.

7.2 External Over-current Detection

The device incorporates an analog comparator DAC circuit to detect an over-current condition. This feature is supported via the **OCS_COMP1** and/or **OCS_COMP2** pin.

7.3 General Purpose Timer

The device incorporates a low power general purpose timer that operates off a 20 kHz oscillator and implements a 16-bit one-shot down counter. When the timer underflows, it asserts the and interrupt and stops counting.

7.4 System Control Registers

This section details the system control registers.

TABLE 7-1: SYSTEM CONTROL REGISTER MAP

Address	Register Name (Symbol)
0000h	Device ID Register (ID_REV)
0004h	USB Vendor ID Register (VID)
0006h	USB Product ID Register (PID)
0008h	USB PD Revision Register (PD_REV)
000Ah	USB Type-C™ Revision Register (C_REV)
000Bh - 000Dh	Reserved for future expansion
000Eh	SPI Test Register (SPI_TEST) (UPD350-B/UPD350-D Only)
001Ah	I2C Slave Address Register (I2C_ADDR) (UPD350-A/UPD350-C Only)

Note:	**RESERVED address space must not be written under any circumstances. Failure to heed this warning may result in untoward operation and unexpected results.**

7.4.1 DEVICE ID REGISTER (ID_REV)

Address: 0000h Size: 32 bits

Bits	Description	Type	Default
31:16	**Device ID (ID)**	RO	Note 7-1
15:0	**Device Revision (REV)**	RO	Note 7-2

Note 7-1 The default value of this field is dependent on the version of the device.
UPD350-A: 0350h
UPD350-B: 0351h
UPD350-C: 0352h
UPD350-D: 0353h

Note 7-2 The default value of this field is dependent on the silicon revision of the device.

ID_REV[7:0] = 00h

ID_REV[15:8] = 01h

ID_REV[23:16] = 02h

ID_REV[31:24] = 03h

7.4.2 USB VENDOR ID REGISTER (VID)

Address: 0004h Size: 16 bits

Bits	Description	Type	Default
15:0	**USB Vendor Identification (VID)**	R/W	0424h

VID[7:0] = 04h

VID[15:8] = 05h

7.4.3 USB PRODUCT ID REGISTER (PID)

Address: 0006h Size: 16 bits

Bits	Description	Type	Default
15:0	**USB Product Identification (PID)**	R/W	0350h

PID[7:0] = 06h

PID[15:8] = 07h

7.4.4 USB PD REVISION REGISTER (PD_REV)

Address: 0008h Size: 16 bits

Bits	Description	Type	Default
15:0	**USB Power Delivery Specification Revision (PD_REV)**	R/W	Note 7-3

Note 7-3 The default value of this field is loaded from the respective OTP field. If OTP is not valid, the default value is 3010h.

PD_REV[7:0] = 08h

PD_REV[15:8] = 09h

7.4.5 USB TYPE-C™ REVISION REGISTER (C_REV)

Address: 000Ah Size: 16 bits

Bits	Description	Type	Default
15:0	**USB Type-C™ Specification Revision (C_REV)**	R/W	Note 7-4

Note 7-4 The default value of this field is loaded from the respective OTP field. If OTP is not valid, the default value is 12h.

C_REV[7:0] = 0Ah

C_REV[15:8] = 0Bh

7.4.6 SPI TEST REGISTER (SPI_TEST) *(UPD350-B/UPD350-D ONLY)*

Address: 000Eh Size: 8 bits

.

Bits	Description	Type	Default
7:0	**SPI Test (SPI_TEST)** This register is used by the host to determine when the chip has come out of powerdown when waking it via the SPI interface.	RO	02h

7.4.7 I²C SLAVE ADDRESS REGISTER (I2C_ADDR) *(UPD350-A/UPD350-C ONLY)*

Address: 001Ah Size: 8 bits

Bits	Description	Type	Default
7	**RESERVED**	RO	-
6:0	**I²C Slave Address** Defines the slave address used by the I²C controller.	R/W	Note 7-5

Note 7-5 The default value for this register is defined by the **CFG_SEL** pin unless the OTP I2C_ADR_OVR_EN bit is set. In this case, the OTP value specified by I2C_ADDR_OVR[6:0] is loaded into the register.

8.0 CABLE PLUG ORIENTATION AND DETECTION

This section details the functions that control and monitor the CC pins, monitor the **VBUS_DET** pin, control the VCONN FETs, and sample the **CFG_SEL** pin.

8.1 CC Comparator

The device integrates a comparator and DAC circuit to implement Type-C attach and detach functions. It supports up to eight programmable thresholds for attach detection between UFP and DFP. When operating as a UFP, the device supports detecting changes in the DFP's advertised thresholds to determine current sourcing capability. The default nominal values for the thresholds detected by the CC comparators are:

- 0.20 V
- 0.40 V
- 0.66 V
- 0.80 V
- 1.23 V
- 1.60 V
- 2.60 V
- 3.0 V Proprietary Mode

TABLE 8-1: CABLE DETECT SUMMARY

Parameter	Threshold CSR	Description	Min	Typ	Max
DFP_ACT_DEF	CC_THR0	Detecting an active cable when configured as DFP and advertising default USB current.		0.20 V	
UFP_DFP_DEF	CC_THR0	Detecting DFP attach when configured as UFP and DFP is advertising default USB current.		0.20 V	
DFP_ACT_1A5	CC_THR1	Detecting an active cable when configured as DFP and advertising 1.5A.		0.40 V	
UFP_DFP_1A5	CC_THR2	Detecting DFP attach when configured as UFP and DFP is advertising 1.5A.		0.66 V	
DFP_ACT_3A0	CC_THR3	Detecting an active cable when configured as DFP and advertising 3.0A.		0.80 V	
UFP_DFP_3A0	CC_THR4	Detecting DFP attach when configured as UFP and DFP is advertising 3.0A.		1.23 V	
DFP_UFP_DEF	CC_THR5	Detecting UFP attach when configured as DFP advertising default USB current.		1.60 V	
DFP_UFP_1A5	CC_THR5	Detecting UFP attach when configured as DFP advertising 1.5A.		1.60 V	
DFP_UFP_3A0	CC_THR6	Detecting UFP attach when configured as DFP advertising 3.0A.		2.60 V	

The following tables summarize the expected thresholds to be matched in the CCx Match Registers (CCx_MATCH) for various configurations.

TABLE 8-2: DFP CC MATCH SUMMARY

CC State	CC THR0	CC THR1	CC THR2	CC THR3	CC THR4	CC THR5	CC THR6	CC THR7
Advertise Default USB Current and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 1.5 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise 3.0 A and connected to powered cable	0	0	0	0	0	0	0	0
Advertise Default USB Current and connected to UFP	1	0	0	0	0	0	0	0
Advertise 1.5 A and connected to UFP	0	1	0	0	0	0	0	0
Advertise 3.0 A and connected to UFP	0	0	0	1	0	0	0	0
Advertise Default USB Current and no connect (vOpen)	1	0	0	0	0	1	0	0
Advertise 1.5 A and no connect (vOpen)	0	1	0	0	0	1	0	0
Advertise 3.0 A and no connect (vOpen)	0	0	0	1	0	0	1	0
Proprietary Mode and no connect (vOpen)	0	0	0	0	0	0	0	1

TABLE 8-3: UFP CC MATCH SUMMARY

CC State	CC THR0	CC_ THR1	CC THR2	CC THR3	CC THR4	CC THR5	CC THR6	CC THR7
Powered cable detected.	0	0	0	0	0	0	0	0
No Connect (SNK.Open)	0	0	0	0	0	0	0	0
DFP Connected and advertising default USB current	1	0	0	0	0	0	0	0
DFP Connected and advertising 1.5 A	1	0	1	0	0	0	0	0
DFP Connected and advertising 3.0 A	1	0	1	0	1	0	0	0
DFP Connected and advertising proprietary current	1	0	1	0	1	0	0	1

8.2 DFP Operation

The device implements current sources to advertise current charging capabilities on both CC pins when operating as a DFP.

When a UFP connection is established, the current driven across the CC pins creates a voltage across the UFP's Rd pull-down that can be detected by the integrated CC comparator. The voltages monitored are summarized in Table 8-4. When connected to an active cable, an alternative pull-down (Ra) appears on the CC pin.

The DFP also integrates two 5V FETs for implementing the VCONN function. This is further discussed in Section 8.8, "VCONN Operation".

TABLE 8-4: SOURCE DETECTION

CC1	CC2	Connection State	CC Comparator State	VBUS	VCONN
Open	Open	Nothing Attached	Monitor both CC pins for attach	Off	Off
Rd	Open	UFP Attached	Monitor **CC1** for detach	On	Off
Open	Rd	UFP Attached	Monitor **CC2** for detach	On	Off
Ra	Open	Powered Cable, No UFP attached	Monitor **CC2** for UFP attach. Monitor **CC1** for cable detach.	Off	Off
Open	Ra	Powered Cable, No UFP attached	Monitor **CC1** for UFP attach. Monitor **CC2** for cable detach.	Off	Off
Ra	Rd	Powered Cable, UFP attached	Monitor **CC2** for UFP detach. **CC1** is not monitored for detach.	On	On
Rd	Ra	Powered Cable, UFP attached	Monitor **CC1** for UFP detach. **CC2** is not monitored for detach.	On	On
Rd	Rd	Debug accessory mode attached	Monitor both CC pins for detach	Off	Off
Ra	Ra	Audio accessory mode attached.	Monitor both CC pins for detach	Off	Off

8.2.1 RP CURRENT SOURCES

In order to advertise the current charging capabilities of the device via the integrated port power controller or external power circuit, Rp current sources are used. The current source can be selected by software. Table 8-5 summarizes the values supported by the current sources in regards to the programmed value.

TABLE 8-5: RP CURRENT SOURCES

DFP Advertisement	Current source (1.7V to 5.5V)	RPx Value
Disabled		00b
Default USB Power	80 uA +/-20%	01b
1.5A @ 5V	180 uA +/-8%	10b
3.0A @ 5V	330 uA +/-8%	11b

The current source coupled with the CC pins for RP advertisement is also used for sampling the **CFG_SEL** pin. When the **CFG_SEL** pin is sampled, current is steered away from the CC pins and no RP value is advertised.

8.3 UFP Operation

When operating as a UFP, the device applies an Rd pull-down on both CC lines and waits for a DFP connection from the assertion of VBUS. The CC comparator is used to determine the advertised current charger capabilities supported by the DFP.

8.4 DRP Operation (Legacy)

In this configuration, software utilizes the device to alternate between a Source and Sink advertisement with an interval of tDRP per the USB Type-C™ Specification.

8.5 DRP Offload

DRP offload enables the device to manage the DRP toggle. This is beneficial as it allows the host CPU to remain in a low power state until a connection is detected.

DRP offload toggles between Source and Sink advertisement by alternating between enabling Rp current sources and Rd pull-downs for a period of tDRP (DRP Time Register). The duty cycle between Source and Sink advertisement is determined by the DRP Duty Cycle Register. The DRP Time Register may be written by firmware or generated automatically via a pseudo random number generator. The latter approach should be used to reduce the probability of collisions when connecting. It is selectable whether the DRP cycle shall first advertise UFP or DFP.

A connection is detected after a successful debounce for a period defined by the Match Debounce Register. VBUS is checked to be below vSafe0v for the DFP case. This results in **IRQ_N** assertion and automatic disablement of the DRP toggle. Firmware must further debounce for the period tPDDebounce before determining if a valid match is present. If a match has not occurred, firmware shall enable DRP again.

A pseudo random number generator, implemented via a LFSR, is utilized to generate the DRP period. The LFSR operates off of the 20 KHz clock and updates every 100 us when enabled.

Hardware limits the total DRP period to be between 50 ms and 100 ms in order to comply with the USB Type-C™ specification.

8.6 Collision Avoidance

An alternative mode of operation is required to enable the CC detection circuit to facilitate software implementation of collision detection which was incorporated into version 3.0 of the USB PD Specification.

In order to avoid message collisions due to asynchronous Messaging (AMS) sent from the Sink, the Source sets Rp to SinkTxOk (3A@5V) to indicate to the Sink that it is OK to initiate an AMS. When the Source wishes to initiate an AMS it sets Rp to SinkTxNG (1.5A@5V). When the Sink detects that Rp is set to SinkTxOk it may initiate an AMS. When the Sink detects that Rp is set to SinkTxNG it shall not initiate an AMS and shall only send Messages that are part of an AMS the Source has initiated.

When operating as a Sink, a mechanism is required for quickly determining whether the Source is advertising SinkTxNG or SinkTxOK on Rp.

A collision avoidance mechanism exists to enable software to instruct the device to sample only a single threshold on a single CC pin. This results in a cycle through both thresholds taking only 100 us, making it easier for software to meet the timing constraints mandated by SinkTxOk in the specification.

8.7 Fast Role Swap (FRS)

This feature is used to detect when a partner source has lost power. Upon detection of FRS signaling, the “Old Sink” transitions to be a Source and begins supplying VBUS.

When operating as a Sink, the FRS mode of operation enables detection of FRS signaling. Detection results in **IRQ_N** assertion and this event may also be mapped as a PIO override source. When operating as a Source, upon detection of loss of power, the device will transmit FRS signaling. This is initiated by either assertion of a selected PIO or a CSR write.

The following FRS related features are supported:

- Ability to detect reception of FRS signaling
- High bandwidth and current boost mode for CC comparator to increase sampling frequency
- Interrupt, and PIO, assertion upon FRS detection
- PIO override support for FRS detection as a source

- Ability to initiate FRS signaling via GPIO assertion or register write.
- Control 5 Ohm (Rsw) pull-down resistor

8.7.1 FRS SINK OPERATION

When operating as a Sink, the device is configured to detect FRS signaling by setting FRS Detect Enable (FRS_DET_EN) in FRS Control Register. The CC detection logic is programmed to detect three thresholds (SinkTxOK, SinkTXNG, FRSWAP) and samples each threshold in round robin fashion. The sampling rate is determined by CC Sample Clock Register.

When a match is detected on FRSWAP threshold, the CC detection logic will “park” at this threshold and continue monitoring the output of the comparator. While “parked” the output of the CC comparator will be sampled at an increased rate of 12 MHz. This higher sampling rate will prevent PD messages from inadvertently looking like FRS signaling which will happen on occasion when the sampling rate is similar or slower than the ~270 kbps rate of PD messages.

It will continue debouncing for the amount of time specified in FRS CC Debounce Register. The FRSWAP threshold is indicated by FRS Threshold Select Register.

If the debounce is successful, then the FRS_RCV_STS interrupt is asserted and the CC detection logic resumes sampling all enabled thresholds. If the FRS debounce fails, the CC detection logic resumes sampling all enabled thresholds.

In this mode of operation the CC Comparator operates at a faster rate in order to minimize the FRS detection latency. This is enabled by placing this the comparator into a high bandwidth mode.

After detecting the FRS signaling, the “old Sink” must start supplying vSafe5V at USB Type-C™ current VBUS no later than tSrcFRSwap (150 us) after VBUS has dropped below vSafe5V. This must be accomplished via circuitry external to the device.

Note:	The upper threshold used for vSafe5V should be used for determining when VBUS has dropped below vSafe5v to help meet tSrcFRSwap requirement.

Note:	Matching of a VBUS threshold may be selected as a source to a PIO override. Additionally, VBUS threshold match ANDed with FRS signal detect may also be used as a PIO override source.

8.7.2 FRS SOURCE OPERATION

The initial Source shall signal a FRS request by driving the CC pin to ground with a resistance of less than 5 Ohms for a period defined by FRS Transmission Length Register. The FRS request signaling is initiated by either a CSR write or GPIO assertion.

The former case is implemented by setting the FRS Request (FRS_REQ_EN) bit in FRS Control Register. This bit self clears after the FRS request is transmitted. For the latter case, the PIO is selected by the FRS Request PIO (FRS_REQ_PIO) field in FRS Control Register.

Transmission of FRS signaling will take precedence over PD MAC TX communication. The FRS PD resistor is enabled in tandem on the CC pin determined by FRS CC Select (FRS_CC_SEL) in FRS Control Register. This configuration remains until FRS transmission has completed.

8.7.3 DEAD BATTERY *(UPD350-A/UPD350-B Only)*

Two variations of the Rd resistor are implemented: Rd (Dead Battery) and Rd (Trimmed). The CC pins are configured to present either Hi-Z or an untrimmed Rd pull-down resistance when connected to a DFP advertising a pull-up resistance.

Figure 8-1 illustrates the configuration for supporting dead battery cases. The UFP pull-up activates the FET in series with RD_DB and enables the untrimmed dead battery pull-down.

FIGURE 8-1: CC RD (DEAD BATTERY)

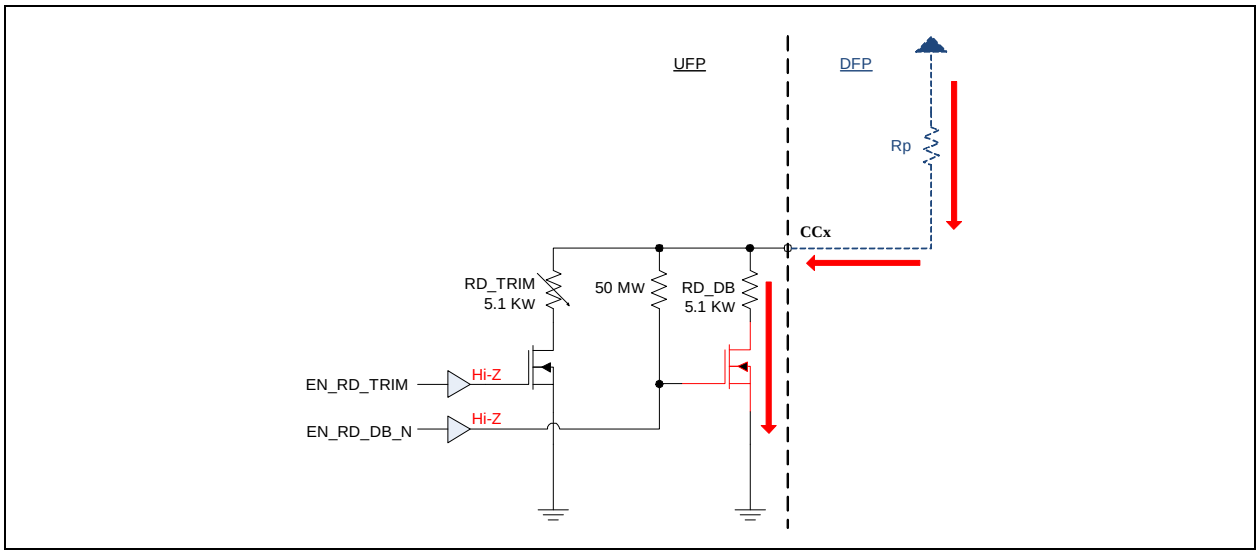
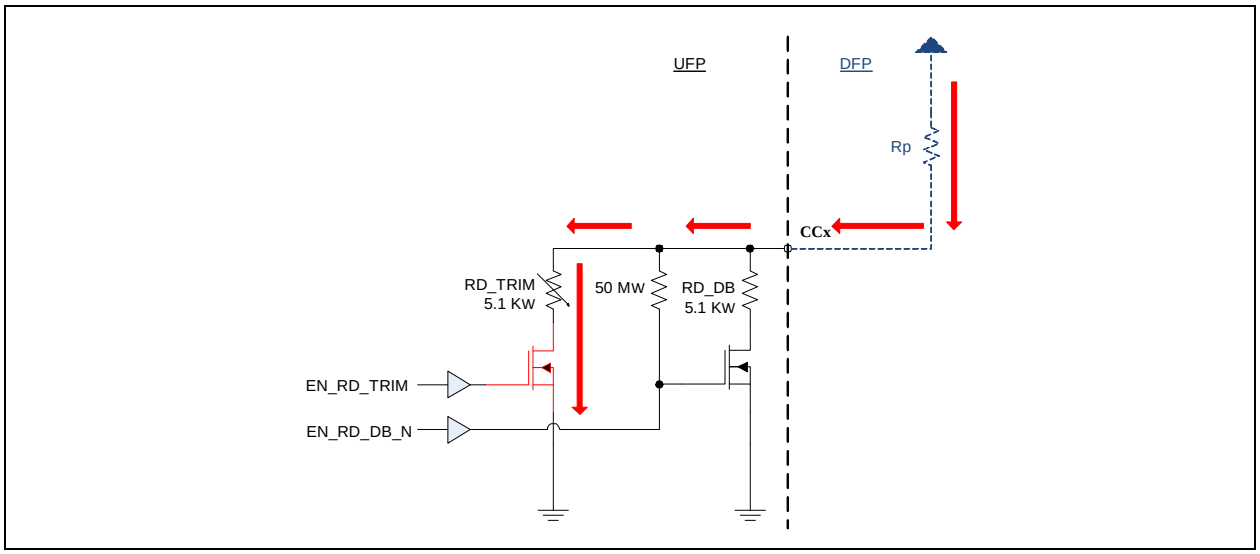


Figure 8-2 illustrates operation after the UFP has been powered over VBUS by the DFP. After the device is powered, EN_RD_DB asserts by default to keep the RD_DB pull-down activated.

Upon powering the host CPU, software simultaneously deasserts EN_RD_DB and asserts EN_RD_TRIM. Going forward the device presents RD_TRIM.

FIGURE 8-2: CC RD (TRIM)



The Rd resistor presented, trimmed or untrimmed, is controlled by the CC1 and CC2 Pull-Down Values in the CC Control Register (CC_CTL). These register fields serve the basis for the EN_RD_TRIM and EN_RD_DB_N control signals depicted.

8.8 VCONN Operation

VCONN is a 5V supply that is used to power circuitry in the USB Type-C™ plug, which is required to implement Electronically Marked Cables. By default, the DFP always sources VCONN when connected to an active cable. However, this may be changed by software by using PD VCONN_SWAP.

The VCONN FETs are enabled/disabled by software via the VCONN1 Control and VCONN2 Control control bits in the CC Control Register (CC_CTL).

APPLICATION NOTE: It is not envisioned to ever enable both FETs simultaneously.

VCONN is monitored for an over current condition via an internal monitoring circuit. A VCONN over current condition is recognized when the event persists for a time longer than specified. When an over-current VCONN event is detected, an interrupt asserts. The device may be configured to automatically disable the VCONN FET upon detection of a CC1/CC2 Back-Drive Error or VCONN Discharge Error. In the event of the detection of a debounced over-current VCONN event, the enabled VCONN FET will be disabled.

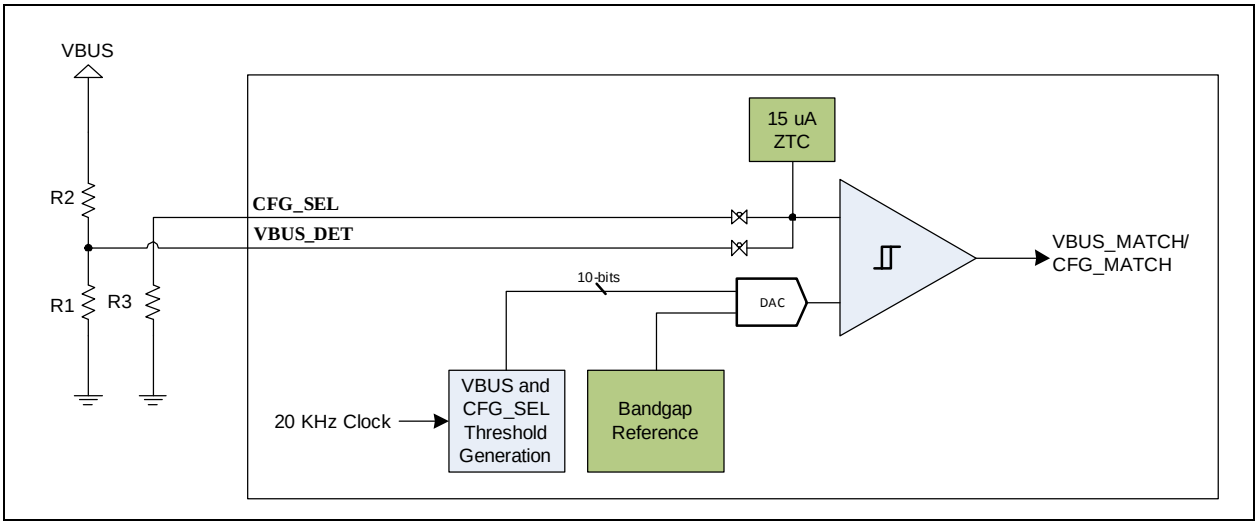
8.9 VBUS Detection

The device implements a comparator for determining when **VBUS** is within a programmed range, vSafe5V, or vSafe0v. VBUS is divided down externally via a 1:9 resistor divider to generate **VBUS_DET**. **VBUS_DET** is compared with an 8-bit threshold generated by an integrated DAC. The comparator is also shared by the **CFG_SEL** pin which is sampled automatically after a system reset

Figure 8-3 illustrates the **VBUS_DET** circuit. In a typical use case, **VBUS_DET** thresholds are programmed to track the following voltage ranges as defined in Table 8-6.

Note:	Table 8-6 illustrates the values of **VBUS_DET** utilizing +/-1% accurate resistors where R1 is 10K Ohms and R2 is 90 kOhms.

FIGURE 8-3: VBUS_DET COMPARATOR



For a DFP, the VBUS comparator is useful to detect when VBUS is within the desired range per PD negotiations. This is the case when VBUS is generated by a source external to the device.

For a UFP, the VBUS comparator is required to determine when a DFP is attached or detached. It may also use the comparator to determine when VBUS is within a new voltage range negotiated via PD.

TABLE 8-6: VBUS DETECTION THRESHOLDS

VBUS	Range	VBUS_DET	Comments
20	21.5	2.11	
	18.5	1.82	
12	13.1	1.29	
	10.9	1.07	
8	8.9	0.88	
	7.1	0.69	
5	5.5	0.51	vSafe5V
	3.67	0.33	
0.68	0.68	0.068	vSafe0V

If supported, the ranges 8V, 12V and 20V may be programmed in VBUS Threshold 2 and VBUS Threshold 3 registers. Likewise 5V range, vSafe5v, can be programmed in VBUS Threshold 0 and VBUS Threshold 1 registers.

The threshold for vSafe0V is programmable.

VBUS_DET monitoring logic operates off of the 20 KHz oscillator which cycles through each threshold. Including vSafe0v, a total of five values are compared.

The VBUS Match Register (VBUS_MATCH) indicates when the value on **VBUS_DET** is higher than the corresponding programmed threshold and can therefore be used to determine is **VBUS** is in the desired range.

A change in the state of the VBUS match may trigger assertion of the **IRQ_N** pin if appropriately configured.

8.9.1 CONFIGURATION SELECTION

The **CFG_SEL** pin shares the comparator with **VBUS** as shown in Figure 8-3. The **CFG_SEL** pin is connected to a resistor divider, typically pulled up to VDDIO. After a system level reset (POR, **RESET_N**, Software Reset), the **CFG_SEL** pin is automatically sampled to configure the device. The internal CFG_SEL_MATCH register is updated automatically and the device configures itself accordingly if standalone mode is detected. The various resistor settings for the **CFG_SEL** pin are detailed in Table 8-7.

Note:	The **CFG_SEL** pin is used to determine the default I^2C slave address and operating mode in the UPD350-A / UPD350-C. For the UPD350-B / UPD350-D, this pin determines the mode in which the part operates (companion or standalone UFP) and can be used for customer specific purposes to provide a discrete value (0-15) based upon the attached resistor value.

Note:	For additional information on device resets, refer to Section 6.7, "Reset Operation," on page 30.

TABLE 8-7: CONFIGURATION SELECT (CFG_SEL) I^2C ADDRESS SETTINGS *(UPD350-A/UPD350-C ONLY)*

Resistor (+/-1%)	Description	CFG_SEL1_MATCH Register
GND	**Companion Mode I^2C Slave Address = 1011_111**	0000h
0.475 K	**Companion Mode I^2C Slave Address = 1011_110**	0001h
0.953 K	**Companion Mode I^2C Slave Address = 1011_101**	0003h
1.43 K	**Companion Mode I^2C Slave Address = 1011_100**	0007h
1.87 K	**Companion Mode I^2C Slave Address = 1101_011**	000Fh
2.37 K	**Companion Mode I^2C Slave Address = 1101_010**	001Fh
2.87 K	**Companion Mode I^2C Slave Address = 1101_001**	003Fh
3.32 K	**Companion Mode I^2C Slave Address = 1101_000**	007Fh
3.83 K	**Standalone UFP Mode I^2C Slave Address = 1011_111**	00FFh
4.22 K	**Standalone UFP Mode I^2C Slave Address = 1011_110**	01FFh
4.75 K	**Standalone UFP Mode I^2C Slave Address = 1011_101**	03FFh
5.23 K	**Standalone UFP Mode I^2C Slave Address = 1011_100**	07FFh
5.62 K	**Standalone UFP Mode I^2C Slave Address = 1101_011**	0FFFh

8.10 Back-Drive Detection

Back-drive detection is implemented on both CC pins, which prevents backwards current flow. The back-drive protection circuit is always operational and triggers when VCCx > VS.

Detection of the back-drive condition causes the CC1 or CC2 Back-Drive Error interrupt to assert.

Hardware supports automatically disabling a VCONN FET on a CC pin in which back-drive was detected after a specified debounce period.

8.11 Standalone UFP *(UPD350-A/UPD350-C Only)*

8.11.1 OVERVIEW

The device supports standalone UFP operation in which no CPU is available to configure the device. A key application for this mode is a USB Type-C™ UFP companion for the Microchip USB58xx/USB59xx family of USB Hubs.

8.11.2 CONFIGURATION

This mode is entered by the appropriate setting of the **CFG_SEL** pin. The device auto-configures itself after a system level reset event.

9.0 BASEBAND CC INTERFACE (BCI)

The device integrates a Baseband CC Interface (BCI) to facilitate USB Power Delivery communication. This module bridges between the PD MAC/BMC and the analog front end. Baseband communication is initiated by the PD MAC, which interfaces to the BCI. The BCI implements the digital functions required to control TX baseband components.

9.1 Baseband TX Data-flow

The key responsibility of the BCI is to generate the wave form required for baseband communication. To this end, the BMC has a group of eight registers that define the Lo-Hi and Hi-Lo transitions for the generated BMC signal.

When instructed to transition from Lo-Hi, the BCI steps through all BB TX Rise Registers. Likewise when instructed to transition from Hi-Lo, the BCI steps through all BB TX Fall Registers.

APPLICATION NOTE: The user may replicate values if it is desired to use less than twelve unique values for this purpose.

9.2 Baseband RX Data-flow

Baseband RX data is received by the BCI from the RX analog front end where it is compared to a threshold programmed by software. The CC RX DAC Value defines the trip point used for reception of baseband data. The field shall be programmed to be 175 mV below the RX Eye center, as defined in the PD Specification for the mode in which the device is operating (Sourcing Power, Sinking Power, Power Neutral).

10.0 POWER DELIVERY MAC

The PD MAC implements certain features of the protocol layer and physical layer of the Universal Serial Bus Power Delivery Specification. On one end the PD MAC interfaces to the software implementing the bulk of protocol and higher level layers and on the other end it interfaces to a BMC encoder / decoder module.

In addition to the normal TX and RX functions, the PD MAC implements the test mode logic defined in the USB PD specification (BIST).

The PD MAC supports the following features:

- Automatic TX Mode for packet framing and CRC32 insertion.
- Raw TX Mode for bit level packet control.
- Automatic GoodCRC response to received messages.
- Automatic BIST Error Count Message in BIST RX Mode.
- GoodCRCTimer implementation.
- Automatic retries with programmable retry count.
- Redundant receive packets automatically dropped in auto response mode.
- 74 byte TX queue.
- 128 byte RX queue.
- Programmable TX Bit-time. Allows for changing operating frequency.
- Programmable preamble length.
- BIST TX and RX logic.
- Programmable TX and RX queue modes - buffer mode and FIFO mode.
- CRC32 generator for TX.
- CRC32 calculator and comparator for RX.

10.1 PD MAC Transmitter

The PD MAC transmitter is comprised of three major blocks:

- **TX Queue:**
  The TX Queue is where software loads the message to be transmitted.
- **TX Control:**
  The TX Control implements the necessary control logic. It is responsible for reading the data from the TX queue and based on the data processing mode (automatic or raw), processing the data to make it suitable (nibbles with control information) for use by the TX Comm. It is also responsible for generating packet framing and terminating the packet in automatic mode, and generating messages for automatic response (GoodCRC and BIST Error Count). TX Control also handles the selection of the SOP type that is to be transmitted.
- **TX Comm:**
  The TX Comm is comprised of a TX CRC generator, a 4b5b encoder, serializer, preamble generator, and TX bit timer. It takes the nibble data, computes and inserts the CRC, 5b encodes, and generates the baseband serial data. Preamble insertion is also performed by this logic.

10.2 PD MAC Receiver

The PD MAC receiver is comprised of three major blocks:

- **RX Queue:**
  The RX Queue is where software reads the received messages.
- **RX Control:**
  The RX Control implements the necessary control logic. It is responsible for validating the received packet, updating the RX Queue status, and triggering automatic responses, if required.
- **RX Comm:**
  The RX Comm is comprised of the Clock and Data Recovery (CDR), RX DES (de-serializer) (serial-to-parallel converter, 4b5b decoder, and framing detector), RX CRC32 (CRC calculator, receive timer), and other logic to detect valid packet reception.

10.3 PD MAC BIST

The PD MAC incorporates BIST functions as defined in the USB PD Specification. It is comprised of a TX and RX block.

The BIST TX block contains a PRBS (Pseudo Random Binary Sequence) generator, BIST pattern generation logic, and its own bit-timing logic. The SOP type used by TX BIST Test Frames is a 20-bit static vector which is created by multiplexing between the five SOP ordered sets based on a register setting. The resultant 20-bit vector is simply bit selected when the packet is transmitted.

The BIST RX block contains a PRBS generator and bit error detection logic. BIST RX is used only during the BIST Receiver Test.

11.0 POWER SWITCH

To enable the device to efficiently support dead battery use cases, an integrated power switch is provided to select between two external +3.3V supplies:

- **3V3_ALW**: +3.3V main power supply input to integrated power switch.
- **3V3_VBUS**: +3.3V power supply input derived from VBUS to the integrated power switch.

The power switch allows the core to be powered from **3V3_ALW** normally, and from **3V3_VBUS** when **3V3_ALW** is not present. This effectively allows connection detection and system wakeup without external processor intervention (external processor in sleep mode).

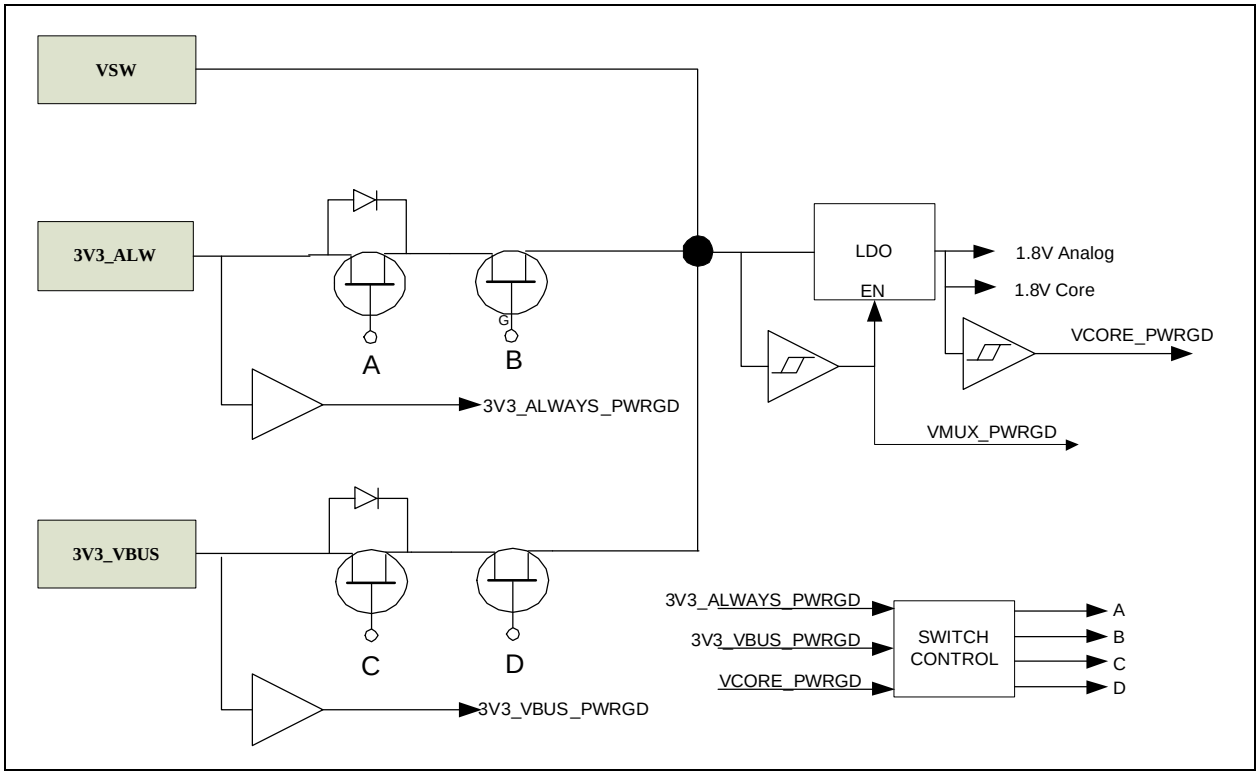
Attached to **3V3_ALW** and **3V3_VBUS** are two FET switches. The first FET switches have a diode across the output.

There are three voltage comparators. VBUS_PWRGD is on when **3V3_VBUS** exceeds 2.7V. 3V3_ALW_PWRGD is on when **3V3_ALW** exceeds 2.7V. VCORE_PWRGD is on when the core voltage reaches an operational level.

If VCORE_PWRGD is not asserted, the part is held in reset. If both VBUS_PWRGD and 3V3_ALW_PWRGD are not asserted, the part is held in reset, regardless of the state of the VCORE_PWRGD.

A block diagram of the internal power switch can be seen in Figure 11-1.

FIGURE 11-1: POWER SWITCH BLOCK DIAGRAM



11.1 Software Override

In the event that both **3V3_VBUS** and **3V3_ALW** are available, the Power Switch automatically selects **3V3_ALW** for operation. This can be overridden by software, which forces the switch to operate off of VBUS. When set, the auto-switch mechanism of the switch is disabled.

12.0 HDMI/DISPLAYPORT HOT PLUG DETECT (HPD)

12.1 Overview

The device provides hardware offload support for detecting the state of a Display Port compliant **HPD** input/output pin to the device. This pin may also be used to implement HDMI alternate mode.

The USB Type-C™ DisplayPort Alternate Mode Specification defines the **HPD** state in terms of two status flags:

- **HPD_STATE**: Indicates whether the HPD's logical state is high or low (denoted as HPD_HIGH or HPD_LOW, respectively). For the purposes of communicating the HPD state over USB, the logical state of HPD is considered as remaining high while receiving an IRQ_HPD, and is low during the time that HPD is being de-bounced on a new mechanical connection. The logical state of HPD transitions from high to low when a low level on the HPD link has been detected for 2ms (i.e., longer than the maximum IRQ_HPD pulse detection time). The logical state of HPD is unchanged during glitches (as specified in DP v1.3) on the HPD link.
- **IRQ_HPD**: Indicates an IRQ_HPD (i.e., a high-to-low transition on HPD followed by a low-to-high transition was detected between 250us and 2ms later, as specified in DP v1.3).

Note:	The **HPD** pin is configured as an input in DisplayPort Source applications, and configured as a push/pull driver in DisplayPort Sink applications.

Note:	HDMI alternate mode requires a 5V level shifter to generate the HPD output. Since the **HPD** pin is 5V tolerant, it can safely be connected directly to HPD when operating as a receiver.

13.0 WATCHDOG TIMER (WDT)

13.1 General Description

The function of the Watchdog Timer (WDT) is to provide a mechanism to detect if the device has failed.

When enabled, the Watchdog Timer circuit will generate a WDT initiated system reset if the user program fails to reload the WDT within a specified length of time known as the WDT Interval.

The Watchdog timer operates off of the 20 KHz Keep Alive Oscillator or 48 MHz Relaxation Oscillator depending on the resolution selected.

A watchdog timer initiated system reset is indicated by assertion of the WDT_INT interrupt.

13.2 I2C/SPI Writes

When a watchdog interrupt is pending, all write operations are blocked until the interrupt is cleared.

14.0 OPERATIONAL CHARACTERISTICS

14.1 Absolute Maximum Ratings*

Supply Voltage (**VS**) (Note 14-1) . . . . . -0.3 V to +6.0 V

Supply Voltage (**VDD33IO**, **3V3_VBUS**, **3V3_ALW**, **VDD_12C**, **VDD18**) (Note 14-1) . . . . . 0 V to +4.0 V

Positive voltage on input signal pins, with respect to ground . . . . . +6.0 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Storage Temperature . . . . . -55°C to +150°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . +/-8 kV

Note 14-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 14.2, "Operating Conditions**", Section 14.5, "DC Characteristics", or any other applicable section of this specification is not implied.

14.2 Operating Conditions**

Supply Voltage (**VS**) . . . . . +4.75 V to +5.25 V

Supply Voltage (**VDD33IO**, **3V3_VBUS**, **3V3_ALW**) . . . . . +3.1 V to +3.47 V

Supply Voltage (**VDD_I2C**) . . . . . Note 14-2

Supply Voltage (**VDD18**) . . . . . +1.62 V to +1.98 V

Positive voltage on input signal pins, with respect to ground . . . . . +3.3 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.3 V

Power Supply Rise Time Max (T_{RT}) (Figure 14-1) *100ms*

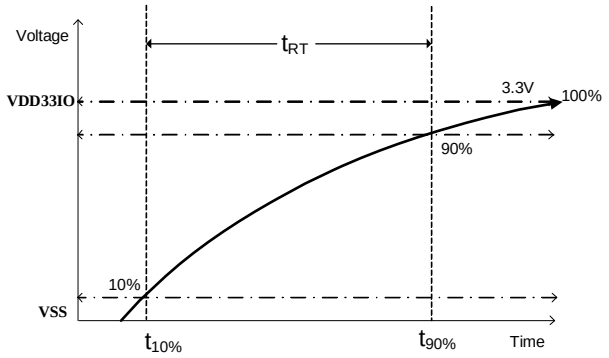
Commercial Ambient Operating Temperature in Still Air (T_A) . . . . . 0°C to +70°C

Industrial and Grade 3 Automotive Ambient Operating Temperature in Still Air (T_A) . . . . . -40°C to +85°C

Note 14-2 To operate the I^2C interface at 1.8 V, connect to 1.8 V (+/-10%), to operate the I^2C interface at 3.3 V, connect to 3.3 V (+/-10%)

**Proper operation of the device is guaranteed only within the ranges specified in this section.

FIGURE 14-1: SUPPLY RISE TIME MODEL



14.3 Package Thermal Specifications

TABLE 14-1: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	°C/W
Thermal Resistance Junction to Ambient	Θ_{JA}	49
Thermal Resistance Junction to Top of Case	Θ_{JC}	6
Thermal Resistance Junction to Board	Θ_{JB}	29
Thermal Resistance Junction to Bottom of Case	Ψ_{JT}	0.7

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

TABLE 14-2: POWER DISSIPATION

Parameter	Symbol	Max	Units
Power Dissipation	P_{dis}	55	mW

Note: This is the worst-case power dissipation as a consequence of maximum loading (before current-limiting protections take effect) upon the internal VBUS power switch, VCONN power switch, 3.3V power-ORing switch, analog blocks, and core digital logic.

14.4 Current Consumption

TABLE 14-3: DEVICE CURRENT CONSUMPTION

Power State	Supply Current		
	Typical	Max	Units
RESET	***110***	**-**	µA
SLEEP	***15***	**-**	µA
HIBERNATE	***80***	**-**	µA
STANDBY	***1.20***	**-**	mA
ATTACHED IDLE (FRS Enabled)	***1.40***	**-**	mA
ATTACHED IDLE (FRS Disabled)	***1.25***	**-**	mA
ACTIVE (with PD packet transmitting)	**-**	***15.0***	mA

Note 1: This table details the power consumption of the UPD350 device as measured during various modes of operation. Refer to Section 6.2, "Power States" for additional information. Power dissipation is determined by temperature, supply voltage, and external source/sin k requirements. Maximum values represent very short bursts of activity over a small amount of time. Typical values represent averaged current consumption over time.

2: **SLEEP** power state is achieved with **PWR_DN** pin asserted

3: **STANDBY** is equivalent to USB Type-C™ specification's Unattached.SRC/Unattached.SNK

4: Currents measured with all 3.3V rails tied together.

14.5 DC Characteristics

TABLE 14-4: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units	Notes
IS Type Input Buffer						
Low Input Level	V_{ILI}	-0.3		0.8	V	
High Input Level	V_{IHI}	2.0		3.6	V	
Negative-Going Threshold	V_{ILT}	1.21	1.33	1.8	V	Schmitt trigger
Positive-Going Threshold	V_{IHT}	1.31	1.58	1.8	V	Schmitt trigger
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	133	0	mV	
Input Leakage (V_{IN} = **VSS** or **VDDIO**)	I_{IH}	-10		10	µA	Note 14-3
Input Capacitance	C_{IN}			3	pF	
O8 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -8 mA
High Output Level	V_{OH}	**VDD33IO** - 0.4			V	I_{OH} = 8 mA

TABLE 14-4: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	Typ	Max	Units	Notes
OD8 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = -8 mA
I2C Type Buffer						Note 14-4

Note 14-3 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 µA per-pin (typical).

Note 14-4 The I2C type buffer conforms to the NXP *I^2C-Bus Specification* (UM10204, Rev. 6). Refer to the *I^2C-Bus Specification* for additional information.

TABLE 14-5: VCONN SOURCE DC PARAMETERS

Parameter	Symbol	Min	Typ	Max	Units	Notes
ILIM	I_{LIM_VCONN}		600		mA	**VS**=5V
On Resistance	R_{ON_VCONN}		270		mΩ	

TABLE 14-6: POWER SWITCH DC PARAMETERS

Parameter	Symbol	Min	Typ	Max	Units	Notes
VSW Load	VSW_Load			100	mA	**3V3_ALW/3V3_VBUS** = 3.3V
VSW Resistance	R_VSW		500		Ω	

14.6 AC Characteristics and Timing

This section details the various AC timing specifications of the device.

14.6.1 **RESET_N** TIMING

Figure 14-2 illustrates the **RESET_N** timing requirements. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified

FIGURE 14-2: RESET_N TIMING

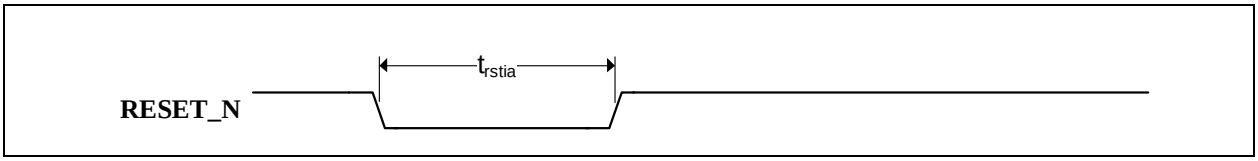


TABLE 14-7: RESET_N TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	1			µs

14.6.2 I²C SLAVE INTERFACE *(UPD350-A/UPD350-C ONLY)*

Figure 14-3 illustrates the I²C slave interface timing requirements. The I²C slave interface can operate in Standard Mode, Fast Mode, or Fast Mode Plus. Refer to Section 4.0, "I2C Slave Controller (UPD350-A/UPD350-C Only)," on page 17 for additional information.

FIGURE 14-3: I²C SLAVE TIMING

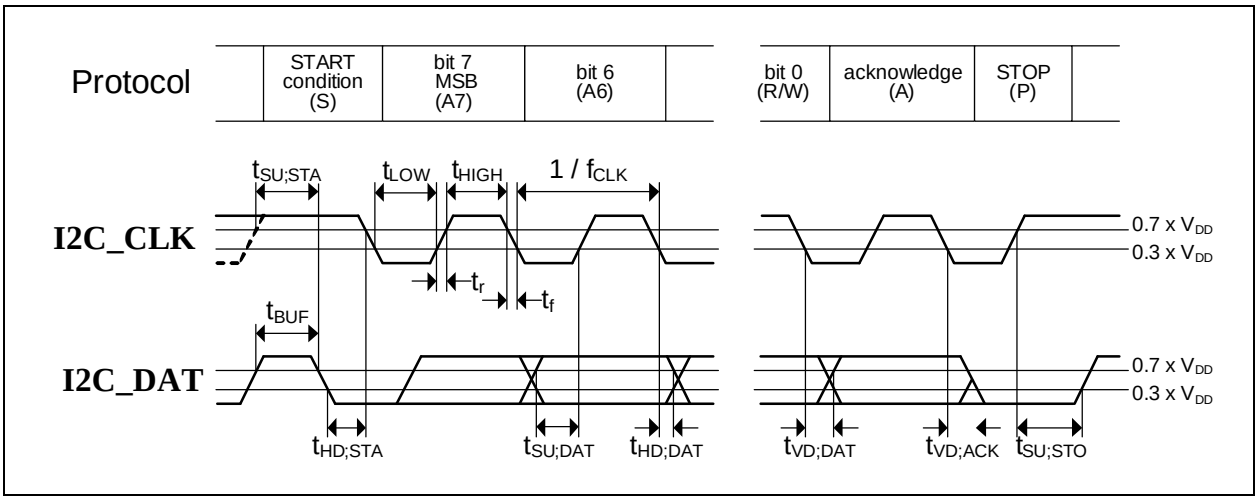


TABLE 14-8: I²C SLAVE TIMING VALUES

Symbol	Description	Min	Max	Units
f_{CLK}	**I2C_CLK** clock frequency	0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
$t_{HD;STA}$	Hold time (repeated) START condition	0.26		µs
$t_{SU;STA}$	Setup time for repeated START condition	0.26		µs
$t_{SU;STO}$	Setup time for STOP condition	0.26		µs
$t_{HD;DAT}$	Data hold time	0		ns
$t_{VD;ACK}$	Data valid acknowledge time (Note 14-5)	0.05	0.45	µs
$t_{VD;DAT}$	Data valid time (Note 14-6)	50	450	ns
$t_{SU;DAT}$	Data setup time	50		ns
t_{LOW}	LOW period of the **I2C_CLK** clock	0.5		µs
t_{HIGH}	HIGH period of the **I2C_CLK** clock	0.26		µs
t_f	Fall time of **I2C_CLK** and **I2C_DAT** (Note 14-7)(Note 14-8)		120	ns
t_r	Rise time of **I2C_CLK** and **I2C_DAT** (Note 14-7)(Note 14-8)		120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter (Note 14-9)		50	ns

Note 14-5 $t_{VD;ACK}$ = time for Acknowledgment signal from **I2C_CLK** LOW to **I2C_DAT** (out) LOW.

Note 14-6 $t_{VD;DAT}$ = minimum time for **I2C_DAT** data out to be valid following **I2C_CLK** LOW.

Note 14-7 A master device must internally provide a hold time of at least 300 ns for the **I2C_DAT** signal (refer to the V_{IL} of the **I2C_CLK** signal) in order to bridge the undefined region **I2C_CLK**'s falling edge.

Note 14-8 The maximum t_f for the **I2C_DAT** and **I2C_CLK** bus lines is specified at 300 ns. The maximum fall time for the **I2C_DAT** output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the **I2C_DAT** and **I2C_CLK** pins and the respective bus lines without exceeding the maximum specified t_f.

Note 14-9 Input filters on the **I2C_DAT** and **I2C_CLK** inputs suppress noise spikes less than 50 ns.

14.6.3 SPI SLAVE INTERFACE *(UPD350-B/UPD350-D ONLY)*

Figure 14-4 and Figure 14-5 illustrate the SPI slave interface input and output timing requirements, respectively. Refer to Section 5.0, "SPI Slave Controller (UPD350-B/UPD350-D Only)," on page 22 for additional information.

FIGURE 14-4: SPI SLAVE INPUT TIMING

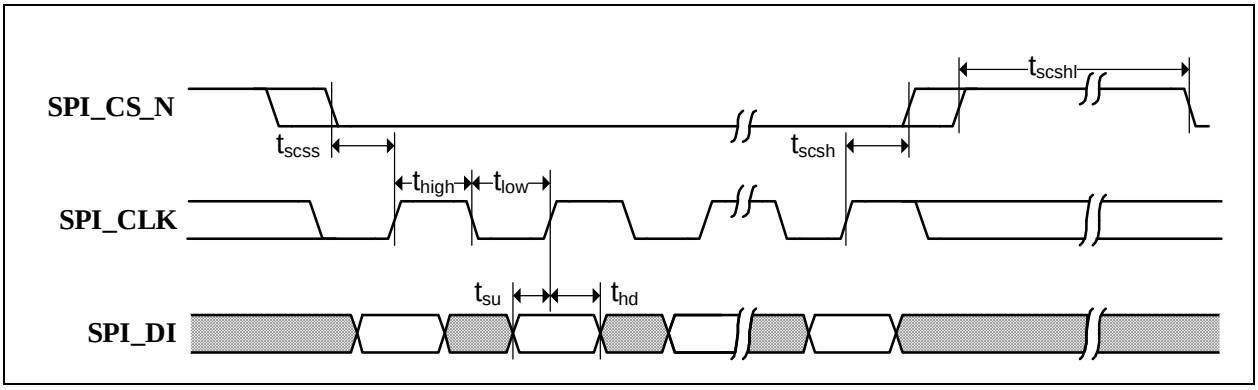


FIGURE 14-5: SPI SLAVE OUTPUT TIMING

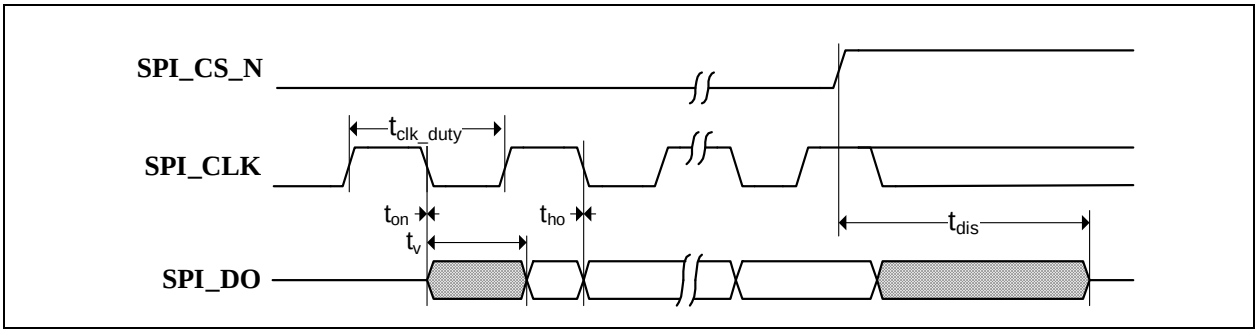


TABLE 14-9: SPI TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
f_{sck}	**SPI_CLK** clock frequency			25	MHz
t_{clk_duty}	**SPI_CLK** high/low duty cycle	40		60	%
t_{scss}	**SPI_CS_N** setup time to **SPI_CLK**	5			ns
t_{scsh}	**SPI_CS_N** hold time from **SPI_CLK**	5			ns
t_{scshl}	**SPI_CS_N** inactive time	100			ns
t_{su}	Data input setup time to **SPI_CLK**	10			ns
t_{hd}	Data input hold time from **SPI_CLK**	4			ns
t_{on}	Data output turn on time from **SPI_CLK**	0			ns
t_v	Data output valid time from **SPI_CLK**			Note 14-10	ns
t_{ho}	Data output hold time from **SPI_CLK**	0			ns
t_{dis}	Data output disable time from **SPI_CS_N** inactive			20	ns

Note 14-10 8.5 or 8.0, depending on loading of 30pF or 10pF, respectively.

15.0 PACKAGE INFORMATION

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 15-1: PACKAGE MARKING INFORMATION

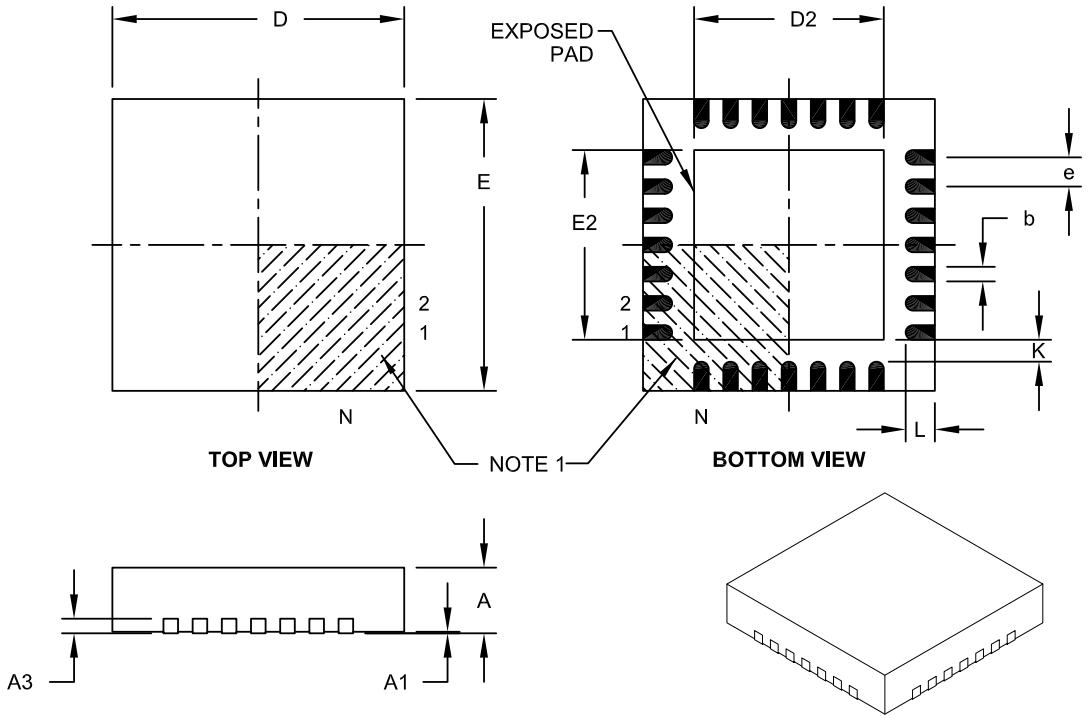
28-SQFN

Legend:		
	x	UPD350 version (“A” or “C” = I^2C interface, “B” or “D” = SPI interface)
	<*i*>	Industrial temperature range indicator
	<V>	Assembly vendor code
	<COO>	Country code
	Y	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 15-2: 28-QFN PACKAGE (DRAWING & DIMENSIONS)

28-Lead Plastic Quad Flat, No Lead Package (MK) – 4x4x0.9 mm Body [QFN]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Contact Width	b	0.17	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

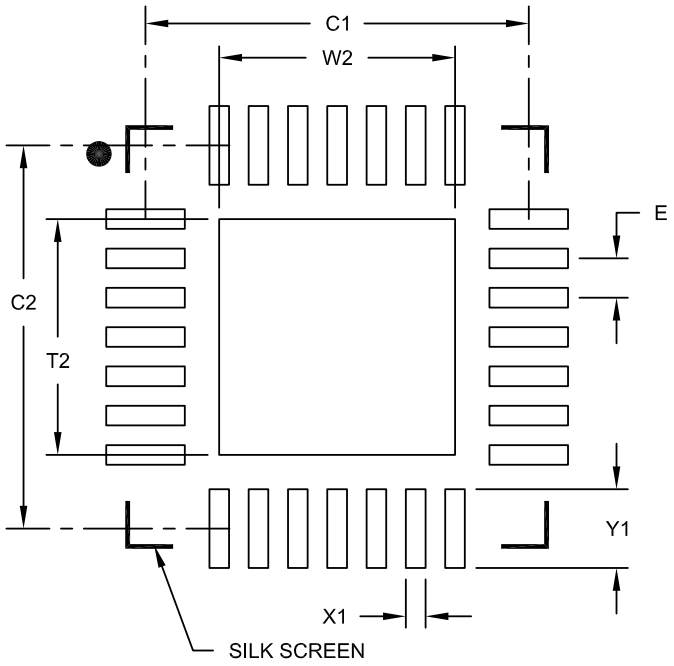
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-144A

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 15-3: 28-QFN PACKAGE (LAND PATTERN)

28-Lead Plastic Quad Flat, No Lead Package (MK) – 4x4x0.9 mm Body [QFN]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			2.40
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width	X1			0.20
Contact Pad Length	Y1			0.80

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2144A

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002643A (03-26-18)	Initial Document Release	

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PART NO.	X	[X](1)	[X]	/XXX	Vxx
Device	Version	Tape & Reel Option	Temp. Range	Package	Automotive Code

Device:	UPD350	
Version:	A	= +1.8V-3.3V I²C Interface, Dead battery support
	B	= SPI Interface, Dead battery support
	C	= +1.8V-3.3V I²C Interface, No dead battery support
	D	= SPI Interface, No dead battery support
Tape and Reel Option:	Blank	= Standard packaging (tray)
	T	= Tape and Reel (Note 1)
Temperature Range:	Blank	= 0°C to +70°C (Commercial)
	-I	= -40°C to +85°C (Industrial and Grade 3 Automotive)
Package:	Q8X	= 28-pin QFN
Automotive Code:	Vxx	= 3 character code with “V” prefix, specifying automotive part

Examples:

a) UPD350A/Q8X
I²C Interface, Dead battery support
Standard packaging,
Commercial temperature,
28-pin QFN package

b) UPD350BT/Q8X
SPI Interface, Dead battery support
Tape and Reel,
Commercial temperature,
28-pin QFN package

c) UPD350B-I/Q8XVAA
SPI Interface, Dead Battery support
Standard packaging,
Industrial Temperature,
28-pin QFN package, Automotive

d) UPD350C/Q8X
I²C Interface, No dead battery support
Standard packaging,
Commercial temperature,
28-pin QFN package

e) UPD350DT-I/Q8X
SPI Interface, No dead battery support
Tape and Reel,
Industrial temperature,
28-pin QFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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