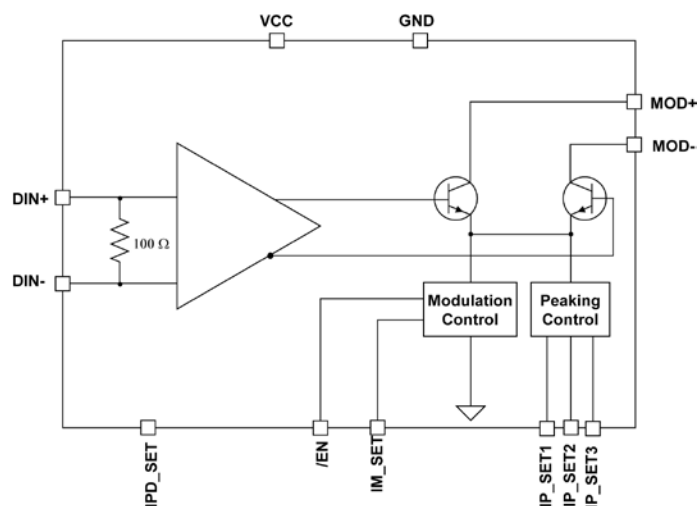




## Functional Block Diagram



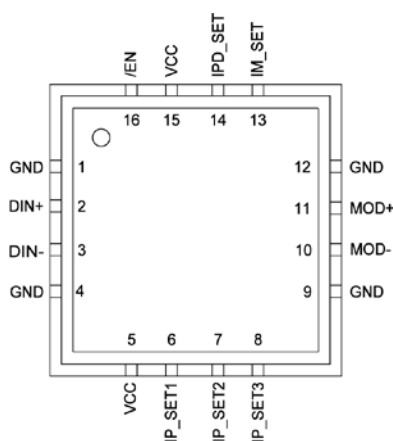
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88992LMG	QFN-16	Industrial	992L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88992LMGTR <sup>(2)</sup>	QFN-16	Industrial	992L with Pb-Free bar-line indicator	NiPdAu Pb-Free

### Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = +25^{\circ}\text{C}$ , DC Electricals only.
2. Tape and Reel.

## Pin Configuration



16-Pin QFN

## Pin Description

Pin Number	Pin Name	Pin Function
2	DIN+	Non-Inverting Input Data. Internally terminated with 50Ω to a reference voltage.
3	DIN-	Inverting Input Data. Internally terminated with 50Ω to a reference voltage.
6	IP_SET1	Peaking Current Setting. Connect this pin to GND and keep pins 7 and 8 open to set peaking-to-modulation current ratio to 5%. Combinations of the three pins, as shown in table below, will set different ratios up to 35%.
7	IP_SET2	Peaking Current Setting. Connect this pin to GND and keep pins 6 and 8 open to set peaking-to-modulation current ratio to 10%. Combinations of the three pins, as shown in table below, will set different ratios up to 35%.
8	IP_SET3	Peaking Current Setting. Connect this pin to GND and keep pins 6 and 7 open to set peaking-to-modulation current ratio to 20%. Combinations of the three pins, as shown in table below, will set different ratios up to 35%.
10	MOD-	Inverted Modulation Current Output. Provides modulation current when input data is negative.
11	MOD+	Non-Inverted Modulation Current Output. Provides modulation current when input data is positive.
13	IM_SET	Modulation Current Setting. The modulation current is set by applying a 0V to 1.2V voltage at this pin.
14	IPD_SET	Peaking Duration Setting. The peaking current duration is set by installing a resistor between this pin and ground. The plot on page 6 shows peaking duration versus the value of the resistor installed.
16	/EN	A low level signal applied to this pin will enable the output stage of the driver. Internally pulled down to ground with 75kΩ resistor.
1, 4, 9, 12	GND	Ground. Ground and exposed pad must be connected to the plane of the most negative potential.
5, 15	VCC	Supply Voltage. Bypass with a 0.1μF//0.01μF low ESR capacitor as close to VCC pin as possible.

## Truth Table

DIN+	DIN-	/EN	MOD+ <sup>(1)</sup>	MOD-	VCSEL Output <sup>(2)</sup>
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	H	L

### Notes:

1.  $I_{MOD} = 0$  when MOD+ = H.
2. Assuming a common anode VCSEL with its cathode tied to MOD+.

## Peaking Current-to-Modulation Current Ratio Setting

IP/I <sub>MOD</sub>	0 %	5 %	10 %	15 %	20 %	25 %	30 %	35 %
IP_SET1	NC	GND	NC	GND	NC	GND	NC	GND
IP_SET2	NC	NC	GND	GND	NC	NC	GND	GND
IP_SET3	NC	NC	NC	NC	GND	GND	GND	GND

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{IN}$ ) ..... -0.5V to +4.0V  
 CML Input Voltage ( $V_{IN}$ ) .....  $V_{CC}-1.2V$  to  $V_{CC}+0.5V$   
 TTL Control Input Voltage ( $V_{IN}$ ) ..... 0V to  $V_{CC}$   
 Lead Temperature (soldering, 20sec.) ..... +260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Supply Voltage ( $V_{CC}$ ) ..... +3.0V to +3.6V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(3)</sup>  
 QFN  
 ( $\theta_{JA}$ ) Still-air ..... 60°C/W  
 ( $\psi_{JB}$ ) ..... 33°C/W

**DC Electrical Characteristics**

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  and  $V_{CC} = 3.0V$  to  $3.6V$ , unless otherwise noted. Typical values are at:  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ\text{C}$ ,  $I_{MOD} = 13\text{mA}$ <sup>(4)</sup>

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	Peaking not used		57	95	mA
		Maximum peaking used		70	110	mA
$I_{MOD}^{(4)}$	Modulation Current	AC-coupled	3		25	mA
$I_{MOD\_OFF}$	Modulation OFF Current	Current at MOD+ and MOD- when the part is disabled			100	$\mu\text{A}$
$V_{MOD\_MIN}$	Minimum Voltage required at the driver output (headroom) for proper operation		1.5			V
$R_{IN}$	Input Resistance (DIN+-to-DIN-)		90	100	110	$\Omega$
$V_{ID}$	Differential Input Voltage Swing		200		2400	mV <sub>PP</sub>
$V_{I_{M\_SET}}$	Voltage Range on $I_{M\_SET}$	$I_{MOD}$ range 3mA – 25mA <sup>(4)</sup>			1.2	V
$V_{IL}$	/EN Input Low				0.8	V
$V_{IH}$	/EN Input High		2			V
	Input Impedance at /EN			75		k $\Omega$

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.  $\theta_{JB}$  uses a 4-layer and  $\theta_{JA}$  in still air unless otherwise stated.
4.  $I_{MOD}$  is defined as the current at the output of the driver. That current splits between the pull-up network at the output and the VCSEL. For a nominal pull-up resistor of 75 $\Omega$  at the output of the driver and a nominal 50 $\Omega$  VCSEL equivalent resistor, 60% of that current goes to the VCSEL.

## AC Electrical Characteristics

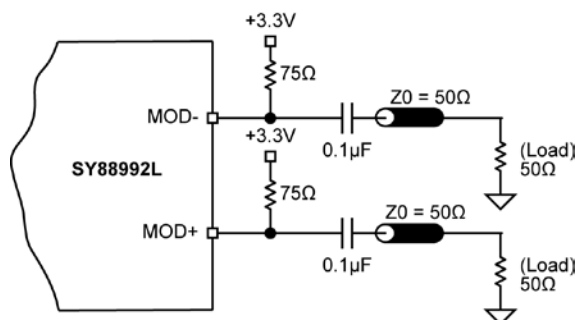
$T_A = -40^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$  and  $V_{CC} = 3.0$  to  $3.6\text{V}$ , unless otherwise noted. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ ,  $I_{MOD} = 13\text{mA}$ <sup>(5)</sup>, and AC-coupled  $50\Omega$  load to ground with  $75\Omega$  pull-up (see Figure below).

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ	0.1		4.25	Gbps
$t_{OFF}^{(6)}$	Turn OFF Time	$50\Omega$ load		1	1.5	ns
$t_{ON}^{(7)}$	Turn ON Time	$50\Omega$ load		1.8	2.5	ns
$t_r$	Output Current Rise Time	20% to 80%, $I_{MOD} = 13\text{mA}$ , no peaking, $50\Omega$ load		65	95	ps
		20% to 80%, $I_{MOD} = 13\text{mA}$ , $I_P/I_{MOD}=20\%$ , $R_{IPD}=1.5\text{k}\Omega$		60	75	ps
$t_f$	Output Current Fall Time	20% to 80%, $I_{MOD} = 13\text{mA}$ , no peaking, $50\Omega$ load		65	95	ps
		20% to 80%, $I_{MOD} = 13\text{mA}$ , $I_P/I_{MOD}=20\%$ , $R_{IPD}=1.5\text{k}\Omega$		60	75	ps
	Total Jitter	@ 2.5Gbps data rate, $50\Omega$ load			30	ps <sub>P</sub>
	Pulse-Width Distortion	$50\Omega$ load			20	ps
$(I_P / I_{MOD})_{Max}$	Maximum Peaking Current-to-Modulation Current Ratio			35		%
$t_P$	Peaking Current Duration <sup>(8)</sup>	$I_{MOD} = 13\text{mA}$ , $R_{IPD\_SET} = 0\Omega$		150		ps

### Notes:

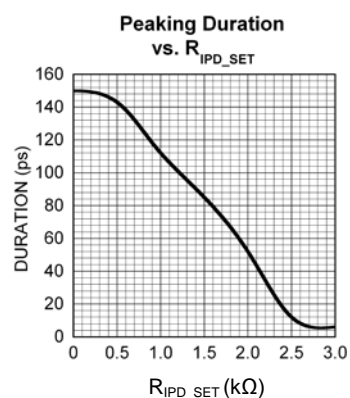
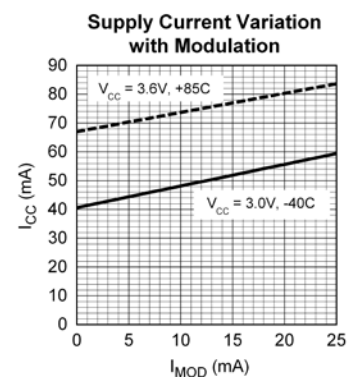
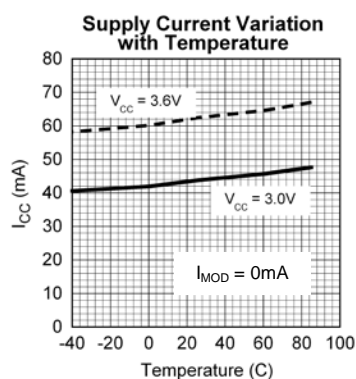
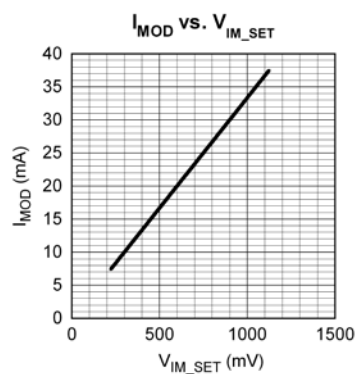
- $I_{MOD}$  is defined as the current at the output of the driver. That current splits between the pull-up network at the output and the VCSEL. For a nominal pull-up resistor of  $75\Omega$  at the output of the driver and a nominal  $50\Omega$  VCSEL equivalent resistor, 60% of that current goes to the VCSEL.
- Turn-OFF time is defined as the delay between the time the signal at /EN rises to 50% of its amplitude and the time when the output of the driver reaches 10% of its steady-state amplitude.
- Turn-ON time is defined as the delay between the time the signal at /EN falls to 50% of its amplitude and the time when the output of the driver reaches 90% of its steady-state amplitude.
- The peaking current duration is the time between the start of the peaking current, which is the same as the start of the modulation current transition, and the time when the peaking current reaches its maximum, i.e., the top of the peak.

## Test Circuit



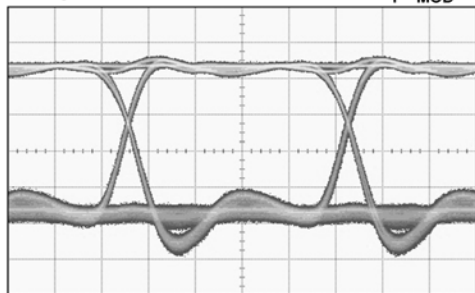
## Typical Operating Characteristics

$T_A = +25^\circ\text{C}$  and  $V_{CC} = 3.3\text{V}$ , unless otherwise noted.



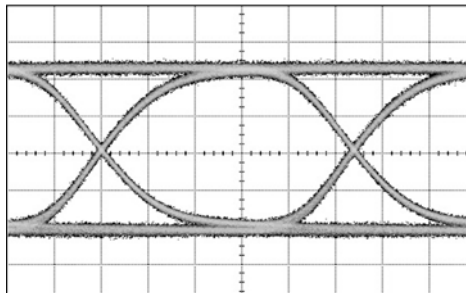
## Typical Waveforms

**Electrical Eye Diagram**  
2.125Gbps, PRBS =  $2^7-1$ , ER = 10dB,  $I_P/I_{MOD} = 0\%$



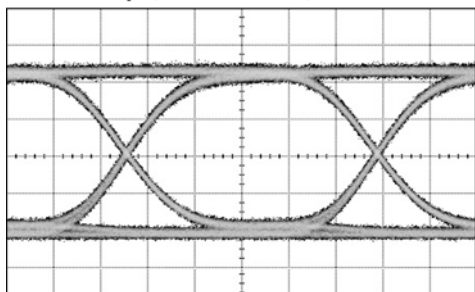
TIME (100ps/div.)

**Optical Eye Diagram**  
1.063Gbps, PRBS =  $2^7-1$ , ER = 10dB



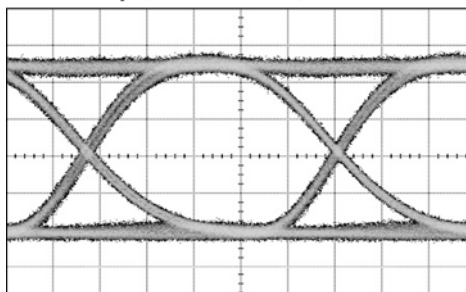
TIME (175ps/div.)

**Optical Eye Diagram**  
1.25Gbps, PRBS =  $2^7-1$ , ER = 10dB



TIME (150ps/div.)

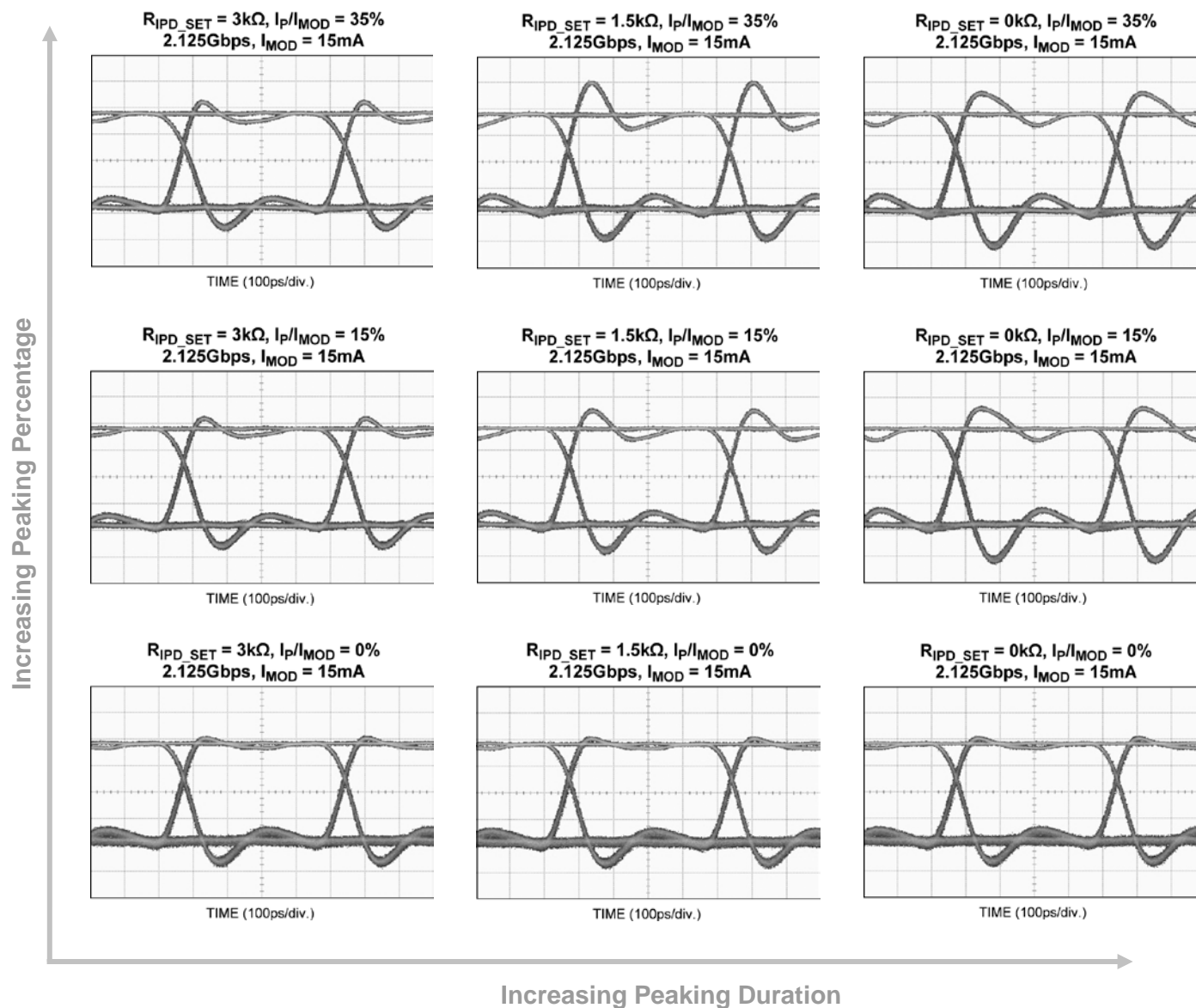
**Optical Eye Diagram**  
2.5Gbps, PRBS =  $2^7-1$ , ER = 10dB



TIME (75ps/div.)

### Peaking Variation with $I_P/I_{MOD}$ Ratio and Peaking Duration

As it can be seen on the set of electrical waveforms below, the amplitude of the peak increases with the peaking-to-modulation current ratio and the width of the peak increases with peaking duration.





## Input and Output Stages

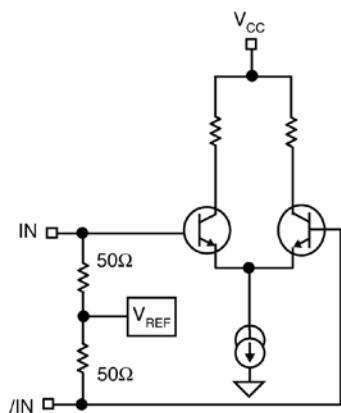


Figure 1a. Simplified Input Stage

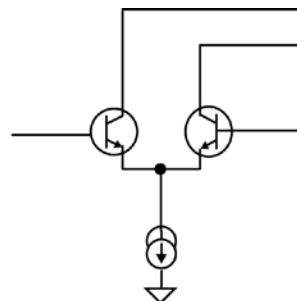


Figure 1b. Simplified Output Stage

## Interfacing the Input to Different Logic Drivers

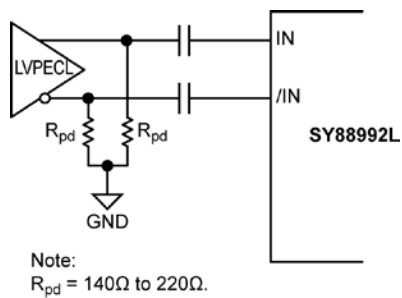


Figure 2a. AC-Coupling to LVPECL Driver

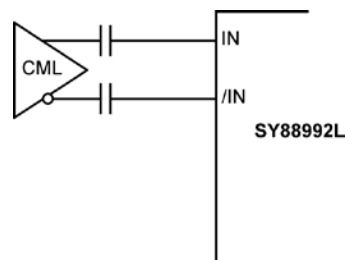


Figure 2b. AC-Coupling to CML Driver

## Driver's Special Features

The SY88992L features a peaking current of programmable amplitude and duration on both the rising and the falling edges. The amplitude of the peaking current is adjustable in steps of 5% of the modulation current from 0% to 35%. As shown in the table on page 3, the ratio between the peaking current and the modulation current ( $I_P/I_{MOD}$ ) can be programmed by connecting pin 6 (IP\_SET1) and/or pin 7 (IP\_SET2) and/or pin 8 (IP\_SET3) to ground. When all these three pins are left open, there is no peaking (ratio 0%). When they're all connected to ground the ratio is maximum (35%).

For each family of VCSELs used with the driver, the user must try many combinations in order to get the best response for the VCSEL. The peaking current duration can be tuned by installing a resistor between pin 14 and ground; 0Ω provides maximum duration and 3kΩ or higher provides the minimum duration. The combined features will improve the VCSEL response for a better optical signal quality. The electrical eye diagrams on page 8 show how the signal changes as the peaking-to-modulation current varies.

## Application Hints

The typical application section on the front page shows how to connect the driver to the VCSEL single-ended. To improve transition time and VCSEL response, the VCSEL can be driven differentially, as shown in Figure 3. Driving the VCSEL differentially will also minimize the cross talk with the rest of the circuitry on the board, especially with the receiver.

The driver is always AC-coupled to the VCSEL and the headroom of the driver is determined by the pull-up network at the output. In Figure 3, the modulation current out of the driver is split between the pull-up network and the VCSEL. If, for example, the total pull-up resistor is twice the sum of the damping resistor and VCSEL equivalent series resistance, only two thirds (2/3) of the modulation current will be used by the VCSEL. Therefore, to maximize the modulation current going through the VCSEL, the total pull-up resistors should be kept as high as possible. One solution consists of using an inductor alone as pull-up, creating a high impedance path for the modulation current and zero ohm (0Ω) path for the DC current. This offers a headroom equal to VCC for the driver

and almost all the modulation current goes into the VCSEL. However, using the inductor alone will cause signal distortion. To avoid this, a combination of resistors and inductors can be used, as shown on figure 3. In this case, the headroom of the driver is  $V_{CC} - R_1 \times \alpha I_{MOD}$ , where  $\alpha I_{MOD}$  is the portion of the modulation current that goes through the pull-up network. For instance, if a modulation current out of the driver of 25mA is considered, with a pull-up resistor of 75Ω, and the VCSEL with the damping resistor total resistance is 50Ω, then the modulation current will split; 10mA to the pull-up resistor and 15mA to the laser. The headroom for the driver will be  $V_{CC} - 75 \times 10 = V_{CC} - 750\text{mV}$  which is way higher than the minimum voltage required for the output stage of the driver to operate properly.

The coupling capacitor creates a low-frequency cutoff in the circuit. Therefore, a proper coupling capacitor value must be chosen to accommodate different data rates in the application. If the value of the capacitor is too high, it may cause problems in high data rate applications. If its value is too small, it won't be able to hold a constant charge between the first bit and the last bit in a long string of identical bits in low data rate application. Both cases lead to higher pattern-dependent jitter in the transmitter signal. 0.1μF is found to be good for applications from 155Mbps to 4.25Gbps.

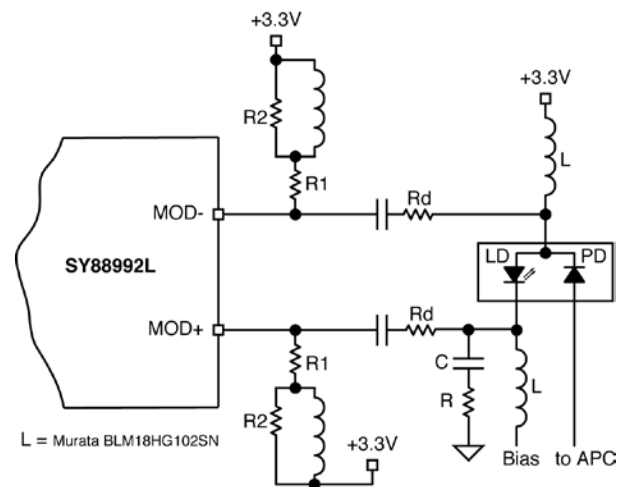
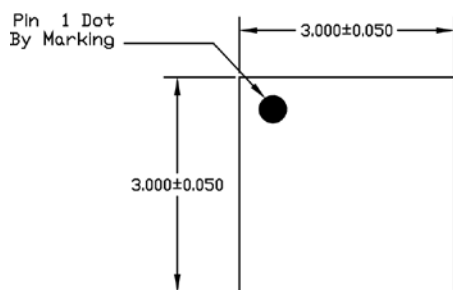
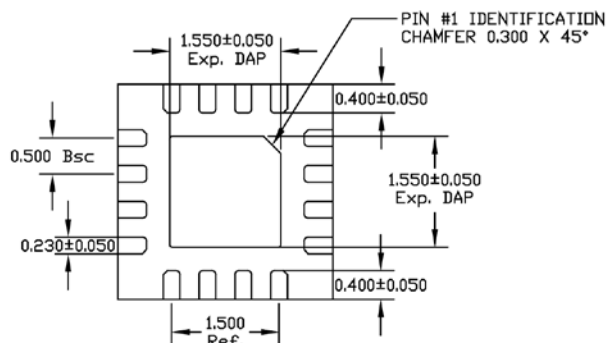


Figure 3. Driving a Common Anode VCSEL Differentially

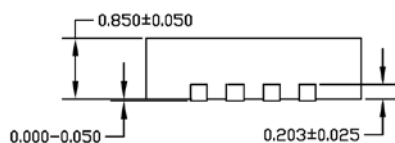
## Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

### 16-Pin (3mm x 3mm) QFN

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