4 X 4 Cross-Point Analog Switch with ±130V T/R Switches

Features

- 16 cross-point analog echo signal matrix switches
- ±130V 20ns T/R switch built-in for each channel
- 50Ω total ON resistance for low insertion loss
- 0.8nV/rt.Hz low RF input noise at 5MHz
- DC to 100MHz small signal bandwidth
- -55dB off-Isolation and -65dB crosstalk
- Shunt switch for LNA fast recovery
- Programmable auto trig levels and time
- ±5V power supply, 2.5V to 3.3V Logic
- 5mA low power supply consumptions
- 20MHz serial interface
- -55dB HD2 very low echo signal distortion

Applications

- Medical imaging ultrasound beamforming receiver
- Software programmable echo multiplex switching
- High resolution phase array ultrasound NDT
- Ultrasonic phase array receiver focusing
- Array PZT transducer echo phase processing
- High speed T/R switch and wave-front summing

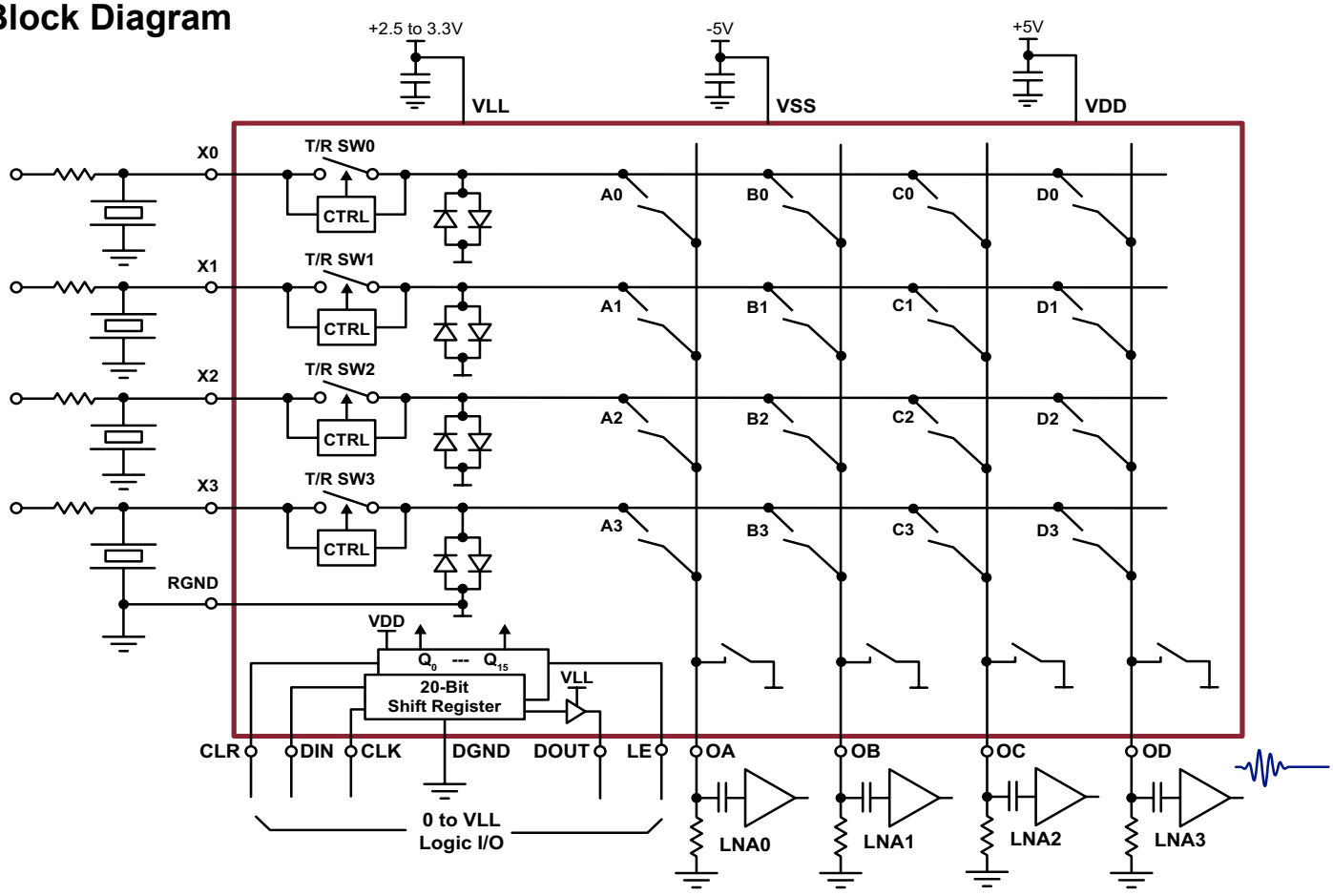
General Description

The MD0201 is a low voltage analog 4x4 cross-point switch with four high voltage T/R switches, voltage limit diode and output shunt switch circuit. It is designed for medical ultrasound image system receiver beamforming applications. It also can be used in NDT and other ultrasound applications.

The MD0201 circuit consists of a low voltage CMOS analog switch and digital logic control serial interface circuits. These analog switches not only have low insertion loss, low noise, and wide frequency response, they also have high off isolation and low channel-to-channel crosstalk. The inputs of the analog switches are connected to the output of the two terminal type of ultrasound T/R switches, and two back-to-back diode voltage limiter circuits.

The buffered serial interface data registers have allowed the IC maximum flexibility to connect large number of channels to form the echo multiplexing, dynamic-focusing circuit for ultrasound image receive beamforming.

Block Diagram



Ordering Information

Part Number	Package Options	Packing
MD0201K6-G	48-Lead (7x7) QFN	260/Tray
MD0201K6-G M933	48-Lead (7x7) QFN	2000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

ESD Sensitive Device

Absolute Maximum Ratings

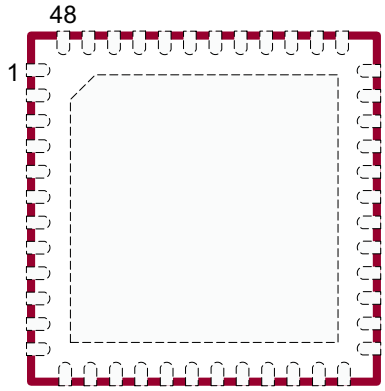
Parameter	Value
GND reference voltage	0V
X0~X3 input pins to GND voltage	0 to ±140V
V_{DD} positive supply	-0.5V to +6.0V
V_{SS} negative supply	+0.5V to -6.0V
V_{LL} logic supply	-0.5V to +4.2V
All logic input pins	-0.5V to +6.0V
Maximum junction temperature	+125°C
Storage temperature range	-65°C to 150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
48-Lead QFN	18°C/W

Pin Configuration



48-Lead QFN
(top view)

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

48-Lead QFN

Package may or may not include the following marks: Si or

Operating Supply Voltages

(Over operating conditions unless otherwise specified, V_{LL} = 3.3V, V_{DD} = +5V, T_j = 25°C)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	Voltage power supply	4.75	5.0	5.25	V	T_A= 0 to 70°C
V_{SS}	Voltage power supply	-5.25	-5.0	-4.75		
V_{LL}	Voltage power supply	2.3	3.3	3.6		
V_{SIG}	Signal input range (p-p)	-	±500	-	mV	5MHz sine wave, no clipping
R_{ON}	Cross-point switch ON resistance	-	50	60	Ω	I_X = ±5.0mA, $V_{X0\sim3}$ = ±300mV
ΔR_{ON}	Ch to Ch R_{ON} difference	-	±5	-	%	Switches ON resistance match within IC.
V_F	Diode forward voltage	-	0.8	1.0	V	1mA
C_T	Diode total capacitance	-	-	15	pF	V_R = 0V, f = 1MHz
I_{FM}	Diode forward continuous current	-	100	-	mA	on 4x4inch PCB, V_F=1.2V
I_{DDQ}	V_{DD} supply current 0MHz	-	2.2	3.0	mA	SDI = SCK = 0, CS = 0
I_{DD30}	V_{DD} supply current 30MHz	-	7.0	30	mA	f_{SCK}= 30MHz, SDI = CS = 0
HD2	Second harmonic distortion	-	-55	-50	dB	5MHz ±300mVp-p sine wave

T/R Switch Characteristics *(Over operating conditions unless otherwise specified, V_{LL} = 3.3V, V_{DD} = +5V, T_j = 25°C)*

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_X	Max $X_{0\sim3}$ to GND input voltage	±130	-	-	V	I_X = ±500µA
R_{TRSW}	T/R switch ON resistance	-	15	-	Ω	I_X = ±5.0mA
V_{TRIP}	$VX_{0\sim3}$ trip point to turn off	-	±1.0	±2.0	V	---
V_{OFF}	Switch turn off voltage	-	±2.0	-	V	I_{A-B} = ±1.0mA
I_{OFF}	Switch off current	-	±200	±300	µA	X_n = ±100V
I_{PEAK}	Peak T/R switch current	-	±60	-	mA	---
T_{OFF}	Turn off time	-	-	20	ns	---
T_{ON}	Turn on time	-	-	20	ns	---
$C_{SW(ON)}$	Switch on capacitance	-	21	-	pF	T/R SW = ON
$C_{SW(OFF)}$	Switch off capacitance	-	15	-	pF	X_n = ±25V

Clock and Logic I/O Characteristics *(Over operating conditions unless otherwise specified, V_{LL} = 3.3V, V_{DD} = +5V, T_j = 25°C)*

V_{IH}	Input logic high voltage	2.5	3.3	5.0	V	---
V_{IL}	Input logic low voltage	0	-	0.6	V	---
I_{IH}	Input logic high current	-	0.4	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---
C_{IN}	Input capacitance	-	2.0	5.0	pF	---
I_{OH}	V_{DOUT} sourcing current	4.0	-	-	mA	V_{LL} = 2.3V, V_{DOUT} = 0
I_{OL}	V_{DOUT} sinking current	4.0	-	-	mA	V_{LL} = V_{DOUT} = 2.3V
V_{OH}	Output logic high voltage	-	1.59	-	V	I_{OH}=-2.0mA
V_{OL}	Output logic low voltage	-	0.67	-	V	I_{OL}=-2.0mA

AC Electrical Characteristics *(Over operating conditions unless otherwise specified, V_{LL} = 3.3V, V_{DD} = +5V, T_j = 25°C)*

$t_{d(on)}$	LV SW turn on time	-	20	30	ns	---
$t_{d(off)}$	LV SW turn off time	-	20	30	ns	---
$t_{co(on)}$	Output shunt switch on time	-	40	50	ns	V_X = 5.0V
$t_{co(off)}$	Output shunt switch off-delay	1.0	2.0	3.0	µs	
V_{STG}	Shunt on-short trig voltage level	-	±0.8	-	V	---
BW	Small signal bandwidth with T/R SW	-	85	-	MHz	R_{LOAD} = 50Ω
Q_C	LV SW charge injection	-	2.6	3.5	pC	V_S =1.0V, R_S = 0Ω, C_{LOAD} = 100pF
K_O	OFF isolation	-	-65	-	dB	at 10MHz, R_{LOAD}= 50Ω
K_{CR}	On channel crosstalk	-	-55	-		
$C_{(ON)}$	On capacitance output to RGND	-	37	-	pF	from OA~OD to RGND
$C_{(OFF)}$	Off capacitance output to RGND	-	23	-		
f_{CLK}	Serial clock frequency	-	25	-	MHz	---

AC Electrical Characteristics *(cont.)* *(Over operating conditions unless otherwise specified, V_{LL} = 3.3V, V_{DD} = +5V, T_j = 25°C)*

Sym	Parameter	Min	Typ	Max	Unit	Conditions
t_{SD}	Setup time before LE rises	-	10	-	ns	At 25MHz V_{DD} = 4.75V V_{LL} = 2.5V
t_{WLE}	Time width of LE	-	20	-		
t_{DO}	CLK delay time to data out	-	13	-		
t_{WCLR}	Time width of CLR	55	15	-		
t_{SU}	Set up time data to clock	-	5.0	-		
t_h	Hold time data from clock	-	5.0	-		
t_{rf}	CLK rise and fall time	1.5	-	-		
V_{SPK}	Spike of shunt switching on	-	60	100	mV	All cross-point switches off, 50Ω on O0~3 to GND 1k on X0~3 to GND
	Spike of shunt switching off	-	10	-		

20-bit Control Shift Registers

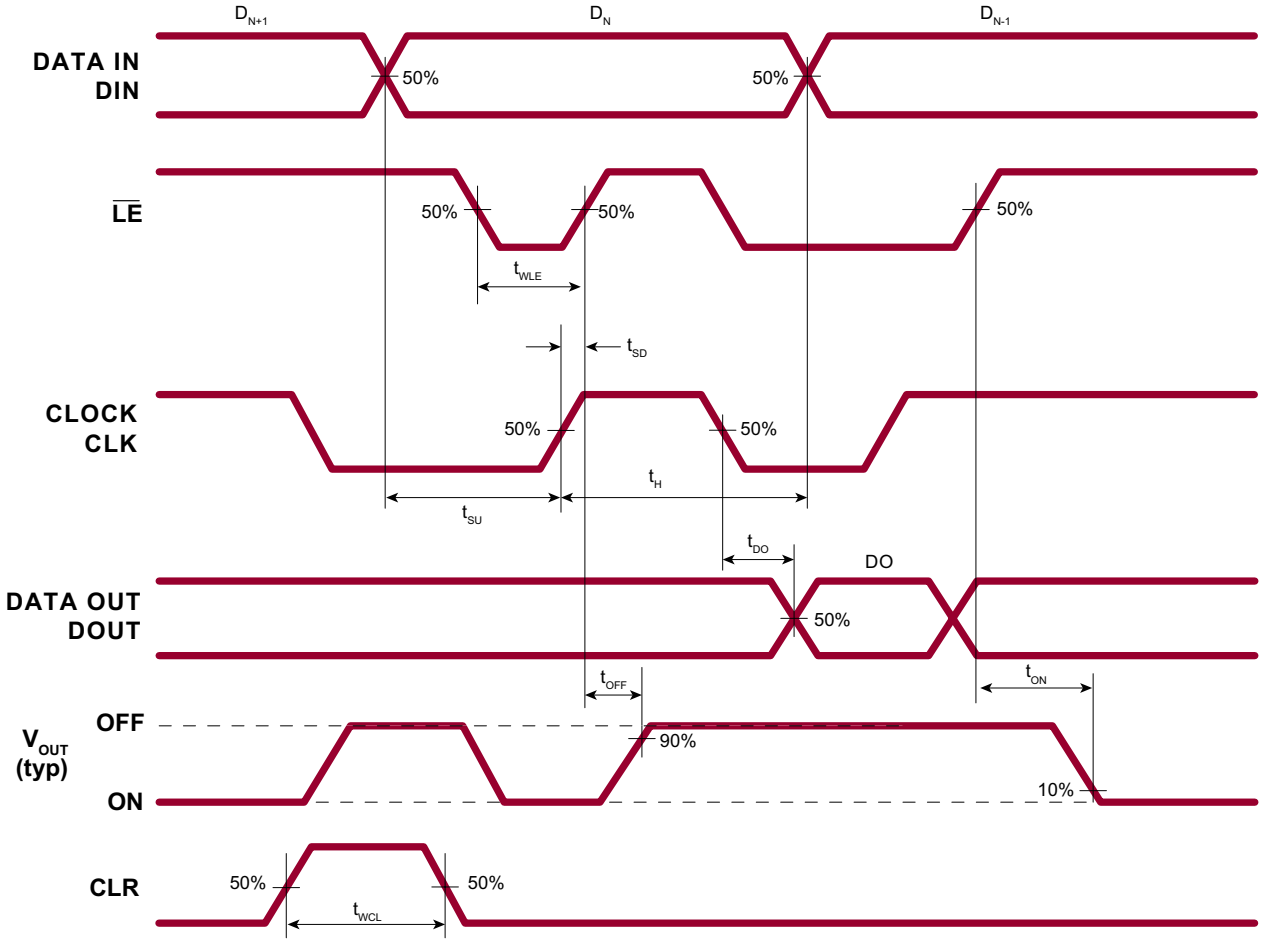
MSB											LSB
Data Bits in the Register											
D19	**D19**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**...**	**D1**	**D0**
Unused	**TMR**	**SSTE**	**FASN**	**SWA0**	**SWB0**	**SWC0**	**SWD0**	**SWA1**	**...**	**SWC3**	**SWD3**

SW[D3:A0]	0	LV switches off*	Low voltage analog cross-point switch on/off control data. Each data bit controls each channel LV switch independently.
	1	LV switches on	
TMR	0	Set on-time to 1.0us*	The shunt switches controlled by a re-trigable one-short timer. TMR sets the one short on-time for all channels.
	1	Set on-time to 2.0us	
SSTE	0	Shunt switch trig Disabled*	SSTE = 0 trig disabled
	1	Shunt switch trig Enabled	
FASN	0	Normal trig *	FASN = 0 trig causing shunt switch on for a period of TMR defined time.
	1	Force all shunt switch on	

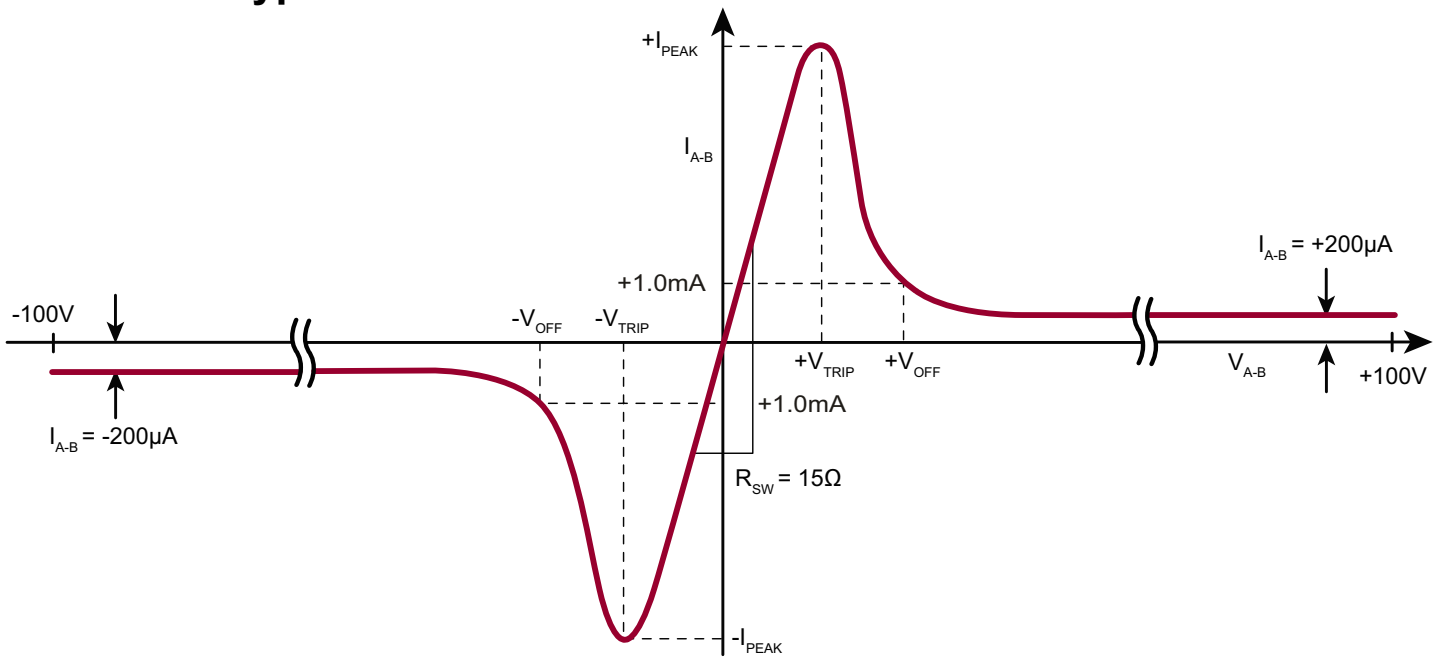
Notes:

1. D[15:0] are the cross-point switch SW[D3:A0] control data bits.
2. Shift in MSB first.
3. D19 is reserved.
4. The * denotes power-on defaults status.

Logic Timing Waveforms



T/R Switch Typical I-V Curve



Pin Description (48-Lead QFN)

Pin	Name	Description
1	NC	Not connected internally to the IC
2	X0	T/R switch channel 0 high voltage input
3	NC	Not connected internally to the IC
4	NC	Not connected internally to the IC
5	X1	T/R switch channel 1 high voltage input
6	NC	Not connected internally to the IC
7	NC	Not connected internally to the IC
8	X2	T/R switch channel 2 high voltage input
9	NC	Not connected internally to the IC
10	NC	Not connected internally to the IC
11	X3	T/R switch channel 3 high voltage input
12	NC	Not connected internally to the IC
13	NC	Not connected internally to the IC
14	NC	Not connected internally to the IC
15	NC	Not connected internally to the IC
16	NC	Not connected internally to the IC
17	NC	Not connected internally to the IC
18	RGND	RF ground, diodes and shunt switch return ground (0V)
19	OA	Low voltage analog switch channel 0 output
20	OB	Low voltage analog switch channel 1 output
21	OC	Low voltage analog switch channel 2 output
22	OD	Low voltage analog switch channel 3 output
23	NC	Not connected internally to the IC
24	NC	Not connected internally to the IC
25	NC	Not connected internally to the IC
26	NC	Not connected internally to the IC
27	NC	Not connected internally to the IC
28	NC	Not connected internally to the IC
29	NC	Not connected internally to the IC
30	NC	Not connected internally to the IC
31	NC	Not connected internally to the IC
32	NC	Not connected internally to the IC
33	NC	Not connected internally to the IC
34	VSS	Negative voltage power supply -5V

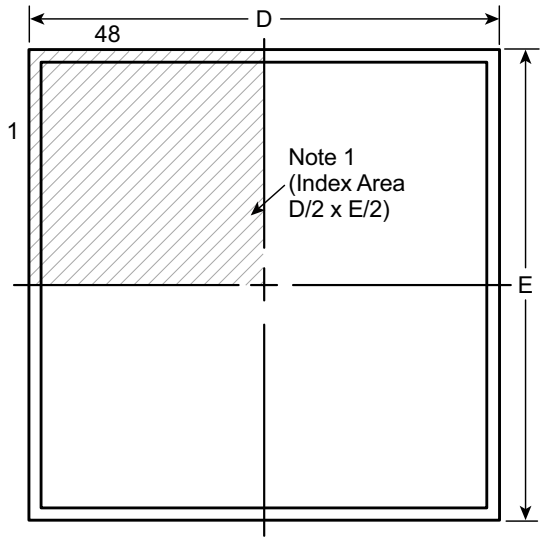
Pin Description (48-Lead QFN)

Pin	Name	Description
35	DGND	Digital control signal ground and VDD return ground (0V)
36	VDD	Positive voltage power supply +5V
37	DGND	Digital control signal ground and VDD return ground (0V)
38	VDD	Positive voltage power supply +5V
39	VLL	Logic supply voltage +2.5 to 3.3V
40	DIN	Serial data input
41	CLR	Data registers clear to all switches off, active high
42	CLK	Serial interface clock input
43	LE	Data registers latch enable, active on rising edge only
44	DOUT	Serial data output
45	NC	Not connected internally to the IC
46	NC	Not connected internally to the IC
47	NC	Not connected internally to the IC
48	NC	Not connected internally to the IC

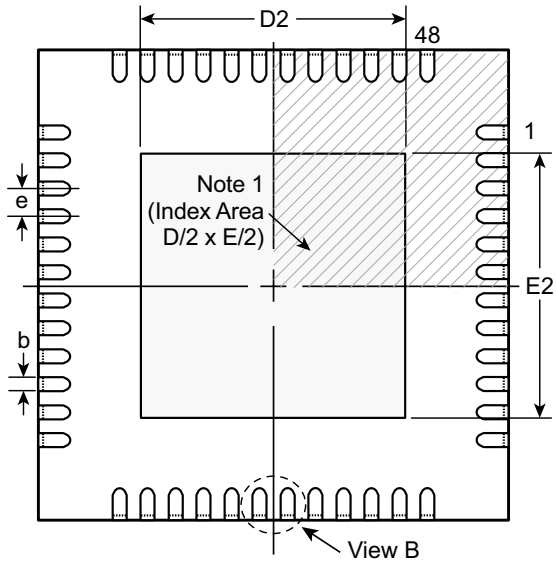
Note: *Thermal pad of the IC package (RGND) must be connected to the RF ground on the PCB.*

48-Lead QFN Package Outline (K6)

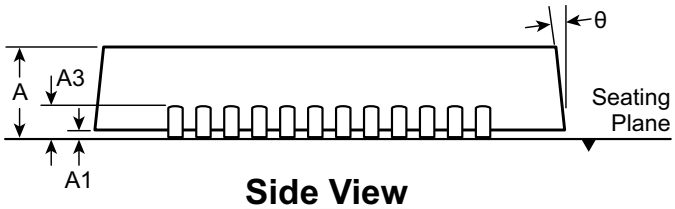
7.00x7.00mm body, 1.00mm height (max), 0.50mm pitch



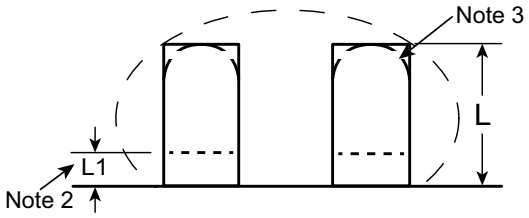
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	6.85*	1.25	6.85*	1.25	0.50 BSC	0.30†	0.00	0°
	NOM	0.90	0.02		0.25	7.00	-	7.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	7.15*	5.45	7.15*	5.45		0.50†	0.15	14°

JEDEC Registration MO-220, Variation VKKD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
Supertex Doc.#: *DSPD-48QFNK67X7P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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